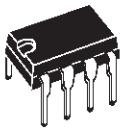
L6569
L6569A

HIGH VOLTAGE HALF BRIDGE DRIVER WITH OSCILLATOR

- HIGH VOLTAGE RAIL UP TO 600V
- BCD OFF LINE TECHNOLOGY
- INTERNAL BOOTSTRAP DIODE STRUCTURE
- 15.6V ZENER CLAMP ON V_S
- DRIVER CURRENT CAPABILITY:
  - SINK CURRENT = 270mA
  - SOURCE CURRENT = 170mA
- VERY LOW START UP CURRENT: 150µA
- UNDER VOLTAGE LOCKOUT WITH HYSTERESIS
- PROGRAMMABLE OSCILLATOR FREQUENCY
- DEAD TIME 1.25µs
- dV/dt IMMUNITY UP TO ±50V/ns
- ESD PROTECTION



Minidip

SO8

ORDERING NUMBERS:

L6569	**L6569D**
L6569A	**L6569AD**

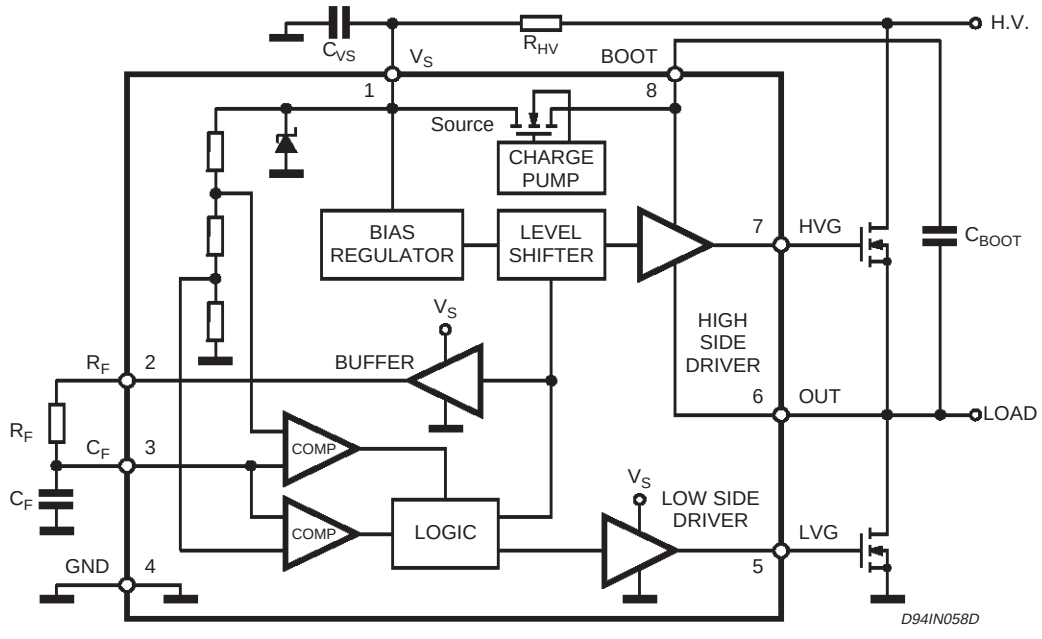
DESCRIPTION

The device is a high voltage half bridge driver with built in oscillator. The frequency of the oscillator can be programmed using external resistor and capacitor. The internal circuitry of the device allows it to be driven also by external logic signal.

The output drivers are designed to drive external n-channel power MOSFET and IGBT. The internal logic assures a dead time [typ. 1.25µs] to avoid cross-conduction of the power devices.

Two version are available: L6569 and L6569A. They differ in the low voltage gate driver start up sequence.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_S (*)	Supply Current	25	mA
V_{CF}	Oscillator Resistor Voltage	18	V
V_{LVG}	Low Side Switch Gate Output	14.6	V
V_{OUT}	High Side Switch Source Output	-1 to V_{BOOT} - 18	V
V_{HVG}	High Side Switch Gate Output	-1 to V_{BOOT}	V
V_{BOOT}	Floating Supply Voltage	618	V
$V_{BOOT/OUT}$	Floating Supply vs OUT Voltage	18	V
dV_{BOOT}/dt	VBOOT Slew Rate (Repetitive)	± 50	V/ns
dV_{OUT}/dt	VOUT Slew Rate (Repetitive)	± 50	V/ns
T_{stg}	Storage Temperature	-40 to 150	°C
T_j	Junction Temperature	-40 to 150	°C
T_{amb}	Ambient Temperature (Operative)	-40 to 125	°C

(*)The device has an internal zener clamp between GND and VS (typical 15.6V).Therefore the circuit should not be driven by a DC low impedance power source.
Note: ESD immunity for pins 6, 7 and 8 is guaranteed up to 900 V (Human Body Model)

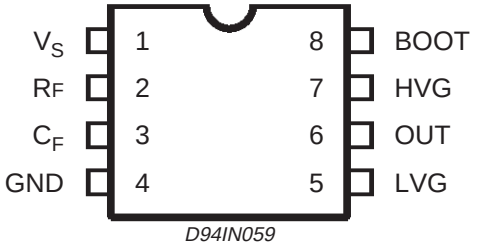
THERMAL DATA

Symbol	Parameter	Minidip	SO8	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-Ambient Max	100	150	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_S	Supply Voltage	10	V_{CL}	V
V_{BOOT}	Floating Supply Voltage	-	500	V
V_{OUT}	High Side Switch Source Output	-1	V_{BOOT} -V_{CL}	V
f_{out}	Oscillation Frequency		200	kHz

PIN CONNECTION



D94IN059

PIN FUNCTION

N°	Pin	Description
1	VS	Supply input voltage with internal clamp [typ. 15.6V]
2	RF	Oscillator timing resistor pin. A buffer set alternatively to V_S and GND can provide current to the external resistor RF connected between pin 2 and 3. Alternatively, the signal on pin 2 can be used also to drive another IC (i.e. another L6569 to drive a full H-bridge)
3	CF	Oscillator timing capacitor pin. A capacitor connected between this pin and GND fixes (together with R_F) the oscillating frequency Alternatively an external logic signal can be applied to the pin to drive the IC.
4	GND	Ground
5	LVG	Low side driver output. The output stage can deliver 170mA source and 270mA sink [typ.values].
6	OUT	Upper driver floating reference
7	HVG	High side driver output. The output stage can deliver 170mA source and 270mA sink [typ.values].
8	BOOT	Bootstrap voltage supply. It is the upper driver floating supply. The bootstrap capacitor connected between this pin and pin 6 can be fed by an internal structure named “bootstrap driver” (a patented structure). This structure can replace the external bootstrap diode.

ELECTRICAL CHARACTERISTCS (V_S = 12V; V_{BOOT} - V_{OUT} = 12V; T_j = 25°C; unless otherwise specified.)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{SUVP}	1	VS Turn On Threshold		8.3	9	9.7	V
V_{SUVN}		VS Turn Off Threshold		7.3	8	8.7	V
V_{SUVH}		VS Hysteresis		0.7	1	1.3	V
V_{CL}		VS Clamping Voltage	I_S = 5mA	14.6	15.6	16.6	V
I_{SU}		Start Up Current	$V_S < V_{SUVN}$		150	250	µA
I_q		Quiescent Current	$V_S > V_{SUVP}$		500	700	µA
I_{BOOTLK}	8	Leakage Current BOOT pin vs GND	V_{BOOT} = 580V			5	µA
I_{OUTLK}	6	Leakage Current OUT pin vs GND	V_{OUT} = 562V			5	µA
$I_{HVG\ SO}$	7	High Side Driver Source Current	V_{HVG} = 6V	110	175		mA
$I_{HVG\ SI}$		High Side Driver Sink Current	V_{HVG} = 6V	190	275		mA
$I_{LVG\ SO}$	5	Low Side Driver Source Current	V_{LVG} = 6V	110	175		mA
$I_{LVG\ SI}$		Low Side Driver Sink Current	V_{LVG} = 6V	190	275		mA

ELECTRICAL CHARACTERISTCS (continued)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{RFO}N$	2	RF High Level Output Voltage	I_{RF} = 1mA	V_S -0.05		V_S -0.2	V
$V_{RF\ OFF}$		RF Low Level Output Voltage	I_{RF} = -1mA	50		200	mV
V_{CFU}	3	CF Upper Threshold		7.7	8	8.2	V
V_{CFL}		CF Lower Threshold		3.80	4	4.3	V
t_d		Internal Dead Time		0.85	1.25	1.65	µs
DC		Duty Cycle, Ratio Between Dead Time + Conduction Time of High Side and Low Side Drivers		0.45	0.5	0.55	
R_{ON}		On resistance of Boostrap LDMOS			120		Ω
V_{BC}		Boostrap Voltage before UVLO	V_S = 8.2	2.5	3.6		V
I_{AVE}	1	Average Current from Vs	No Load, fs = 60KHz		1.2	1.5	mA
f_{out}	6	Oscillation Frequency	R_T = 12K; C_T = 1nF	57	60	63	kHz

OSCILLATOR FREQUENCY

The frequency of the internal oscillator can be programmed using external resistor and capacitor.

The nominal oscillator frequency can be calculated using the following equation:

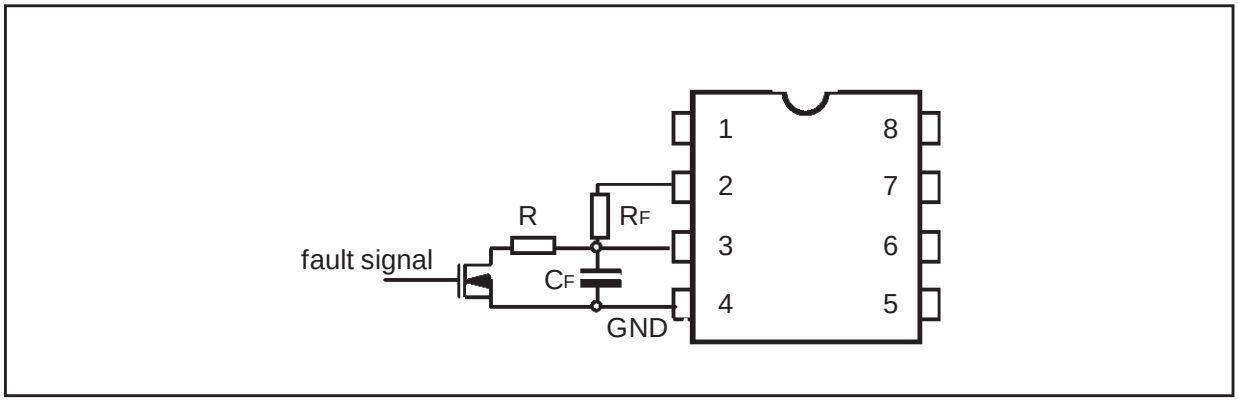
$$f_{OSC} = \frac{1}{2 \cdot R_F \cdot C_F \cdot In2} = \frac{1}{1.3863 \cdot R_F \cdot C_F}$$

Where R_F and C_F are the external resistor and capacitor.

The device can be driven in "shut down" condition keeping the C_F pin close to GND, but some cares have to be taken:

1. When C_F is to GND the high side driver is off and the low side is on
2. The forced discharge of the oscillator capacitor C_F must not be shorter than 1us: a simple way to do this is to limit the current discharge with a resistive path imposing $R \cdot C_F > 1\mu s$ (see fig.1)

Figure 1.



Bootstrap Function

The L6569 has an internal Bootstrap structure that enables the user to avoid the external diode needed, in similar devices, to perform the charge of the bootstrap capacitor that, in turns, provide an appropriate driving to the Upper External Mosfet.

The operation is achieved with an unique structure (patented) that uses a High Voltage Lateral DMOS driven by an internal charge pump (see Block Diagram) and synchronized, with a 50 nsec delay, with the Low Side Gate driver (LVG pin), actually working as a synchronous rectifier .

The charging path for the Bootstrap capacitor is closed via the Lower External Mosfet that is driven ON (i.e. LVG High) for a time interval:

$$T_C = R_F \cdot C_F \cdot \ln 2 \rightarrow 1.1 \cdot R_F \cdot C_F$$

starting from the time the Supply Voltage V_S has reached the Turn On Voltage (V_{SUVP} = 9 V typical value).

After time T_1 (see waveform Diagram) the LDMOS that charges the Bootstrap Capacitor, is on with a R_{ON}=120Ω (typical value).

In the L6569A a different start up procedure is followed (see waveform Diagram). The Lower External Mosfet is drive OFF until V_S has reached the Turn On Threshold (V_{SUVPp}), then again the T_C time interval starts as above.

Being the LDMOS used to implement the bootstrap operation a "bi-directional" switch the current flowing into the BOOT pin (pin 8) can lead an undue stress to the LDMOS itself if a ZERO VOLTAGE SWITCHING operations is not ensured, and then an high voltage is applied to the BOOT pin. This condition can occur, for example, when the load is removed and an high resistive value is placed in series with the gate of the external Power Mos. To help the user to secure his design a SAFE OPERATING AREA for the Bootstrap LDMOS is provided (fig. 7).

Let's consider the steps that should be taken.

1) Calculate the Turn on delay (td) of your Lower Power MOS:

$$t_d = (R_g + R_{id}) \cdot C_{iss} \cdot \ln\left[\frac{1}{1 - \frac{V_{TH}}{V_S}}\right]$$

2) Calculate the Fall time (tf) of your Lower Power MOS:

$$t_f = \frac{R_g + R_{id}}{V_S - V_{TH}} \cdot Q_{gd}$$

where:

R_g = External gate resistor

R_{id} = 50Ω, typical equivalent output resistance of the driving buffer (when sourcing current)

V_{TH}, C_{iss} and Q_{gd} are Power MOS parameters

V_S = Low Voltage Supply.

3) Sketch the VBOOT waveform (using log-log scales) starting from the Drain Voltage of the Lower Power MOS (remember to add the Vs, your Low Voltage Supply, value) on the Bootstrap LDMOS SOA . On fig. 8 an example is given where:

V_S = Low Voltage Supply

V_{HV} = High Voltage Supply Rail

The V_{BOOT} voltage swing must fall below the curve identified by the actual operating frequency of your application.

DEMO BOARD

To allow an easy evaluation of the device, a P.C. board dedicated to lamp ballast application has been designed.

Fig.11 shows the electrical schematic of a typical ballast application, while the PC and component layout is given in Fig12. This application has been designed to work with both the 110+/-20%V and the 220 +/- 20%V mains by means of a voltage doubler configuration at the bulk capacitor. The ballast inductance and the operating frequency are especially designed for a 18 W Sylvania De-luxe T/E type bulb. The PTC for preheat at the start up and the two back to back synchronization diodes, makes this application easy to implement and safe in operation.

part	value
R1	15ohm 1W
R2, R3	22 ohm
R4	27K
R5	100K 1/2W
R6	47ohm
R7, R9	180K
R8	120K 1/2W
D1	18V zener
D2, D3	BYW100-100
D4,D5,D6,D7	1N4007
D8	1N4148
C1	560pF 50V
C2, C5	47µF 250V
C3	4.7µF 25V
C4	100nF 50V
C6	100nF 250V
C7-C8	8.2nF 630V
C9	470pF 630V
RV1	PTC 150ohm
Q1, Q2	STD2NB50-1
L1	2.4mH

Figure 2. Waveforms (L6569)

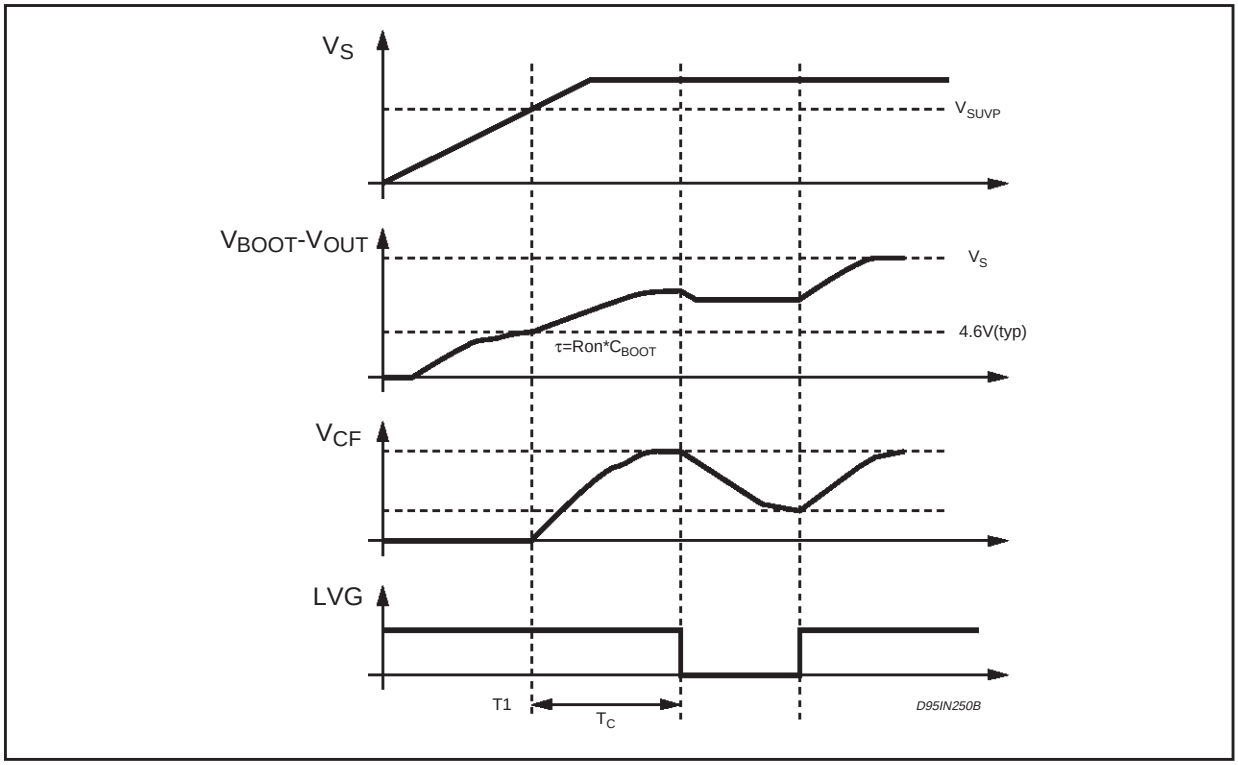


Figure 3. Waveforms (L6569A)

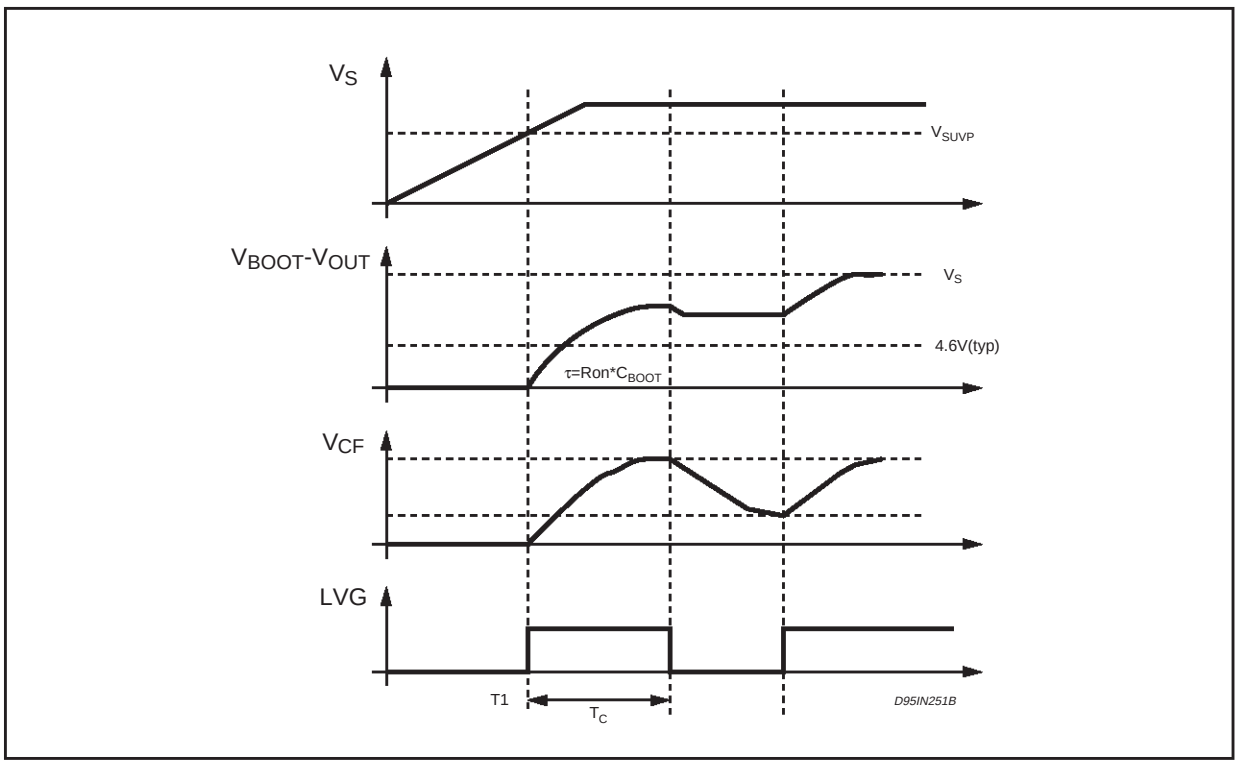


Figure 4. Typical Dead Time vs. Temperature Dependency

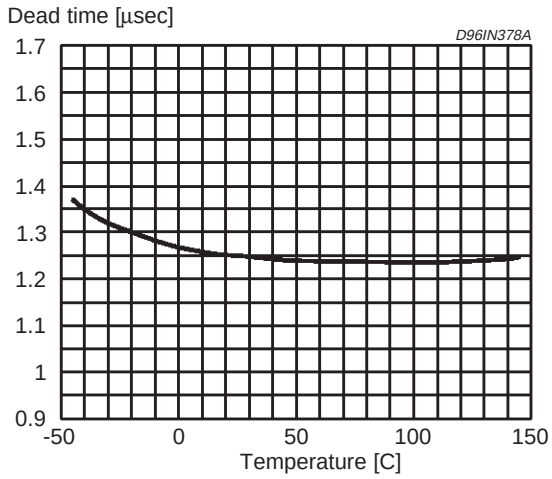


Figure 5. Typical Frequency vs Temperature Dependency

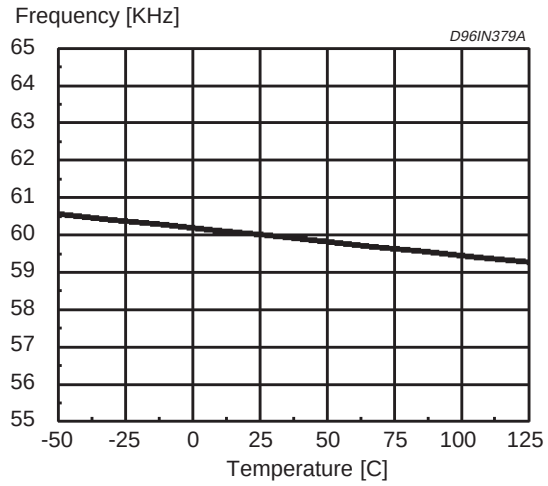


Figure 6. Typical and Theoretical Oscillator Frequency vs Resistor Value

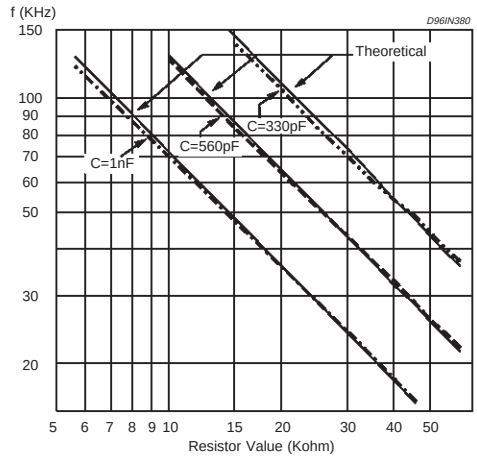


Figure 7. V_{boot} pin SOA for different Operating Frequency @ T_j = 125°C

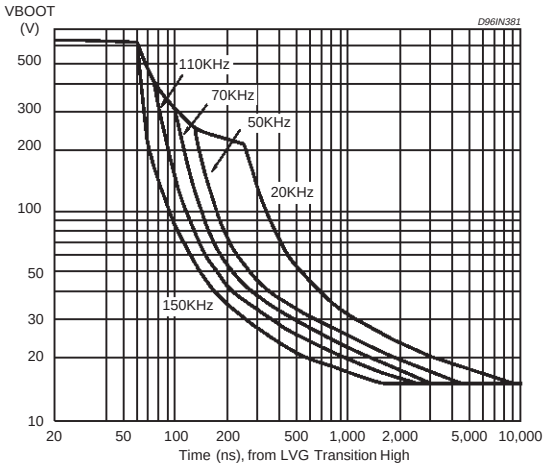


Figure 8. V_{boot} pin SOA @ T_j = 125°C

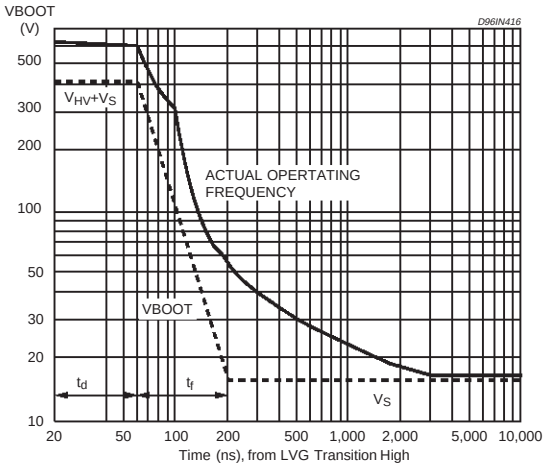
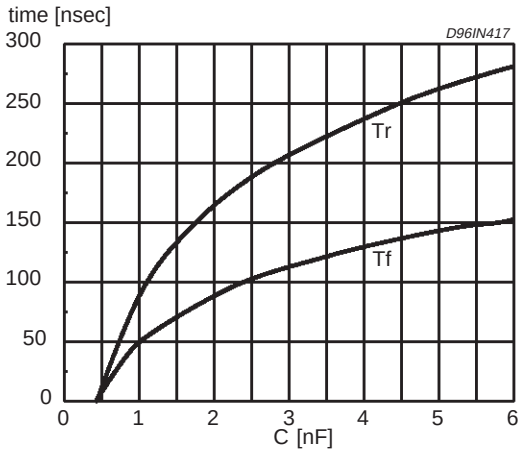


Figure 9. Typical Rise and Fall Times vs. Load Capacitance



For both high and low side buffers @25°C Tamb

Figure 10. Quiescent Current vs. Supply Voltage.

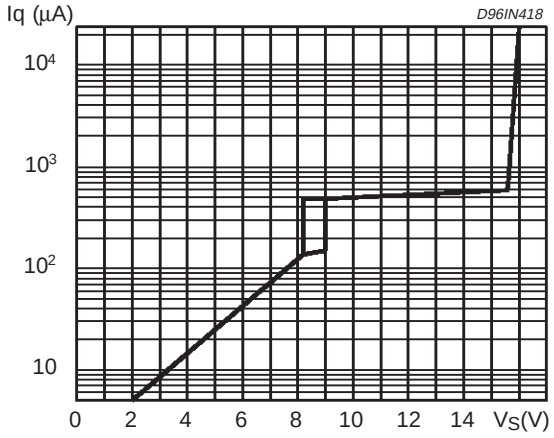


Figure 11. CFL Demoboard 110/220V Inputs.

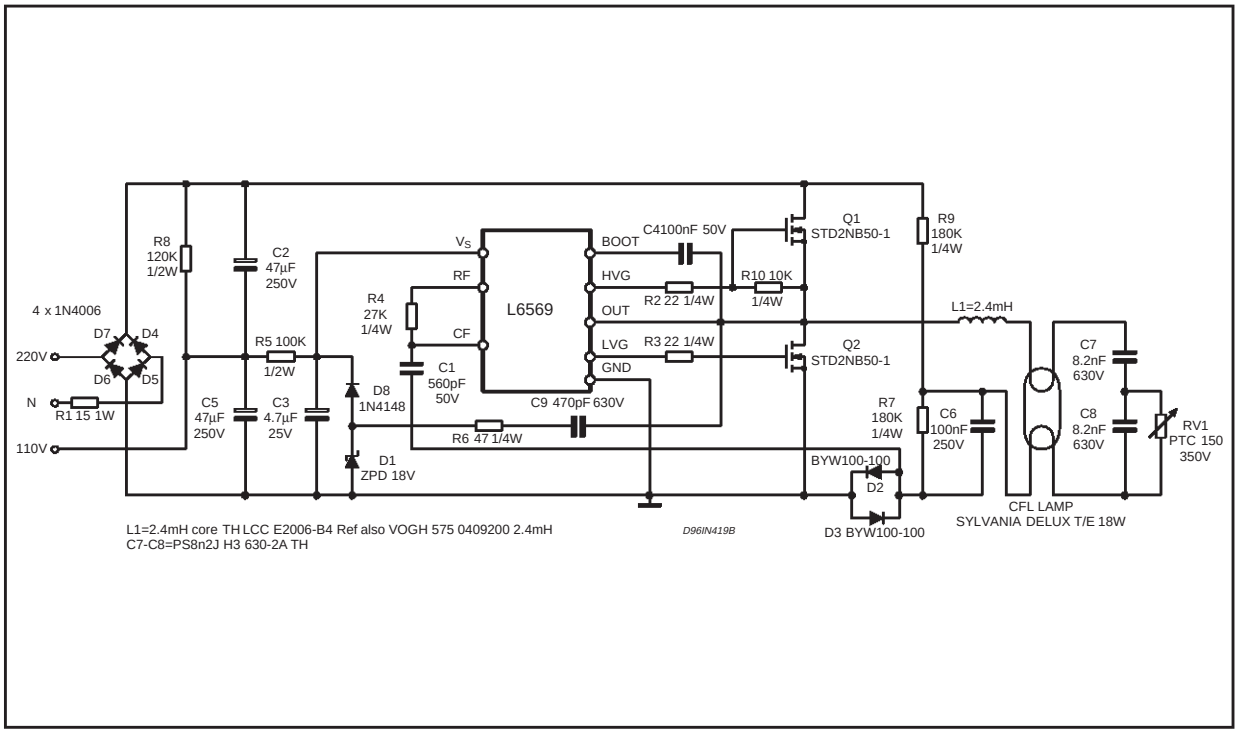
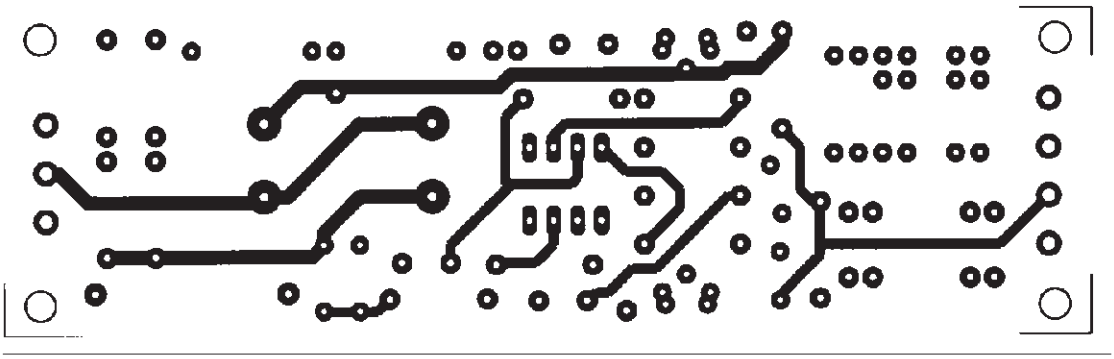
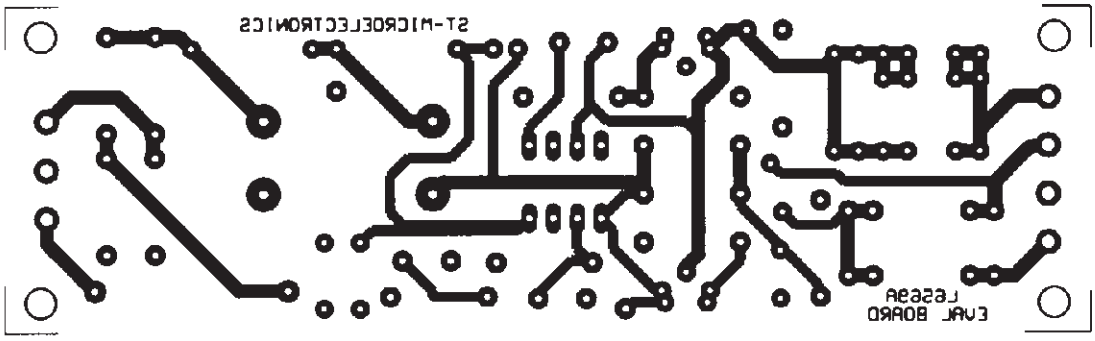


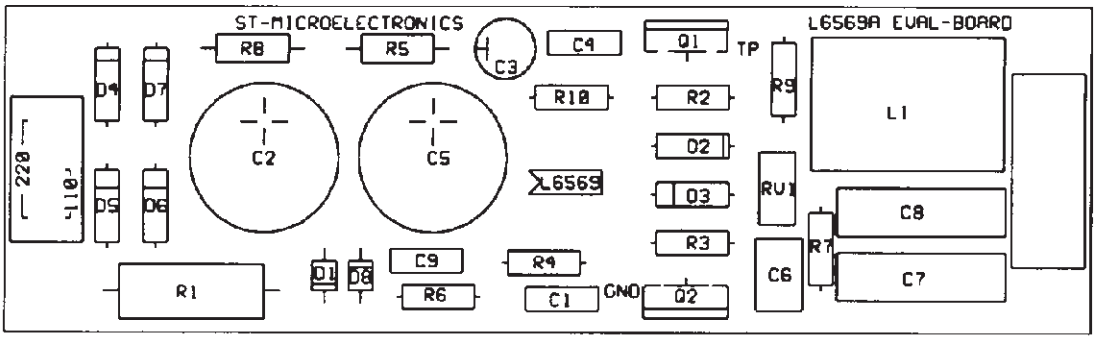
Figure 12. PC Board and Components Layout.



Component Side



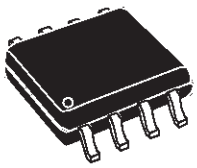
Copper Side



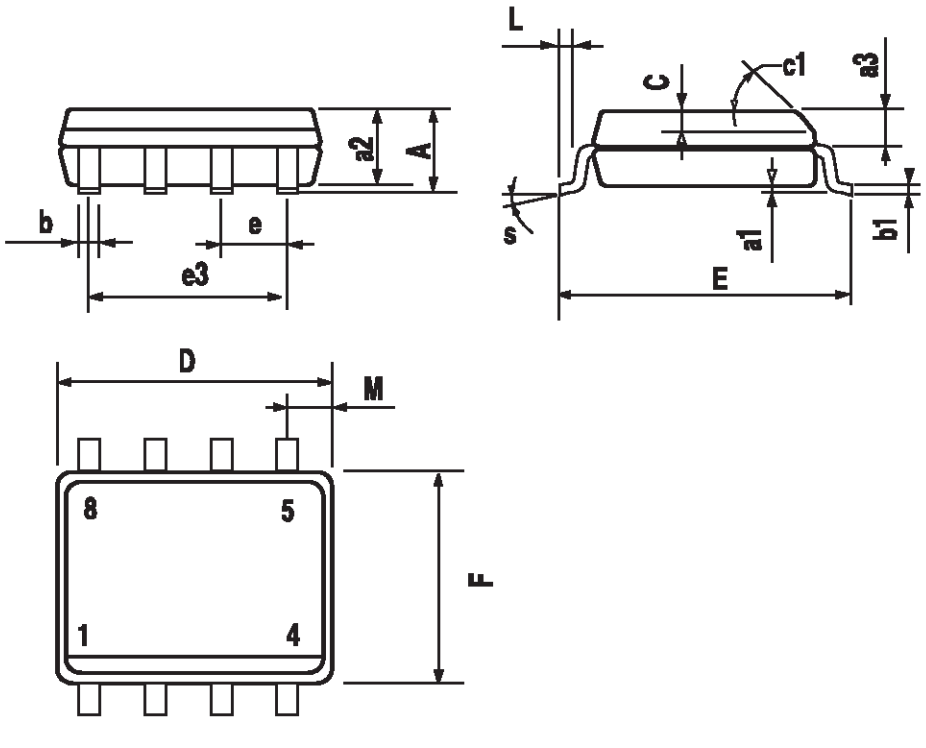
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).

OUTLINE AND MECHANICAL DATA

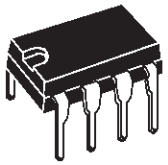


SO8



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

OUTLINE AND MECHANICAL DATA



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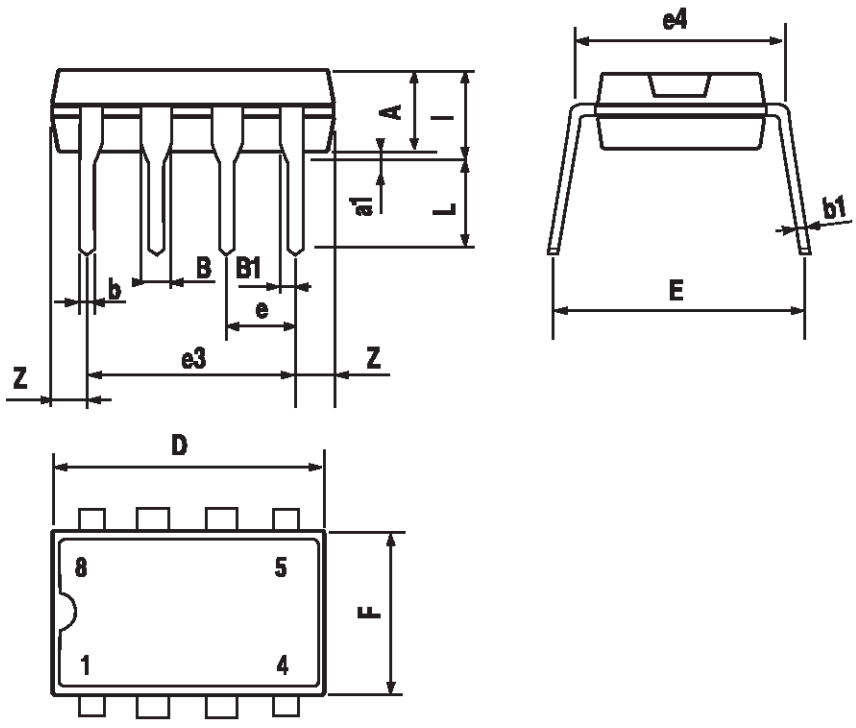

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