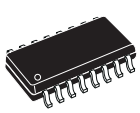
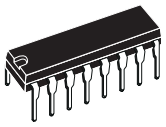
L6574

CFL/TL BALLAST DRIVER PREHEAT AND DIMMING

- HIGH VOLTAGE RAIL UP TO 600V
- dV/dt IMMUNITY ± 50 V/ns IN FULL TEMPERATURE RANGE
- DRIVER CURRENT CAPABILITY:
  250mA SOURCE
  450mA SINK
- SWITCHING TIMES 80/40ns RISE/FALL
- WITH 1nF LOAD
- CMOS SHUT DOWN INPUT
- UNDER VOLTAGE LOCK OUT
- PREHEAT AND FREQUENCY SHIFTING TIMING
- SENSE OP AMP FOR CLOSED LOOP CONTROL OR PROTECTION FEATURES
- HIGH ACCURACY CURRENT CONTROLLED OSCILLATOR
- INTEGRATED BOOTSTRAP DIODE
- CLAMPING ON VS.
- SO16, DIP 16 PACKAGES





SO16N **DIP16**

ORDERING NUMBERS:
L6574D **L6574**

DESCRIPTION

In order to ensure voltage ratings in excess of 600V, the L6574 is manufactured with BCD OFF LINE technology, which makes it well suited for lamp ballast applications.

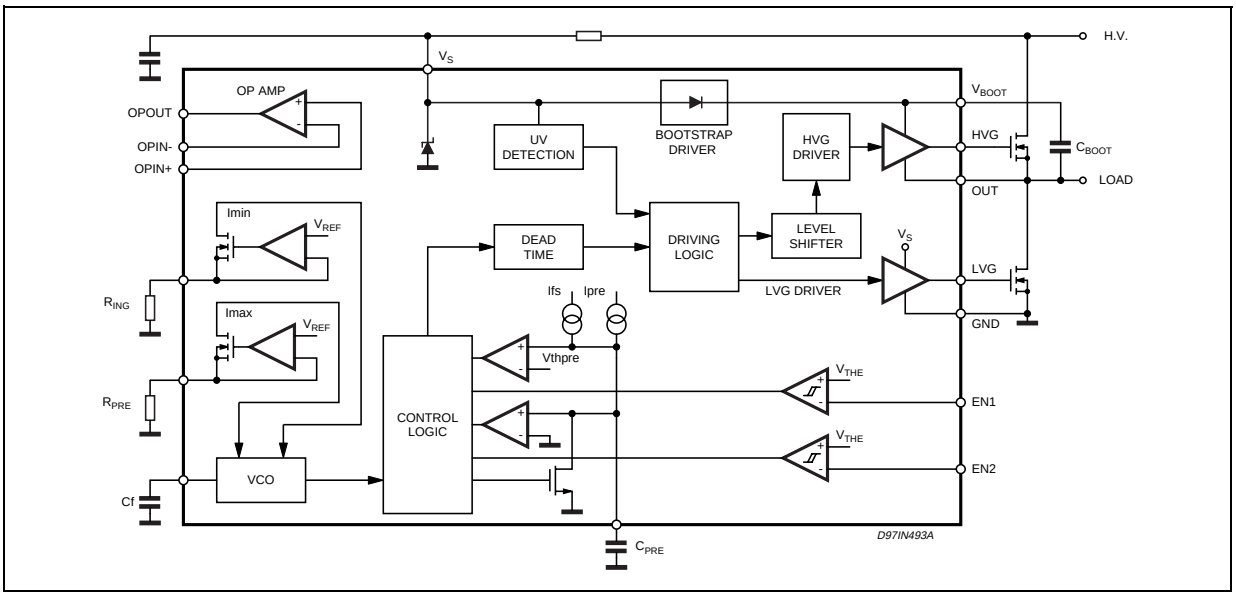
The device is intended to drive two power MOSFETS, in the classical half bridge topology, ensuring all the features needed to drive and properly control a fluorescent bulb.

A dedicated timing section in the L6574 allows the user set the necessary parameters for proper preheat and ignition of the lamp.

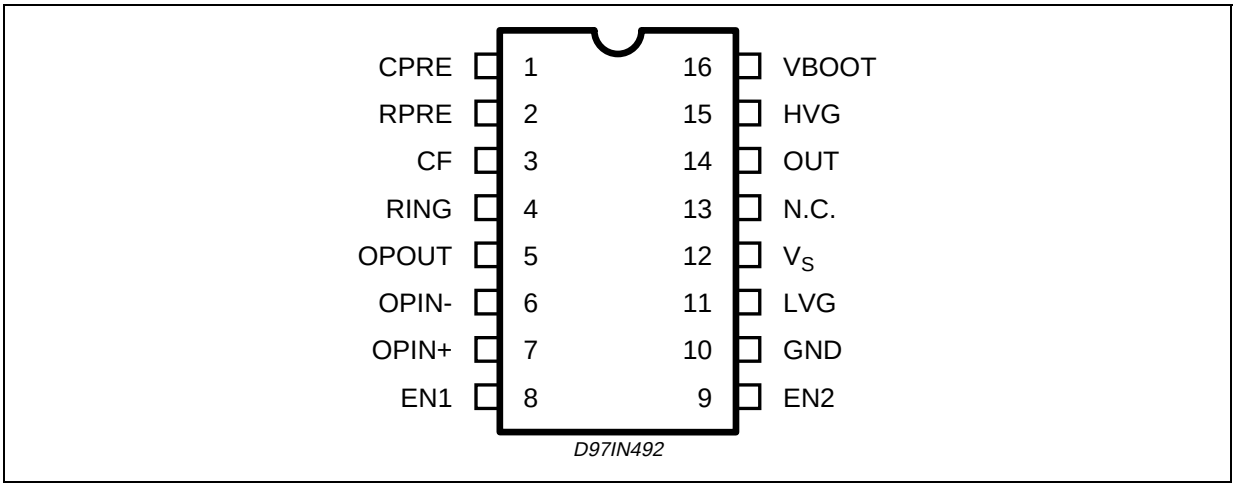
Also, an OP AMP is available to implement closed loop control of the lamp current during normal lamp burning.

An integrated bootstrap section, eliminating the normally required bootstrap diode and the zener clamping on Vs, makes the L6574 well suited for low cost applications where few additional components are needed to build a high performance ballast.

BLOCK DIAGRAM



PIN CONNECTION (top view)



THERMAL DATA

Symbol	Parameter		DIP16	SO16N	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to ambient	Max.	80	120	°C/W

PIN DESCRIPTION

N°	Pin	Function
1	CPRE	Preheat Timing Capacitor. The capacitor C_{PRE} sets the preheating and the frequency shift time, according to the relations: $t_{PRE} = K_{PRE} \cdot C_{PRE}$ and $t_{SH} = K_{FS} \cdot C_{PRE}$ (typ. K_{PRE} = 1.5s/µF, K_{FS} = 0.15s/µF). This feature is obtained by charging CPRE with two different currents. During tPRE this current is independent of the external components, so CPRE is charged up to 3.5V (preheat timing comparator threshold). During t_{SH} the current depends on R_{PRE} value (i.e. on the difference between f_{PRE} and f_{IGN}). In this way t_{SH} is always set at $0.1t_{PRE}$. In steady state the voltage at pin 1 is 5V.
2	RPRE	Maximum Oscillation Frequency Setting. The resistance connected between this pin and ground sets the fPRE value, fixing the difference between f_{PRE} and f_{IGN} ($f_{PRE} > f_{IGN}$). At the end of the Start-up procedure, the effect current drown from R_{PRE} is over. The voltage at this pin is fixed at V_{REF} =2V.
3	CF	Oscillator Frequency Setting. The capacitor C_F, along with to R_{PRE} and R_{IGN}, sets f_{PRE} and f_{ING}. In normal operation this pin shows a triangular wave.
4	RIGN	Minimum Oscillation Frequency Setting. The resistance connected between this pin and ground sets the f_{IGN} value. The voltage at this pin is fixed at V_{REF} =2V.
5	OPout	Out of the operational amplifier. To implement a feedback control loop this pin can be connected to the RIGN pin by means an appropriate circuitry.
6	OPin-	Inverting Input of the operational amplifier.
7	OPin+	Non Inverting Input of the operational amplifier.
8	EN1	Enable 1. This pin (active high), forces the device in a latched shutdown state (like in the under voltage conditions). There are two ways to resume normal operation: – the first is to reduce the supply voltage below the undervoltage threshold and then increase it again until the valid supply is recognised. – the second is activating EN2 input. The enable 1 is especially designed for strong fault (e.g. in case of lamp disconnection).

PIN DESCRIPTION (continued)

N°	Pin	Function
9	EN2	Enable 2. EN2 input (active high) restarts the start-up procedure (preheating and ignition sequence). This features is useful if the lamp does not turn-on after the first ignition sequence .
10	GND	Ground.
11	LVG	Low Side Driver Output. This pin must be connected to the low side power MOSFET gate of the half bridge. A resistor connected between this pin and the power MOS gate can be used to reduce the peak current.
12	VS	Supply Voltage. This pin, connected to the supply filter capacitor, is internally clamped (15.6V typical).
13	N.C.	Non Connected. This pin set a distance between the pins related to the HV and those related to the LV side.
14	OUT	High Side Driver Floating Reference. This pin must be connected close to the source of the high side power MOS or IGBT.
15	HVG	High Side Driver Output. This pin must be connected to the high side power MOSFET gate of the half bridge. A resistor connected between this pin and the power MOS gate can be used to reduce the peak current.
16	VBOOT	Bootstrapped Supply Voltage. Between this pin and VS must be connected the bootstrap capacitor. A patented integrated circuitry replaces the external bootstrap diode, by means of a high voltage DMOS, synchronously driven with the low side power MOSFET.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_S	Supply Current (*)	25	mA
V_{LVG}	Low Side Output	-0.3 to Vs +0.3	V
V_{OUT}	High Side Reference	-1 to VBOOT -18	V
V_{HVG}	High Side Output	-1 to VBOOT	V
V_{BOOT}	Floating Supply Voltage	-1 to 618	V
dV_{BOOT}/dt	V_{BOOT} pin Slew rate (repetitive)	±50	V/ns
dV_{OUT}/dt	OUT pin Slew Rate (repetitive)	±50	V/ns
V_{ir}	Forced Input Voltage (pins Ring, Rpre)	-0.3 to 5	V
V_{ic}	Forced Input Voltage (pins Cpre, Cf)	-0.3 to 5	V
V_{EN1}, V_{EN2}	Enable Input Voltage	-0.3 to 5	V
I_{EN1}, I_{EN2}	Enable Input Current	±3	mA
V_{opc}	Sense Op Amp Common Mode Range	-0.3 to 5	V
V_{opd}	Sense Op Amp Differential Mode Range	±5	V
V_{opo}	Sense Op Amp Output Voltage (forced)	4.6	V
T_{stg}, T_j	Storage Temperature	-40 to +150	°C
T_{amb}	Ambient Temperature	-40 to +125	°C

(*) The device has an internal Clamping Zener between GND and the V_{CC} pin, it must not be supplied by a Low Impedance Voltage Source.

Note: ESD immunity for pins 14, 15 and 16 is guaranteed up to 900V (Human Body Model)

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	10 to V_{CL}	V
V_{OUT} (*)	High Side Reference	-1 to V_{BOOT}-V_{CL}	V
V_{BOOT} (*)	Floating Supply Voltage	500	V

(*) If the condition Vboot - Vout < 18 is guaranteed, Vout can range from -3 to 580V.

ELECTRICAL CHARACTERISTCS

(V_S = 12V; V_{BOOT}-V_{OUT} = 12V; T_{amb} = 25°C)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage							
V_{suvp}	12	V_S Turn On Threshold		9.5	10.2	10.9	V
V_{suvn}		V_S Turn Off Threshold		7.3	8	8.7	V
V_{suvh}		Supply Voltage Under Voltage Hysteresys			2.2		V
V_{cl}		Supply Voltage Clamping		14.6	15.6	16.6	V
I_{su}		Start Up Current	$V_S < V_{suvn}$			250	µA
I_q		Quiescent Current, fout = 60kHz, no load.	$V_S > V_{supv}$		2		mA
High voltage Section							
$I_{bootleak}$	16	BOOT pin leakage current	V_{BOOT} = 580V			5	µA
$I_{outleak}$	14	OUT pin Leakage Current	V_{OUT} = 562V			5	µA
High/Low Side Drivers							
I_{hvgso}	15	High Side Driver Source Current	V_{HVG}-V_{OUT} = 0	170	250		mA
I_{hvgsi}	15	High Side Driver Sink Current	V_{HVG}-V_{BOOT} = 0	300	450		mA
I_{hvgso}	11	Low Side Drive Source Current	VLVG-GND = 0	170	250		mA
I_{lvgsi}	11	Low Side Drive Source Current	V_{LVG}-V_S = 0	300	450		mA
t_{rise}	15, 11	Low/High Side Output Rise Time	C_{load} = 1nF		80	120	ns
t_{fall}		Low/High Side Output Fall Time	C_{load} = 1nF		50	80	ns
Oscillator							
Dc	14	Output Duty Cycle		48	50	52	%
f_{ing}	14	Minimum Output Oscillation Frequency	C_F = 470pF; R_{ing} = 50kΩ	58.2	60	61.8	kHz
f_{pre}	14	Maximum Output Oscillation Frequency	C_F = 470pF; R_{ing} = 50kΩ; R_{pre} = 47kΩ	114	120	126	kHz
V_{ref}	2,4	Voltage to current converters threshold		1.9	2	2.1	V
I_{Vref}	2,4	Reference Current		0		120	µA
t_d	14	Dead Time between Low and High Side Conduction		0.8	1.25	1.7	µs

ELECTRICAL CHARACTERISTCS (continued)
(V_S = 12V; V_{BOOT}-V_{OUT} = 12V; T_{amb} = 25°C)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Timing Section							
k_{pre}	1	Pre Heat Timing constant	C_{pre} = 330nF	1.15	1.5	1.85	s/µF
k_{fs}		Frequency Shift Timing Constant	C_{pre} = 330nF	0.115	0.15	0.185	s/µF
V_{thpre}		Pre Heat Timing Comparator Threshold		3.3	3.5	3.7	V
Sense OP AMP							
I_{ib}	6,7	Input Bias current				0.1	µA
V_{io}		Input Offset Voltage		-10		10	mV
R_{out}	5	Ouput Resistance		200		300	Ω
I_{out+}		Sink Output Current	V_{out} = 0.2V	0.5			mA
I_{out-}		Source Output Current	V_{out} = 4.5V	0.5			mA
V_{ic}	6,7	Common Mode Input Range		-0.2		3	V
GBW		Sense Op Amp Gain Band Width Product			1		MHz
Gdc		DC Open Loop Gain			80		dB
Comparators							
V_{the}	8,9	Enabling Comparators Threshold		0.56	0.6	0.64	V
V_{hy}e		Enabling Comparators Hysteresis		20		100	mV
t_{pulse}		Minimum Pulse lenght			200		ns

High/Low Side Driving Section:

High and low side driving sections provide the proper drive to the external power MOSFET. A high sink/ source driving current (450/250 mA typical) ensures fast switching times when a size 4 external power MOSFET needs to be driven.

Bootstrap Section:

A patented integrated bootstrap section replaces an external bootstrap diode. This section together with a bootstrap capacitor provides the bootstrap voltage to drive the high side power MOSFET. This function is achieved using a high voltage DMOS driver which is driven synchronously with the low side external power MOSFET.

For a safe operation, current flow into the Vboot pin is inhibited, even though ZVS operation may not be ensured.

Timing Section:

To set the proper preheat time (tpre=kpre*Cpre) for the bulb, a capacitor is connected to the Cpre pin which is charged with a fixed current. During tpre, the output is switching at fpre (see Oscillator Section). When the tpre expires, the Cpre capacitor is discharged and then recharged with a different current. This sets a second time interval tsh (0.1 times the selected preheat time tpre) during which frequency shifting from fpre to fing is performed to ensure lamp ignition.

Oscillator Section:

A voltage controlled oscillator, with the selected frequencies fpre and fing, drives the output half bridge. Independently selected, fpre is effective during tpre and fing is effective during normal lamp burning. When working open loop, fpre and fing are the highest and lowest allowed oscillation frequencies.

Closed loop control of the lamp current under normal operation can be achieved with the L6574. This is accomplished by automatic adjustment of the oscillator frequency. The OP AMP output is fed through a resistor diode network to the Ring pin. See AN 993.

OP AMP Section:

The integrated OP AMP offers low output impedance, wide bandwidth, high input impedance and wide common mode range. It can be readily used to implement closed loop control (see Oscillator Section) of the lamp current.

EN1, EN2 Comparators:

Two CMOS comparators, with thresholds set at 0.6 V (typical) are available to implement protection methods (such as overvoltage, lamp removal, etc.). Short pulses (>200nsec) at the comparator inputs are recognized.

The EN1 input (active high) forces the L6574 in the shut down state (e.g. LVG low, HVG low, oscillator stopped) in the event of an undervoltage condition. Normal operating condition is resumed after a power-off power-on sequence or when EN2 input is high.

The EN2 input (active high) also restarts a preheat sequence (see timing diagrams).

TIMING DIAGRAMS

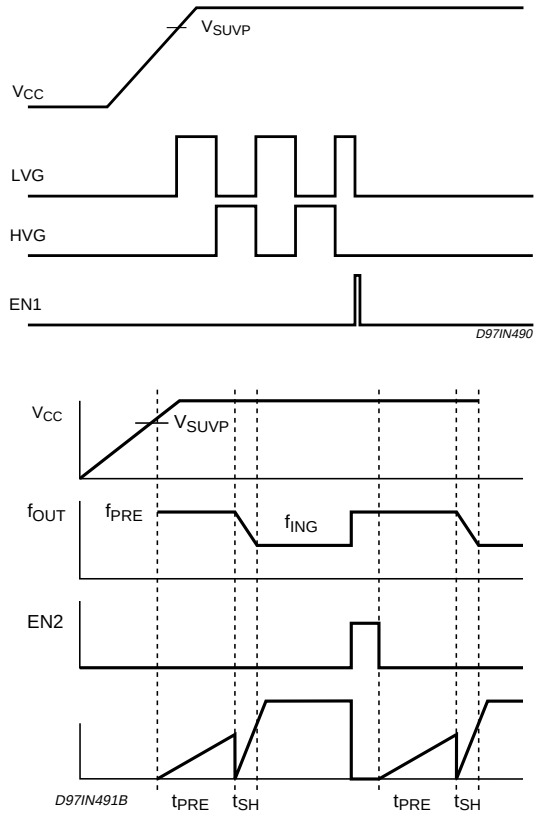


Figure 1. f_{ING} vs. R_{ING}.

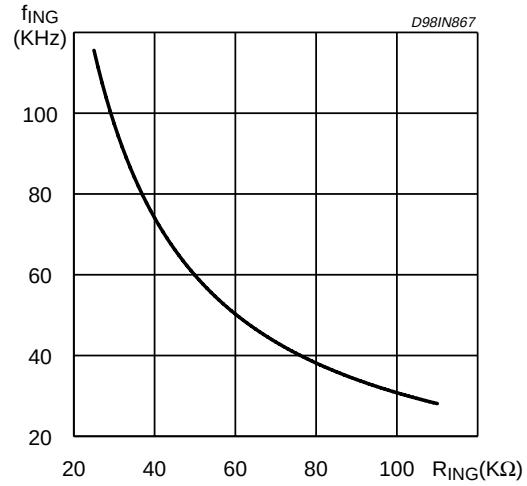


Figure 2. Δf vs. R_{PRE}, with R_{ING} = 33kΩ

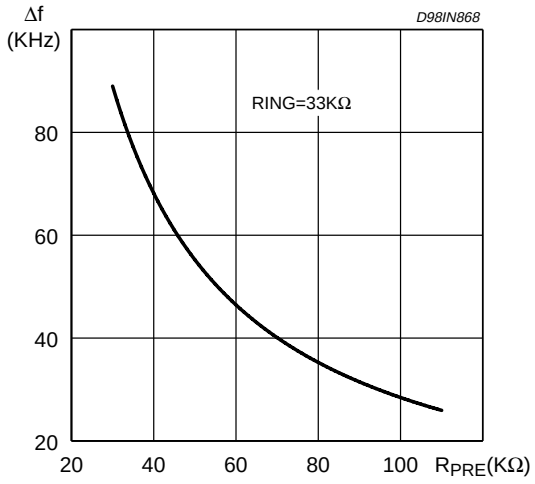


Figure 3. Δf vs. R_{PRE}, with R_{ING} = 50kΩ

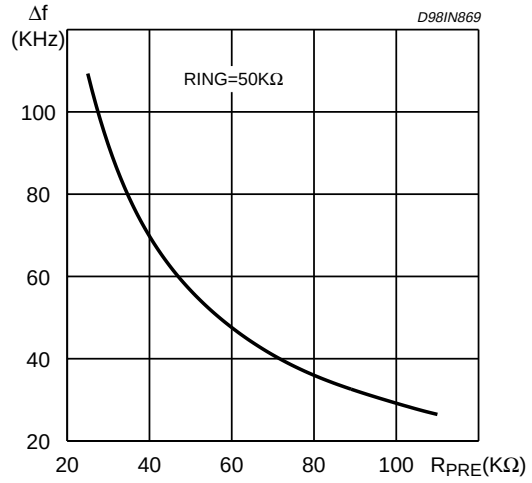


Figure 4. Δf vs. R_{PRE}, with R_{ING} = 100kΩ

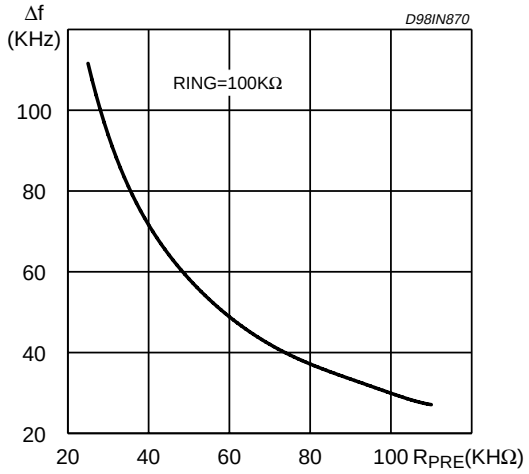


Figure 5. f_{ING} vs. temperature.

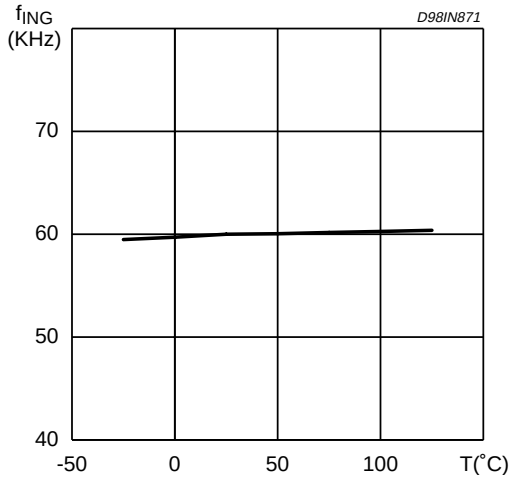
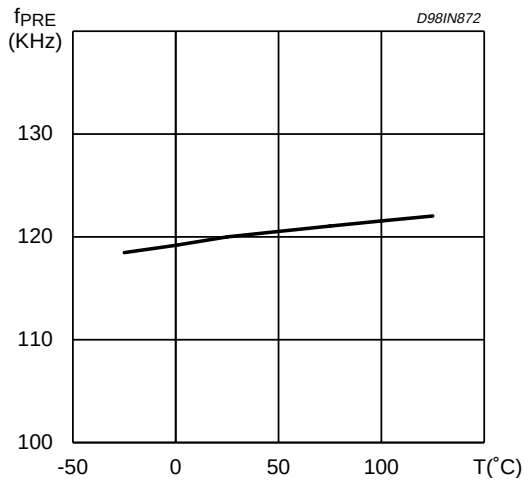


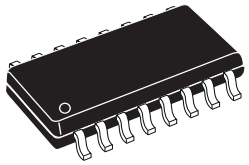
Figure 6. f_{PRE} vs. temperature.



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45˚ (typ.)					
D (1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F (1)	3.8		4	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.4		1.27	0.016		0.050
M			0.62			0.024
S	8˚(max.)					

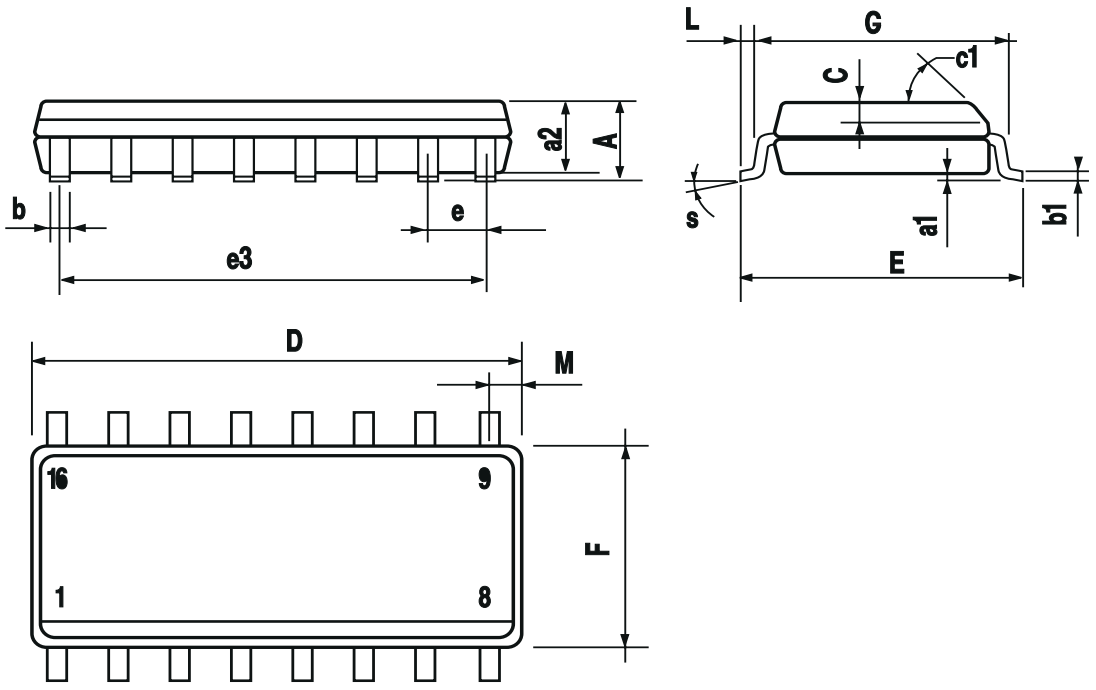
OUTLINE AND MECHANICAL DATA

Weight: 0.20gr



SO16 Narrow

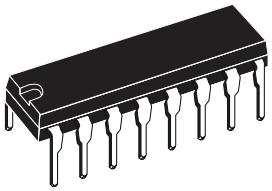
(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).



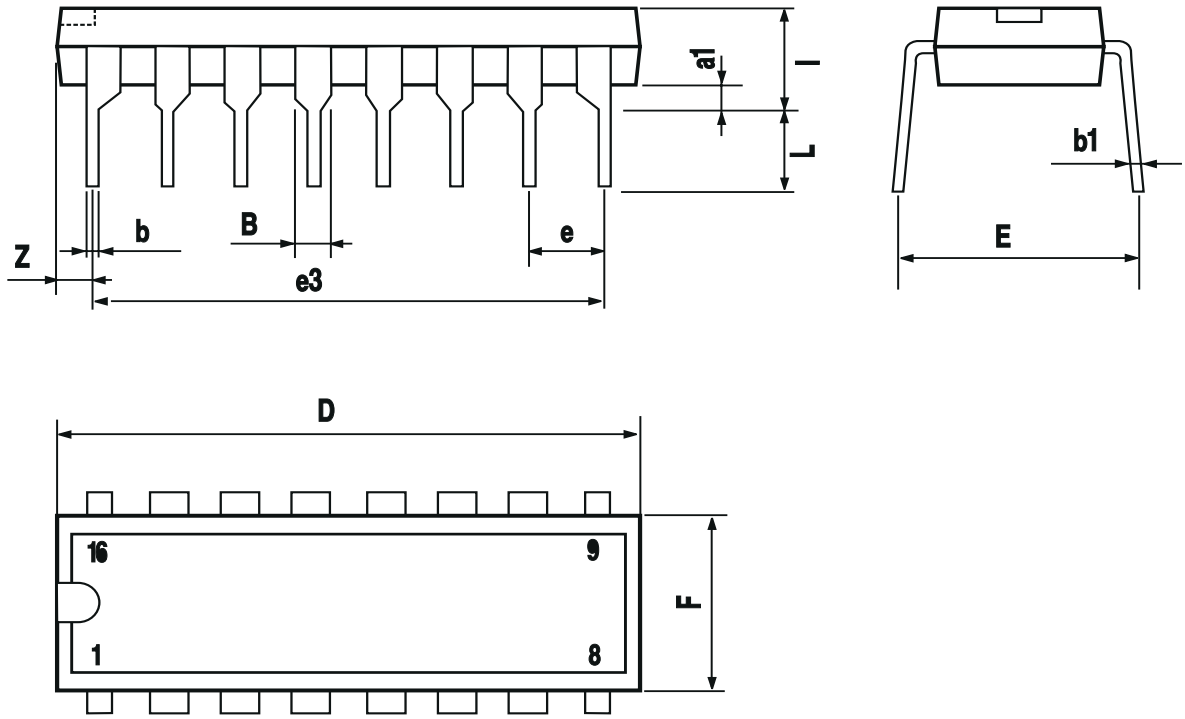
0016020

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA



DIP16



X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Gate Drivers ***category:***

Click to view products by STMicroelectronics ***manufacturer:***

Other Similar products are found below :

00053P0231 56956 57.404.7355.5 LT4936 57.904.0755.0 5882900001 00600P0005 00-9050-LRPP 00-9090-RDPP 5951900000 01-1003W-10/32-15 0131700000 00-2240 LTP70N06 LVP640 5J0-1000LG-SIL LY1D-2-5S-AC120 LY2-US-AC240 LY3-UA-DC24 00576P0020 00600P0010 LZN4-UA-DC12 LZNQ2M-US-DC5 LZNQ2-US-DC12 LZP40N10 00-8196-RDPP 00-8274-RDPP 00-8275-RDNP 00-8722-RDPP 00-8728-WHPP 00-8869-RDPP 00-9051-RDPP 00-9091-LRPP 00-9291-RDPP 0207100000 0207400000 01312 0134220000 60713816 M15730061 61161-90 61278-0020 6131-204-23149P 6131-205-17149P 6131-209-15149P 6131-218-17149P 6131-220-21149P 6131-260-2358P 6131-265-11149P CS1HCPU63