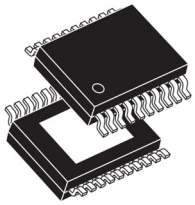
L6730
L6730B

Adjustable step-down controller with synchronous rectification

Features

- Input voltage range from 1.8 V to 14 V
- Supply voltage range from 4.5 V to 14 V
- Adjustable output voltage down to 0.6 V with ±0.8% accuracy over line voltage and temperature (0°C~125°C)
- Fixed frequency voltage mode control
- t_{ON} lower than 100 ns
- 0% to 100% duty cycle
- Selectable 0.6 V or 1.2 V internal voltage reference
- External input voltage reference
- Soft-start and inhibit
- High current embedded drivers
- Predictive anti-cross conduction control
- Selectable uvlo threshold (5 V or 12 V BUS)
- Programmable high-side and low-side $R_{DS(on)}$ sense overcurrent protection
- Switching frequency programmable from 100 kHz to 1 MHz
- Master/slave synchronization with 180° phase shift
- Pre-bias start up capability (L6730)
- Selectable source/sink or source only capability after soft-start (L6730)
- Selectable constant current or hiccup mode overcurrent protection after soft-start (L6730B)
- Power Good output with programmable delay
- Overvoltage protection with selectable latched/not-latched mode
- Thermal shut-down
- Package: HTSSOP20



HTSSOP20

Applications

- High performance / high density DC-DC modules
- Low voltage distributed DC-DC
- niPOL converters
- DDR memory supply
- DDR memory bus termination supply

Table 1. Device summary

Order codes	Package	Packing
L6730	HTSSOP20	Tube
L6730TR	HTSSOP20	Tape and reel
L6730B	HTSSOP20	Tube
L6730BTR	HTSSOP20	Tape and reel

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1 Summary description

The controller is an integrated circuit designed using BiCMOS-DMOS, v5 (BCD5) technology that provides complete control logic and protection for high performance, step-down DC/DC and niPOL converters.

It is designed to drive N-Channel MOSFETs in a synchronous rectified buck converter topology. The output voltage of the converter can be precisely regulated down to 600 mV, with a maximum tolerance of ±0.8%, or to 1.2 V, when one of the internal references is used. It is also possible to use an external reference from 0 V to 2.5 V.

The input voltage can range from 1.8 V to 14 V, while the supply voltage can range from 4.5 V to 14 V. High peak current gate drivers provide for fast switching to the external power section and the output current can be in excess of 20 A, depending on the number of the external MOSFETs used. The PWM duty cycle can range from 0% to 100% with a minimum on-time ($T_{ON(MIN)}$) lower than 100 ns, making conversions with a very low duty cycle and very high switching frequency possible.

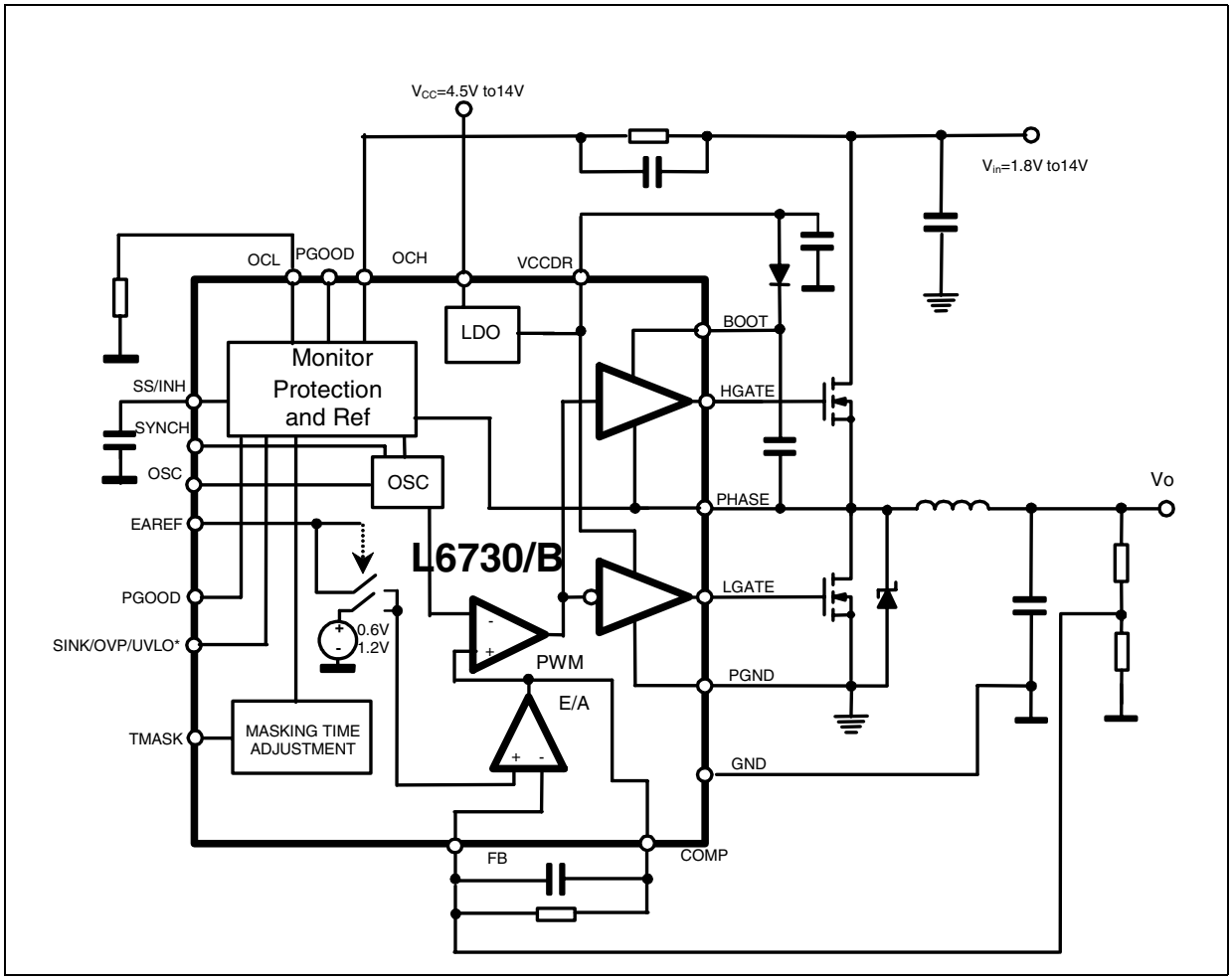
The device provides voltage-mode control. It includes a 400 kHz free-running oscillator that is adjustable from 100 kHz to 1 MHz. The error amplifier features a 10 MHz gain-bandwidth-product and 5 V/µs slew-rate that permits to realize high converter bandwidth for fast transient response. The device monitors the current by using the $R_{DS(ON)}$ of both the high-side and low-side MOSFET(s), eliminating the need for a current sensing resistor and guaranteeing an effective over current-protection in all the application conditions. When necessary, two different current limit protections can be externally set through two external resistors. A leading edge adjustable blanking time is also available to avoid false over-current-protection (OCP) intervention in every application condition.

It is possible to select the HICCUP mode or the constant current protection (L6730B) after the soft-start phase.

During this phase constant current protection is provided. It is possible to select the sink-source or the source-only mode capability (before the device powers on) by acting on a multifunction pin (L6730). The L6730 disables the sink mode capability during the soft-start in order to allow a proper start-up also in pre-biased output voltage conditions. The L6730B can always sink current and, so it can be used to supply the DDR memory BUS termination. Other features include Master-Slave synchronization (with 180° phase shift), Power-Good with adjustable delay, over voltage-protection, feed back disconnection, selectable UVLO threshold (5 V and 12 V Bus), and thermal shutdown. The HTSSOP20 package allows the realization for very compact DC/DC converters.

1.1 Functional description

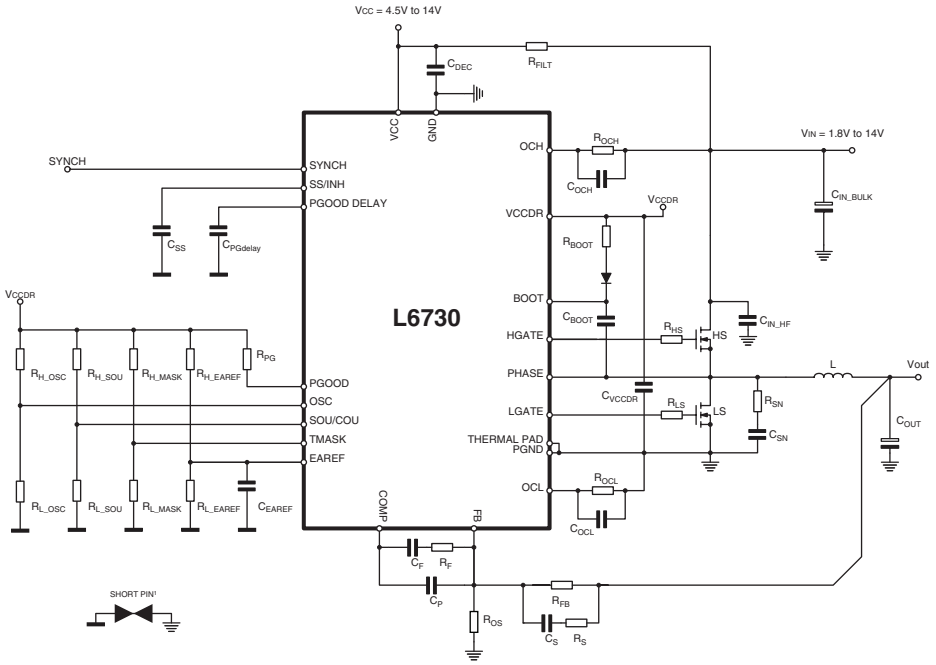
Figure 1. Block diagram



Note: In the L6730B the multifunction pin is: CC/OVP/UVLO.

1.2 Application circuit

Figure 2. Application circuit



NOTE 1: In module application it is recommended to place the short pin on the module where device is mounted.

2 Electrical data

2.1 Maximum rating

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND and PGND, OCH, PGOOD	-0.3 to 18	V
V_{BOOT} - V_{PHASE}	Boot voltage	0 to 6	V
V_{HGATE} - V_{PHASE}		0 to V_{BOOT} - V_{PHASE}	V
V_{BOOT}	BOOT	-0.3 to 24	V
V_{PHASE}	PHASE	-1 to 18	V
	PHASE spike, transient < 50ns (F_{SW} = 500kHz)	-3	
		+24	
	SS, FB, EAREF, SYNC, OSC, OCL, LGATE, COMP, S/O/U, TMASK, PGOODELAY, V_{CCDR}	-0.3 to 6	V
OCH Pin	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002 “human body model” acceptance criteria: “normal performance”	±1500	V
PGOOD Pin		±1000	
OTHER PINS		±2000	

2.2 Thermal data

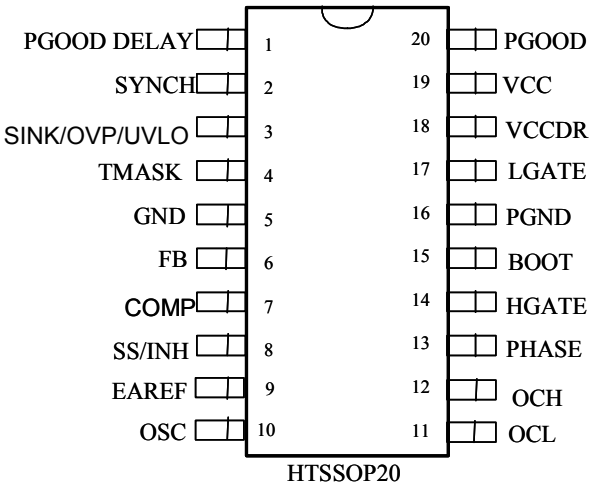
Table 3. Thermal data

Symbol	Description	Value	Unit
R_{thJA} (1)	Max. thermal resistance junction to ambient	50	°C/W
T_{STG}	Storage temperature range	-40 to +150	°C
T_J	Junction operating temperature range	-40 to +125	°C
T_A	Ambient operating temperature range	-40 to +85	°C

1. Package mounted on demonstration board

3 Pin connections and functions

Figure 3. Pins connection (top view)



Note: In the L6730B the multifunction pin is: CC/OVP/UVLO.

Table 4. Pin connection

Pin n.	Name	Description
1	PGOOD DELAY	A capacitor connected between this pin and GND introduces a delay between the internal PGOOD comparator trigger and the external signal rising edge. No delay can be introduced on the falling edge of the PGOOD signal. The delay can be calculated with the following formula: $PGDelay = 0.5 \cdot C(pF)$ [µs]
2	SYNCH	Two or more devices can be synchronized by connecting the SYNCH pins together. The device operating with the highest Fsw will be the Master device. The Slave devices will operate at 180° phase shift from the Master. The best way to synchronize devices is to set their Fsw at the same value. If it is not used, the SYNCH pin can be left floating.
3	SINK/OVP/UVLO L6730 CC/OVP/UVLO L6730B	With this pin it is possible: To enable-disable the sink mode current capability after SS (L6730); To enable-disable the constant current OCP after SS (L6730B); To enable-disable the latch mode for the OVP; To set the UVLO threshold for the 5 V BUS and 12 V BUS. The device captures the analog value present at this pin at the start-up when V_{CC} meets the UVLO threshold.

Table 4. Pin connection (continued)

Pin n.	Name	Description
4	T_{MASK}	The user can select two different values for the leading edge blanking time on the peak overcurrent protection by connecting this pin to V_{CCDR} or GND. The device captures the analog value present at this pin at the start-up when V_{CC} meets the UVLO threshold.
5	GND	All the internal references are referenced to this pin. Connect to the PCB signal ground.
6	FB	This pin is connected to the error amplifier inverting input. Connect it to Vout through the compensation network. This pin is also used to sense the output voltage in order to manage the over voltage conditions and the PGood signal.
7	COMP	This pin is connected to the error amplifier output and used to compensate the voltage control loop.
8	SS/INH	The soft-start time is programmed connecting an external capacitor from this pin and GND. The internal current generator forces a current of 10mA through the capacitor. This pin is also used to inhibit the device: when the voltage at this pin is lower than 0.5V the device is disabled.
9	EAREF	It is possible to set two internal references 0.6V / 1.2V or provide an external reference from 0V to 2.5V: V_{EAREF} from 0% to 80% of V_{CCDR} -> external reference V_{EAREF} from 80% to 95% of V_{CCDR} -> V_{REF}=1.2V V_{EAREF} from 95% to 100% of V_{CCDR} -> V_{REF}=0.6V An internal clamp limits the maximum V_{EAREF} at 2.5V (typ.). The device captures the analog value present at this pin at the start-up when V_{CC} meets the UVLO threshold.
10	OSC	Connecting an external resistor from this pin to GND, the external frequency can be increased according with the following equation: $Fsw = 400KHz + \frac{9.88 \cdot 10^6}{R_{OSC}(K\Omega)}$ Connecting a resistor from this pin to V_{CCDR} (5V), the switching frequency can be lowered according with the following equation: $Fsw = 400KHz - \frac{3.01 \cdot 10^7}{R_{OSC}(K\Omega)}$ If the pin is left open, the switching frequency is 400 KHz. Normally this pin is at a voltage of 1.2V. In OVP the pin is pulled up to 4.5V (only in latched mode). Don't connect a capacitor from this pin to GND.

Table 4. Pin connection (continued)

Pin n.	Name	Description
11	OCL	A resistor connected from this pin to ground sets the valley- current-limit. The valley current is sensed through the low-side MOSFET(s). The internal current generator sources a current of 100µA (I_{OCL}) from this pin to ground through the external resistor (R_{OCL}). The over-current threshold is given by the following equation: $I_{VALLEY} = \frac{I_{OCL} \cdot R_{OCL}}{2 \cdot R_{DSonLS}}$ Connecting a capacitor from this pin to GND helps in reducing the noise injected from V_{CC} to the device, but can be a low impedance path for the high-frequency noise related to the GND. Connect a capacitor only to a “clean” GND.
12	OCH	A resistor connected from this pin and the high-side MOSFET(s) drain sets the peak-current-limit. The peak current is sensed through the high-side MOSFET(s). The internal 100µA current generator (I_{OCH}) sinks a current from the drain through the external resistor (R_{OCH}). The over-current threshold is given by the following equation: $I_{PEAK} = \frac{I_{OCH} \cdot R_{OCH}}{R_{DSonHS}}$
13	PHASE	This pin is connected to the source of the high-side MOSFET(s) and provides the return path for the high-side driver. This pin monitors the drop across both the upper and lower MOSFET(s) for the current limit together with OCH and OCL.
14	HGATE	This pin is connected to the high-side MOSFET(s) gate.
15	BOOT	The high-side driver is supplied through this pin. Connect a capacitor from this pin to the PHASE pin, and a diode from V_{CCDR} to this pin (cathode versus BOOT).
16	PGND	This pin has to be connected closely to the low-side MOSFET(s) source in order to reduce the noise injection into the device. Connect to the PCB power ground plane.
17	LGATE	This pin is connected to the low-side MOSFET(s) gate.
18	V_{CCDR}	5V internally regulated voltage. It is used to supply the internal drivers and as a voltage reference. Filter it to GND with at least a 1µF ceramic cap.
19	V_{CC}	Supply voltage pin. The operative supply voltage range is from 4.5V to 14V.
20	PGOOD	This pin is an open collector output and it is pulled low if the output voltage is not within the specified thresholds (90%-110%). If not used it may be left floating. Pull up this pin to V_{CCDR} with a 10K resistor to obtain a logical signal.
-	Thermal PAD	Thermal Pad connects the silicon substrate and makes good thermal contact with the PCB. Connect to the PCB power ground plane.

4 Electrical characteristics

V_{CC} = 12 V, T_A = 25°C unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CC} supply current						
I_{CC}	V_{CC} stand by current	OSC = open; SS to GND		7	9	mA
	V_{CC} quiescent current	OSC= open; HG = open, LG = open, PH=open		8.5	10	
Power-ON						
5V BUS	Turn-ON V_{CC} threshold	V_{OCH} = 1.7V	4.0	4.2	4.4	V
	Turn-OFF V_{CC} threshold	V_{OCH} = 1.7V	3.6	3.8	4.0	
12V BUS	Turn-ON V_{CC} threshold	V_{OCH} = 1.7V	8.3	8.6	8.9	
	Turn-OFF V_{CC} threshold	V_{OCH} = 1.7V	7.4	7.7	8.0	
$V_{IN\ OK}$	Turn-ON V_{OCH} threshold		1.1	1.25	1.47	
	Turn-OFF V_{OCH} threshold		0.9	1.05	1.27	
V_{CCDR} regulation						
	V_{CCDR} voltage	V_{CC} =5.5V to 14V I_{DR} = 1mA to 100mA	4.5	5	5.5	V
Soft start and inhibit						
I_{SS}	Soft start current	SS = 2V	7	10	13	µA
		SS = 0 to 0.5V	20	30	45	
Oscillator						
f_{OSC}	Initial accuracy	OSC = OPEN	380	400	420	kHz
$f_{OSC,RT}$	Total accuracy	RT = 390KΩ to V_{CCDR} RT = 18KΩ to GND	-15		15	%
ΔV_{OSC}	Ramp amplitude			2.1		V
Output voltage (1.2V MODE)						
V_{FB}	Output voltage		1.190	1.2	1.208	V
Output voltage (0.6 MODE)						
V_{FB}	Output voltage		0.597	0.6	0.603	V
Error amplifier						
R_{EAREF}	EAREF input resistance	Vs. GND	70	100	150	kΩ

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{FB}	I.I. bias current	V_{FB} = 0V		0.290	0.5	µA
Ext Ref Clamp			2.3			V
V_{OFFSET}	Error amplifier offset	Vref = 0.6V	-5		+5	mV
G_V	Open loop voltage gain	Guaranteed by design		100		dB
GBWP	Gain-bandwidth product	Guaranteed by design		10		MHz
SR	Slew-rate	COMP = 10pF Guaranteed by design		5		V/µs
Gate drivers						
R_{HGATE_ON}	High side source resistance	V_{BOOT} - V_{PHASE} = 5V		1.7		Ω
R_{HGATE_OFF}	High side sink resistance	V_{BOOT} - V_{PHASE} = 5V		1.12		Ω
R_{LGATE_ON}	Low side source resistance	V_{CCDR} = 5V		1.15		Ω
R_{LGATE_OFF}	Low side sink resistance	V_{CCDR} = 5V		0.6		Ω
Protections						
I_{OCH}	OCH current source	V_{OCH} = 1.7V	90	100	110	µA
I_{OCL}	OCL current source		90	100	110	µA
OVP	Over voltage trip (V_{FB} / V_{EAREF})	V_{FB} rising V_{EAREF} = 0.6V		120		%
		V_{FB} falling V_{EAREF} = 0.6V		117		%
I_{OSC}	OSC sourcing current	V_{FB} > OVP Trip V_{OSC} = 3V		30		mA
Power Good						
	Upper threshold (V_{FB} / V_{EAREF})	V_{FB} rising	108	110	112	%
	Lower threshold (V_{FB} / V_{EAREF})	V_{FB} falling	88	90	92	%
V_{PGOOD}	PGOOD voltage low	I_{PGOOD} = -5mA		0.5		V

Table 6. Thermal characterizations (V_{CC} = 12 V)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Oscillator						
f_{OSC}	Initial accuracy	OSC = OPEN; T_J = 0°C~ 125°C	376	400	424	kHz
Output voltage (1.2V MODE)						
V_{FB}	Output voltage	T_J = 0°C~ 125°C	1.188	1.2	1.212	V
		T_J = -40°C~ 125°C	1.185	1.2	1.212	V
Output voltage (0.6V MODE)						
V_{FB}	Output voltage	T_J = 0°C~ 125°C	0.596	0.6	0.605	V
		T_J = -40°C~ 125°C	0.593	0.6	0.605	V

5 Device description

5.1 Oscillator

The switching frequency is internally fixed to 400 kHz. The internal oscillator generates the triangular waveform for the PWM charging and discharging an internal capacitor (F_{SW} = 400 kHz). This current can be varied using an external resistor (R_T) connected between OSC pin and GND or V_{CCDR} in order to change the switching frequency. Since the OSC pin is maintained at fixed voltage (typ. 1.2 V), the frequency is increased (or decreased) proportionally to the current sunk (sourced) from (into) the pin. In particular by connecting R_T versus GND the frequency is increased (current is sunk from the pin), according to the following relationship:

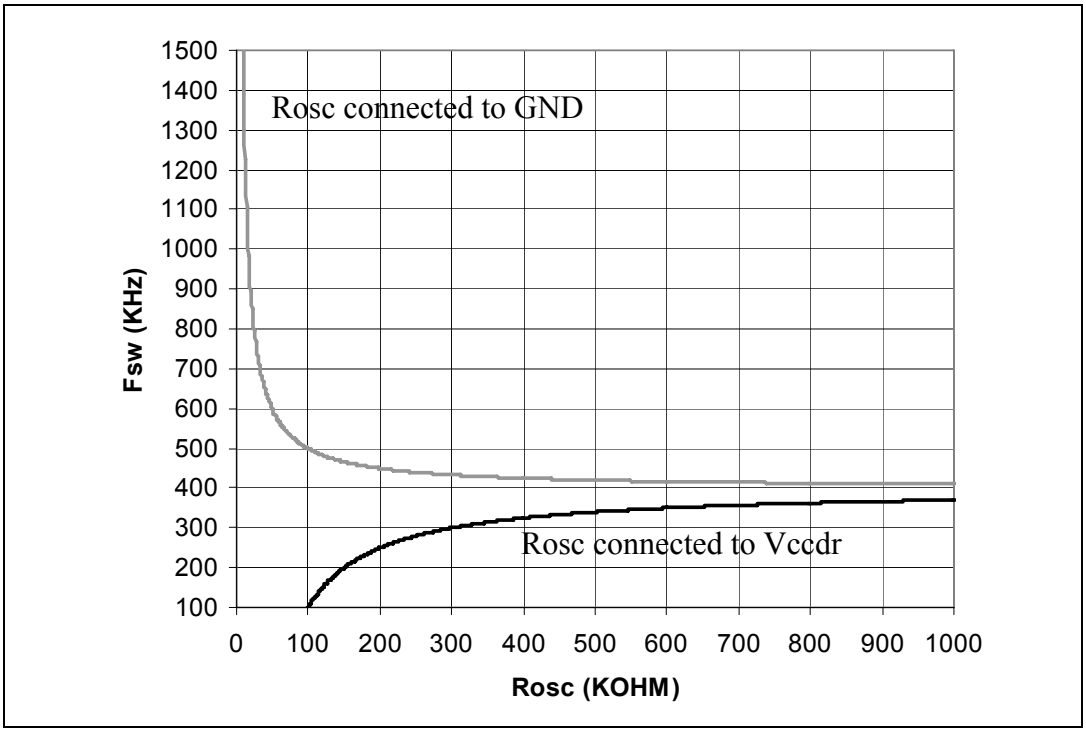
$$Fsw = 400KHz + \frac{9.88 \cdot 10^6}{R_{OSC}(K\Omega)} \quad (1)$$

Connecting R_T to V_{CCDR} reduces the frequency (current is sourced into the pin), according to the following relationship:

$$Fsw = 400KHz - \frac{3.01 \cdot 10^7}{R_{OSC}(K\Omega)} \quad (2)$$

Switching frequency variation vs. R_T is shown in *Figure 4*.

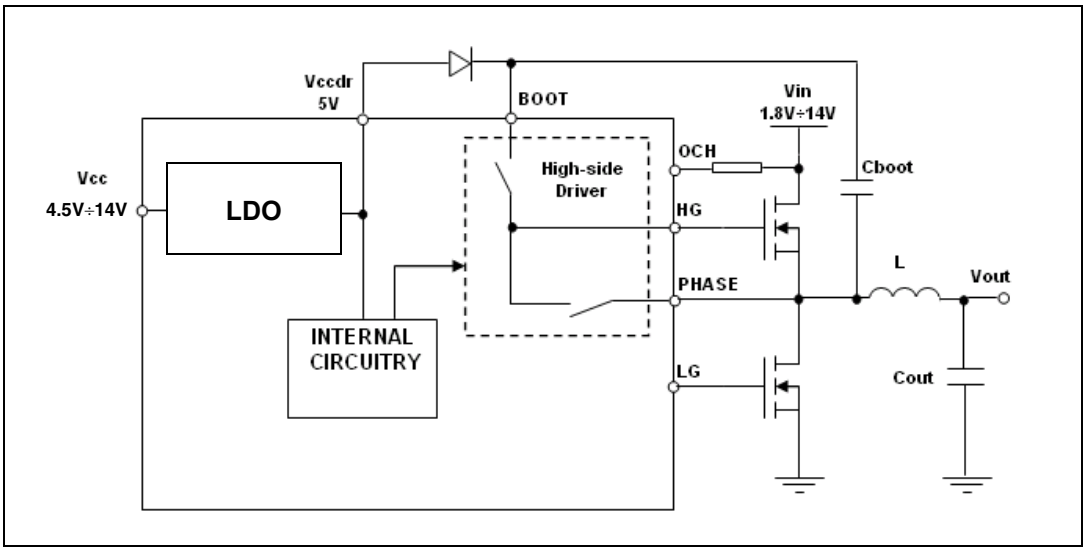
Figure 4. Switching frequency variation versus RT



5.2 Internal LDO

An internal LDO supplies the internal circuitry of the device. The input of this stage is the V_{CC} pin and the output (5 V) is the V_{CCDR} pin (see *Figure 5*).

Figure 5. LDO block diagram



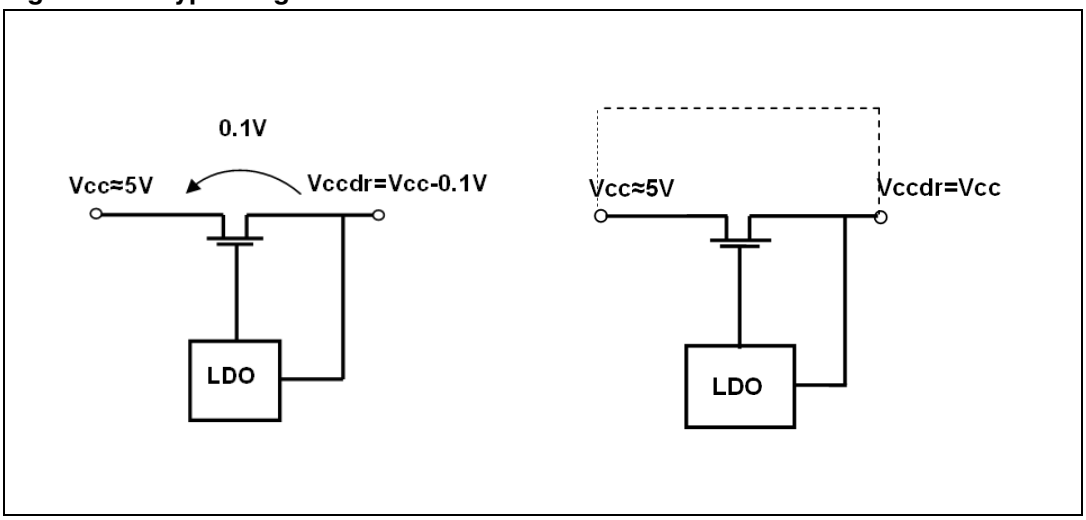
5.3 Bypassing the LDO to avoid the voltage drop with low Vcc

The LDO can be by passed by providing 5 V voltage directly to V_{CCDR}. In this case Vcc and V_{CCDR} pins must be shorted together as shown in *Figure 6.* V_{CCDR} pin must be filtered with at least 1 µF capacitor to sustain the internal LDO during the recharge of the bootstrap capacitor. V_{CCDR} also represents a voltage reference for Tmask pin, S/O/U pin (L6730) or CC/O/U pin (L6730B) and PGOOD pin (see *Table 4: Pin connection*).

If Vcc ≈ 5 V the internal LDO works in dropout with an output resistance of about 1 Ω.

The maximum LDO output current is about 100 mA, and so the output voltage drop can be 100 mV. The LDO can be bypassed to avoid this.

Figure 6. Bypassing the LDO



5.4 Internal and external references

It is possible to set two internal references, 0.6 V and 1.2 V, or provide an external reference from 0 V to 2.5 V. The maximum value of the external reference depends on the V_{CC}: with V_{CC} = 4 V the clamp operates at about 2 V (typ.), while with V_{CC} greater than 5 V the maximum external reference is 2.5 V (typ).

- V_{EAREF} from 0% to 80% of V_{CCDR} –> External reference
- V_{EAREF} from 80% to 95% of V_{CCDR} –> V_{REF} = 1.2 V
- V_{EAREF} from 95% to 100% of V_{CCDR} –> V_{REF} = 0.6 V

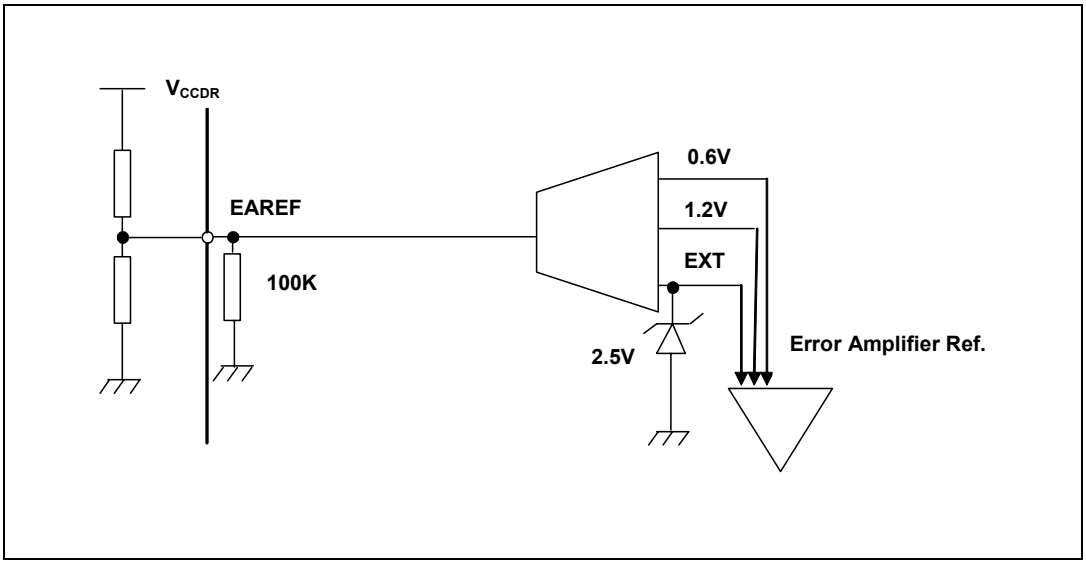
Providing an external reference from 0V to 450 mV the output voltage will be regulated but some restrictions must be considered:

- The minimum OVP threshold is set at 300 mV.
- The under-voltage-protection doesn't work.
- The PGOOD signal remains low.

To set the resistor divider it must be considered that a 100 kΩ pull-down resistor is integrated into the device (see *Figure 7.*). Finally it must be taken into account that the voltage at the EAREF pin is captured by the device at the start-up when Vcc is about 4 V.

5.5 Error amplifier

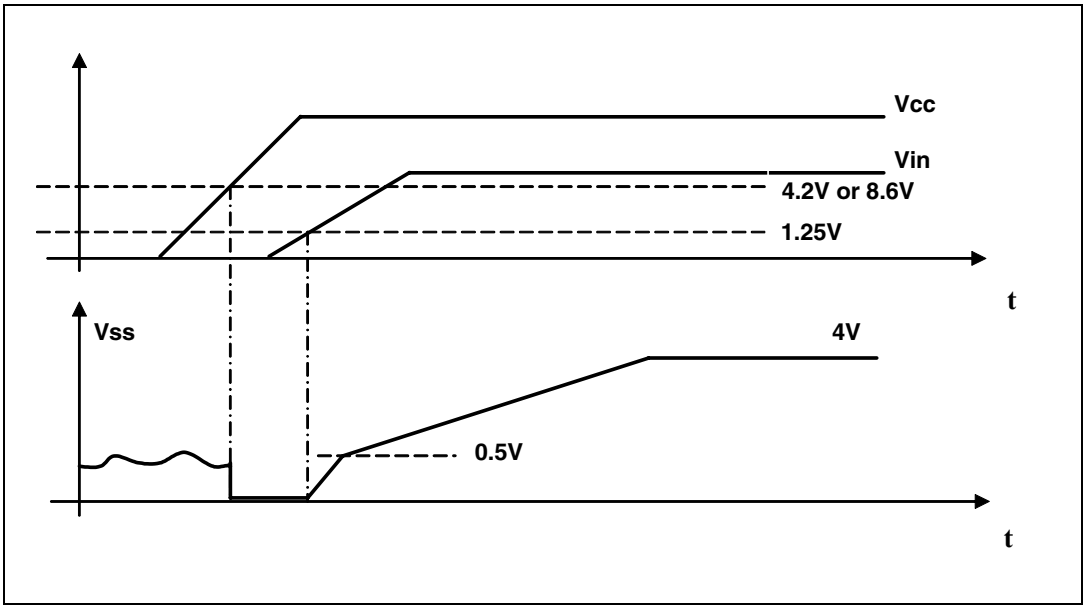
Figure 7. Error amplifier reference



5.6 Soft-start

When both V_{CC} and V_{IN} are above their turn-on thresholds (V_{IN} is monitored by the OCH pin) the start-up phase takes place. Otherwise the SS pin is internally shorted to GND. At start-up, a ramp is generated charging the external capacitor C_{SS} with an internal current generator. The initial value for this current is 35 µA and charges the capacitor up to 0.5 V. After that it becomes 10 µA until the final charge value of approximately 4 V (see *Figure 5*).

Figure 8. Device start-up: voltage at the SS pin



The output of the error amplifier is clamped with this voltage (Vss) until it reaches the programmed value. No switching activity is observable if V_{SS} is lower than 0.5 V and both MOSFETs are off. When Vss is between 0.5 V and 1.1 V the low-side MOSFET is turned on because the output of the error amplifier is lower than the valley of the triangular wave and so the duty-cycle is 0%. As V_{SS} reaches 1.1 V (i.e. the oscillator triangular wave inferior limit) even the high-side MOSFET begins to switch and the output voltage starts to increase. The L6730 - L6730B can only source current during the soft-start phase in order to manage the pre-bias start-up applications. This means that when the startup occurs with output voltage greater than 0V (pre-bias startup), even when Vss is between 0.5 V and 1.1 V the low-side MOSFET is kept OFF (see *Figure 9* and *Figure 10*).

Figure 9. Start-up without pre-bias

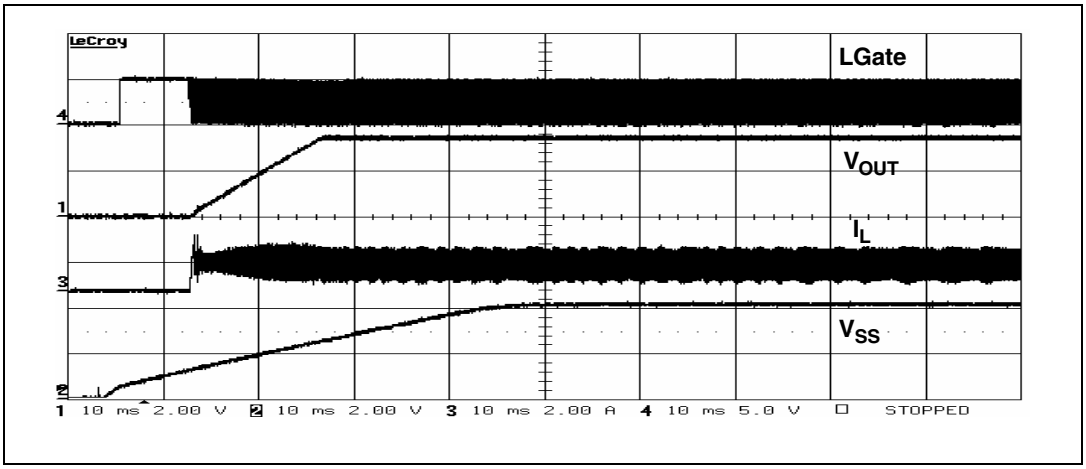
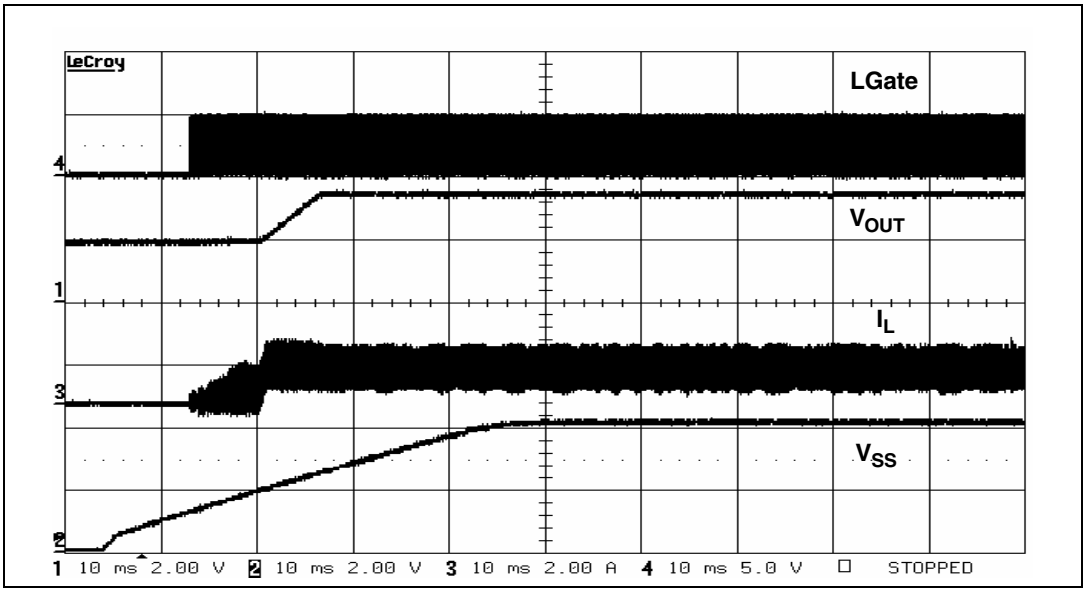


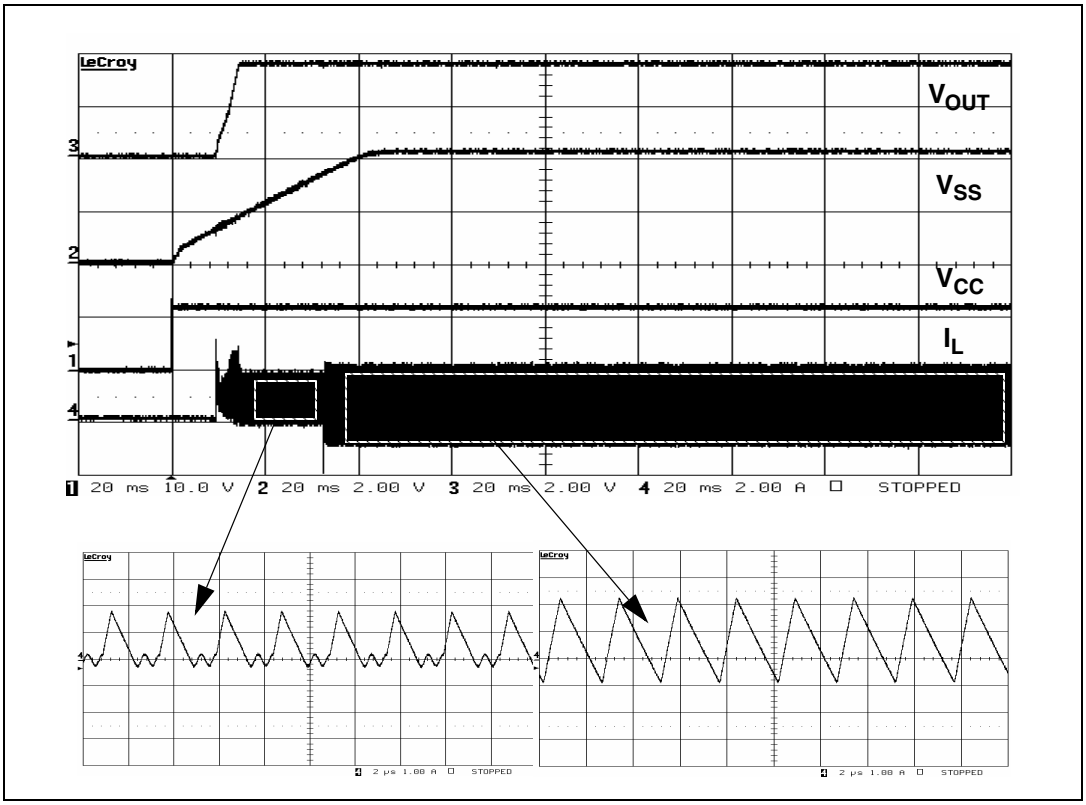
Figure 10. Start-up with pre-bias



The L6730B can always sink current and so it can be used to supply the DDR memory termination BUS. If overcurrent is detected during the soft-start phase, the device provides constant current-protection. In case there is short soft-start time and/or small inductor value and/or high output capacitors value and thus, in case of high ripple current during the soft-start, the converter can start-up in anyway and limit the current (*Chapter 5.8: Monitoring and*

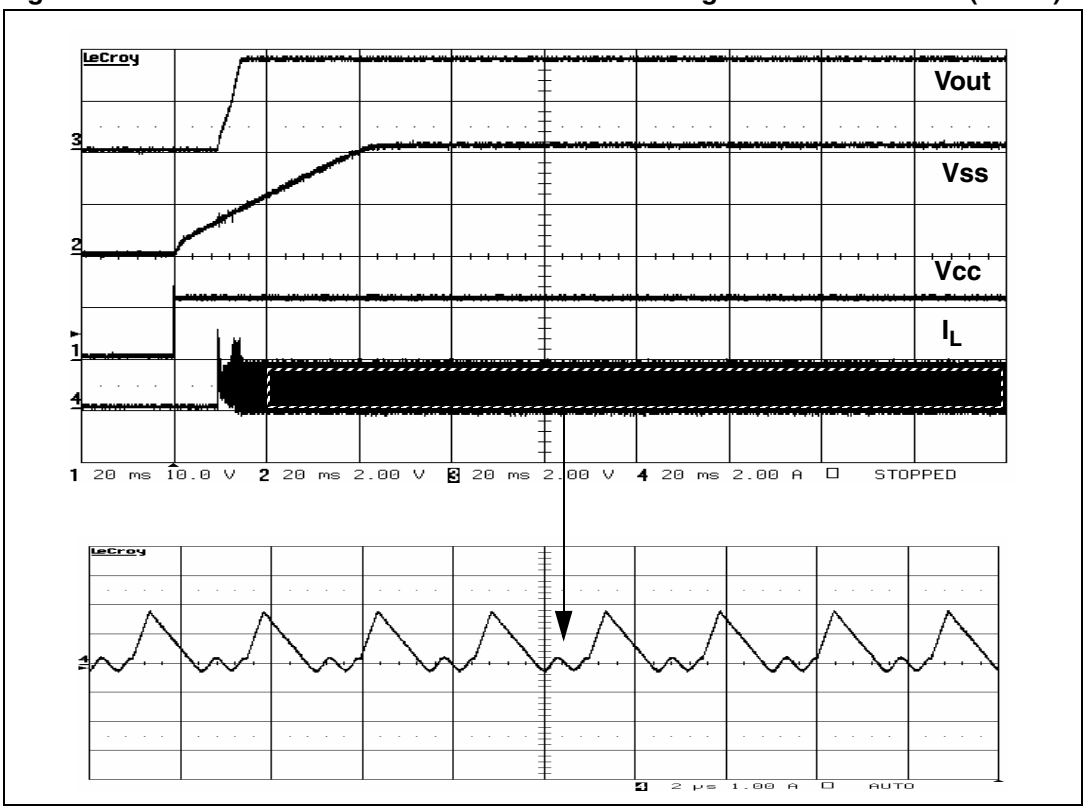
protection on page 21) but not enter into HICCUP mode. The soft-start phase ends when V_{SS} reaches 3.5 V. After that the over current-protection triggers the HICCUP mode (L6730). With the L6730B there is the possibility to set the HICCUP mode or the constant current mode after the soft-start acting on the multifunction pin CC/O/U. With the L6730 the low-side MOSFET(s) management after soft-start phase depends on the S/O/U pin state (see related section). If the sink mode is enabled the converter can sink current after soft-start (see *Figure 11*) while, if the sink mode is disabled the converter never sinks current (see *Figure 12*).

Figure 11. Sink mode enabled: Inductor current during and after soft-start (L6730)



During normal operation, if any under voltage is detected on one of the two supplies (V_{CC}, V_{IN}), the SS pin is internally shorted to GND by an internal switch so the SS capacitor is rapidly discharged. Two different turn-on UVLO thresholds can be set: 4.2 V for 5 V BUS and 8.6 V for 12 V BUS.

Figure 12. Sink mode disabled: Inductor current during and after soft-start (L6730)



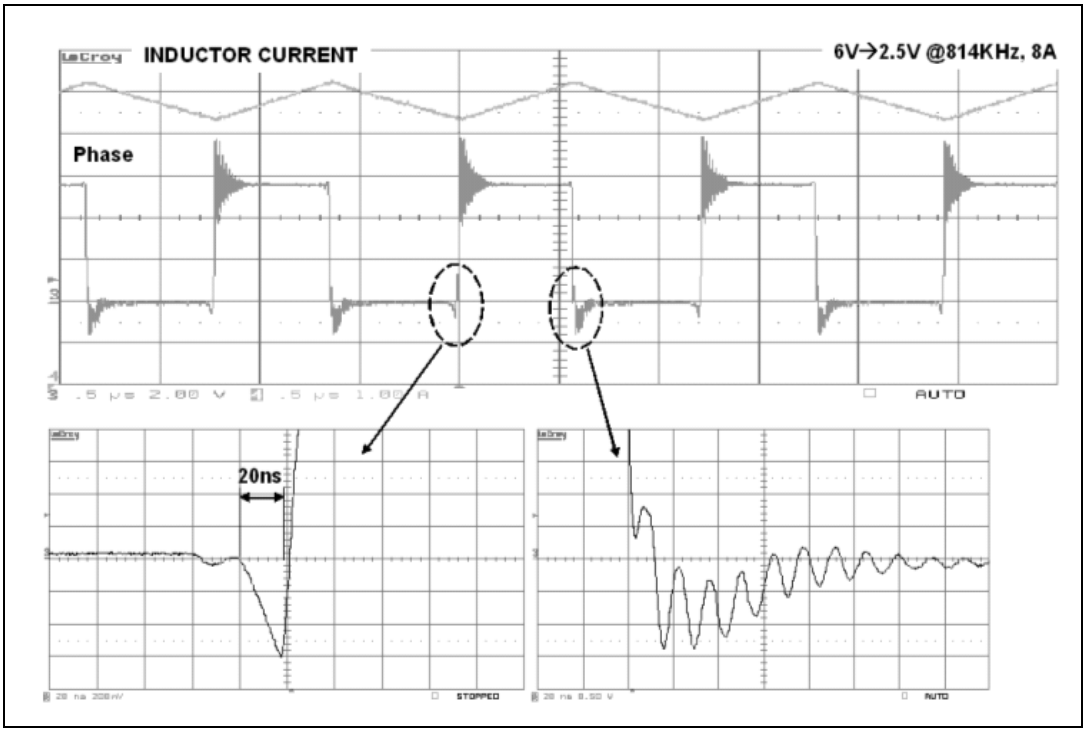
5.7 Driver section

The high-side and low-side drivers allow for the use of different types of power MOSFETs (also multiple MOSFETs to reduce the R_{DSON}), maintaining fast switching transitions. The low-side driver is supplied by V_{CCDR} while the high-side driver is supplied by the BOOT pin. A predictive dead time control avoids MOSFETs cross-conduction maintaining very short dead time duration (see *Figure 13.*).

The control monitors the phase node in order to sense the low-side body diode recirculation. If the phase node voltage is less than a certain threshold (–350 mV typ.) during the dead time, it will be reduced in the next PWM cycle. The predictive dead time control does not work when the high-side body diode is conducting because the phase node does not go

negative. This situation happens when the converter is sinking current for example and, in this case, an adaptive dead time control operates.

Figure 13. Dead times



5.8 Monitoring and protection

The output voltage is monitored by the FB pin. If it is not within ±10% (typ.) of the programmed value, the Power-Good (PGOOD) output is forced low. The PGOOD signal can be delayed by adding an external capacitor on PGDelay pin (see *Table 4: Pin connection* and *Figure 14.*); this can be useful to perform cascade sequencing. The delay can be calculated with the following formula:

$$PGDelay = 0.5 \cdot C(pF)$$

The device provides over voltage protection: when the voltage sensed on FB pin reaches a value 20% (typ) greater than the reference, the low-side driver is turned on. If the OVP not-latched mode has been set the low-side MOSFET is kept on as long as the overvoltage is detected (see *Figure 15.*).The OVP latched-mode has been set the low-side MOSFET is

turned on until V_{CC} is toggled (see *Figure 16*). In case of latched-mode OVP the OSC pin is forced high (4.5 V typ) if an over voltage is detected.

Figure 14. PGOOD signal

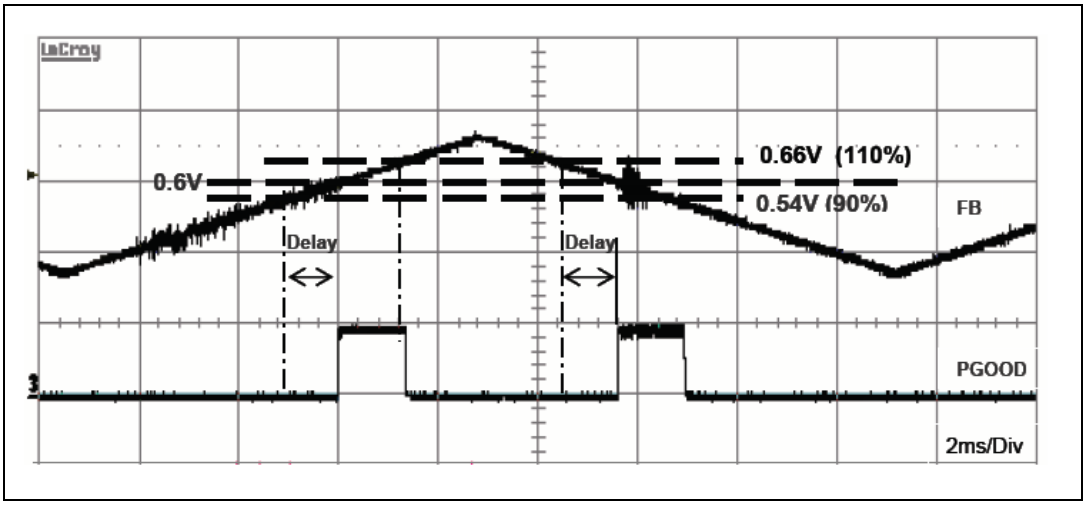


Figure 15. OVP not latched

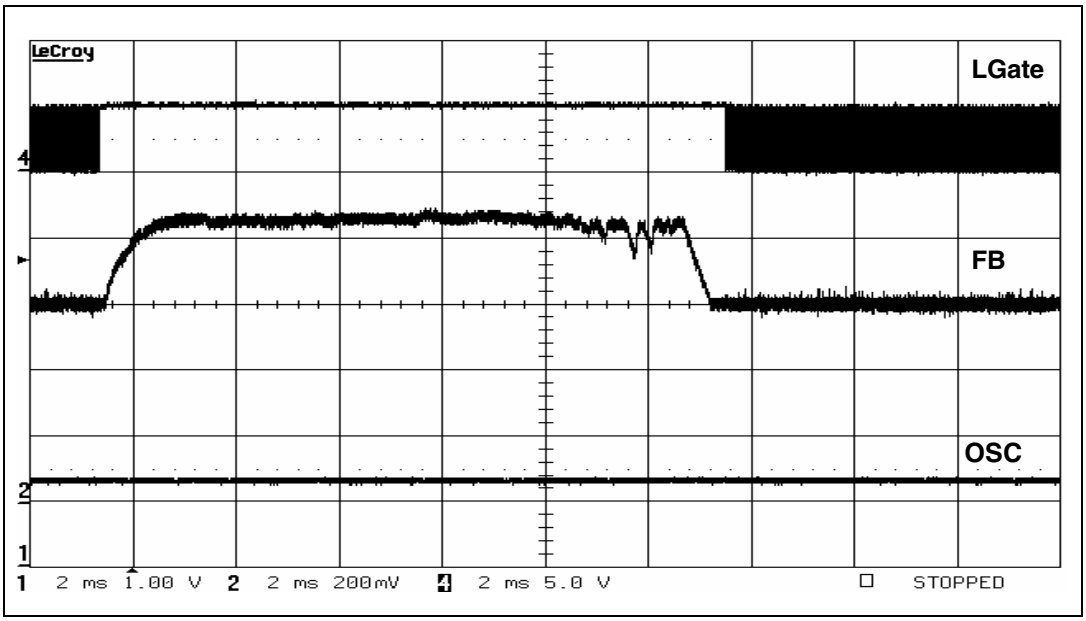
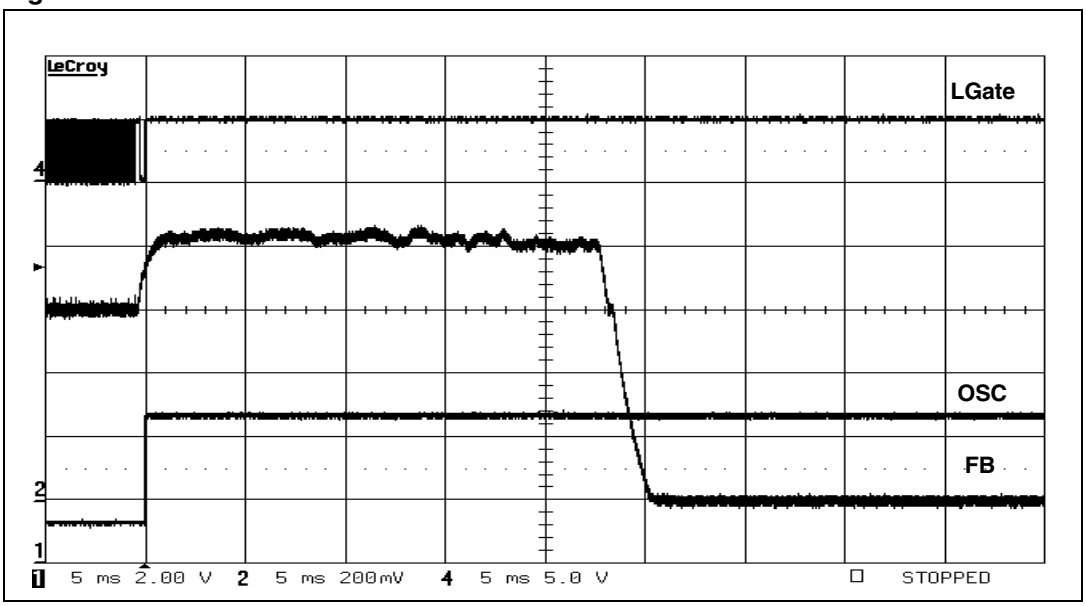


Figure 16. OVP latched



There is an electrical network between the output terminal and the FB pin and therefore the voltage at this pin is not a perfect replica of the output voltage. If the converter can sink current, in the most of cases the low-side will be turned on before the output voltage exceeds the over-voltage threshold because the error amplifier will throw off balance in advance.

Even if the device does not report an overvoltage event, the behavior is the same because the low-side is turned on immediately. Instead, if the sink mode is disabled, the low-side will be turned on only when the overvoltage protection (OVP) operates and not before because the current can not be reversed. In this case, a delay between the output voltage rising and FB voltage rising can appear and the OVP can turn on late. *Figure 17* and *Figure 18* show an overvoltage event in the cases of the sink being enabled or disabled. The output voltage rises with a slope of 100 mVµs, emulating the breaking of the high-side MOSFET as an overvoltage occurs.

Figure 17. OVP with sink enabled: the low-side MOSFET is turned-on in advance

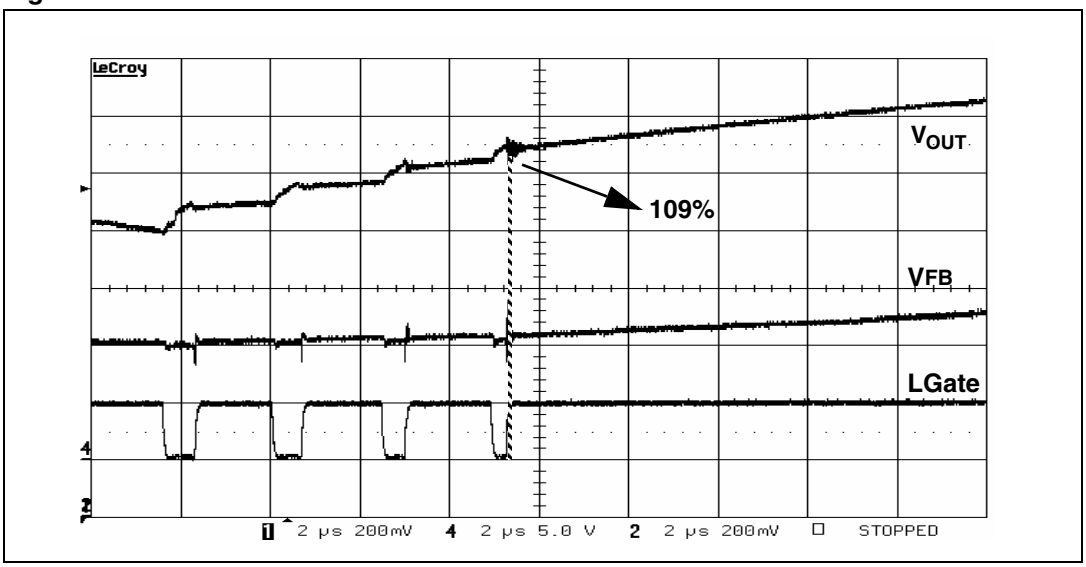
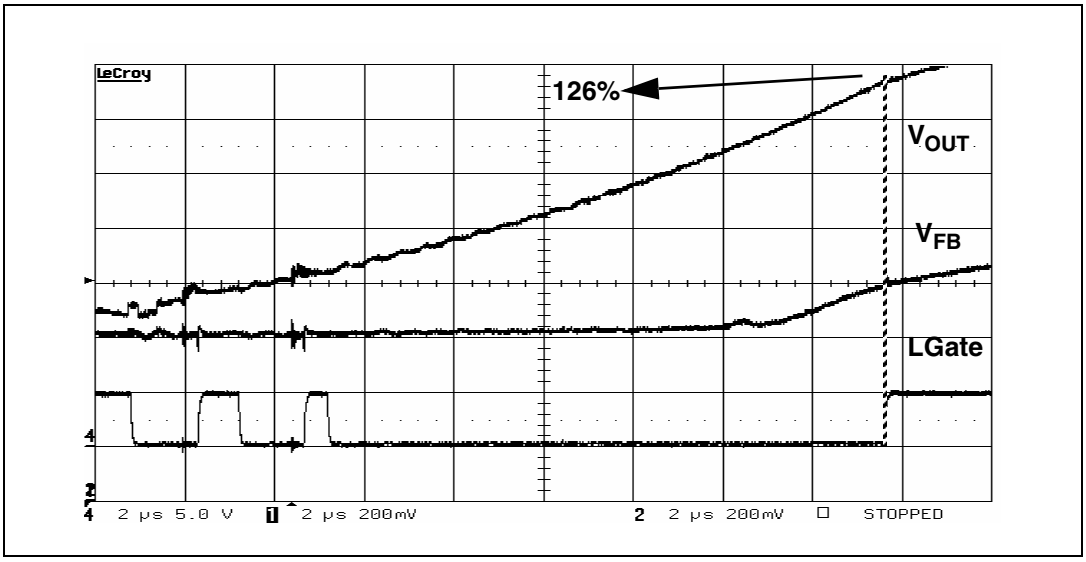


Figure 18. OVP with sink disabled: delay on the OVP operation



The L6730B can always sink current and so the OVP will operate always in advance. The device realizes the over-current-protection (OCP) sensing the current both on the high-side MOSFET(s) and the low-side MOSFET(s) and so 2 current limit thresholds can be set (see OCH pin and OCL pin in *Table 4: Pin connection*):

- Peak current limit
- Valley current limit

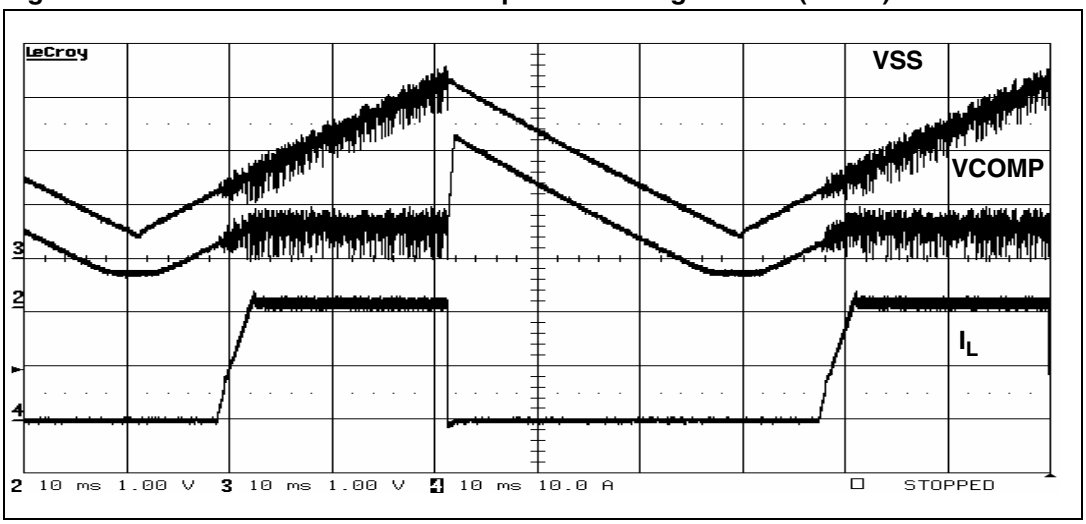
The peak current protection is active when the high-side MOSFET(s) is turned on, after an adjustable masking time (see *Chapter 5.10 on page 27*). The valley-current-protection is enabled when the low-side MOSFET(s) is turned on after a fix masking time of about 400 ns. If, when the soft-start phase is completed, an over current event occurs during the on time (peak-current-protection) or during the off time (valley-current-protection) the device

enters in HICCUP mode (L6730): the high-side and low-side MOSFET(s) are turned off, the soft-start capacitor is discharged with a constant current of 10 µA and when the voltage at the SS pin reaches 0.5 V the soft-start phase restarts. During the soft-start phase the OCP provides a constant-current-protection. If during the T_{ON} the OCH comparator triggers an over current the high-side MOSFET(s) is immediately turned-off (after the masking time and the internal delay) and returned-on at the next pwm cycle. The limit of this protection is that the Ton can't be less than masking time plus propagation delay (see *Chapter 5.9: Adjustable masking time on page 27*) because during the masking time the peak-current-protection is disabled. In case of very hard short circuit, even with this short T_{ON}, the current could escalate. The valley-current-protection is very helpful in this case to limit the current. If during the off-time the OCL comparator triggers an over current, the high-side MOSFET(s) is not turned-on until the current is over the valley-current-limit. This implies that, if it is necessary, some pulses of the high-side MOSFET(s) will be skipped, guaranteeing a maximum current due to the following formula:

$$I_{MAX} = I_{VALLEY} + \frac{Vin - Vout}{L} \cdot T_{ON,MIN} \quad (4)$$

In constant current protection a current control loop limits the value of the error amplifier's output (comp), in order to avoid its saturation and thus recover faster when the output returns in regulation. *Figure 19* shows the behaviour of the device during an over current condition that persists also in the soft-start phase.

Figure 19. Constant current and hiccup mode during an OCP (L6730)



Using the L6730B there is the possibility to set the constant-current-protection also after the soft-start. The following figures show the behaviour of the L6730B during an overcurrent event.

Figure 20 shows the intervention of the peak OCP: the high-side MOSFET(s) is turned-off when the current exceeds the OCP threshold. In this way the duty-cycle is reduced, the V_{OUT} is reduced and so the maximum current can be fixed even if the output current is escalating. *Figure 21* shows the limit of this protection: the on-time can be reduced only to the masking time and, if the output current continues to increase, the maximum current can increase too. Notice how the Vout remains constant even if the output current increases because the on-time cannot be reduced anymore.

Figure 20. Peak overcurrent-protection in constant-current-protection (L6730B)

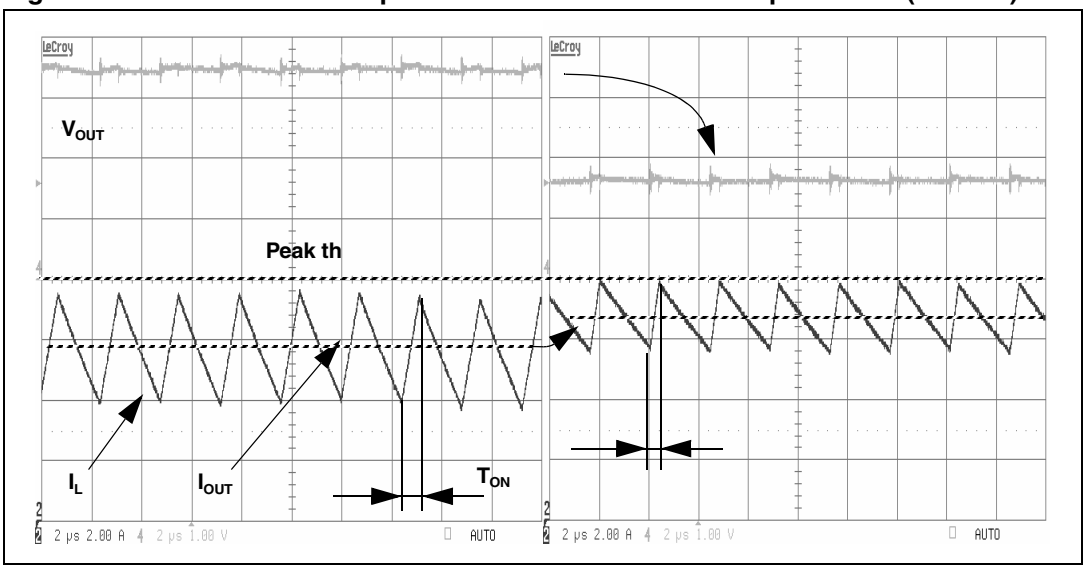
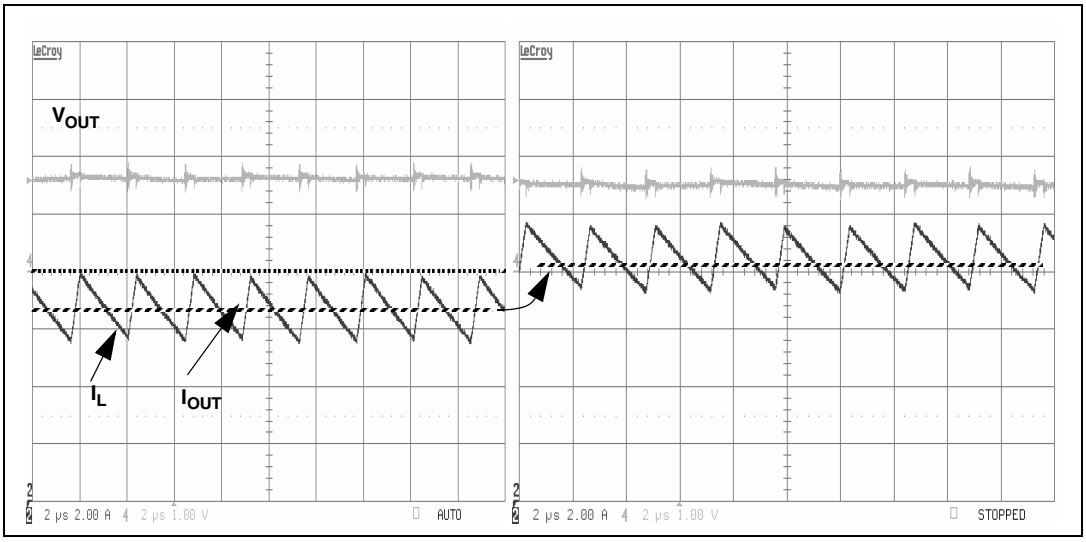


Figure 21. Peak OCP in case of heavy overcurrent (L6730B)



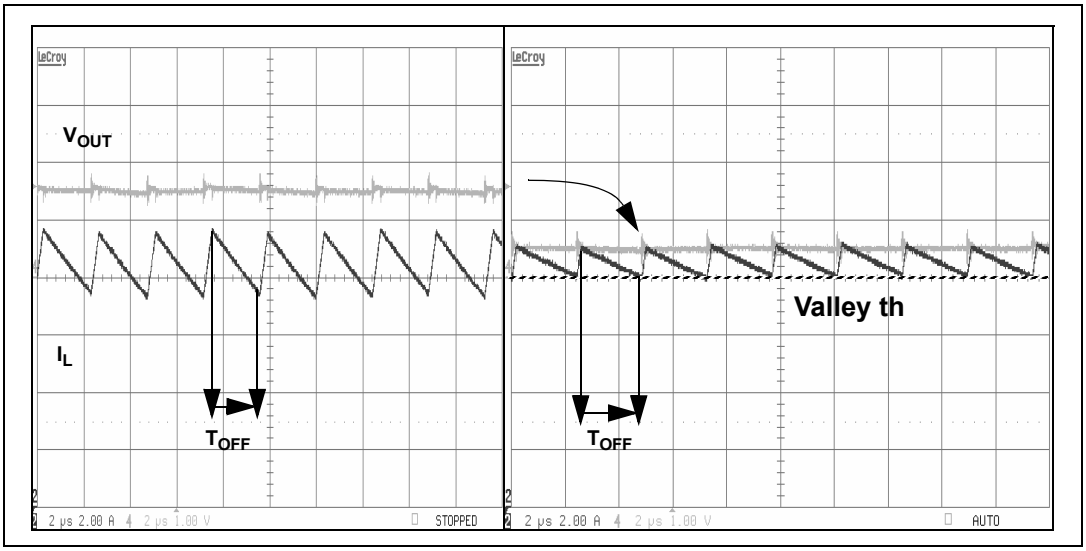
If the current is higher than the valley OCP threshold during the off-time, the high-side MOSFET(s) will not be turned ON. In this way the maximum current can be limited (*Figure 22*).

During the constant-current-protection if the Vout becomes lower than 80% of the programmed value an UV (under-voltage) is detected and the device enters in HICCUP mode. The under-voltage-lock-out (UVLO) is adjustable by the multifunction pin (see *Chapter 5.10 on page 27*). It's possible to set two different thresholds:

- 4.2 V for 5 V bus
- 8.6 V for 12 V bus

Working with a 12 V BUS, setting the UVLO at 8.6 V can be very helpful to limit the input current in case of BUS fall.

Figure 22. Valley OCP (L6730B)



5.9 Adjustable masking time

By connecting the masking time pin to V_{CCDR} or GND it is possible to select two different values for the peak current protection leading edge blanking time. This is useful to avoid any false OCP trigger due to spikes and oscillations generated at the turn-on of the high-side MOSFET(s). The amount of this noise depends very much on the layout, MOSFETs, free-wheeling diode, switched current, and input voltage.

When good layout and medium current are used, the minimum masking time can be chosen, while in case of higher noise, it is better to select the maximum masking time. By connecting the t_{MASK} pin to V_{CCDR} the masking time is about 400 ns, while connecting it to GND results in about 260 ns masking time.

5.10 Multifunction pin (S/O/U L6730) (CC/O/U L6730B)

With this pin it is possible:

- To enable disable the sink mode current capability (L6730) or the constant current protection (L6730B) at the end of the soft-start
- To enable or disable the latch-mode for the OVP
- To set the UVLO threshold for 5 V BUS and 12 V busses

Table 7 shows how to set the different options through an external resistor divider:

Figure 23. External resistor

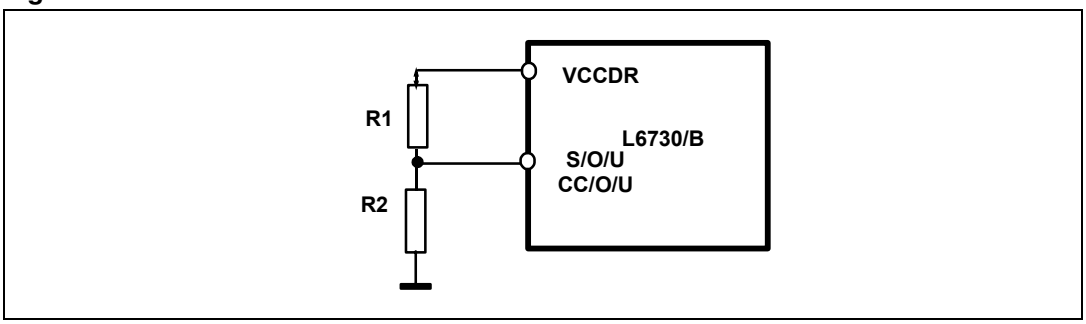


Table 7. S/O/U and CC/O/U pin

R1	R2	V_{SOU}/V_{CCDR}	UVLO	OVP	SINK CC
N.C	0Ω	0	5V BUS	Not latched	Not
11KΩ	2.7KΩ	0.2	5V BUS	Not latched	Yes
6.2KΩ	2.7KΩ	0.3	5V BUS	Latched	Not
4.3KΩ	2.7KΩ	0.4	5V BUS	Latched	Yes
2.7KΩ	2.7KΩ	0.5	12V BUS	Not latched	Not
1.8KΩ	2.7KΩ	0.6	12V BUS	Not latched	Yes
1.2KΩ	2.7KΩ	0.7	12V BUS	Latched	Not
0Ω	N.C	1	12V BUS	Latched	Yes

5.11 Synchronization

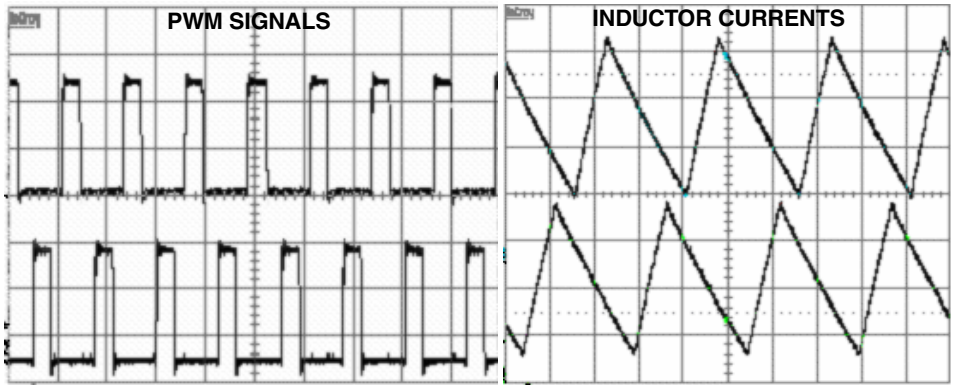
The presence of many converters on the same board can generate beating frequency noise. To avoid this it is important to make them operate at the same switching frequency. Moreover, a phase shift between different modules helps to minimize the RMS current on the common input capacitors. *Figure 24* shows the results of two modules in synchronization. Two or more devices can be synchronized simply connecting together the SYNCH pins. The device with the higher switching frequency will be the Master while the other one will be the slave. The slave controller will increase its switching frequency reducing the ramp amplitude proportionally and then the modulator gain will be increased.

To avoid a huge variation of the modulator gain, the best way to synchronize two or more devices is to make them work at the same switching frequency and, in any case, the switching frequencies can differ for a maximum of 50% of the lowest one. If, during synchronization between two (or more) L6730, it's important to know in advance which the master is, it's timely to set its switching frequency at least 15% higher than the slave. Using an external clock signal (f_{EXT}) to synchronize one or more devices that are working at a different switching frequency (f_{SW}) it is recommended to follow the below formula:

$$f_{SW} \leq f_{EXT} \leq 1{,}3 \cdot f_{SW}$$

The phase shift between master and slaves is approximately done 180°.

Figure 24. Synchronization



5.12 Thermal shutdown

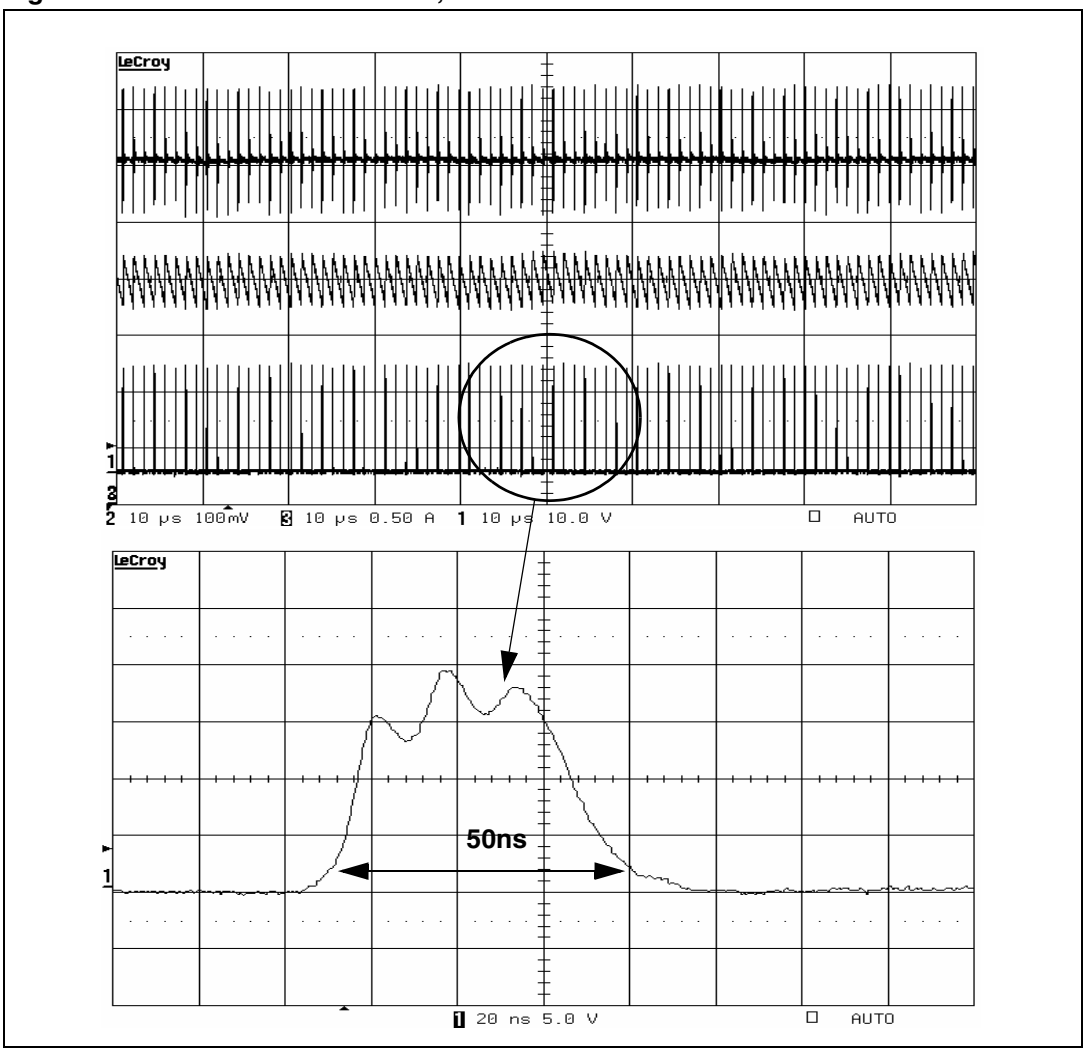
When the junction temperature reaches 150°C ±10°C, the device enters in thermal shutdown.

Both MOSFETs are turned OFF and the soft-start capacitor is rapidly discharged with an internal switch. The device does not restart until the junction temperature goes down to 120°C and, in any case, until the voltage at the soft-start pin reaches 500 mV.

5.13 Minimum ON-time $T_{ON(MIN)}$

The device can manage minimum ON times lower than 100 ns. This feature comes from the control topology as well as from the particular L6730/B overcurrent protection system. In a voltage mode controller, the current does not have to be sensed to perform regulation and, in the case of L6730/B, it does not have to be sensed for the overcurrent protection either because valley current protection can operate during the OFF time. The first advantage related of this feature is the achievement of extremely low conversion ratios. *Figure 25* shows a conversion from 14 V to 0.5 V at 820 kHz with a t_{ON} of about 50 ns. The ON time is limited by the MOSFET turn-on and turn-off times.

Figure 25. 14 V -> 0.5 V@820 kHz, 5 A



5.14 Bootstrap anti-discharging system

This built-in anti-discharging system keeps the voltage going across the bootstrap capacitor from going below 3.3 V. An internal comparator senses the voltage across the external bootstrap capacitor and helps to keep it charged, eventually turning on the low-side MOSFET for approximately 200 ns. If the bootstrap capacitor is not charged up enough, the high-side MOSFET cannot be effectively turned on and it will present a higher $R_{DS(on)}$. In some cases, the OCP can be also triggered. There are up to two conditions during which the bootstrap capacitor can be discharged:

- fan power supply failure, and
- no sink at zero current operation.

5.14.1 Fan power supply failure

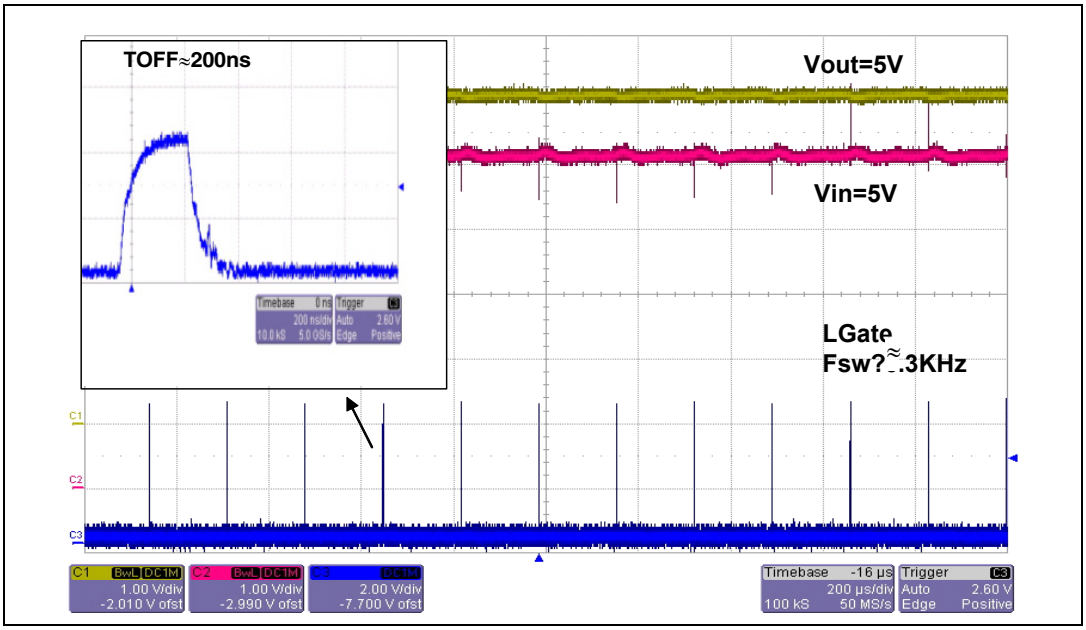
In many applications the fan is driven by a DC motor that uses a DC/DC converter. Often only the speed of the motor is controlled by varying the voltage applied to the input terminal and there is no control on the torque because the current is not directly controlled. The current has to be limited in case of overload or short-circuit, but without stopping the motor.

With the L6730B, the current can be limited without shutting down the system because constant current protection is provided. In order to vary the motor speed, the output voltage of the converter must be varied. Both L6730 and L6730B have a dedicated EAREF pin (see *Figure 4*) which provides an external reference to the non-inverting input of the error-amplifier.

In these applications the duty cycle depends on the motor's speed and sometimes a 100% duty cycle setting has to be used to attain the maximum speed. In these conditions, the bootstrap capacitor can not be recharged and the system cannot work properly. Some PWM controllers limit the maximum duty cycle to 80 or 90% in order to keep the bootstrap capacitor charged, but this makes performance during the load transient worse. The "bootstrap anti-discharging system" allows the L6730x to work at 100% without any problem.

Figure 26.: 100% duty cycle operation on page 31 shows the following picture illustrates the device behavior when the input voltage is 5 V and a 100% duty cycle is set by an external reference.

Figure 26. 100% duty cycle operation



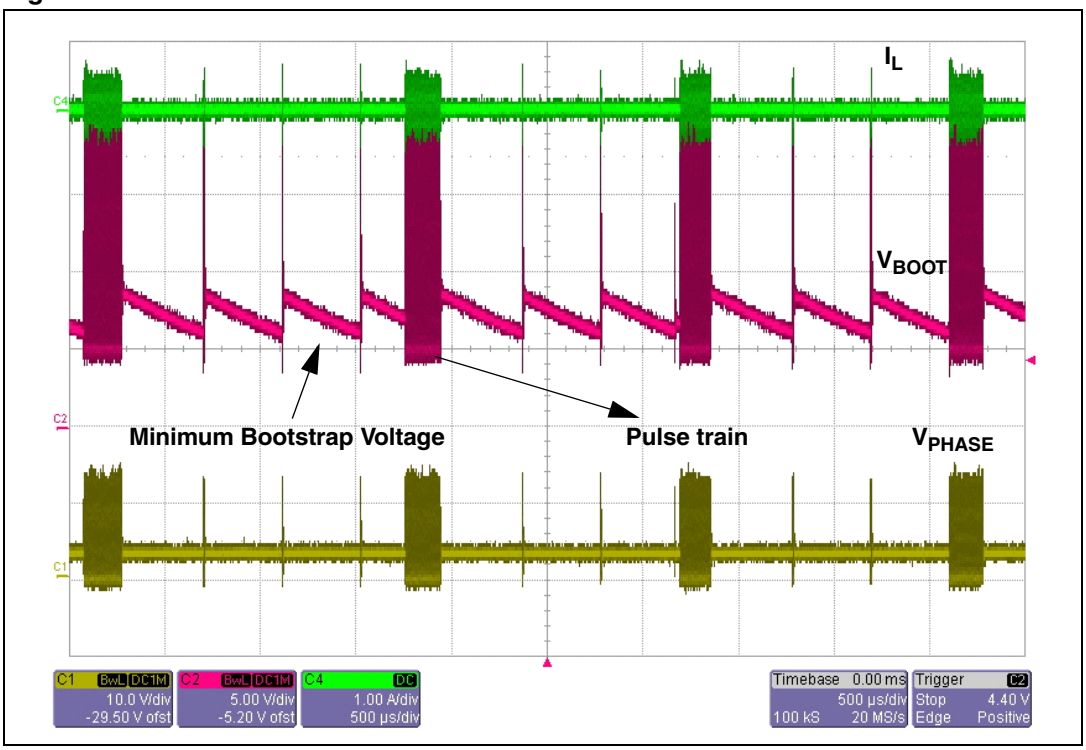
5.14.2 No-sink at zero current operation

The L6730 can work in no-sink mode. If output current is zero the converter skip some pulses and works with a lower switching frequency. Between two pulses can pass a relatively long time (say 200-300 µs) during which there's no switching activity and the current into the inductor is zero. In this condition the phase node is at the output voltage and in some cases this is not enough to keep the bootstrap cap charged. For example, if Vout is 3.3 V the voltage across the bootstrap cap is only 1.7 V. The high-side MOSFET cannot be

effectively turned-on and the regulation can be lost. Thanks to the “bootstrap anti-discharging system” the bootstrap cap is always kept charged. The following picture shows the behaviour of the device in the following conditions: 12 V -> 3.3 V@0 A.

It can be observed that between two pulses trains the low-side is turned-on in order to keep the bootstrap cap charged.

Figure 27. 12 V -> 3.3 V@0 A in no-sink



6 Application details

6.1 Inductor design

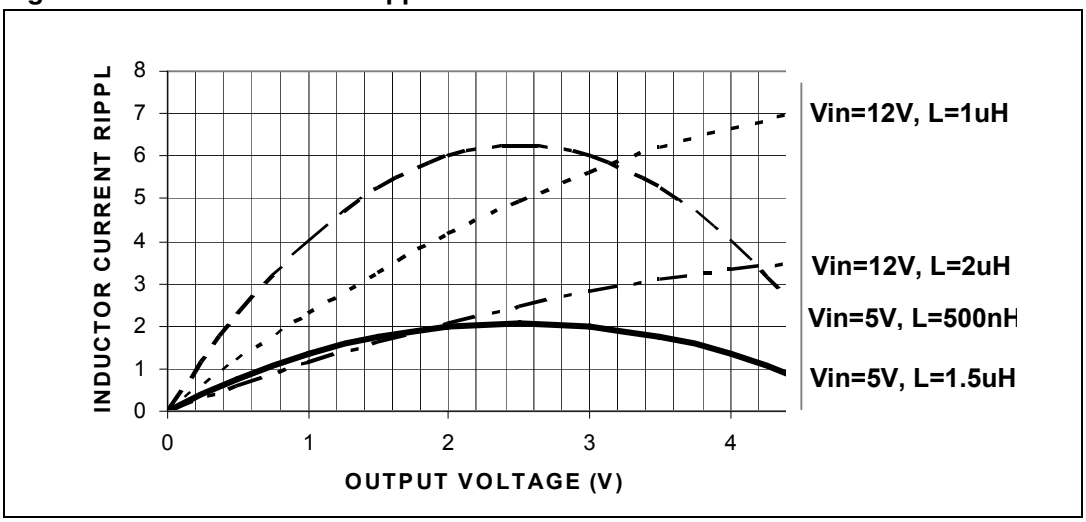
The inductance value is defined by a compromise between the transient response time, the efficiency, the cost and the size. The inductor has to be calculated to maintain the ripple current (ΔI_L) between 20% and 30% of the maximum output current. The inductance value can be calculated with the following relationship:

$$L \cong \frac{Vin - Vout}{Fsw \cdot \Delta I_L} \cdot \frac{Vout}{Vin} \quad (6)$$

Where F_{SW} is the switching frequency, V_{IN} is the input voltage and V_{OUT} is the output voltage. *Figure 28* shows the ripple current vs. the output voltage for different values of the inductor, with V_{IN} = 5 V and V_{IN} = 12 V at a switching frequency of 400 kHz.

Increasing the value of the inductance reduces the current ripple but, at the same time, increases the converter response time to a load transient. If the compensation network is well designed, during a load transient the device is able to set the duty cycle to 100% or to 0%. When one of these conditions is reached, the response time is limited by the time required to change the inductor current. During this time the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitor size.

Figure 28. Inductor current ripple



6.2 Output capacitors

The output capacitors are basic components for the fast transient response of the power supply. They depend on the output voltage ripple requirements, as well as any output voltage deviation requirement during a load transient. During a load transient, the output capacitors supply the current to the load or absorb the current stored into the inductor until the converter reacts. In fact, even if the controller recognizes immediately the load transient and sets the duty cycle at 100% or 0%, the current slope is limited by the inductor value. The output voltage has a first drop due to the current variation inside the capacitor (neglecting the effect of the ESL):

$$\Delta Vout_{ESR} = \Delta Iout \cdot ESR \quad (7)$$

Moreover, there is an additional drop due to the effective capacitor discharge or charge that is given by the following formulas:

$$\Delta Vout_{COUT} = \frac{\Delta Iout^2 \cdot L}{2 \cdot Cout \cdot (Vin, \min \cdot D \max - Vout)} \quad (8)$$

$$\Delta Vout_{COUT} = \frac{\Delta Iout^2 \cdot L}{2 \cdot Cout \cdot Vout} \quad (9)$$

Formula (8) is valid in case of positive load transient while the formula (9) is valid in case of negative load transient. D_{MAX} is the maximum duty cycle value that in the L6730/B is 100%. For a given inductor value, minimum input voltage, output voltage and maximum load transient, a maximum ESR, and a minimum C_{OUT} value can be set. The ESR and C_{OUT} values also affect the static output voltage ripple. In the worst case the output voltage ripple can be calculated with the following formula:

$$\Delta Vout = \Delta I_L \cdot (ESR + \frac{1}{8 \cdot Cout \cdot Fsw}) \quad (10)$$

Usually the voltage drop due to the ESR is the biggest one while the drop due to the capacitor discharge is almost negligible.

6.3 Input capacitors

The input capacitors have to sustain the RMS current flowing through them, that is:

$$Irms = Iout \cdot \sqrt{D \cdot (1 - D)} \quad (11)$$

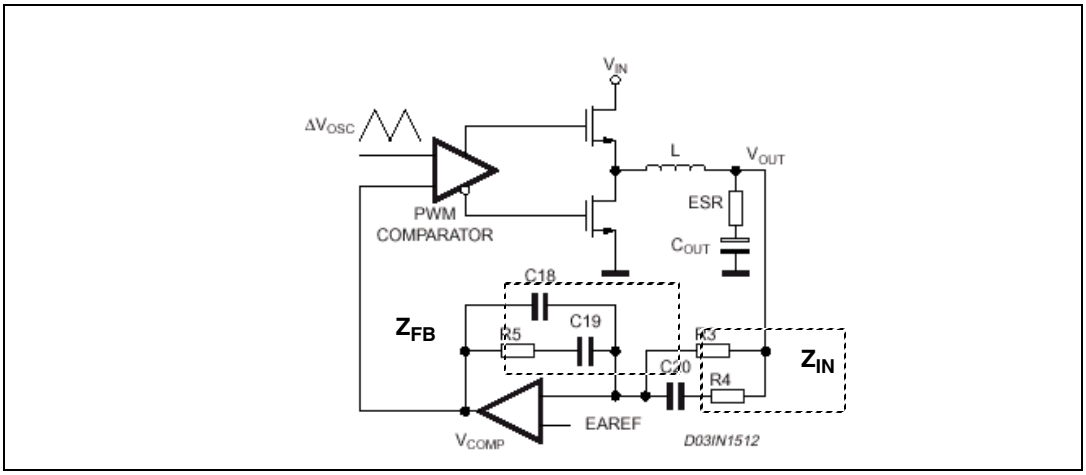
Where D is the duty cycle. The equation reaches its maximum value, $I_{OUT}/2$ with D = 0.5. The losses in worst case are:

$$P = ESR \cdot (0.5 \cdot Iout)^2 \quad (12)$$

6.4 Compensation network

The loop is based on a voltage mode control (*Figure 29*). The output voltage is regulated to the internal/external reference voltage and scaled by the external resistor divider. The error amplifier output V_{COMP} is then compared with the oscillator triangular wave to provide a pulse-width modulated (PWM) with an amplitude of V_{IN} at the PHASE node. This waveform is filtered by the output filter. The modulator transfer function is the small signal transfer function of V_{OUT}/V_{COMP}. This function has a double pole at frequency F_{LC} depending on the L-Cout resonance and a zero at F_{ESR} depending on the output capacitor's ESR. The DC Gain of the modulator is simply the input voltage V_{IN} divided by the peak-to-peak oscillator voltage: V_{OSC}.

Figure 29. Compensation network



The compensation network consists in the internal error amplifier, the impedance networks Z_{IN} (R3, R4 and C20) and Z_{FB} (R5, C18 and C19). The compensation network has to provide a closed loop transfer function with the highest 0dB crossing frequency to have fastest transient response (but always lower than fsw/10) and the highest gain in DC conditions to minimize the load regulation error. A stable control loop has a gain crossing the

0 dB axis with -20 dB/decade slope and a phase margin greater than 45°. To locate poles and zeroes of the compensation networks, the following suggestions may be used:

- Modulator singularity frequencies:

$$\omega_{LC} = \frac{1}{\sqrt{L \cdot Cout}} \quad (13) \qquad \omega_{ESR} = \frac{1}{ESR \cdot Cout} \quad (14)$$

- Compensation network singularity frequencies:

$$\omega_{P1} = \frac{1}{R_5 \cdot \left(\frac{C_{18} \cdot C_{19}}{C_{18} + C_{19}} \right)} \quad (15) \qquad \omega_{P2} = \frac{1}{R_4 \cdot C_{20}} \quad (16)$$

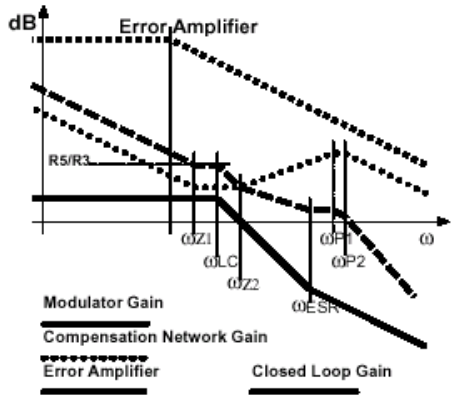
$$\omega_{Z1} = \frac{1}{R_5 \cdot C_{19}} \quad (17) \qquad \omega_{Z2} = \frac{1}{C_{20} \cdot (R_3 + R_4)} \quad (18)$$

- Compensation network design:
  - Put the gain R_5/R_3 in order to obtain the desired converter bandwidth

$$\varpi_C = \frac{R_5}{R_3} \cdot \frac{Vin}{\Delta Vosc} \cdot \varpi_{LC} \quad (18)$$

  - Place ω_{Z1} before the output filter resonance ω_{LC};
  - Place ω_{Z2} at the output filter resonance ω_{LC};
  - Place ω_{P1} at the output capacitor ESR zero ω_{ESR};
  - Place ω_{P2} at one half of the switching frequency;
  - Check the loop gain considering the error amplifier open loop gain.

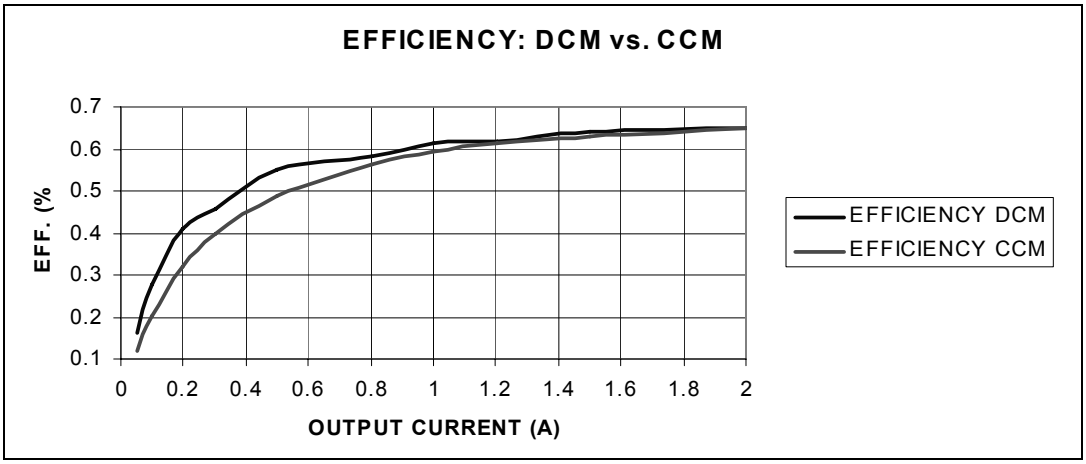
Figure 30. Asymptotic bode plot of converter's open loop gain



6.5 Two quadrant or one quadrant operation mode (L6730)

After the soft-start phase the L6730 can work in source only (one quadrant operation mode) or in sink/source (two quadrant operation mode), depending on the setting of the multifunction pin (see *Chapter 5.10 on page 27*). The choice of one or two quadrant operation mode is related to the application. One quadrant operation mode permits to have a higher efficiency at light load, because the converter works in discontinuous mode (see *Figure 31*). Nevertheless in some cases, in order to maintain a constant switching frequency, it's preferable to work in two quadrants, even at light load. In this way the reduction of the switching frequency due to the pulse skipping is avoided. To parallel two or more modules is requested the one quadrant operation in order not to have current sinking between different converters. Finally the two quadrant operation allows faster recovers after negative load transient. For example, let's consider that the load current falls down from I_{OUT} to 0A with a slew rate sufficiently greater than L/V_{OUT} (where L is the inductor value). Even considering that the converter reacts instantaneously setting to 0% the duty-cycle, the energy $½*L*I_{OUT}^2$ stored in the inductor will be transferred to the output capacitors, increasing the output voltage. If the converter can sink current this overvoltage can be faster eliminated.

Figure 31. Efficiency in discontinuous-current-mode and continuous-current-mode

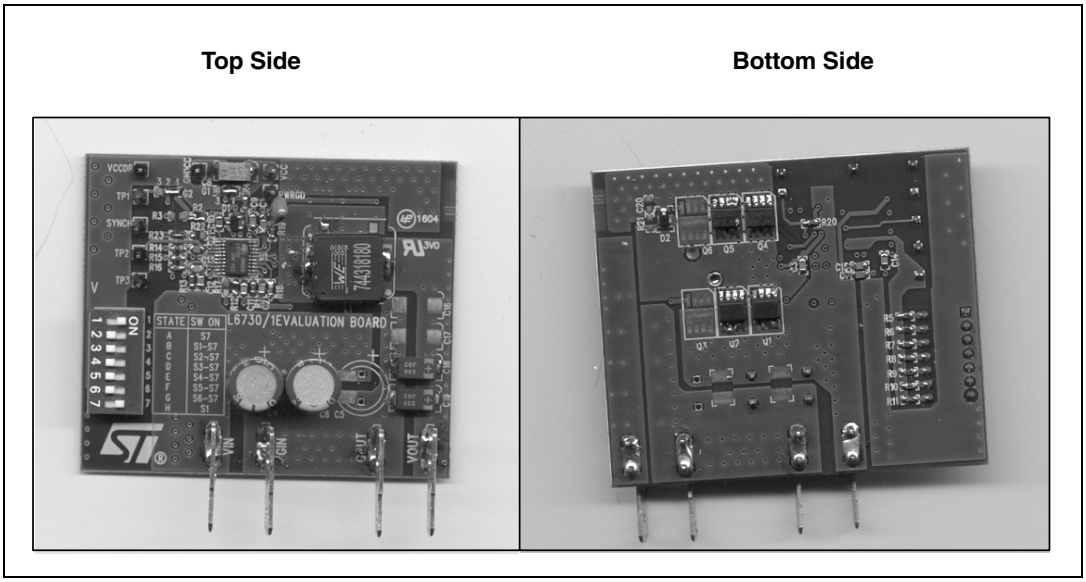


7 L6730 demonstration board

7.1 Description

L6730 demonstration board realizes in a four layer PCB a step-down DC/DC converter and shows the operation of the device in a general purpose application. The input voltage can range from 4.5 V to 14 V and the output voltage is at 3.3 V. The module can deliver an output current in excess of 30 A. The switching frequency is set at 400 kHz (controller free-running F_{SW}) but it can be increased up to 1 MHz. A 7 positions dip-switch allows to select the UVLO threshold (5 V or 12 V bus), the OVP intervention mode and the sink-mode current capability.

Figure 32. Demonstration board picture



7.2 PCB layout

Figure 33. Top layer

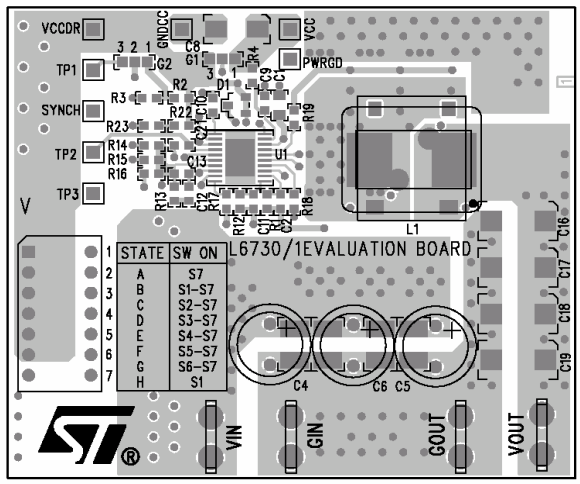


Figure 34. Power ground layer

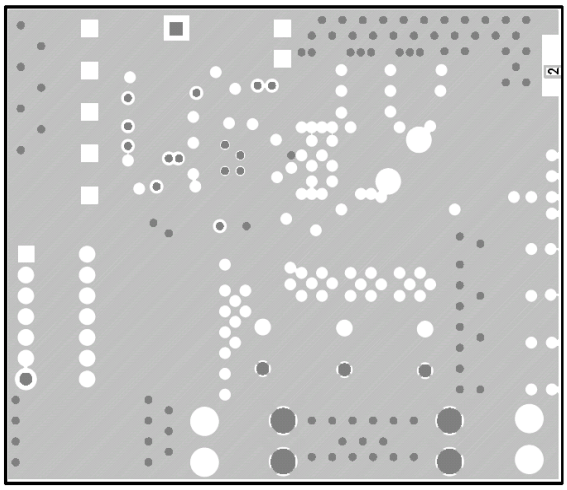


Figure 35. Signal ground layer

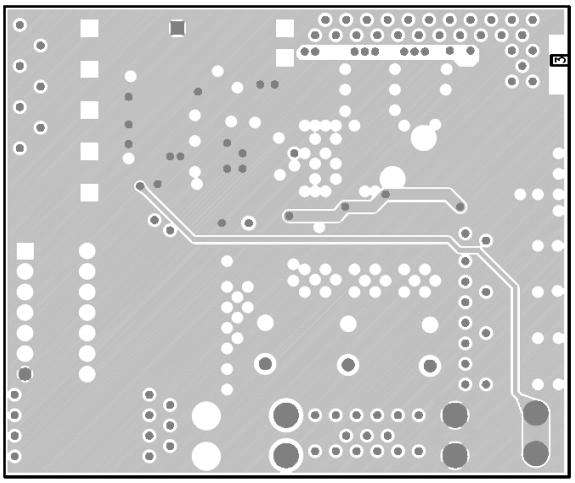


Figure 36. Bottom layer

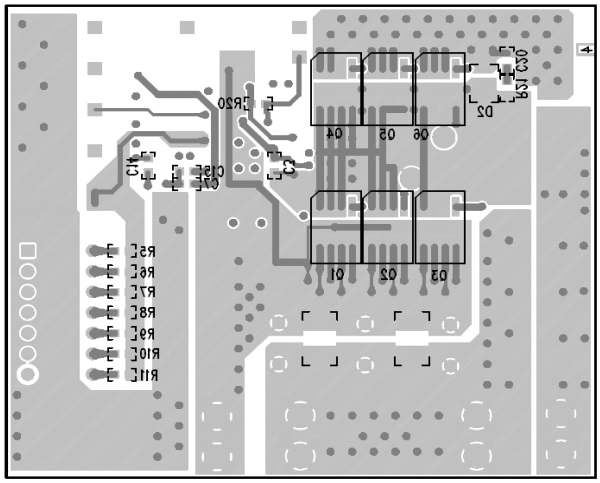


Figure 37. Demonstration board schematic

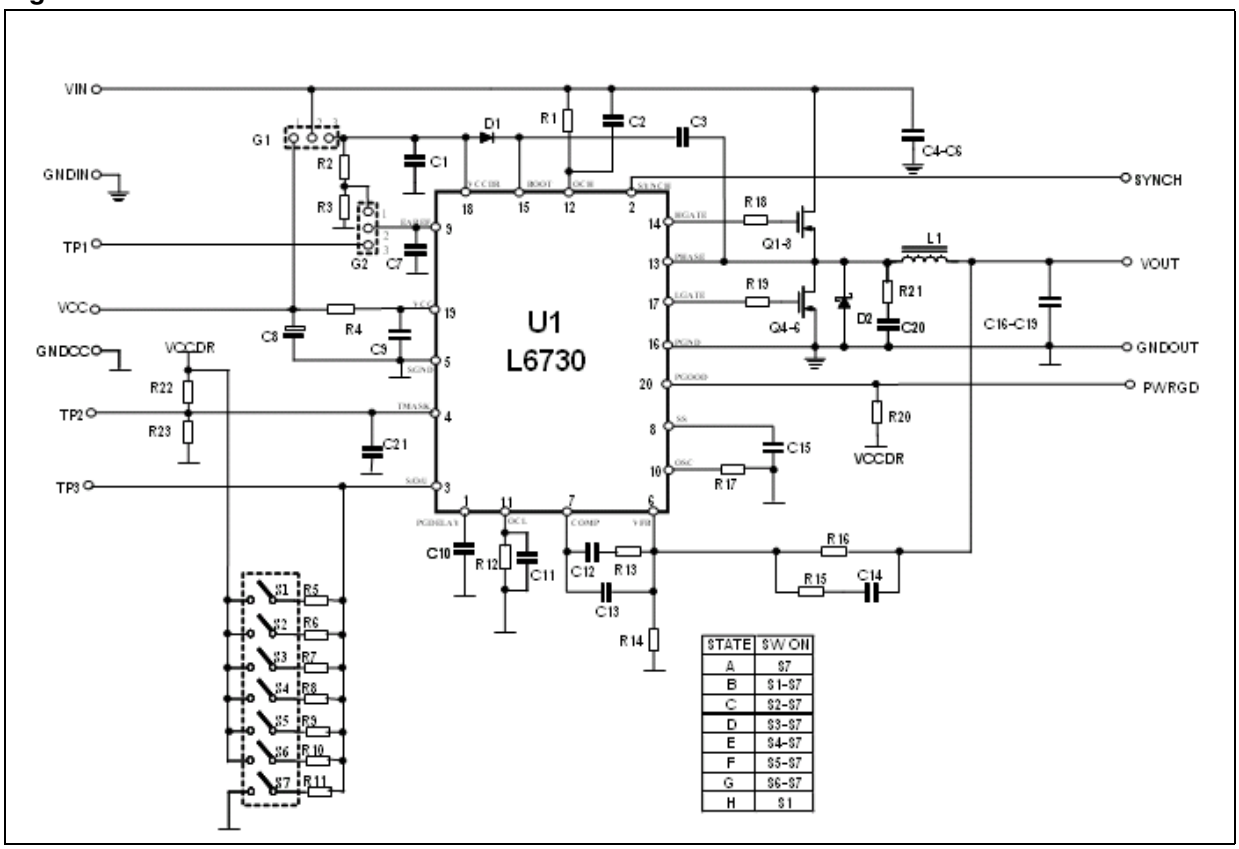


Table 8. Demonstration board part list

Reference	Value	Manufacturer	Package	Supplier
R1	820Ω	Neohm	SMD 0603	IFARCAD
R2	0Ω	Neohm	SMD 0603	IFARCAD
R3	N.C.			
R4	10Ω 1% 100mW	Neohm	SMD 0603	IFARCAD
R5	11K 1% 100mW	Neohm	SMD 0603	IFARCAD
R6	6K2 1% 100mW	Neohm	SMD 0603	IFARCAD
R7	4K3 1% 100mW	Neohm	SMD 0603	IFARCAD
R8	2K7 1% 100mW	Neohm	SMD 0603	IFARCAD
R9	1K8 1% 100mW	Neohm	SMD 0603	IFARCAD
R10	1K2 1% 100mW	Neohm	SMD 0603	IFARCAD
R11	2K7 1% 100mW	Neohm	SMD 0603	IFARCAD
R12	1K	Neohm	SMD 0603	IFARCAD
R13	2K7 1% 100mW	Neohm	SMD 0603	IFARCAD

Table 8. Demonstration board part list (continued)

Reference	Value	Manufacturer	Package	Supplier
R14	1K 1% 100mW	Neohm	SMD 0603	IFARCAD
R15	1K 1% 100mW	Neohm	SMD 0603	IFARCAD
R16	4K7 1% 100mW	Neohm	SMD 0603	IFARCAD
R17	N.C.			
R18	2.2Ω	Neohm	SMD 0603	IFARCAD
R19	2.2Ω	Neohm	SMD 0603	IFARCAD
R20	10K 1% 100mW	Neohm	SMD 0603	IFARCAD
R21	N.C.			
R22	N.C.			
R23	0Ω	Neohm	SMD 0603	IFARCAD
C1	220nF	Kemet	SMD 0603	IFARCAD
C3-C7-C9-C15-C21	100nF	Kemet	SMD 0603	IFARCAD
C2	1nF.	Kemet	SMD 0603	IFARCAD
C4-C6	100uF 20V	OSCON 20SA100M	RADIAL 10X10.5	SANYO
C8	4.7uF 20V	AVX	SMA6032	IFARCAD
C10	10nF	Kemet	SMD 0603	IFARCAD
C11	N.C.			
C12	47nF	Kemet	SMD 0603	IFARCAD
C13	1.5nF	Kemet	SMD 0603	IFARCAD
C14	4.7nF	Kemet	SMD 0603	IFARCAD
C18-C19	330uF 6.3V	POSCAP 6TPB330M	SMD	SANYO
C20	N.C.			
L1	1.8uH	Panasonic	SMD	ST
D1	1N4148	ST	SOT23	IFARCAD
D2	STS1L30M	ST	DO216AA	ST
Q1-Q2	STS12NH3LL	ST	SO8	ST
Q4-Q5	STSJ100NH3LL	ST	SO8	ST
U1	L6730	ST	HTSSOP20	ST
SWITCH	DIP SWITCH 7 POS.			ST

Table 9. Other inductor manufacturer

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
WURTH ELEKTRONIC	744318180	1.8	20
SUMIDA	CDEP134-2R7MC-H	2.7	15
EPCOS	HPI_13 T640	1.4	22
TDK	SPM12550T-1R0M220	1	22
TOKO	FDA1254	2.2	14
COILTRONICS	HCF1305-1R0	1.15	22
	HC5-1R0	1.3	27

Table 10. Other capacitor manufacturer

Manufacturer	Series	Capacitor value (µF)	Rated voltage (V)
TDK	C4532X5R1E156M	15	25
	C3225X5R0J107M	100	6.3
NIPPON CHEMI-CON	25PS100MJ12	100	25
PANASONIC	ECJ4YB0J107M	100	6.3

8 I/O Description

Figure 38. Demonstration board

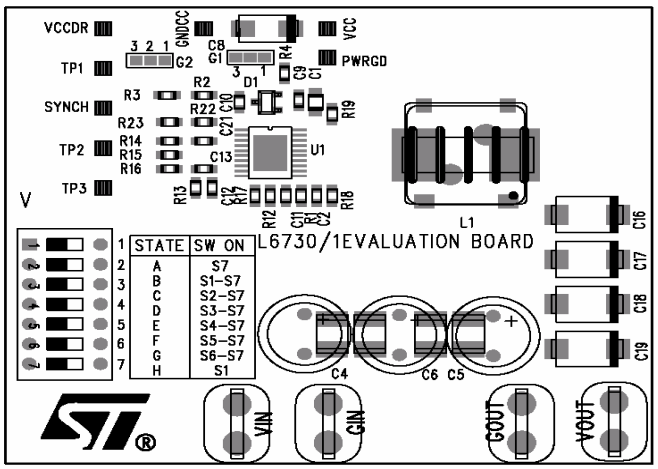


Table 11. I/O functions

Symbol	Function
Input (Vin-Gin)	The input voltage can range from 1.8V to 14V. If the input voltage is between 4.5V and 14V it can supply also the device (through the V_{CC} pin) and in this case the pin 1 and 2 of the jumper G1 must be connected together.
Output (V_{OUT}-G_{OUT})	The output voltage is fixed at 3.3V but it can be changed by replacing the resistor R14 of the output resistor divider: $$Vo = V_{REF} \cdot (1 + \frac{R_{16}}{R_{14}})$$ The over-current-protection limit is set at 15A but it can be changed by replacing the resistors R1 and R12 (see OCL and OCH pin in *Table 4: Pin connection*).
V_{CC}-GND_{CC}	Using the input voltage to supply the controller no power is required at this input. However the controller can be supplied separately from the power stage through the V_{CC} input (4.5-14V) and, in this case, jumper G1 must be left open.
V_{CCDR}	An internal LDO provides the power into the device. The input of this stage is the V_{CC} pin and the output (5V) is the V_{CCDR} pin. The LDO can be bypassed, providing directly a 5V voltage from V_{CCDR} and Gndcc. In this case the pins 1 and 3 of the jumper G1 must be shorted.
TP1	This pin can be used as an input or as a test point. If all the jumper G2 pins are shorted, TP1 can be used as a test point of the voltage at the EAREF pin. If the pins 2 and 3 of G2 are connected together, TP1 can be used as an input to provide an external reference for the internal error amplifier (see section 4.3. Internal and external references).

Table 11. I/O functions (continued)

Symbol	Function
TP2	This test point is connected to the Tmask pin (see *Table 4: Pin connection*).
TP3	This test point is connected to the S/O/U pin (see *Chapter 5.10 on page 27*).
SYNCH	This pin is connected to the synch pin of the controller (see *Chapter 5.11 on page 28*).
PWRGD	This pin is connected to the PGOOD pin of the controller.
DIP SWITCH	Different positions of the dip switch correspond to different settings of the multifunction pin (S/O/U) (CC/O/U).

Table 12. Dip switch

UVLO	OVP	SINK CC	Vsou/V_{CCDR}	DIP switch	State
5V	Not latched	Not	0	S7	A
5V	Not latched	Yes	0.2	S1-S7	B
5V	Latched	Not	0.3	S2-S7	C
5V	Latched	Yes	0.4	S3-S7	D
12V	Not latched	Not	0.5	S4-S7	E
12V	Not latched	Yes	0.6	S5-S7	F
12V	Latched	Not	0.7	S6-S7	G
12V	Latched	Yes	1	S1	H

9 Efficiency

The following figures show the demo board efficiency versus load current for different values of input voltage and switching frequency:

Figure 39. Demonstration board efficiency 400 kHz

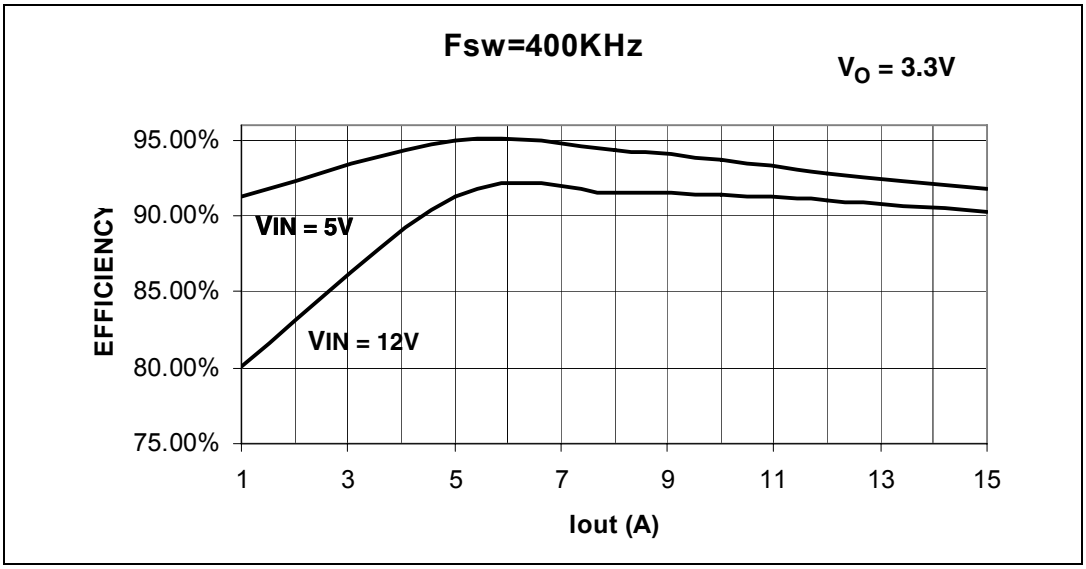


Figure 40. Demonstration board efficiency 645 kHz

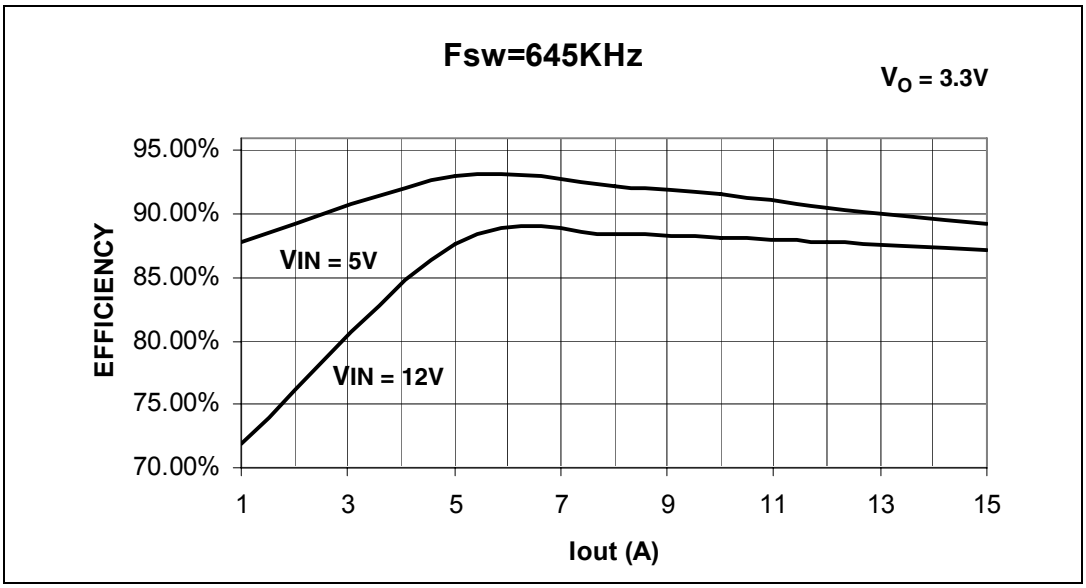


Figure 41. Demonstration board efficiency 1 MHz

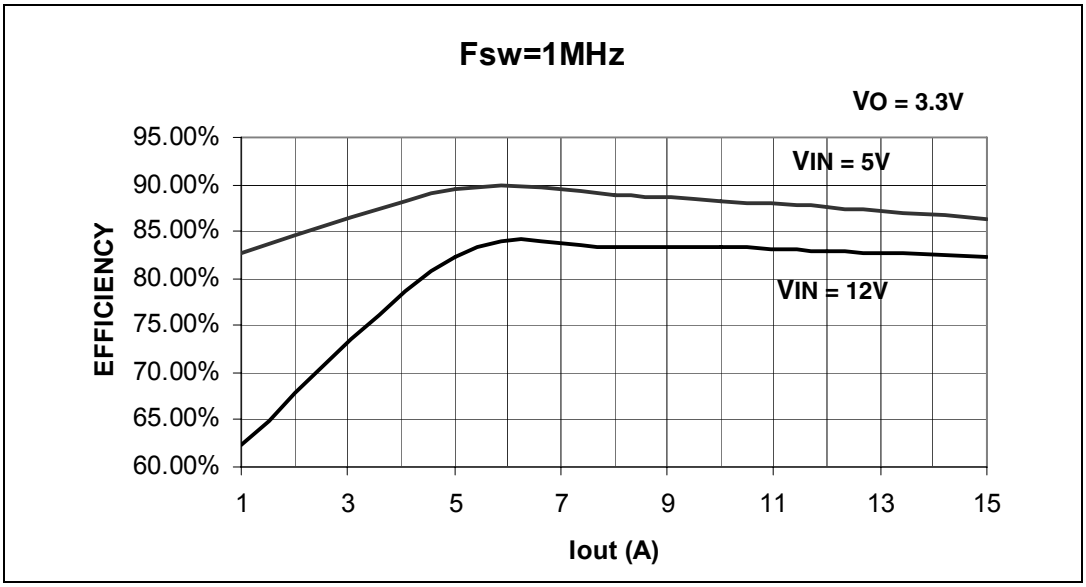
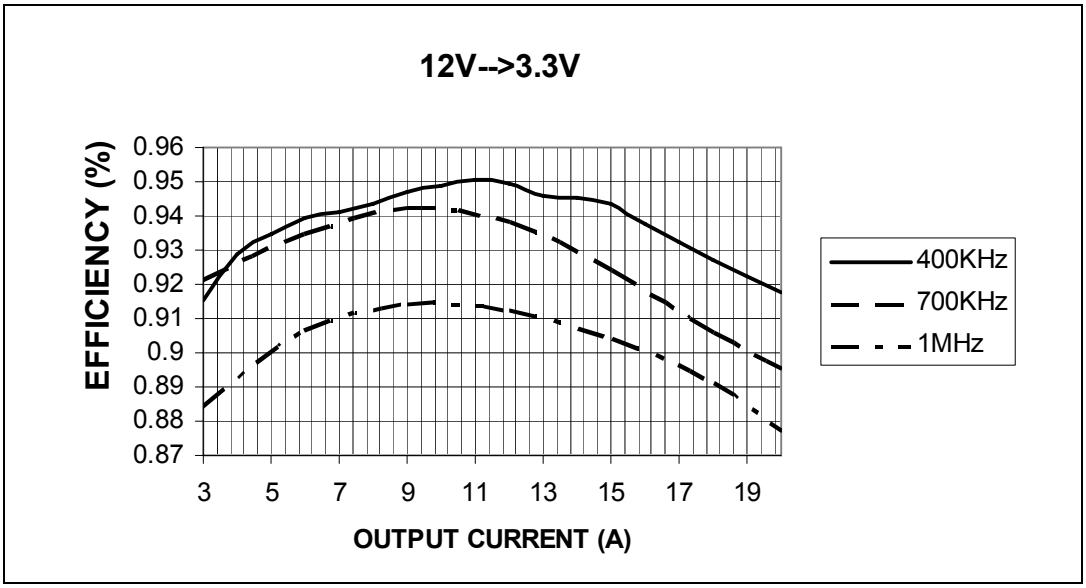


Figure 42. Efficiency with 2xSTS12NH3LL+2XSTSJ100NH3LL



10 POL demonstration board

10.1 Description

A compact demonstration board has been designed to manage currents in the range of 10-15 A. *Figure 39* shows the schematic and *Table 10* the part list. Multi-layer-ceramic-capacitors (MLCCs) have been used on the input and the output in order to reduce the overall size.

Figure 43. Pol demonstration board schematic

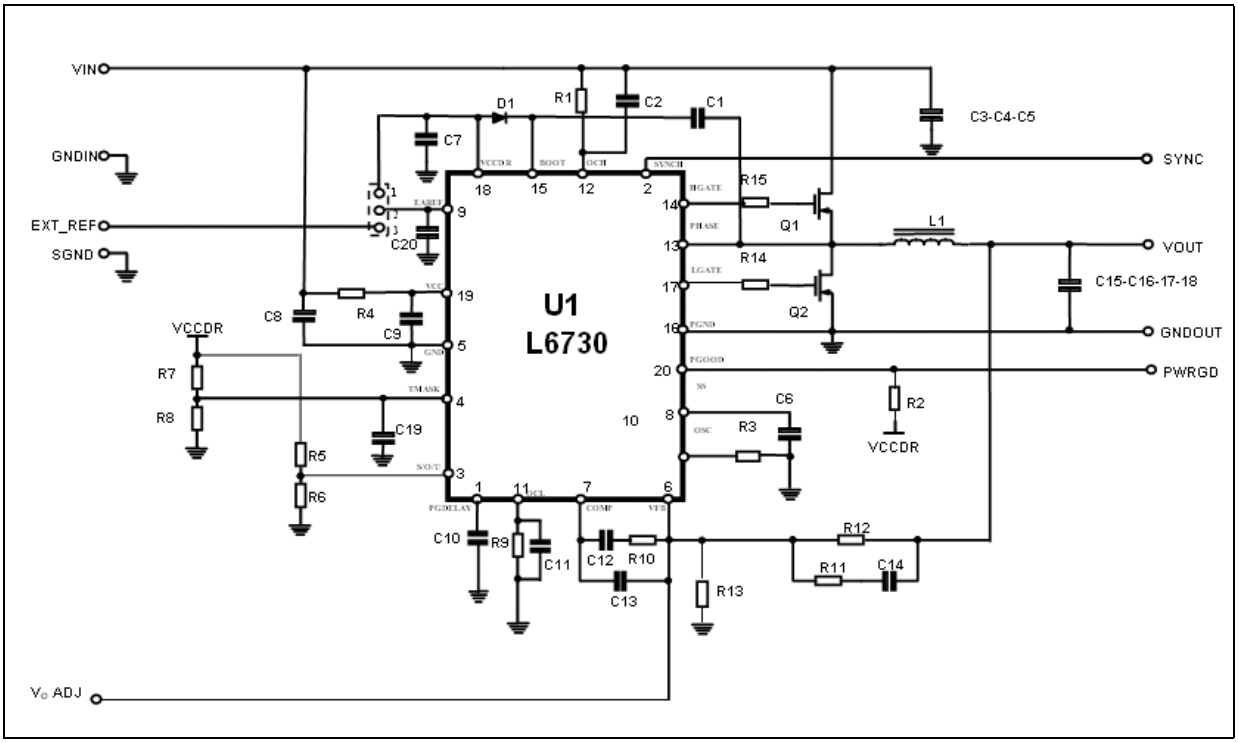


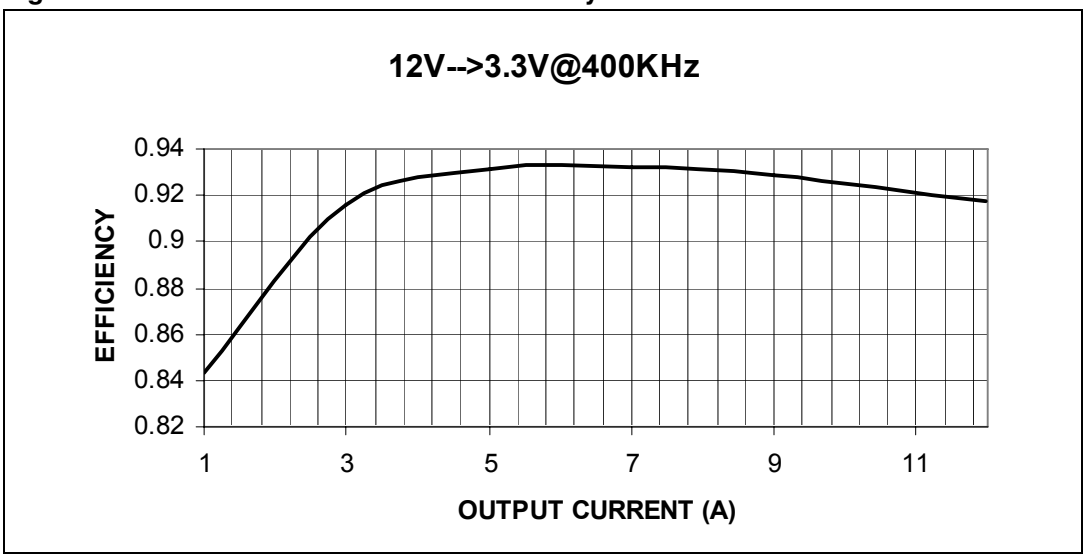
Table 13. Pol demonstration board part list

Reference	Value	Manufacturer	Package	Supplier
R1	1K8Ω	Neohm	SMD 0603	IFARCAD
R2	10KΩ	Neohm	SMD 0603	IFARCAD
R3	N.C.			
R4	10Ω	Neohm	SMD 0603	IFARCAD
R5	11K 1% 100mW	Neohm	SMD 0603	IFARCAD
R6	2K7 1% 100mW	Neohm	SMD 0603	IFARCAD
R7	N.C.	Neohm	SMD 0603	IFARCAD
R8	0Ω	Neohm	SMD 0603	IFARCAD
R9	3K 1% 100mW	Neohm	SMD 0603	IFARCAD
R10	4K7 1% 100mW	Neohm	SMD 0603	IFARCAD

Table 13. Pol demonstration board part list (continued)

Reference	Value	Manufacturer	Package	Supplier
R11	15Ω 1% 100mW	Neohm	SMD 0603	IFARCAD
R12	4K7 1% 100mW	Neohm	SMD 0603	IFARCAD
R13	1K 1% 100mW	Neohm	SMD 0603	IFARCAD
R14	2.2Ω	Neohm	SMD 0603	IFARCAD
R15	2.2Ω	Neohm	SMD 0603	IFARCAD
C1-C7	220nF	Kemet	SMD 0603	IFARCAD
C6- C19-C20-C9	100nF	Kemet	SMD 0603	IFARCAD
C2	1nF	Kemet	SMD 0603	IFARCAD
C11	N.C.			
C12	68nF	Kemet	SMD 0603	IFARCAD
C13	220pF	Kemet	SMD0603	IFARCAD
C8	4.7uF 20V	AVX	SMA6032	IFARCAD
C14	6.8nF	Kemet	SMD 0603	IFARCAD
C3-C4-C5	15uF	TDK MLC C4532X5R1E156M	SMD1812	IFARCAD
C15-C16-C17-C18	100uF	PANASONIC MLC P/N ECJ4YBOJ107M	SMD 1210	IFARCAD
L1	1.8uH	Panasonic	SMD	ST
D1	STS1L30M	ST	DO216AA	ST
Q1	STS12NH3LL	ST	POWER SO8	ST
Q2	STSJ100NH3LL	ST	POWER SO8	ST
U1	L6730	ST	HTSSOP20	ST

Figure 44. Pol demonstration board efficiency



11 Package mechanical data

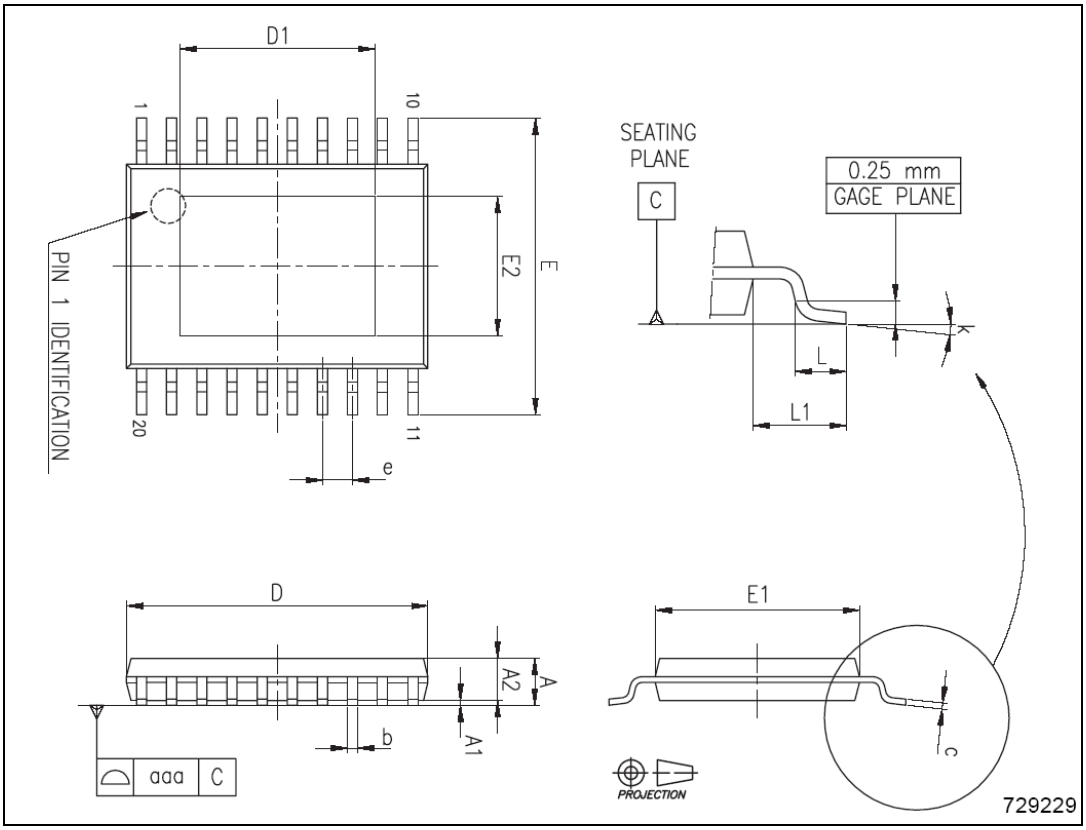
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 14. HTSSOP20 mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.200			0.047
A1			0.150			0.006
A2	0.800	1.000	1.050	0.031	0.039	0.041
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.003		0.008
D(1)	6.400	6.500	6.600	0.252	0.256	0.260
D1(3)	2.200			0.087		
E	6.200	6.400	6.600	0.244	0.252	0.260
E1(2)	4.300	4.400	4.500	0.170	0.173	0.177
E2(3)	1.500			0.059		
e		0.650			0.025	
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.000			0.039	
k	0° min., 8° max.					
aaa			0.100			0.004

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension “E1” does not include interlead flash or protrusions. Intelead flash or protrusions shall not exceed 0.25mm per side.
3. The size of exposed pad is variable depending of leadframe design pad size. End user should verify “D1” and “E2” dimensions for each device application.

Figure 45. Package dimensions



12 Revision history

Table 15. Document revision history

Date	Revision	Changes
21-Dec-2005	1	Initial release
29-May-2006	2	New template, thermal data updated
07-Dec-2009	3	Updated *Table 4 on page 8* and added *Section 1.2 on page 6*

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