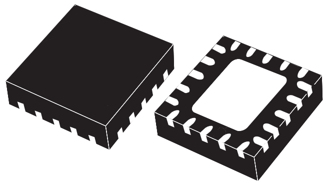
High performance 3 A ULDO linear regulator

Features

- Up to 5 V input voltage range
- 60 mΩ max $R_{DS(on)}$
- 35 μA shut-down current
- 3 A maximum output current
- Split bias and power supplies
- Adjustable output voltage: 0.5 V to 3.0 V
- Excellent load and line regulation: 1 % accuracy (over temperature)
- MLCC supported
- Programmable soft-start
- Short-circuit protection
- 3.5 A overcurrent protection
- Thermal shut-down
- VFQFPN20 4 x 4 x 1.0 mm package

Applications

- Motherboard
- Mobile PC
- Hand-held instruments
- PCMCIA cards
- Processors I/O
- Chipset and RAM supply



VFQFPN20
(4.0 x 4.0 x 1.0 mm)

Description

L6935 is an ultra low drop output linear regulator operating up to 5 V input and is able to support output current up to 3 A. Designed with an internal low-$R_{DS(on)}$ N-channel MOSFET, it can be used for on-board DC-DC conversions saving in real estate, list of components and power dissipation.

Bias input and power input are split to allow linear conversion from buses lower than 1.2 V minimizing power losses.

L6935 provides the application with an adjustable voltage from 0.5 V to 3.0 V with a voltage regulation accuracy of 1 %. soft-start is available to program the output voltage rise-time according to the external capacitor connected.

Enable and Power Good functions make L6935 suitable for complex systems and programmable start-up sequencing.

The current limit at 3 A protects the system during a short circuit. The current is sensed in the power DMOS in order to limit the power dissipation. Thermal shut down limits the internal temperature at 150 °C with a hysteresis of 20 °C.

Table 1. Device summary

Order codes	Package	Packing
L6935	VFQFPN20	Tube
L6935TR		Tape and reel

Contents

1 Typical application circuit and block diagram

1.1 Application circuit

Figure 1. Typical application circuit - VIN = VBIAS

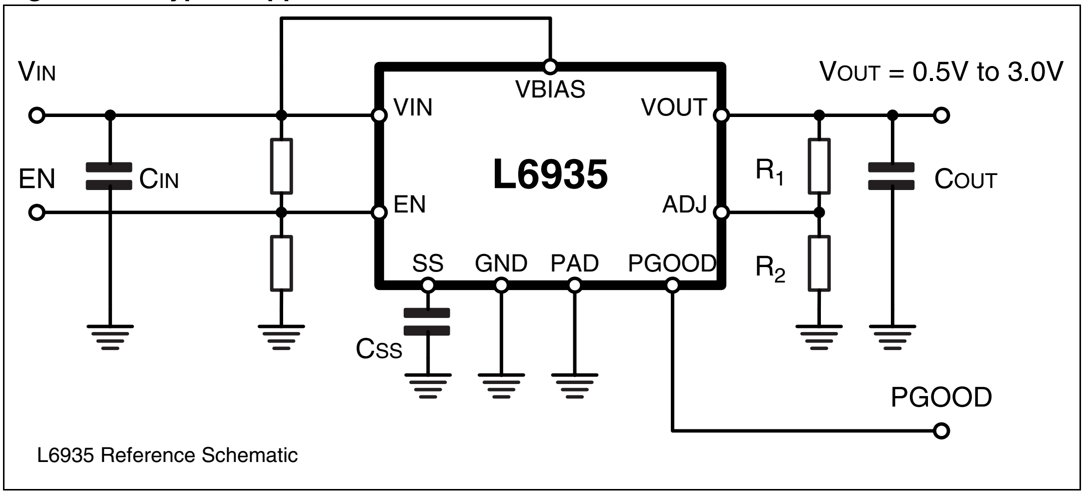
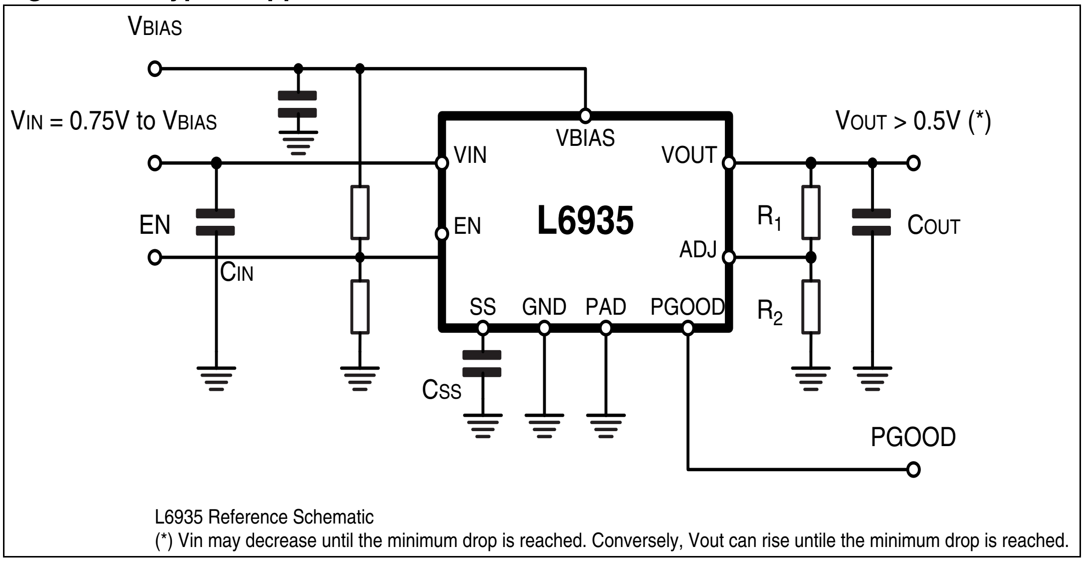
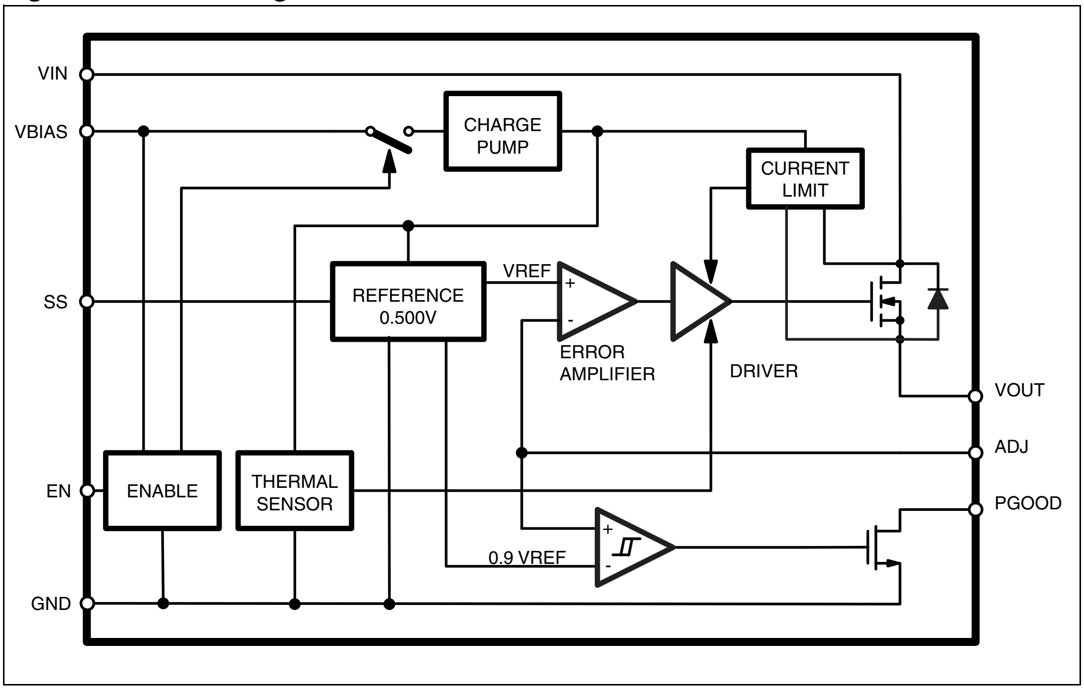


Figure 2. Typical application circuit - VIN ≠ VBIAS



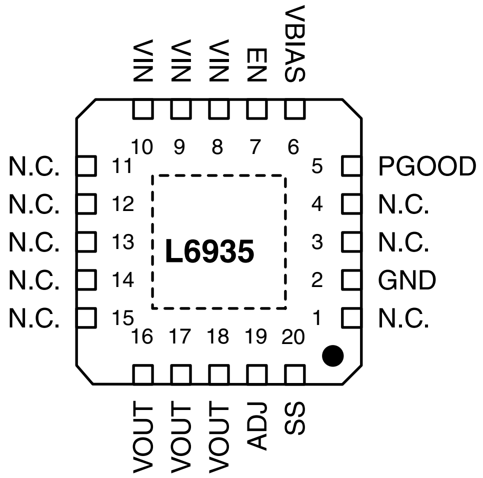
1.2 Block diagram

Figure 3. Block diagram



2 Pins description and connection diagrams

Figure 4. Pins connection (top view)



2.1 Pin descriptions

Table 2. Pins descriptions

Pin #	Name	Function
1	N.C.	Not internally connected.
2	GND	Ground connection. Connect to PCB ground plane.
3, 4	N.C.	Not internally connected.
5	PGOOD	Power Good output flag: the pin is open drain and it is forced low if the output voltage is lower than 90 % of the programmed voltage. If not used, it can be left floating.
6	VBIAS	Input bias supply. This pin supplies the internal logic to drive the power N-channel MOSFET that realize the voltage conversion. Connect directly to V_{IN} or to a different supply ranging from V_{IN} to 5 V. The voltage connected to this pin MUST always be higher or equal that V_{IN}.
7	EN	Enables the device if a voltage higher than 1 V is applied. When pulled low, the device is in low-power consumption: everything inside the controller is kept OFF. See *Section 6.2* for details about EN signal and power sequencing.
8 to 10	VIN	Power supply voltage. This pin is connected to the drain of the internal N-channel MOSFET. Filter to GND with capacitor larger than the one used for V_{OUT}.
11 to15	N.C.	Not internally connected.
16 to 18	VOUT	Regulated output voltage. This pin is connected to the source of the internal N-mos. MLCC capacitor are supported. Filter to GND with capacitor smaller than the one used for V_{IN}.

Table 2. Pins descriptions (continued)

Pin #	Name	Function
19	ADJ	Feedback for the IC regulation. Connecting this pin through a voltage divider to V_{OUT}, it is possible to program the output voltage between 0.5 V and 3.0 V.
20	SS	Soft-start pin. The soft-start time is programmed connecting an external capacitor C_{SS} from this pin to GND. In steady state regulation, the voltage at this pin is 3.3 V.
PAD	GND	Ground connection. Connect to PCB GND Plane with enough VIAs to improve thermal conductivity.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VIN	to GND	5.5	V
VBIAS, EN, PGOOD	to GND	6	V
SS, VOUT	to GND	-0.3 to 3.3	V
ADJ	to GND	-0.3 to 1	V
Maximum withstanding voltage range test condition: CDF-AEC-Q100-002 “human body model” acceptance criteria: “normal performance”		±1000	V

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient[(1)]	55	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-50 to 150	°C
T_J	Junction temperature range	-25 to 150	°C

1. Measured with the component mounted on demonstration board in free air (22 x 28.5 mm - 2 layer 70 µm copper).

3.3 Electrical characteristics

Table 5. Electrical characteristics
(V_{IN} = 5 V, V_{BIAS} = 5 V; T_A = 25 °C unless otherwise specified).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Recommended operating conditions						
VIN	Operating supply voltage	$V_{IN} = V_{BIAS}$ $V_{BIAS} < 5$ V			5.0 V_{BIAS}	V
VBIAS	UVLO	V_{BIAS} rising			1.275	V
I_{IN}	Quiescent current	Iout = 0 A		2.3	3	mA
	Shut-down current	$V_{IN} = V_{BIAS}$ = 3.3 V $V_{IN} = V_{BIAS}$ = 5.0 V			25 40	µA
Voltage regulation						
VOUT	Output voltage	Io = 0.1 A; V_{IN} = 3.3 V; ADJ = OUT	0.496	0.500	0.504	V
ADJ	Line regulation	Vin = 3.30 V +/- 10 %; Io = 10 mA Vin = 4.50 V +/- 10 %; Io = 10 mA			2.5 2.5	mV
	Load regulation	Vin = 3.3 V; Io = 100 mA to 3 A			7	mV
	Ripple rejection (1)	F = 100...120 Hz; Io = 10 mA Vin = 3 V; ΔVin = 2 Vpp; Vout = 1 V		45		dB
$R_{DS(on)}$	Drain-to-source resistance	Io = 3 A		30	60	mΩ
Enable, SS and protections						
I_{OCP}	Current limiting	Vo = 1.8 V	3.15	3.50	3.85	A
PGOOD	Power Good threshold	V_{ADJ} falling, wrt Ref.	77		85	%
	Hysteresis			10		%
	Voltage low	I = -1 mA			0.4	V
EN	Enable threshold	EN rising			1.05	V
SS	Soft start current	Vss = 0 V		1.0		µA
OT	Thermal shut-down	Temperature rising (1)		150		°C
		Hysteresis (1)		20		°C

1. Parameter guaranteed by design, not tested in production

4 Typical performances

Figure 5. Output voltage and OC threshold vs junction temperature

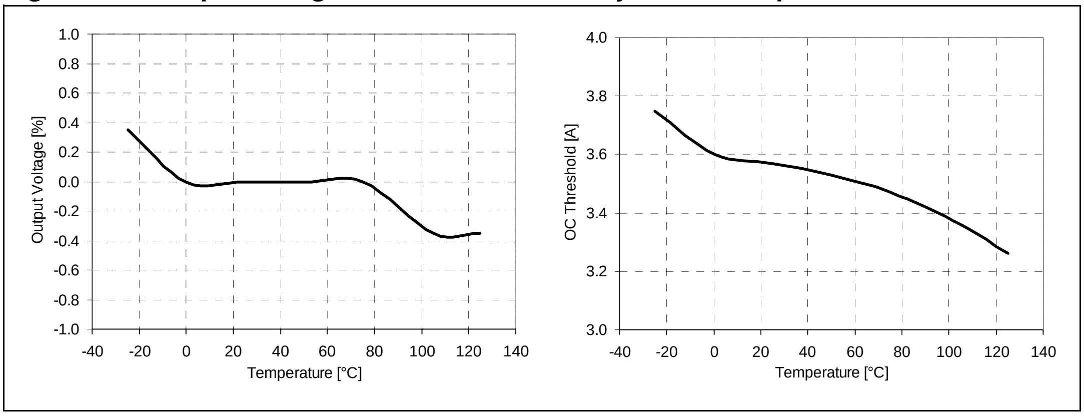


Figure 6. Quiescent and shutdown current vs junction temperature

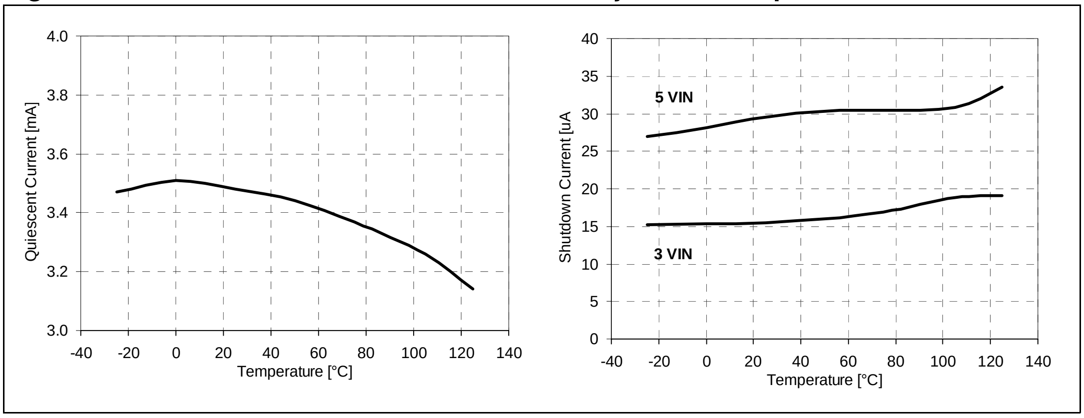


Figure 7. Line regulation

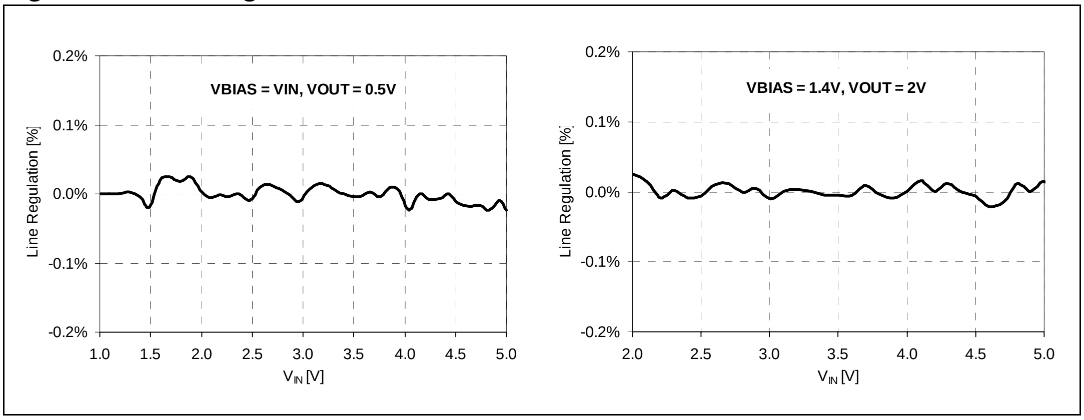
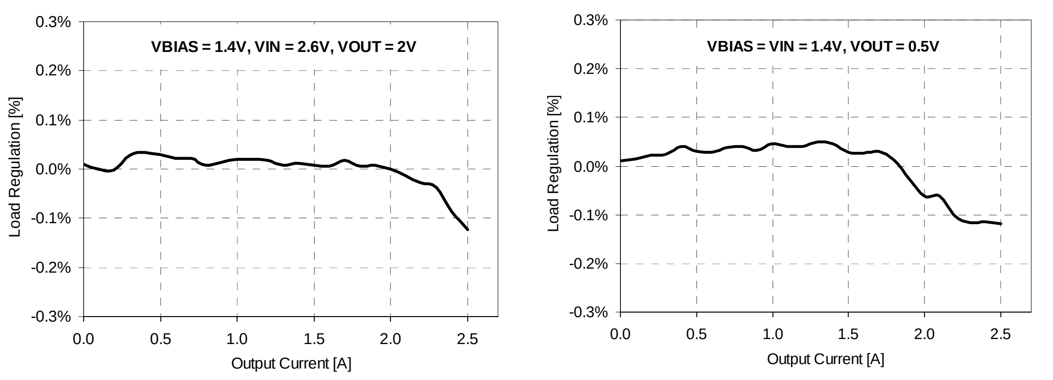


Figure 8. Load regulation



5 Device description

5.1 Soft-start

L6935 implements a soft-start feature to smoothly charge the output filter avoiding high in-rush currents to be required to the input power supply.

The soft-start process begins as soon as V_{BIAS} reaches UVLO and ENABLE is asserted. A constant current $I_{SS} = 1.0\ \mu A$ is sourced through the SS pin: connecting an external capacitor (C_{SS}) to this pin a voltage ramp is implemented; the voltage ramp internally clamps the E.A. reference, resulting in a controlled slope for the output voltage. As the voltage on C_{SS} reaches the V_{REF} value the internal clamp is released.

In this way, the soft-start process lasts for:

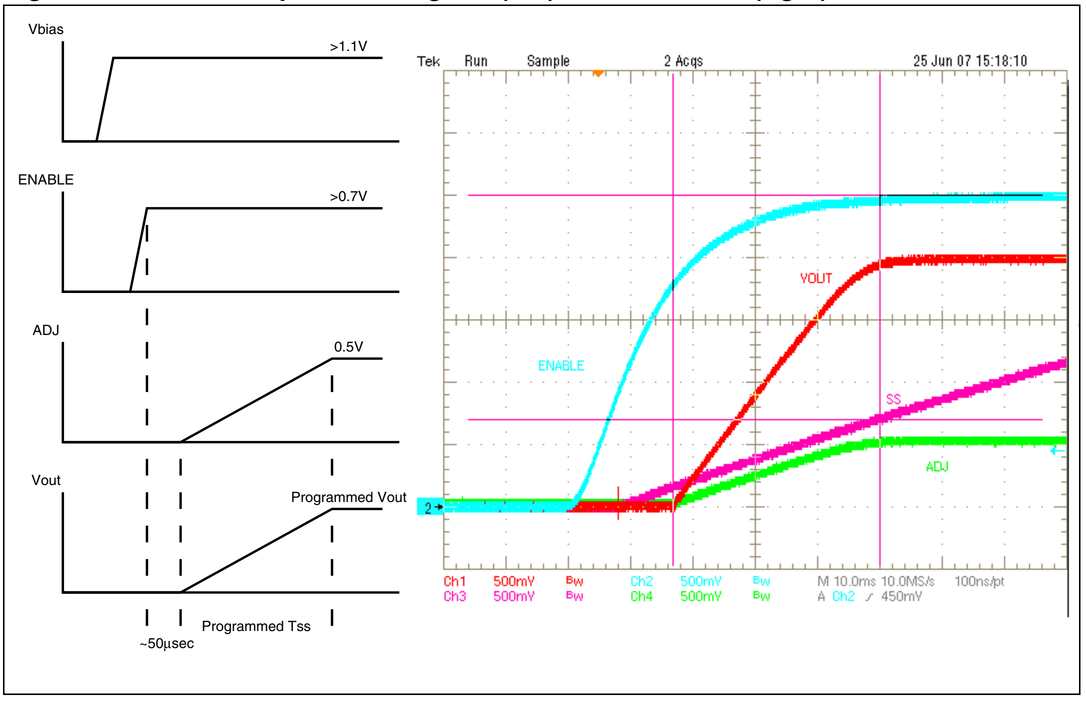
$$T_{SS} = C_{SS} \cdot \frac{V_{REF}}{I_{SS}} = 5 \cdot 10^5 \cdot C_{SS}[F]$$

where C_{SS} is the external capacitor [F] and T_{SS} is the soft-start time [sec.].

If the device is disabled (ENABLE low) and the VBIAS is still present, the SS pin is clamped to GND for a fixed time of about 50 µs. in order to discharge the residual charge present on C_{SS}: in this way, the device will be ready for a new SS process as ENABLE is asserted again.

Figure 9 describes a typical soft-start process.

Figure 9. Soft start process diagram (left) and measured (right)

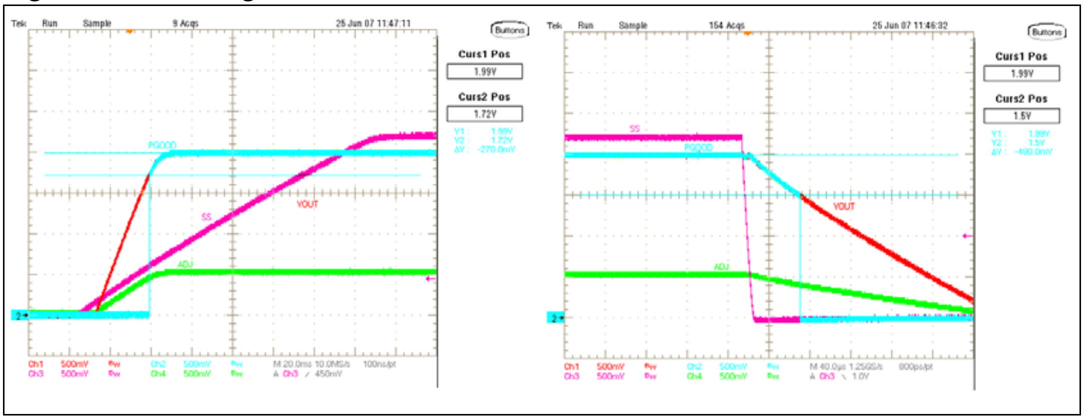


5.2 Power Good

L6935 presents a PGOOD flag, an open drain output that is grounded during all the soft start procedure, and is left free when V_{OUT} reaches 90 % of the programmed value.

An hysteresis of 10 % is also provided in order to avoid false triggering due to the noise generated by the application. *Figure 10* shows the PGOOD commutations.

Figure 10. Power good window



5.3 V_{IN} vs V_{BIAS}

L6935 provides the flexibility to supply the internal logic (VBIAS) with a supply different than the power input (VIN). The aim of this feature is to provide low-drop regulation still having the supply voltage to correctly drive the internal power mosfet so optimizing the conversion. VIN drives only the drain of the power DMOS and it can be kept as low as possible ($V_{IN} > V_{OUT} + V_{DROPmin}$), while V_{BIAS} drives the control section. V_{BIAS} must be typically higher than V_{IN}.

5.4 Protections

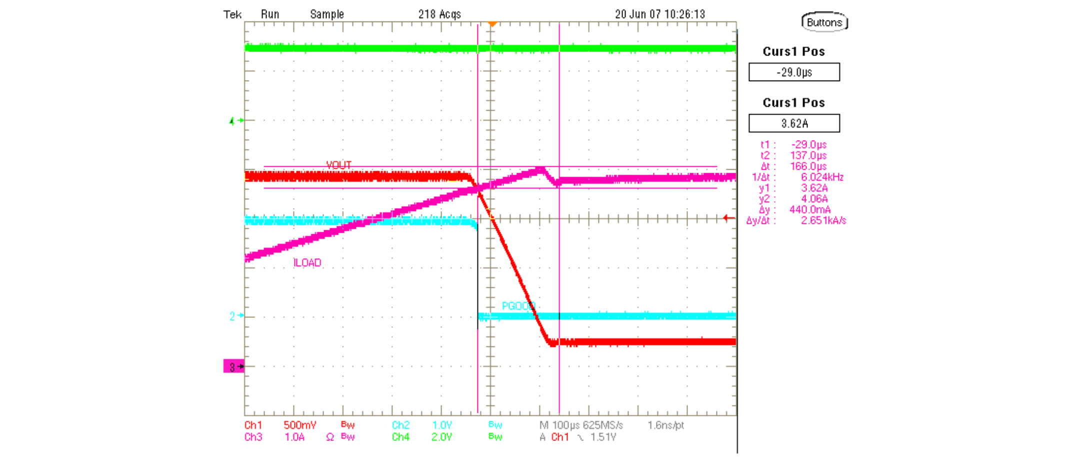
L6935 is equipped with a set of protections in order to protect both the load and the device from electrical overstress. Each protection does not latch the device, that returns to work properly as the perturbation disappear.

5.4.1 Over-current protection

An over current protection is provided: if the current that flows through the power DMOS is greater than 3.5 A, the device adjust the power DMOS driving voltage in order to keep constant the delivered current (I_{OUT}). Anyhow the output may drop also causing the PGOOD to be set low.

Figure 11 show the way the OCP intervention: as the threshold value is reached by I_{OUT}, the device forces a lower output current (~3.5 A).

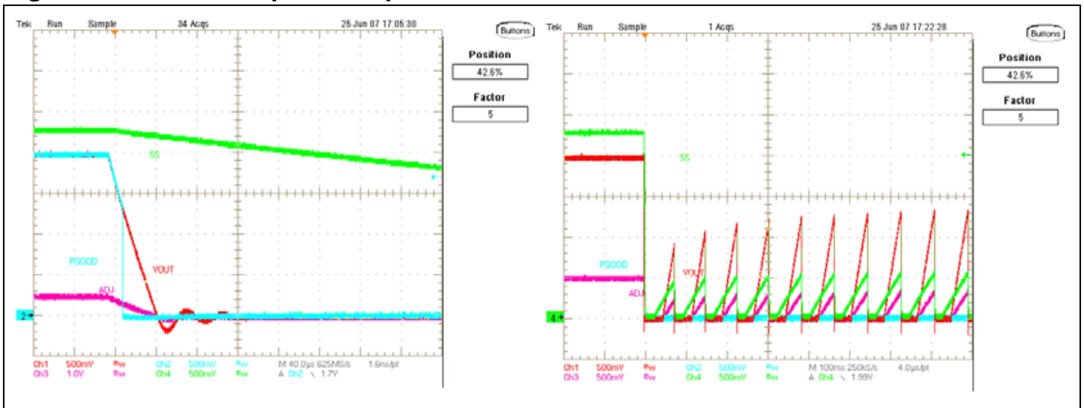
Figure 11. Over-current protection



5.4.2 Thermal protection

The device constantly monitors its internal temperature. As the silicon reaches a 150 °C, the control circuit turns off the power DMOS, and stays off until a safe temperature of 150° - 20° = 130 °C. *Figure 12* shows how the over-temperature protection intervention.

Figure 12. Over-temperature protection



6 Application information

L6935 is the best choice in smart linear regulator applications, due to its own small size, high power delivered and high regulation accuracy. Furthermore thermal shut-down and OCP guarantee the highest reliability for each application.

V_{IN} can be separated by V_{BIAS}: in this way the device can regulate the output voltage even if $V_{IN} < V_{BIAS}$, resulting in a better performance. In fact, the power dissipated decreases as V_{IN} get lower, according to the relationship $P_{DISS} = (V_{IN} - V_{OUT}) \times I_{OUT}$.

6.1 Components selection

6.1.1 Input capacitor

The choice of the input capacitor value depends on the several factor such as load transient requirements, input source (battery or DC/DC converter) and its distance from the input capacitor. Generally speaking, a capacitor with the lowest ESR possible should be chosen: a value within the range [10 µF; 100 µF] can be sufficient in many cases.

6.1.2 Output capacitor

The choice of the output capacitor value basically depends on the load transient requirement. Output capacitor must be sized according to the dynamic requests of the load. A too small capacitor may exhibit huge voltage drop after a load transient is applied: a value greater than 10 µF should be used.

In order to guarantee a good reliability, at least X5R type should be used as I/O capacitors.

Different kinds of input/output capacitors can be used: *Table 6.* shows a few tested examples.

Table 6. Input/output capacitor selection guide

Manufacturer	Type	I/O cap. value	Rated voltage
Murata - GRM31CR61ExxxK(1)	MLCC, SMD1206, X5R	10...100 µF	6.3 - 25 V
Panasonic - ECJ3YB1AxxxM	MLCC, SMD1206, X5R	10...100 µF	10 - 25 V
Panasonic - EEFFD0HxxxR	SPCap - SMD7343 28 mΩ ESR	10...100 µF	4 - 8 V
Sanyo - 8TPE100MPC2	POSCAP, SMD6032 25 mΩ ESR	10...100 µF	6.3 - 25 V
TDK - C3216X5R0JxxxMT	MLCC, SMD1210, X5R	10...100 µF	6.3 V

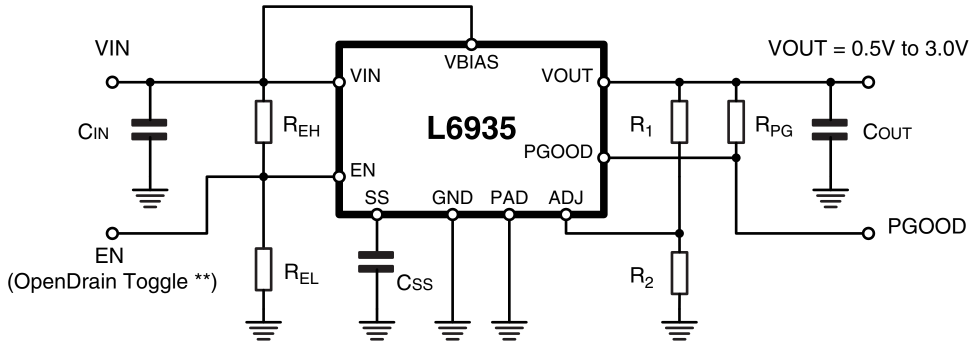
1. xxx in the part numbers stands for 106 (10 µF), 226 (22 µF)... 105 (100 µF)

6.2 VIN, VBIAS and sequencing

Different configurations for VIN and VBIAS are possibleand the power sequencing must consider the different timings in which the power suppliesbecomes available. In order to properly drive the device internal logic, it is reccomendedto control the sequence between EN signal and the VIN / VBIAS application: the device need to result being disabled when VBIAS crosses the UVLO threshols. Furthermore, in case of VIN <> VBIAS, the EN signal needs to be driven by the last-coming between the two supplies.

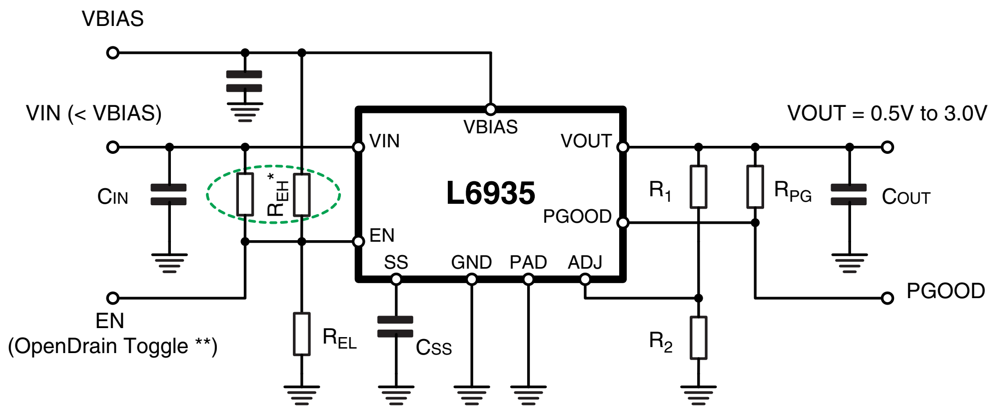
It is reccomended to drive the EN pin with a resistor divider connected as reported into *Figure 13* and *Figure 14*.

Figure 13. Recommended circuit for VBIAS = VIN



** Drive EN with external Open-Drain Signal.

Figure 14. Reccomended circuit for VBIAS ≠ VIN



* EN Divider (R_{EH}) needs to be connected to the Last-Coming rail between VCC and VIN.

** Drive EN with external Open-Drain Signal.

7 Demonstration board description

Figure 15 and *Figure 16* show the schematic and the layout of the demonstration board designed for L6935. V_{IN} and V_{BIAS} may be different and, in this case, R4 must not be mounted. C3 defines the Soft-Start timer, according to the relationship described in the *Section 5.1*.

The value of the output divider R_1 / R_2 have to be designed in order to program the desired V_{OUT} value, according to the following equation:

$$V_{OUT} = 0.5 \cdot \left(1 + \frac{R_1}{R_2}\right)$$

Figure 15. Demonstration board schematic

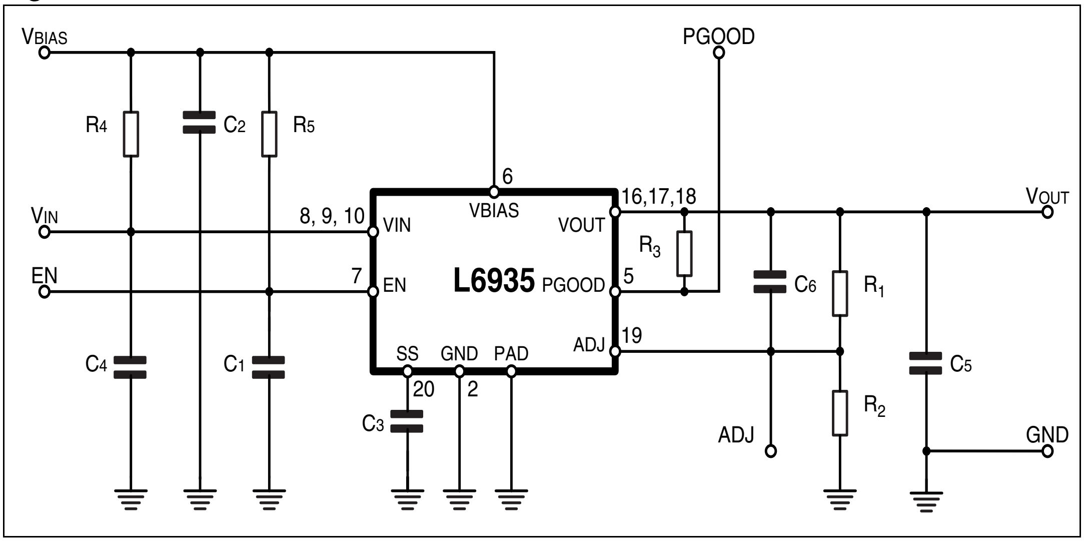
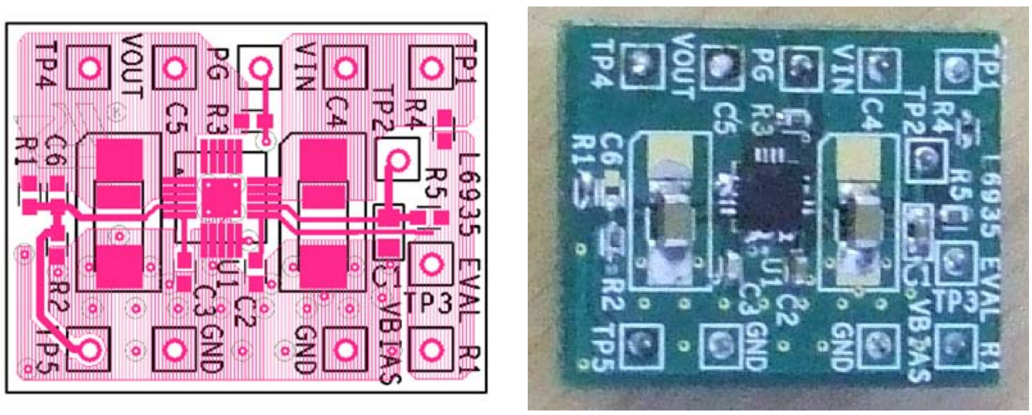


Figure 16. Demonstration board layout



Different values for R_1 are available in order to program the value of V_{OUT} (R_2 = 10 kΩ)

V_{OUT} = 0.50 V_{DC} @ R_1 = 0 Ω

V_{OUT} = 0.75 V_{DC} @ R_1 = 5 kΩ

V_{OUT} = 1.00 V_{DC} @ R_1 = 10 kΩ

V_{OUT} = 1.25 V_{DC} @ R_1 = 15 kΩ

V_{OUT} = 1.50 V_{DC} @ R_1 = 20 kΩ

V_{OUT} = 3.00 V_{DC} @ R_1 = 50 kΩ

Table 7. L6935 demonstration board bill of material

Reference	Description
C1, C2, c3	Chip capacitor 100 nF - 6.3 V - X5R
C4	Murata chip capacitor (GRM31CR60J226K) 1206, X5R, 6.3-25V, 22 µF
C5	Murata chip capacitor (GRM31CR61E106K) 1206, X5R, 6.3-25V, 10 µF
C6	Not mounted
R1	Chip resistor 15 kΩ +/-0.1% - 1/16 W
R2	Chip resistor 10 kΩ +/-0.1% - 1/16 W
R3, R5	Chip resistor 10 kΩ +/-5% - 1/16 W
R4	Chip resistor 0 Ω

8 VFQFPN20 mechanical data and package dimensions

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

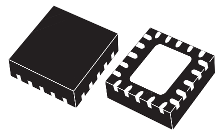
Figure 17. VFQFPN20 mechanical data and package dimensions

DIMENSIONS						
REF.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	31.496	35.433	39.370
A1		0.02	0.05		0.787	1.969
A2		0.65	1.00		25.591	39.370
A3		0.25			9.843	
b	0.18	0.23	0.30	7.087	9.055	11.811
D	3.85	4.00	4.15	151.57	157.48	163.39
D2	2.70	2.80	2.90	106.30	110.24	114.17
E	3.85	4.00	4.15	151.57	157.48	163.39
E2	2.70	2.80	2.90	106.30	110.24	114.17
e	0.45	0.50	0.55	17.717	19.685	21.654
L	0.3	0.4	0.5	11.811	15.748	19.685
ddd			0.08			3.150

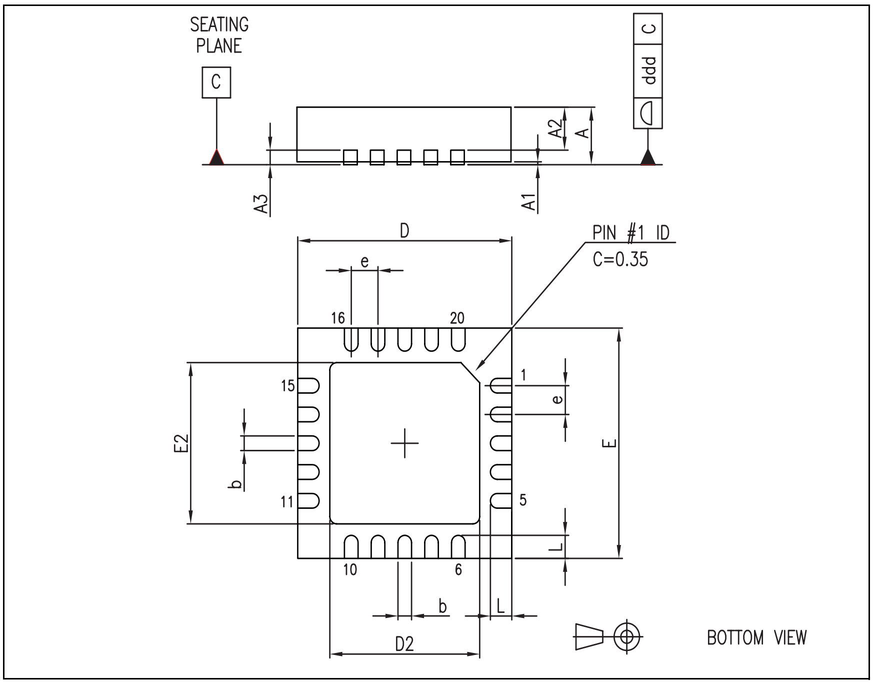
PACKAGE AND PACKING INFORMATION

Very **F**ine **Q**uad **F**lat **P**ackage **N**o lead

Weight: not available



VFQFPN20 (4x4x1.00mm)



9 Revision history

Table 8. Document revision history

Date	Revision	Changes
20-May-2008	1	Initial release