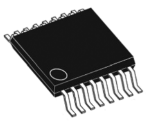
L7987

life.augmented

61 V 3 A asynchronous step-down switching regulator with adjustable current limitation

Datasheet - production data



HTSSOP16 (R_{TH} = 40 °C/W)

Features

- 3 A DC output current
- 4.5 V to 61 V operating input voltage
- $R_{DS,ON}$ = 250 mΩ typ.
- Adjustable f_{SW} (250 kHz - 1.5 MHz)
- Low IQ-SHD (11 µA typ. from V_{IN})
- Low IQ (1 mA typ. - V_{IN} 24 V - V_{OUT} 3.3 V)
- Output voltage adjustable from 0.8 V to V_{IN}
- Synchronization
- Adjustable soft-start time
- Adjustable current limitation
- Low dropout operation (12 µs max.)
- V_{BIAS} improves efficiency at light load
- PGOOD open collector output
- Output voltage sequencing
- Digital frequency foldback in short-circuit
- Peak current foldback in short-circuit
- Auto-recovery thermal shutdown

Applications

- Designed for 24 V bus
- Fail safe tolerant system
- Programmable logic controllers (PLCs)

Description

The L7987 device is a step-down monolithic switching regulator able to deliver up to 3 A DC. The output voltage adjustability ranges from 0.8 V to V_{IN}. The wide input voltage range and the 100% duty cycle capability meet the fail safe specifications for industrial systems. The embedded switchover feature on the V_{BIAS} pin maximizes the efficiency at light load. The adjustable current limitation, designed to select the inductor RMS current accordingly with the nominal output current, and the high switching frequency capability make the size of the application compact. Pulse-by-pulse current sensing with digital frequency foldback implements an effective constant current protection over the different application conditions. The peak current foldback decreases the stress of the power components in heavy short-circuit condition. The PGOOD open collector output can also implement output voltage sequencing during the power-up phase. Multiple devices can be synchronized sharing the SYNCH pin to prevent beating noise in low noise applications like sensors with A/D conversion.

Contents

1 Application schematic and block diagram

Figure 1. Application schematic

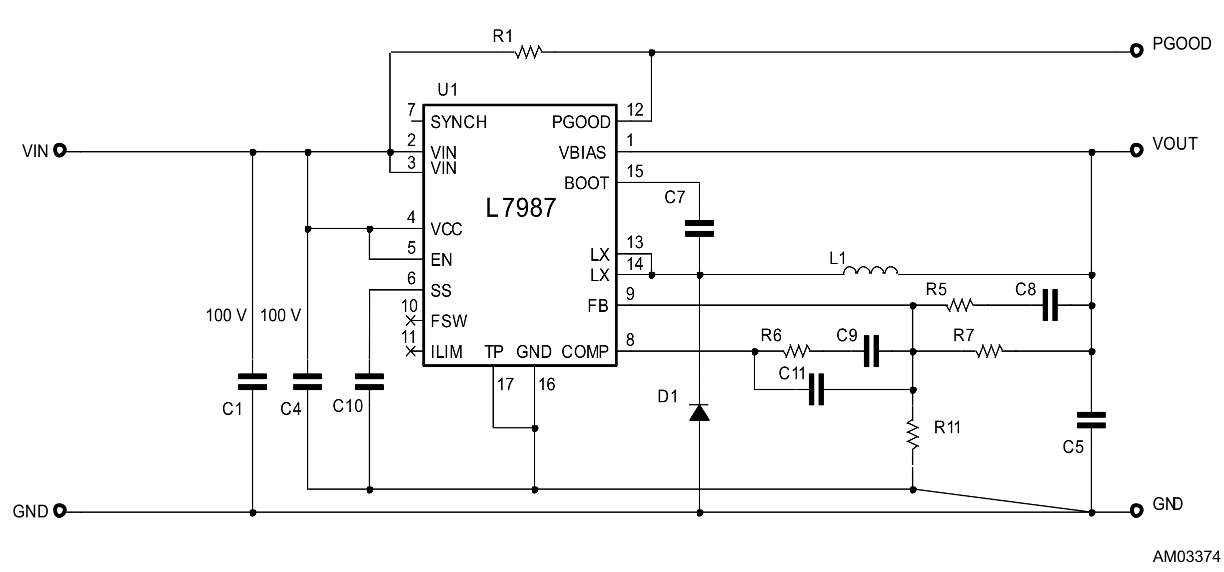
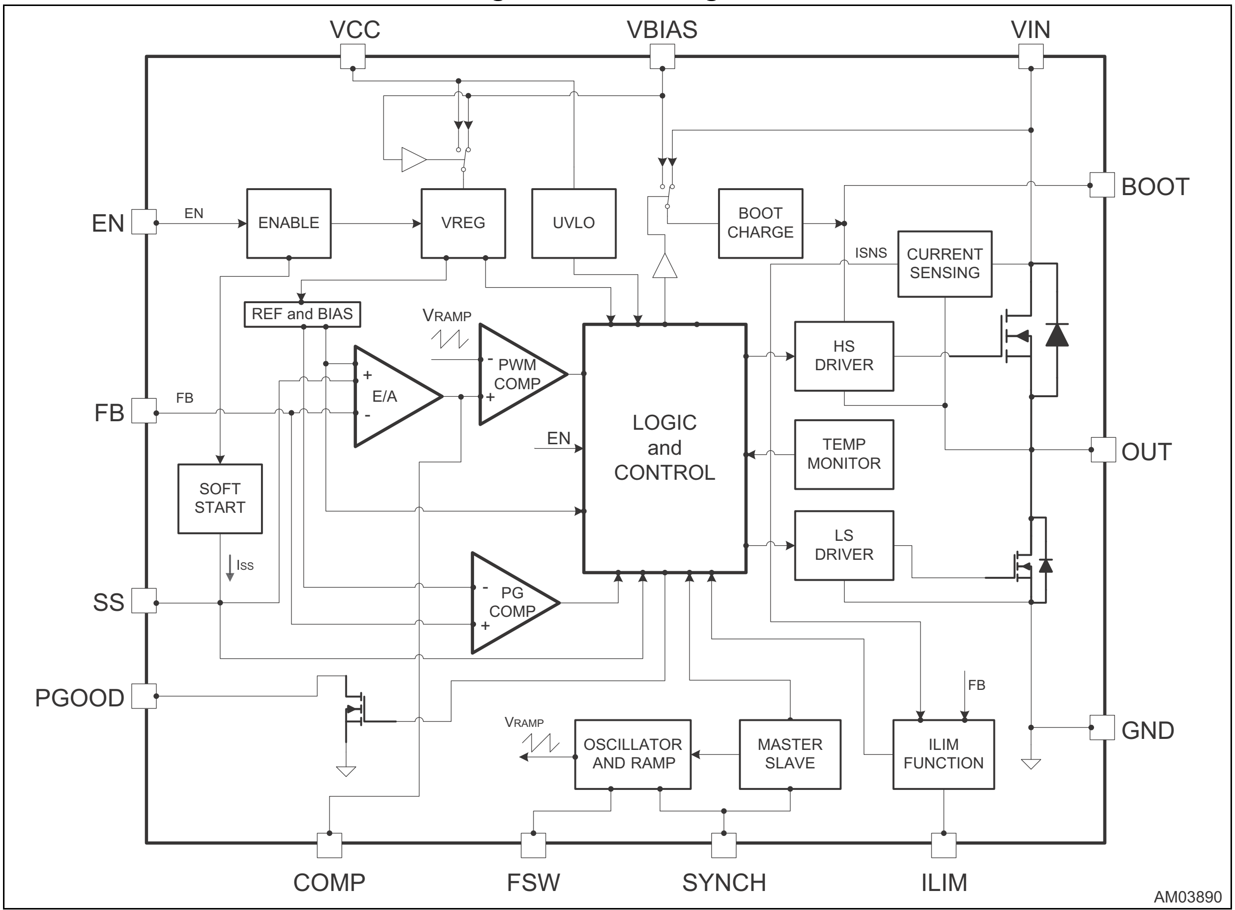


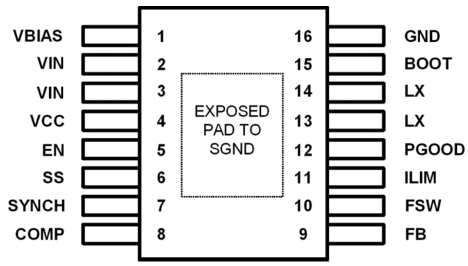
Figure 2. Block diagram



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top view)



2.2 Pin description

Table 1. Pin description

Number	Pin	Description
1	VBIAS	Auxiliary input that can be used to supply part of the analog circuitry to increase the efficiency at light load. Typically connected to the regulated output voltage or to an external voltage rail higher than 3 V. Connect to the signal GND if not used or bypass with a 1 µF ceramic capacitor if supplied by the output voltage or by an auxiliary rail.
2	VIN	DC input voltage
3	VIN	DC input voltage
4	VCC	Filtered DC input voltage to the internal circuitry. Bypass to the signal GND by a 1 µF ceramic capacitor.
5	EN	Active high enable pin. Connect to the VCC pin if not used.
6	SS	An internal current generator (5 µA typ.) charges the external capacitor to implement the soft-start.
7	SYNCH	Master / slave synchronization
8	COMP	Output of the error amplifier. The designed compensation network is connected at this pin.
9	FB	Inverting input of the error amplifier.
10	FSW	A pull-down resistor to GND selects the switching frequency.
11	ILIM	A pull-down resistor to GND selects the peak current limitation.
12	PGOOD	The PGOOD open collector output is driven low when the output voltage, sensed on the FB pin, is out of regulation.
13	LX	Switching node
14	LX	Switching node
15	BOOT	Connect an external capacitor (100 nF typ.) between BOOT and LX pins. The gate charge required to drive the internal n-DMOS is recovered by an internal regulator during the off-time
16	GND	Signal GND
-	E.P.	Exposed pad must be connected to signal GND.

2.3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
V_{IN}		-0.3	61	V
V_{CC}		-0.3	61	V
BOOT	V_{BOOT} - GND	-0.3	65	V
	V_{BOOT} - V_{LX}	-0.3	4	V
V_{BIAS}		-0.3	V_{CC}	V
EN		-0.3	V_{CC}	V
PGOOD		-0.3	VCC	V
LX		-0.3	V_{IN} + 0.3	V
SYNCH		-0.3	5.5	V
SS		-0.3	3.6	V
FSW		-0.3	3.6	V
COMP		-0.3	3.6	V
I_{LIM}		-0.3	3.6	V
FB		-0.3	3.6	V
T_J	Operating temperature range	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C
T_{LEAD}	Lead temperature (soldering 10 sec.)		260	°C
I_{HS}	High-side RMS current		3	A

2.4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient (device soldered on the STMicroelectronics® demonstration board)	40	°C/W

2.5 ESD protection

Table 4. ESD protection

Symbol	Test condition	Value	Unit
ESD	HBM	2	KV
	CDM	500	V

3 Electrical characteristics

All the population tested at T_J = 25 °C, V_{IN} = V_{CC} = 24 V and V_{EN} =3 V unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		(1)	4.5		61	V
$R_{DSON\ HS}$	High side RDSON	I_{SW} = 0.5 A			0.2	0.32	Ω
		I_{SW} = 0.5 A	(1)		0.2	0.42	Ω
f_{SW}	Switching frequency	FSW floating		233	250	267	kHz
		FSW floating	(1)	225	250	275	kHz
	Selected switching frequency	R_{SW} = 10 k Ω		1350	1500	1650	kHz
I_{PK}	Peak current limit	ILIM floating; V_{FB} = 0.6 V	(2)	3.4	4.0	4.6	A
	Selected peak current limit	R_{ILIM} = 100 kΩ V_{FB} = 0.6 V	(2)	0.68	0.85	1.01	A
I_{SKIP}	Pulse skipping peak current		(2)		0.5		A
V_{FOLD}	Feedback foldback level		(3)		400		mV
T_{ONMAX}	Maximum on time				12		µs
T_{ONMIN}	Minimum on time				120	150	ns
T_{OFFMIN}	Minimum off time		(3)		360		ns
VCC / VBIAS							
V_{CCH}	V_{CC} UVLO rising threshold		(1)	3.85	4.10	4.30	V
V_{CCHYST}	V_{CC} UVLO hysteresis		(1)	160	250	340	mV
SWO	V_{BIAS} threshold	Switch internal supply from V_{CC} to V_{BIAS}. V_{BIAS} ramping up from 0 V.	(1)	2.84	2.90	2.96	V
		Hysteresis	(3)		80		mV
	V_{CC} - V_{BIAS} threshold	Switch internal supply from V_{CC} to V_{BIAS}. V_{IN} = V_{CC} = 24 V, V_{BIAS} falling from 24 V to GND.	(1)	3.35	4.05	4.90	V
		Hysteresis	(3)		750		mV
Power consumption							
I_{SHTDWN}	Shutdown current from V_{IN}	V_{EN} = GND			11	16	µA
I_{QUIESC}	Quiescent current from V_{IN} and V_{CC}	LX floating, V_{FB} = 1 V, V_{BIAS} = GND, FSW floating			2.5	3.4	mA
I_{QOPVIN}	Quiescent current from V_{IN} and V_{CC}	LX floating, V_{FB} = 1 V, V_{BIAS} = 3.3 V, FSW floating			1.0	1.4	mA
$I_{QOPVBIAS}$	Quiescent current from V_{BIAS}				1.6	2.4	mA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
Enable							
V_{EN}	Device OFF level			0.06		0.30	V
	Device ON level			0.35		0.90	V
Soft start							
$T_{SSSETUP}$	Soft start setup time	Delay from UVLO rising to switching activity	(3)		640		µs
$I_{SS\ CH}$	C_{SS} charging current	V_{SS} = GND		4.3	5.0	5.7	µA
Error amplifier							
V_{FB}	Voltage feedback			0.792	0.800	0.808	V
V_{FB}	Voltage feedback		(1)	0.788	0.800	0.812	V
V_{COMPH}		V_{FB} = GND; V_{SS} = 3.2 V		3.2	3.35	3.5	V
V_{COMPL}		V_{FB} =1 V; V_{SS} = 3.2 V				0.1	V
I_{FB}	FB biasing current	V_{FB} =3.6 V			5	50	nA
$I_{OSOURCE}$		V_{FB} =GND; SS pin floating; V_{COMP} =2 V	(3)		3.1		mA
I_{OSINK}	Output stage sinking capability	Unity gain buffer configuration (FB connected to COMP). COMP voltage variation due to I_{OSINK} injection lower than ± 0.1 · V_{FB}	(3)		5		mA
A_{V0}	Error amplifier gain		(3)		100		dB
GBWP		Unity gain buffer configuration (FB connected to COMP). No load on COMP pin.	(3)		23		MHz
Synchronization (fan out: 5 slave devices max.)							
$f_{SYN\ MIN}$	Synchronization frequency	FSW floating		280			kHz
V_{SYNOUT}	Master output amplitude	I_{LOAD} = 4 mA		2.45			V
		I_{LOAD} = 0 A; pin SYNCH floating				3.8	
V_{SYNOW}	Output pulse width	I_{LOAD} = 0 A; pin SYNCH floating		155	225	275	ns
V_{SYNIH}	SYNCH slave high level input threshold			2.0			V
V_{SYNIL}	SYNCH slave low level input threshold					1.0	V
I_{SYN}	Slave SYNCH pull-down current	V_{SYNCH} = 5 V		550	750	950	µA
V_{SYNIW}	Input pulse width			200			ns
PGOOD							
V_{PGDTH}	PGOOD rising threshold	V_{FB} rising		0.67	0.70	0.73	V
$V_{PGDHYST}$	PGOOD hysteresis	V_{FB} falling	(3)		30		mV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{PGDLOW}	PGOOD low level	IPGD = 1 mA, V_{FB} = GND			30		mV
I_{PGDLKG}	PGOOD leakage current	V_{PGOOD} = 61 V;V_{FB} = 0.8 V				0.1	µA
Thermal shutdown							
T_{SHDWN}	Thermal shutdown temperature		(3)		170		°C
T_{HYS}	Thermal shutdown hysteresis		(3)		15		°C

1. Specifications referred to T_J from -40 to +125 °C. Specifications in the -40 to +125 °C temperature range are assured by design, characterization and statistical correlation.
2. Parameter tested in static condition during testing phase. Parameter value may change over dynamic application condition.
3. Not tested in production.

4 Functional description

The L7987 device is based on a voltage mode, constant frequency control loop. The output voltage VOUT, sensed by the feedback pin (FB), is compared to an internal reference (0.8 V) providing an error signal on the COMP pin. The COMP voltage level is then compared to a fixed frequency sawtooth ramp, which finally controls the on- and off-time of the power switch.

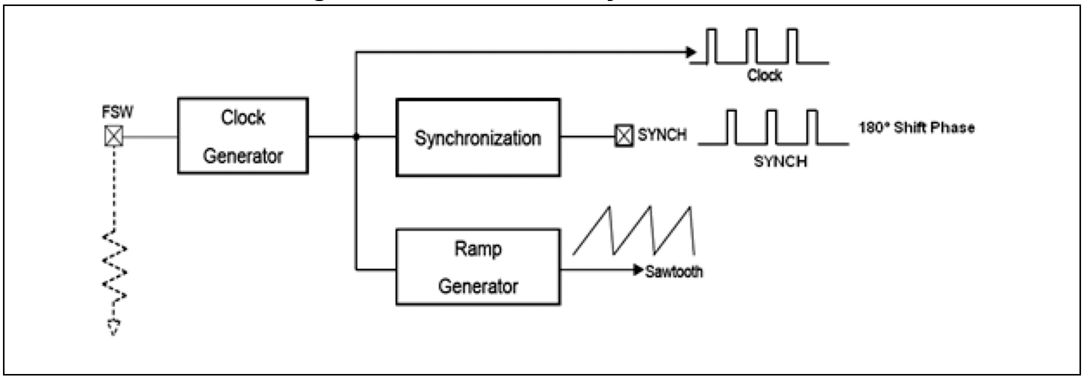
The main internal blocks are shown in the block diagram in *Figure 2 on page 4* and can be summarized as follow.

- The fully integrated oscillator that provides the sawtooth ramp to modulate the duty cycle and the synchronization signal. Its switching frequency can be adjusted by an external resistor. The input voltage feed-forward is implemented.
- The soft-start circuitry to limit inrush current during the start-up phase.
- The voltage mode error amplifier.
- The pulse width modulator and the relative logic circuitry necessary to drive the internal power switch.
- The high-side driver for embedded N-channel Power MOSFET switch and bootstrap circuitry. A dedicated high resistance low-side MOSFET, for anti-boot discharge management purposes, is also present.
- The peak current limit sensing block, with programmable threshold, to handle overload and short-circuit conditions including current foldback and a thermal shutdown block, to prevent thermal runaway.
- The voltage regulator and internal reference, to supply the internal circuitry and provide a fixed internal reference. The switchover function from VCC to VBIAS can be implemented for higher efficiency. This block also implements a voltage monitor circuitry (UVLO) that checks the input and internal voltages.
- The output voltage monitor circuitry which releases the PGOOD signal if the sensed output voltage is above 87% of the target value.

4.1 Oscillator and synchronization

Figure 4 shows the block diagram of the oscillator circuit. The internal oscillator provides a constant frequency clock, whose frequency depends on the resistor externally connected between the FSW pin and ground.

Figure 4. Oscillator and synchronization

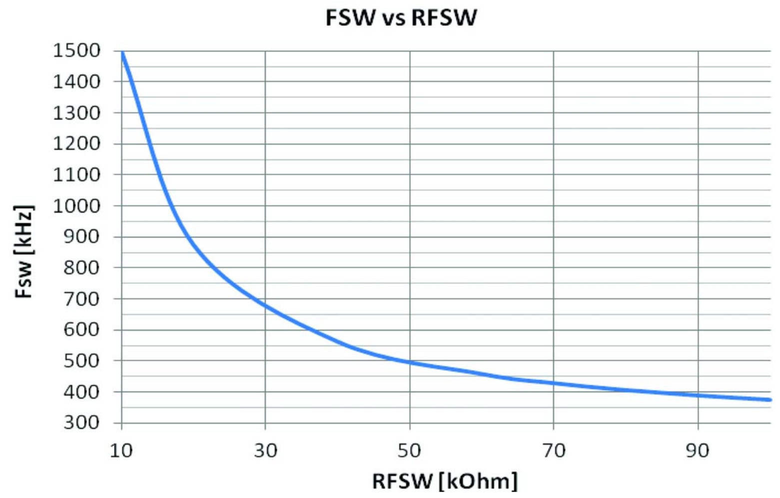


If the FSW pin is left floating, the programmed frequency is 250 kHz (typ.); if FSW pin is connected to an external resistor the programmed switching frequency can be increased up to 1.5 MHz, as shown in *Figure 5*. The required R_{FSW} value (expressed in kΩ) is estimated by *Equation 1*:

Equation 1

$$F_{SW} = 250kHz + \frac{12500}{R_{FSW}}$$

Figure 5. Switching frequency programmability



To improve the line transient performance, keeping the PWM gain constant versus the input voltage, the input voltage feed-forward is implemented by changing the slope of the sawtooth ramp, according to the input voltage change (*Figure 6* a).

The slope of the sawtooth also changes if the oscillator frequency is programmed by the external resistor. In this way a frequency feed-forward is implemented (*Figure 6* b) in order to keep the PWM modulator gain constant versus the switching frequency.

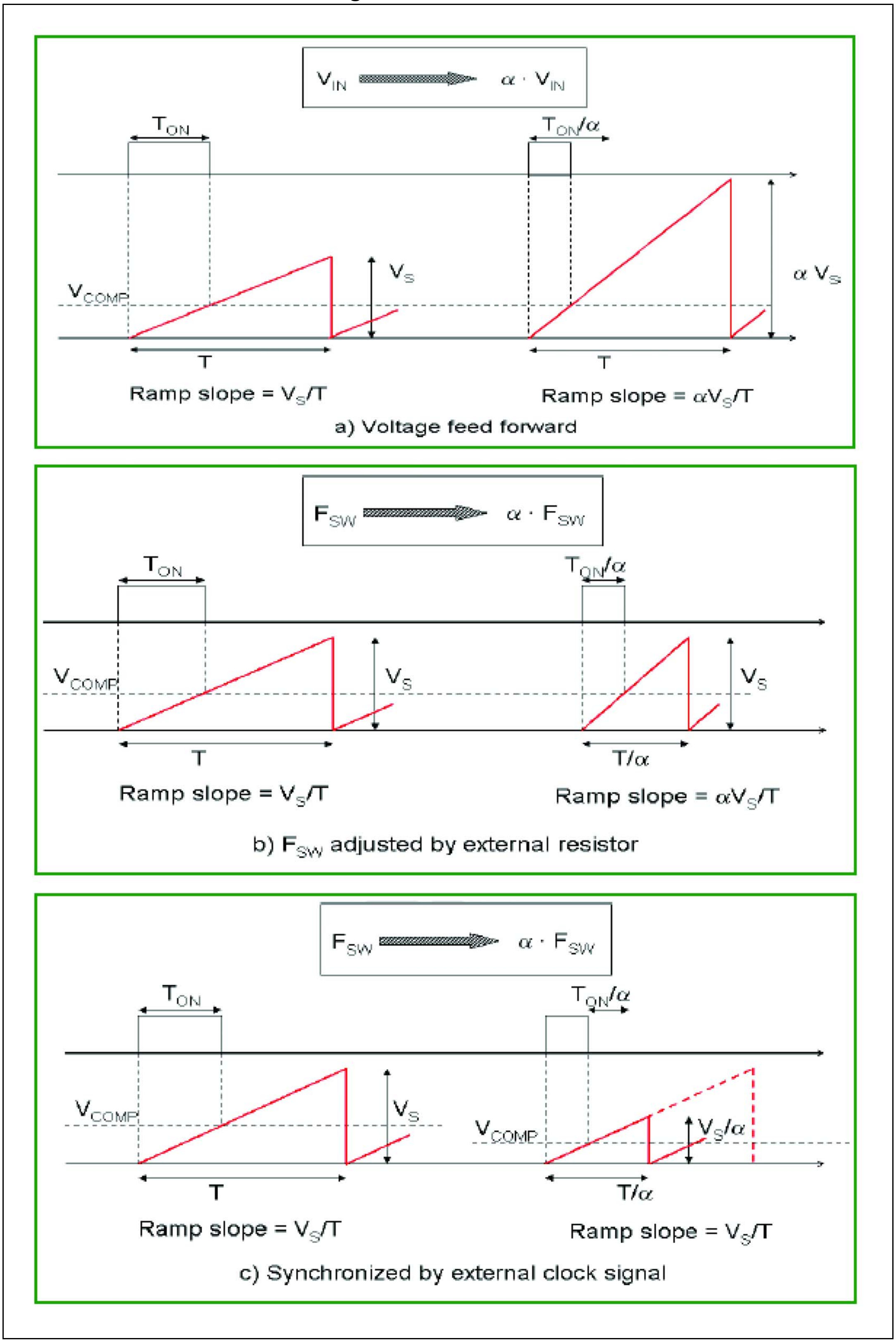
On the SYNCH pin the synchronization signal is generated. This signal has a phase shift of 180° with respect to the clock. This delay is useful when two devices are synchronized connecting the SYNCH pins together. When SYNCH pins are connected, the device with a higher oscillator frequency works as master, so the slave device switches at the frequency of the master but with a delay of half a period. This helps reducing the RMS current flowing through the input capacitor. Up to five L7987s can be connected to the same SYNCH pin; however, the clock phase shift from master switching frequency to slaves input clock is 180°.

The L7987 device can be synchronized to work at a higher frequency, in the range 250 kHz - 1500 kHz, providing an external clock signal on the SYNCH pin. The synchronization changes the sawtooth amplitude, also affecting the PWM gain (*Figure 6* c). This change must be taken into account when the loop stability is studied. In order to minimize the change of PWM gain, the free running frequency should be set (with a resistor on the FSW pin) only slightly lower than the external clock frequency.

This pre-adjusting of the slave IC switching frequency keeps the truncation of the ramp sawtooth negligible.

In case two or more (up to five) L7987 SYNCH pins are tied together, the L7987 IC with higher programmed switching frequency is typically the master device; however, the SYNCH circuit is also able to synchronize with a slightly lower external frequency, so the frequency pre-adjustment with the same resistor on the FSW pin, as suggested above, is required for a proper operation.

Figure 6. Feed-forward

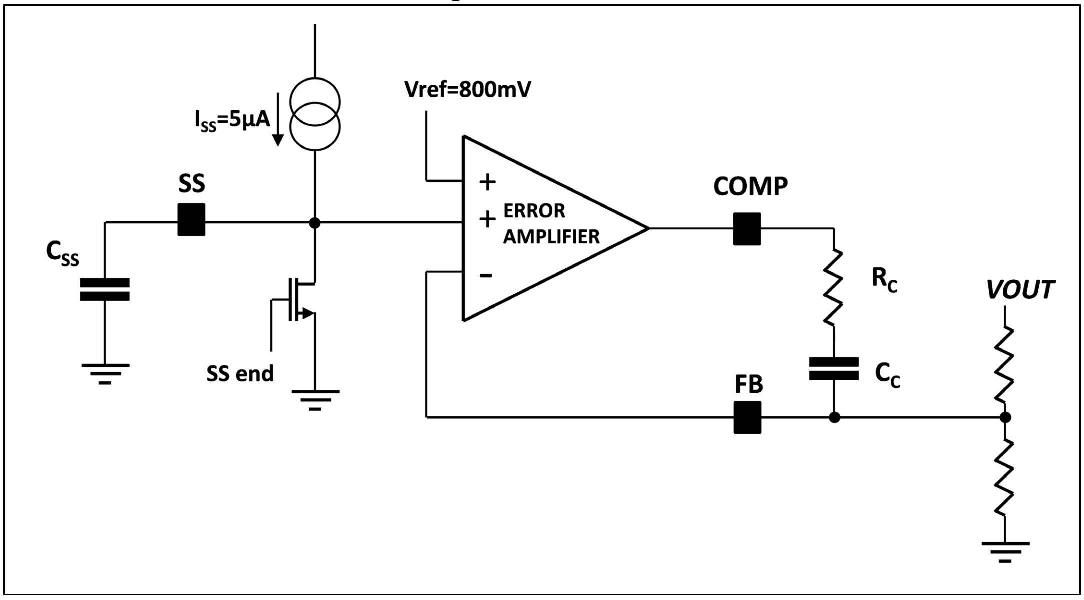


4.2 Soft-start

The soft-start is essential to assure a correct and safe startup of the step-down converter. It avoids inrush current surge and makes the output voltage increase monotonically.

The soft-start is performed by charging an external capacitor, connected between the SS pin and ground, with a constant current (5 µA typ.). The SS voltage is used as reference of the switching regulator and the output voltage of the converter tracks the ramp of the SS voltage. When the SS pin voltage reaches 0.8 V level, the error amplifier switches to the internal 0.8 V ± 1% reference to regulate the output voltage.

Figure 7. Soft-start



During the soft-start period the current limit is set to the nominal value.

The dV_{SS}/dt slope is programmed in agreement with *Equation 2*:

Equation 2

$$C_{SS} = \frac{I_{SS} \bullet T_{SS}}{V_{REF}} = \frac{5\mu A \bullet T_{SS}}{0.8V}$$

Before starting the C_{SS} capacitor charge, the soft-start circuitry turns-on the discharge switch shown in *Figure 7* for $T_{SSDISCH}$ minimum time, in order to completely discharge the C_{SS} capacitor.

As a consequence, the maximum value for the soft-start capacitor, which assures an almost complete discharge in case of EN signal toggle, is provided by:

Equation 3

$$C_{SS-MAX} \le \frac{T_{SSDISCH}}{5 \bullet R_{SSDISCH}} \cong 270nF$$

given $T_{SSDISCH}$ = 530 µs and $R_{SSDISCH}$ = 380 Ω typical values.

The enable feature allows to put the device into standby mode. With the EN pin lower than 0.32 V the device is disabled and the power consumption is reduced to less than 11 µA (typ.). With the EN pin higher than 1.16 V, the device is enabled. If the EN pin is left floating, an internal pull-down current ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also VCC compatible.

4.3 Error amplifier and light-load management

The error amplifier (E/A) provides the error signal to be compared with the sawtooth to perform the pulse width modulation. Its non inverting input is internally connected to a 0.8V voltage reference and its inverting input (FB) and output (COMP) are externally available for feedback and frequency compensation. In this device the error amplifier is a voltage mode operational amplifier, therefore, with high DC gain and low output impedance.

The uncompensated error amplifier characteristics are summarized in *Table 6*.

Table 6. Error amplifier characteristics

Parameters	Value
Low frequency gain (A0)	100 dB
GBWP	23 MHz
Output voltage swing	0 to 3.5 V
Source/sink current capability	2 mA / 5 mA

In continuous conduction working mode (CCM), the transfer function of the power section has two poles due to the LC filter and one zero due to the ESR of the output capacitor. Different kinds of compensation networks can be used depending on the ESR value of the output capacitor.

If the zero introduced by the output capacitor helps to compensate the double pole of the LC filter, a type II compensation network can be used. Otherwise, a type III compensation network must be used (see *Section 5.4 on page 23* for details on the compensation network design).

In case of light load (i.e. if the output current is lower than the half of the inductor current ripple) the L7987 device enters pulse-skipping working mode. The HS MOS is kept off if the COMP level is below 200 mV (typ.); when this bottom level is reached the integrated switch is turned on until the inductor current reaches I_{SKIP} value. So, in discontinuous conduction working mode (DCM), the HS MOS on-time is only related to the time necessary to charge the inductor up to I_{SKIP} level. Due to current sensing comparator delay, the actual inductor charge current is slightly impacted by V_{IN} and inductance level.

In order to let the bootstrap capacitor recharge, in case of extremely light load the L7987 is able to pull-down the LX net through an integrated small LS MOS. In this way the bootstrap recharge current can flow from V_{IN} through C_{BOOT}, LX and the LS MOS.

This mechanism is activated if the HS MOS has been kept turned-off for more than 3 ms (typ.).

4.4 Low VIN operation

In normal operation (i.e. VOUT programmed lower than input voltage) when the HS MOS is turned off, a minimum off time (T_{OFFMIN}) interval is performed.

In case the input voltage falls close or below the programmed output voltage (low dropout, LDO) the L7987 control loop is able to increase the duty cycle up to 100%. However, in order to keep the boot capacitor properly recharged, a maximum HS MOS on time is limited (T_{ONMAX}). When this limit is reached the HS MOS is turned-off and a pull-down resistor between LX and GND is turned on until one of the following conditions is met:

- A negative current limit (300 mA typ.) is reached
- A timeout (1 µs typ.) is reached.

So doing the L7987 device is able to work in low dropout operation, due to the advanced boot capacitor management, and the effective maximum duty cycle is about 12 µs / 13 µs = 92%.

4.5 Overcurrent protection

The L7987 device implements an overcurrent protection by sensing the current flowing through the Power MOSFET. Due to the noise created by the switching activity of the Power MOSFET, the current sensing circuitry is disabled during the initial phase of the conduction time. This avoids an erroneous detection of a fault condition. This interval is generally known as “masking time” or “blanking time”. The masking time is about 120 ns.

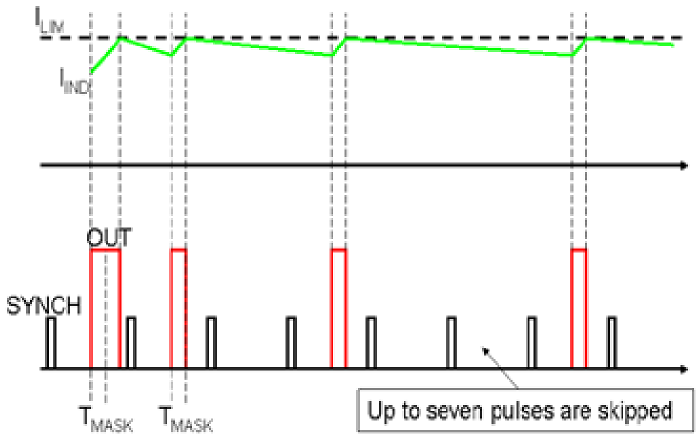
If the overcurrent limit is reached, the Power MOSFET is turned off implementing pulse-by-pulse overcurrent protection. In the overcurrent condition, the device can skip turn-on pulses in order to keep the inductor current constant and equal to the current limit, assuming only a slight drift due to input and output voltage variation.

If, at the end of the “masking time”, the current is higher than the overcurrent threshold, the Power MOSFET is turned off and one pulse is skipped. If, at the following switching on, when the “masking time” ends, the current is still higher than the overcurrent threshold, the device skips two pulses. This mechanism is repeated and the device can skip up to seven pulses (refer to *Figure 8*).

If at the end of the “masking time” the current is lower than the overcurrent threshold, the number of skipped cycles is decreased by one unit.

As a consequence, the overcurrent/short-circuit protection acts by switching off the Power MOSFET and reducing the switching frequency down to one eighth of the default switching frequency, in order to keep constant the output current close to the current limit.

Figure 8. OCP and frequency scaling



If the sensed output voltage, monitored through FB pin, falls below the V_{FOLD} threshold (400 mV typ.) the peak current limit threshold is reduced to 1/3 of the nominal value. This additional feature helps to reduce the IC stress in case of output short-circuit.
As soon as the FB pin increases above the V_{FOLD} threshold, the full peak current limit threshold is restored. This fold back protection is disabled during the soft-start.

This kind of overcurrent protection is effective if the inductor can be completely discharged during HS MOS turn-off time, in order to avoid the inductor current to run away. In case of output short-circuit the maximum switching frequency can be computed by *Equation 4*.

Equation 4

$$F_{SW,\,MAX} \le \frac{8 \bullet (V_F + R_{DCR} \bullet I_{LIM})}{V_{IN} - (R_{ON} + R_{DCR}) \bullet I_{LIM}} \bullet \frac{1}{T_{ON,\,MIN}}$$

Assuming V_F = 0.6 V the freewheeling diode direct voltage, R_{DCR} = 30 mΩ the inductor parasitic resistance, $I_{LIM} = I_{PK}$ = 1.47 A the peak current limit during foldback protection, R_{ON} = 0.25 Ω the HS MOS resistance and $T_{ON,MIN}$ = 120 ns the minimum HS MOS on duration, the maximum FSW frequency which avoids the inductor current run away in case of output short-circuit and V_{IN} = 61 V is 708 kHz.

If the programmed switching frequency is higher than the above computed limit, an estimation of the inductor current in case of output short-circuit fault is provided by *Equation 5*:

Equation 5

$$I_{LIM} = \frac{F_{SW} \bullet T_{ON} \bullet V_{IN} - 8 \bullet V_F}{8 \bullet R_{DCR} + F_{SW} \bullet T_{ON,\,MIN} \bullet (R_{ON} + R_{DCR})}$$

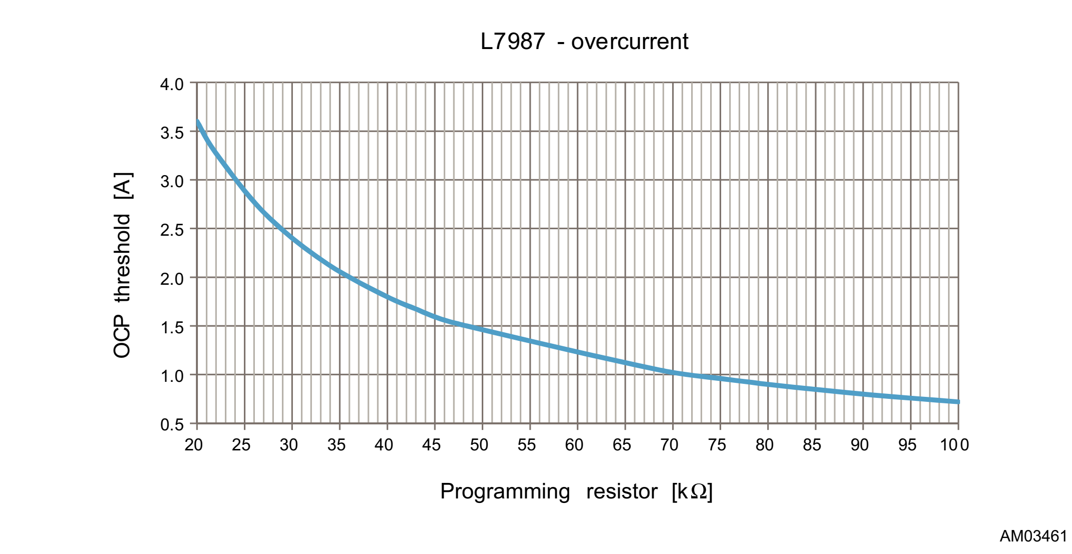
The peak current limit threshold (I_{LIM}) can be programmed in the range 0.85 A - 3.6 A by selecting the proper R_{ILIM} resistor, as suggested in *Equation 6*:

Equation 6

$$R_{ILIM} = 20k\Omega \bullet \frac{I_{PK}}{I_{LIM}}$$

I_{PK} is the default L7987 current limit in case of R_{ILIM} not mounted, as shown in *Table 5 on page 8*.

Figure 9. Current limit and programming resistor



The minimum programmed current limit can't be lower than I_{SKIP} = 0.5 A (typical), also in case of foldback detection.

4.6 Overtemperature protection

It is recommended that the device never exceeds the maximum allowable junction temperature. This temperature increase is mainly caused by the total power dissipated from the integrated Power MOSFET.

To avoid any damage to the device when reaching high temperature, the L7987 device implements a thermal shutdown feature: when the junction temperature reaches 170 °C (typ.) the device turns off the Power MOSFET and shuts down.

When the junction temperature drops to 155 °C (typ.), the device restarts with a new soft-start sequence.

5 Application information

5.1 Input capacitor selection

The input capacitor must be rated for the maximum input operating voltage and the maximum RMS input current.

Since the step-down converters input current is a sequence of pulses from 0 A to I_{OUT}, the input capacitor must absorb the equivalent RMS current which can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors must be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency.

The RMS input current (flowing through the input capacitor) is roughly estimated by:

Equation 7

$$I_{CIN,RMS} \cong I_{OUT} \bullet \sqrt{D \bullet (1 - D)}$$

Actual DC/DC conversion duty cycle, D = V_{OUT}/V_{IN}, is influenced by a few parameters:

Equation 8

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{IN,MIN} - V_{SW,MAX}}$$

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{IN,MAX} - V_{SW,MIN}}$$

where V_F is the freewheeling diode forward voltage and V_{SW} the voltage drop across the internal high-side MOSFET. Considering the range D_{MIN} to D_{MAX} it is possible to determine the maximum $I_{CIN,RMS}$ flowing through the input capacitor.

The input capacitor value must be dimensioned to safely handle the input RMS current and to limit the VIN and VCC ramp-up slew-rate to 0.5 V/µs maximum, in order to avoid the device active ESD protections turn-on.

Different capacitors can be considered:

- **Electrolytic capacitors**
  These are the most commonly used due to their low cost and wide range of operative voltage. The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.
- **Ceramic capacitors**
  If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to the very low ESR). The drawback is their high cost.
- **Tantalum capacitors**
  Small, good quality tantalum capacitors with very low ESR are becoming more available. However, they can occasionally burn if subjected to very high current, for example when they are connected to the power supply.

The amount of the input voltage ripple can be roughly overestimated by *Equation 9*.

Equation 9

$$V_{IN,PP} = \frac{D \bullet (1-D) \bullet I_{OUT}}{C_{IN} \bullet F_{SW}} + R_{ES,IN} \bullet I_{OUT}$$

In case of MLCC ceramic input capacitors, the equivalent series resistance ($R_{ES,IN}$) is negligible.

In addition to the above considerations, a ceramic capacitor with an appropriate voltage rating and with a value 1 µF or higher should always be placed across VIN and power ground and across VCC and the IC GND pins, as close as possible to the L7987device. This solution is necessary for spike filtering purposes.

5.2 Output capacitor selection

The output capacitor is very important in order to satisfy the output voltage ripple requirement. Using a small inductor value is useful to reduce the size of the choke but increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required. Nevertheless, the ESR of the output capacitor introduces a zero in the open loop gain, which helps to increase the phase margin of the system. If the zero goes to very high frequency, typical drawback in case of ceramic output capacitor application, a type III compensation network must be designed.

The current in the output capacitor has a triangular waveform which generates a voltage ripple across it. This ripple is due to the capacitive component (charge and discharge of the output capacitor) and the resistive component (due to the voltage drop across its ESR). So the output capacitor must be selected in order to have a voltage ripple compliant with the application requirements.

The amount of the voltage ripple can be estimated starting from the current ripple obtained by the inductor selection. Assuming ΔI_L the inductor current ripple, the output voltage ripple is roughly overestimated by *Equation 10*.

Equation 10

$$\Delta V_{OUT,PP} \cong \Delta I_L \bullet R_{ES,OUT} + \frac{\Delta I_L}{8 \bullet F_{SW} \bullet C_{OUT}}$$

Usually the resistive component of the ripple is much higher than the capacitive one, if the output capacitor adopted is not a multi-layer ceramic capacitor (MLCC) with very low ESR value.

The output capacitor is important also for loop stability: it fixes the double LC filter pole and the zero due to its ESR.

The output capacitor is also the key component that provides the current to the load during a load transient which exceeds the system bandwidth. So, if the high slew rate load transient is required by the application, the output capacitor must be designed in order to sustain the load transient or absorbs the energy stored in the inductor until the converter reacts.

In fact, even if the controller detects immediately the load variation and sets the duty cycle at 100% or 0%, the output current slope is limited by the inductor value, the input and output voltage.

The output voltage has a drop or overshoot that depends on the ESR and capacitive charge/discharge, as roughly estimated in *Equation 11*:

Equation 11

$$\Delta V_{OUT-LT} \cong \Delta I_{OUT} \bullet R_{ES,\,OUT} + \Delta I_{OUT} \bullet \frac{L \bullet \Delta I_{OUT}}{2 \bullet C_{OUT} \bullet \Delta V_L}$$

where ΔV_L is the voltage applied to the inductor during the load appliance or load release.

Equation 12

$$\Delta V_L = \begin{cases} D_{MAX} \bullet (V_{IN} - V_{OUT}) \\ V_{OUT} \end{cases}$$

MLCC capacitors have typically low ESR to minimize the ripple but also have low capacitance that does not minimize the voltage deviation during dynamic load variations. Electrolytic capacitors, on the other hand, have a large capacitance which minimizes voltage deviation during load transients whereas they do not show the same ESR values as the MLCCs, resulting then in higher ripple voltages.
A mix between an electrolytic and MLCC capacitor can be used to minimize ripple as well as reducing voltage deviation in dynamic mode.
The high bandwidth error amplifier of the L7987 and external compensation feature let design a wide range of output filter configurations (including all MLCC solutions) and perform fast transient response.

5.3 Inductor selection

The inductance value fixes the current ripple flowing through the output capacitor. So the minimum inductance value, in order to have the expected current ripple, must be selected. The rule to fix the current ripple value is to have a ripple at 20% - 40% of the output current. In the continuous conduction mode (CCM), the required inductance value can be calculated by *Equation 13*:

Equation 13

$$L = \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\Delta I_L \bullet F_{SW}}$$

In order to guarantee a maximum current ripple in every condition, *Equation 13* must be evaluated in case of maximum input voltage, assuming V_{OUT} fixed.

Increasing the value of the inductance help to reduce the current ripple but, at the same time, strongly impacts the converter response time to a dynamic load change. The response time is the time required by the inductor to change its current from the initial to the final value. Until the inductor has finished its charging (or discharging) time, the output current is supplied (or recovered) by the output capacitors.

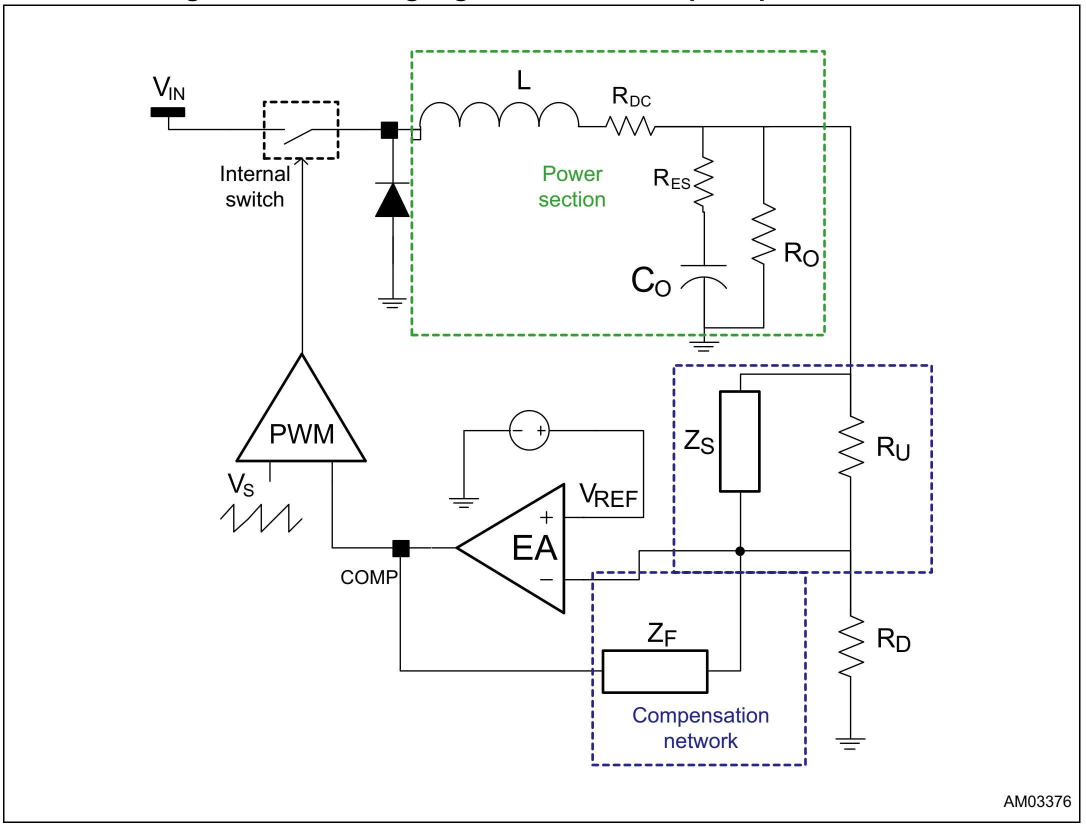
Further, if the compensation network is properly designed, during a load variation the device is able to properly change the duty cycle so improving the control loop transient response. When this condition is reached the response time is only limited by the time required to change the inductor current, basically by V_{IN}, V_{OUT} and L.

Minimizing the response time, at the end, can help to decrease the output filter total cost and to reduce the application area.

5.4 Compensation network

The compensation network must assure stability and good dynamic performance. The loop of the L7987 device is based on the voltage mode control. The error amplifier is an operational amplifier with high bandwidth. So, by selecting the compensation network the E/A is considered as ideal, that is, its bandwidth is much larger than the system one.

Figure 10. Switching regulator control loop simplified model



The transfer function of the PWM modulator, from the error amplifier output (COMP pin) to the LX pin results in an almost constant gain, due to the voltage feed-forward which generates a sawtooth with amplitude V_S directly proportional to the input voltage:

Equation 14

$$G_{PWO} = \frac{V_{IN}}{V_S} = \frac{1}{k_{FF}} = 30$$

The synchronization of the device with an external clock provided through the SYNCH pin can modify the PWM modulator gain (see *Section 4.1 on page 11* to understand how this gain changes and how to keep it constant in spite of the external synchronization).

The transfer function of the power section (i.e. the L-C_O filters and the output load) is the ratio of the parallel of C_O and R_O and the sum of L and the parallel of C_O and R_O, including L and C_O parasitics:

Equation 15

$$G_{LC}(s) = \frac{R_O \oplus \left(R_{ES} + \frac{1}{sC_O}\right)}{R_O \oplus \left(R_{ES} + \frac{1}{sC_O}\right) + sL + R_{DC}} =$$

$$= \frac{R_O \cdot (1 + sC_O R_{ES})}{s^2 LC_O \cdot (R_O + R_{ES}) + s \cdot (L + C_O R_O R_{DC} + C_O R_{ES} R_{DC} + C_O R_{ES} R_O) + R_{DC} + R_O}$$

given L, R_{DC}, C_O, R_{ES} and R_O the parameters shown in *Figure 10*. The power section transfer function can be rewritten as follows:

Equation 16

$$G_{LC}(s) = G_{LCO} \bullet \frac{1 + \frac{s}{2\pi \bullet f_{zESR}}}{1 + \frac{s}{2\pi \bullet Q \bullet f_{LC}} + \left(\frac{s}{2\pi \bullet f_{LC}}\right)^2};$$

$$G_{LCO} = \frac{R_O}{R_O + R_{DC}} \cong 1$$

Equation 17

$$f_{zESR} = \frac{1}{2\pi \bullet C_O R_{ES}};$$

$$f_{LC} = \frac{1}{2\pi\sqrt{LC_O}\sqrt{\frac{R_O + R_{ES}}{R_O + R_{DC}}}} \cong \frac{1}{2\pi\sqrt{LC_O}\sqrt{\frac{R_O + R_{ES}}{R_O}}}$$

Equation 18

$$Q = \frac{\sqrt{LC_O} \bullet \sqrt{R_O + R_{DC}} \bullet \sqrt{R_O + R_{ES}}}{L + C_O \bullet (R_O R_{DC} + R_O R_{ES} + R_{ES} R_{DC})} \cong \frac{\sqrt{LC_O} \bullet \sqrt{R_O} \bullet (R_O + R_{ES})}{L + C_O R_O R_{ES}}$$

with the assumption that the inductor parasitic resistance, R_{DC}, is negligible compared to R_O. The closed loop gain is then given by:

Equation 19

$$G_{LOOP}(s) = G_{LC}(s) \bullet G_{PWO}(s) \bullet G_{COMP}(s)$$

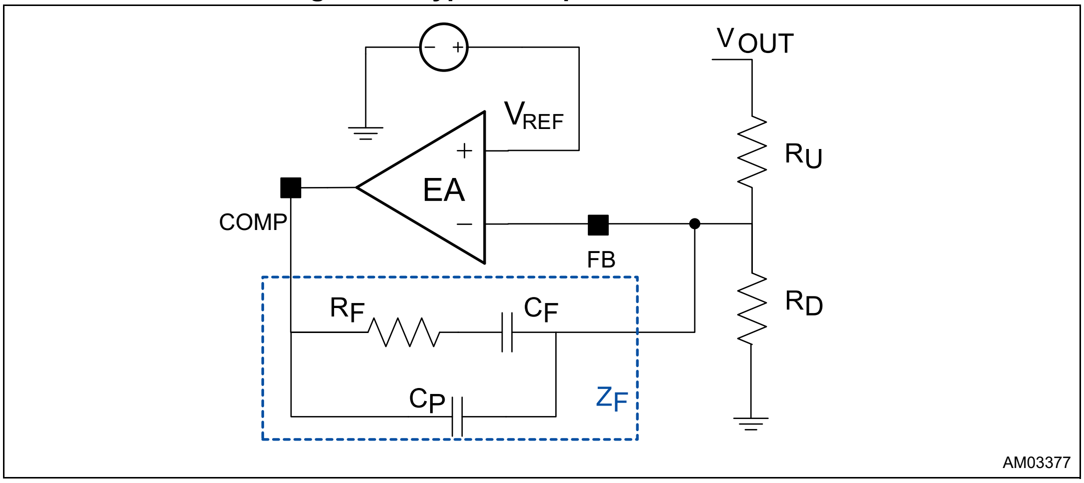
As noted in *Section 5.2 on page 21*, two different kinds of network can compensate the loop, depending on the value of f_{zESR}, lower or higher than the regulator required bandwidth.

In *Section 5.4.1* and *Section 5.4.2* the guidelines to select the type II and type III compensation network are illustrated.

5.4.1 Type II compensation network

If the equivalent series resistance (R_{ES}) of the output capacitor introduces a zero with a frequency lower than the desired bandwidth (that is: $2\pi \bullet R_{ES} \bullet C_O > 1/BW$), this zero helps stabilize the loop. Electrolytic capacitors show non-negligible ESR (> 30 mΩ typically), so with this kind of output capacitor the type II network combined with the zero of the ESR allows to stabilize the loop.

Figure 11. Type II compensation network



The type II compensation network transfer function, from V_{OUT} to COMP, is computed in *Equation 20*.

Equation 20

$$G_{COMPII}(s) = -\frac{Z_F(s)}{R_U} = -\frac{1}{R_U} \cdot \frac{1 + sC_F R_F}{s \cdot (C_F + C_P) \cdot (1 + sC_F \oplus C_P R_F)} = -\frac{1 + \frac{s}{2\pi \cdot f_{Z1}}}{\frac{s}{2\pi \cdot f_{P0}} \cdot \left(1 + \frac{s}{2\pi \cdot f_{P1}}\right)}$$

Equation 21

$$f_{Z1} = \frac{1}{2\pi \cdot C_F \cdot R_F}; \quad f_{P0} = \frac{1}{2\pi \cdot (C_F + C_P) \cdot R_U}; \quad f_{P1} = \frac{1}{2\pi \cdot C_F \oplus C_P \cdot R_F}$$

The following suggestions can be followed for a quite common compensation strategy, assuming that $C_P << C_F$.

- Starting from *Equation 19*, in case of type II compensation network and electrolytic output capacitors the control loop gain module at $s = 2\pi \bullet F_{BW}$ allows to fix the R_F/R_U ratio:

Equation 22

$$\left|G_{LOOP,II}(s = 2\pi \cdot f_{BW})\right| \cong \frac{1}{k_{FF}} \cdot \frac{(f_{LC})^2}{f_{zESR}} \cdot \frac{R_F}{R_U} \cdot \frac{1}{f_{BW}} = 1$$

After choosing the regulator bandwidth (typically $F_{BW} < 0.2 \bullet F_{SW}$) and a value for R_U, usually between 1 kΩ and 50 kΩ, in order to achieve C_F and C_P not comparable with parasitic capacitance of the board, the R_F required value is computed by *Equation 22*.

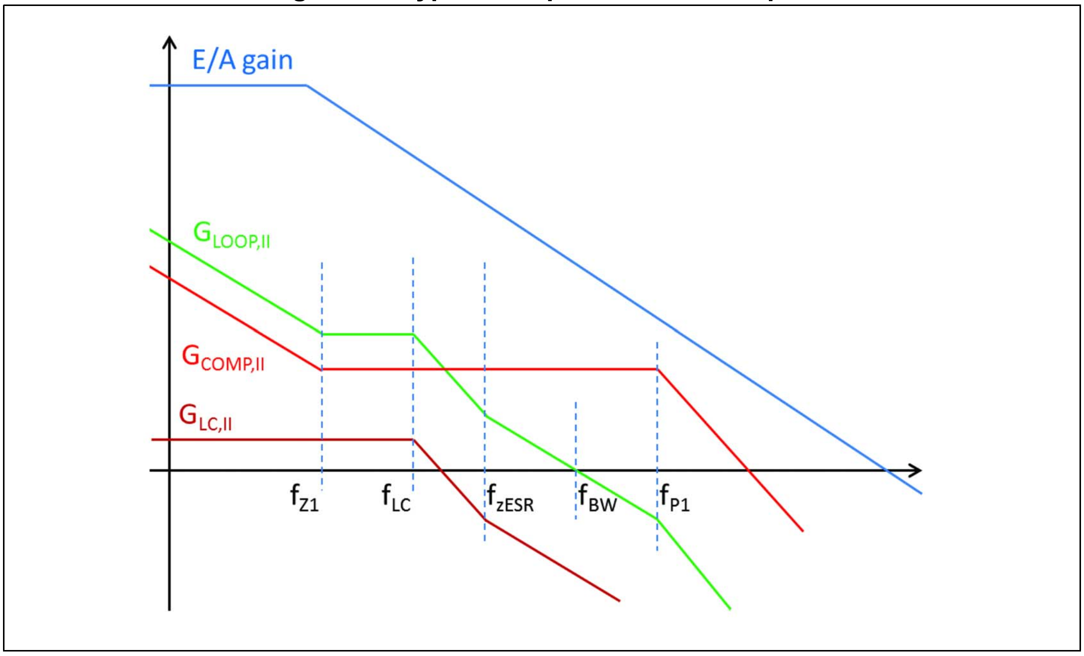
- Select C_F in order to place F_{Z1} below F_{LC} (typically $0.1 \bullet F_{LC}$)
- Select C_P in order to place F_{P1} at $0.5 \bullet F_{SW}$

Equation 23

$$C_F = \frac{1}{2\pi \bullet R_F \bullet 0.1 \bullet f_{LC}} ; C_P = \frac{1}{2\pi \bullet R_F \bullet 0.5 \bullet f_{SW}}$$

The resultant control loop and other transfer functions gain are shown in *Figure 12*.

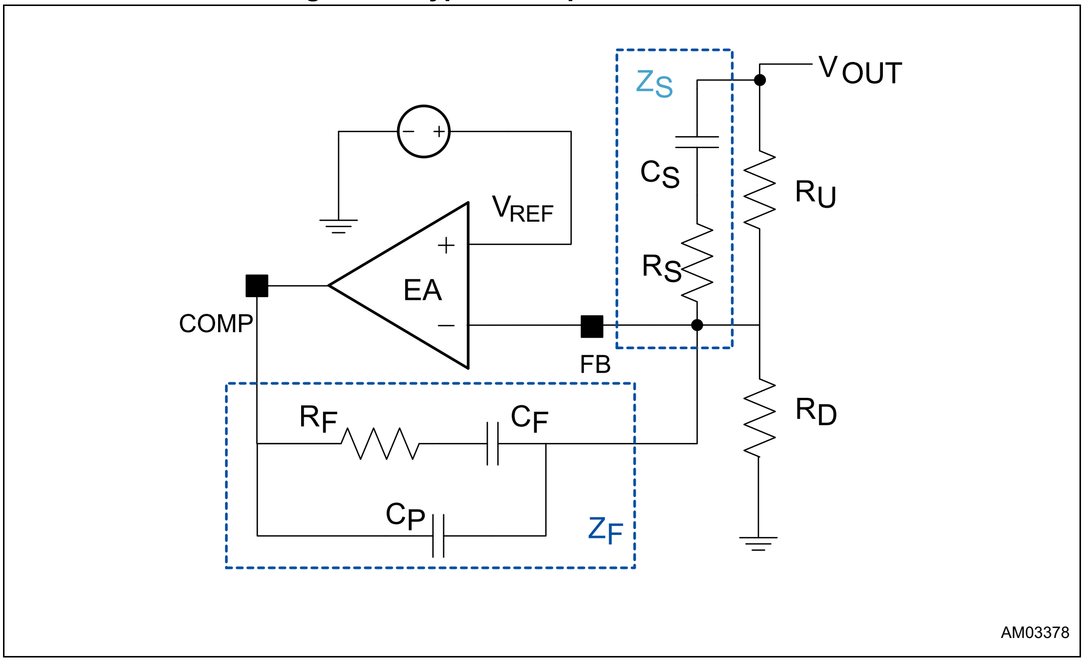
Figure 12. Type II compensation - bode plot



5.4.2 Type III compensation network

If F_{zESR} is higher than the target loop bandwidth, as usually happens if the output filter is based on MLCC ceramic capacitors, a type III compensation network must be designed.

Figure 13. Type III compensation network



The type III compensation network transfer function, from VOUT to COMP, is computed in *Equation 24*.

Equation 24

$$G_{COMPIII}(s) = -\frac{Z_F(s)}{R_U // Z_S(s)} = -1 \cdot \frac{\left(1+\frac{s}{2\pi \cdot f_{Z1}}\right) \cdot \left(1+\frac{s}{2\pi \cdot f_{Z2}}\right)}{\frac{s}{2\pi \cdot f_{P0}} \cdot \left(1+\frac{s}{2\pi \cdot f_{P1}}\right) \cdot \left(1+\frac{s}{2\pi \cdot f_{P2}}\right)}$$

In addition to what shown in *Equation 21*, two more singularities are proper of this compensation network:

Equation 25

$$f_{Z2} = \frac{1}{2\pi \bullet C_s \bullet \ (R_U + R_S)};$$

$$f_{P2} = \frac{1}{2\pi \bullet C_S R_S}$$

The following suggestions can be followed for a quite common compensation strategy, assuming that $C_P << C_F$ and $R_S << R_U$.

- Starting from *Equation 19 on page 24*, in case of type III compensation network and MLCC ceramic output capacitors the control loop gain module at s = 2 π • F_{BW} allows to fix the R_F/R_U ratio:

Equation 26

$$\left|G_{LOOP,III}(s = 2\pi \cdot f_{BW})\right| \cong \frac{1}{k_{FF}} \cdot \frac{f_{LC}}{f_{BW}} \cdot \frac{R_F}{R_U} = 1$$

After choosing the regulator bandwidth (typically $F_{BW} < 0.2 \cdot F_{SW}$) and a value for R_U, usually between 1 kΩ and 50 kΩ, in order to achieve C_F and C_P not comparable with parasitic capacitance of the board, the R_F required value is computed by *Equation 26*.

- Select C_F in order to place F_{Z1} below F_{LC} (typically 0.1 • F_{LC})
- Select C_P in order to place F_{P1} at 0.5 • F_{SW}

Equation 27

$$C_F = \frac{1}{2\pi \bullet R_F \bullet 0.1 \bullet f_{LC}};$$

$$C_P = \frac{1}{2\pi \bullet R_F \bullet 0.5 \bullet f_{SW}}$$

- Select C_S in order to place F_{Z2} at F_{LC}
- Select R_S in order to place F_{P2} at 0.5 • F_{SW}

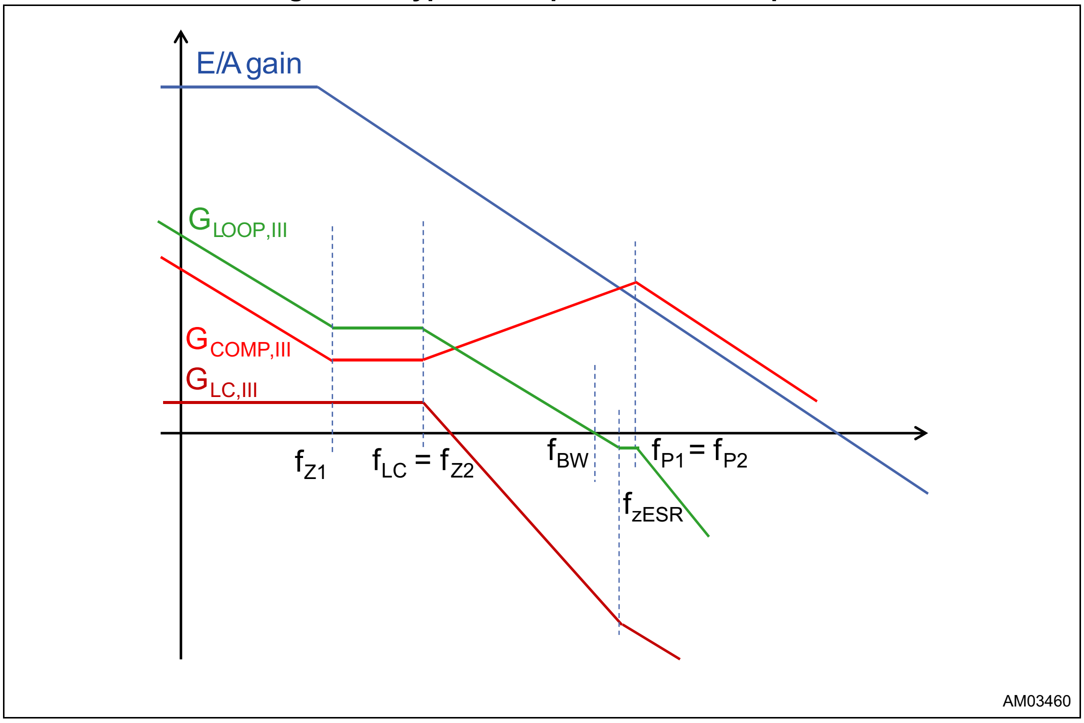
Equation 28

$$C_S = \frac{1}{2\pi \bullet R_U \bullet f_{LC}};$$

$$R_S = \frac{1}{2\pi \bullet C_S \bullet 0.5 \bullet f_{SW}}$$

The resultant control loop and other transfer functions gain are shown in *Figure 14*.

Figure 14. Type III compensation - bode plot



5.5 Thermal considerations

The thermal design is important to prevent the thermal shutdown of the device if junction temperature goes above 170 °C (typ.). The three different sources of losses within the device are:

- Conduction losses due to the non-negligible RDSON of the power switch; these are equal to:

Equation 29

$$P_{HS,ON} = R_{HS,ON} \bullet D \bullet (I_{OUT})^2$$

where *D* is the duty cycle of the application and the maximum RDSON in the full temperature range is 380 mΩ. Note that the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but actually it is quite higher in order to compensate the losses of the regulator. So the conduction losses increase compared with the ideal case;

- Switching losses due to Power MOSFET turn ON and OFF; these can be calculated as:

Equation 30

$$P_{HS,SW} = V_{IN} \bullet I_{OUT} \bullet \frac{(T_{RISE} + T_{FALL})}{2} \bullet f_{SW} \cong V_{IN} \bullet I_{OUT} \bullet T_{TR} \bullet f_{SW}$$

where T_{RISE} and T_{FALL} are the overlap times of the voltage across the power switch (V_{DS}) and the current flowing into it during turn ON and turn OFF phases.

T_{TR} is the equivalent switching time. For this device the typical value for the equivalent switching time is 20 ns.

- Quiescent current losses, calculated as

Equation 31

$$P_Q = V_{IN} \bullet I_{QOPVIN} + V_{BIAS} \bullet I_{QOPVBIAS}$$

where I_{QOPVIN} and $I_{QOPVBIAS}$ are the L7987 quiescent current in case of separate bias supply. If the switchover feature is not used, the IC quiescent current is the only one from VIN, I_{QUIESC}, as summarized in *Table 5 on page 8*.

The junction temperature T_J can be calculated as:

Equation 32

$$T_J = T_A + R_{th,JA} \bullet P_{TOT}$$

where T_A is the ambient temperature and P_{TOT} is the sum of the power losses just seen. R_{thJA} is the equivalent thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junction to the ambient. For this device the path through the exposed pad is the one conducting the largest amount of heat. The R_{thJA}, measured on the demonstration board described in *Section 5.6*, is about 40 °C/W for the HTSSOP16 package.

5.6 Layout considerations

The PCB layout of the switching DC/DC regulators is very important to minimize the noise injected in high impedance nodes and interference generated by the high switching current loops. Two separated ground areas must be considered: the signal ground and the power ground.

In a step-down converter the input loop (including the input capacitor, the Power MOSFET and the freewheeling diode) is the most critical one. This is due to the fact that high value pulsed currents are flowing through it. In order to minimize the EMI, this loop must be as short as possible. The input loop, including also the output capacitor, must be referred to the power ground. All the other components are referred to the signal ground.

The feedback pin (FB) connection to the external resistor divider is a high impedance node, so the interference can be minimized by placing the routing of the feedback node as far as possible from the high current paths. To reduce the pick-up noise, the resistor divider must be placed very close to the device.

To filter the high frequency noise, a small bypass capacitor (1 µF or higher) must be added as close as possible to the input voltage pin of the device for both VIN and VCC pins.

Thanks to the exposed pad of the device, the ground plane helps to reduce the junction to ambient thermal resistance; so a wide ground plane enhances the thermal performance of the converter, allowing high power conversion.

The exposed pad must be connected to the signal GND pin. The connection to the ground plane must be achieved by taking care of the above mentioned input loop, in order to avoid high current flowing through the signal GND. Refer to *Section 6* for the L7987 layout example.

6 Demonstration board

In this section the L7987 demonstration board is described. The default settings are:

- Programmed V_{OUT} = 3.3 V
- Max. I_{OUT} = 3 A
- F_{SW} = 500 kHz
- V_{BIAS} = V_{OUT}
- Soft-start 3.5 ms

Figure 15. L7987 demonstration board schematic

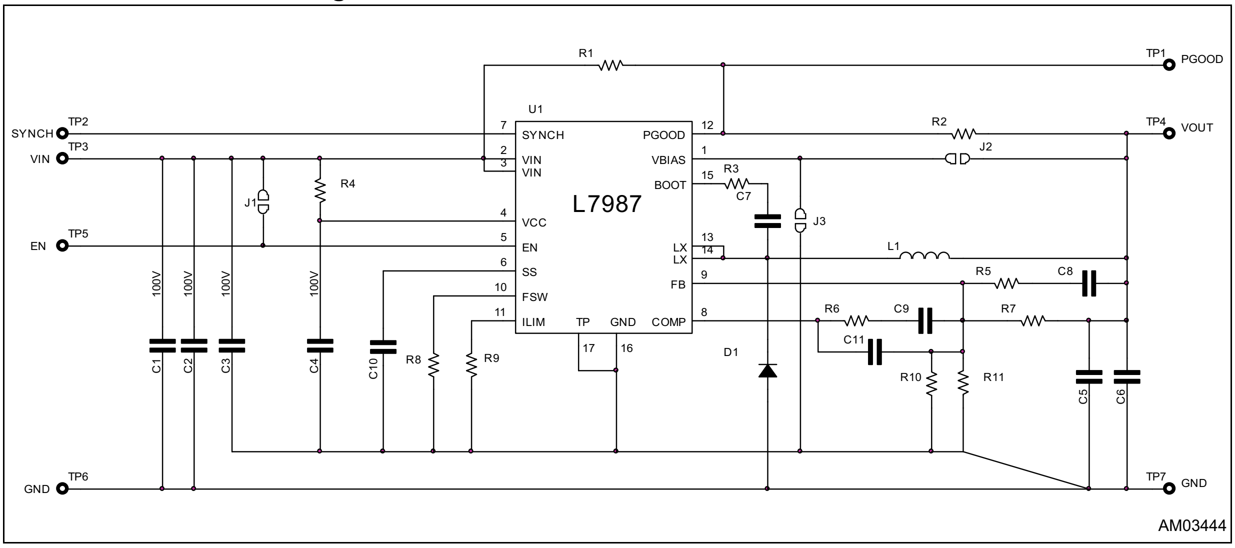


Table 7. L7987 demonstration board component list

Reference	Part	Package	Note	Manufacturer P/N
C1, C2	4.7 µF	1210	X7S/100 V/10%	TDK C3225X7S2A475K
C3, C4	1 µF	0805	X7S/100 V/10%	TDK C2012X7S2A105K
C5	47 µF	1206	X5R/16 V/20%	TDK C3216X5R1C476M
C6	N. M.			
C7	100 nF	0603	10 V	
C8	10 nF	0603	10 V	
C9	33 nF	0603	10 V	
C10	22 nF	0603	10 V	
C11	1 nF	0603	10 V	
R1, R9, R10	N. M.			
R2	100 kΩ	0603		
R3, R4	0 Ω	0603		
R5	68 Ω	0603	1% tolerance	

Table 7. L7987 demonstration board component list (continued)

Reference	Part	Package	Note	Manufacturer P/N
R6	620 Ω	0603	1% tolerance	
R7	6.8 kΩ	0603	1% tolerance	
R8	47 kΩ	0603	1% tolerance	
R11	2.2 kΩ	0603	1% tolerance	
L1	10 µH	5 x 5	4.9 A sat./ 41 mΩ	Coilcraft XAL5050-103
D1	STPS3L60	SMB flat	60 V - 3 A Schottky rectifier	STMicroelectronics STPS3L60
U1	L7987	HTSSOP16		STMicroelectronics L7987

Figure 16. L7987 demonstration board layout (top and bottom)

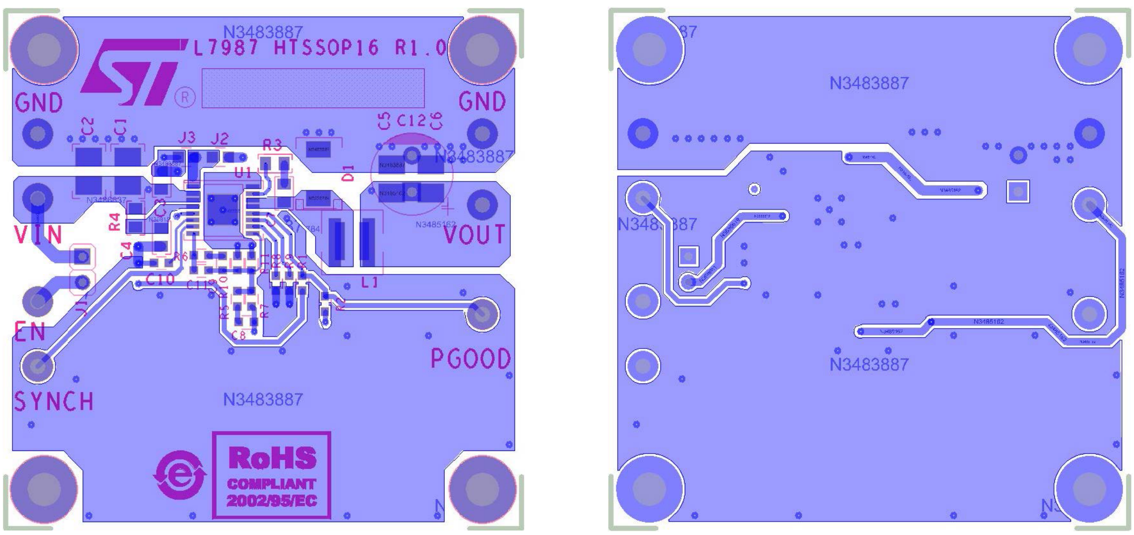


Figure 17. Efficiency vs. output current. VOUT = 3.3 V, FSW = 500k Hz.

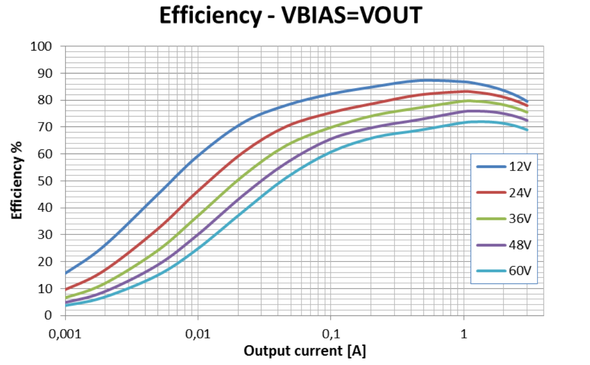


Figure 18. Junction temperature increase vs. output current. TAMB = 25 °C.

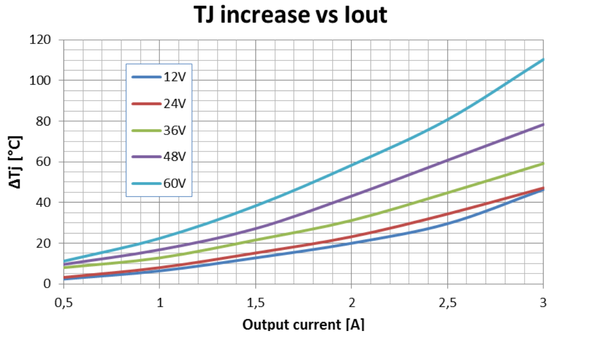


Figure 19. Input quiescent current vs. input voltage. No load.

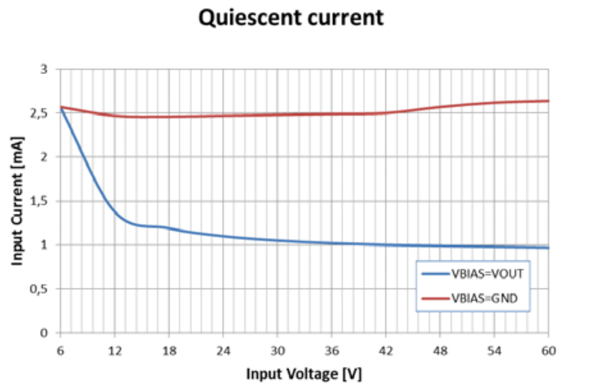


Figure 20. Input shutdown current vs. input voltage

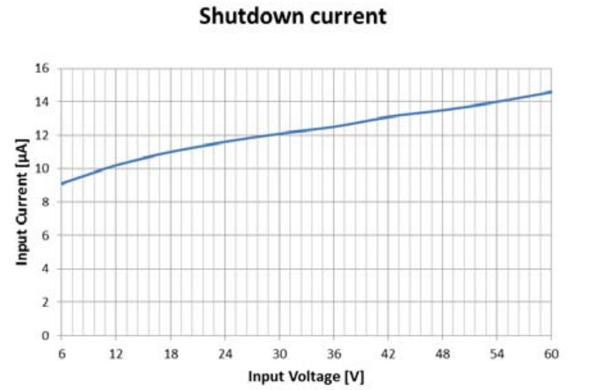


Figure 21. Load regulation. VOUT = 3.3 V, FSW = 500 kHz.

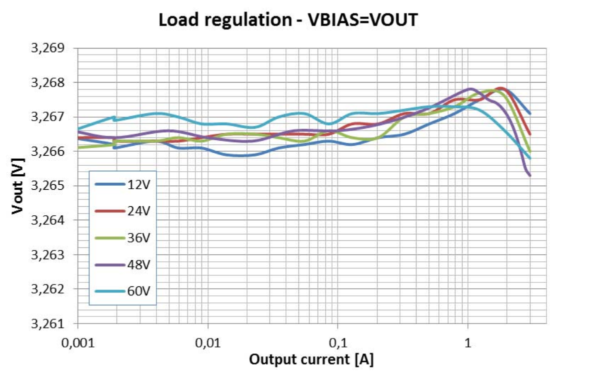
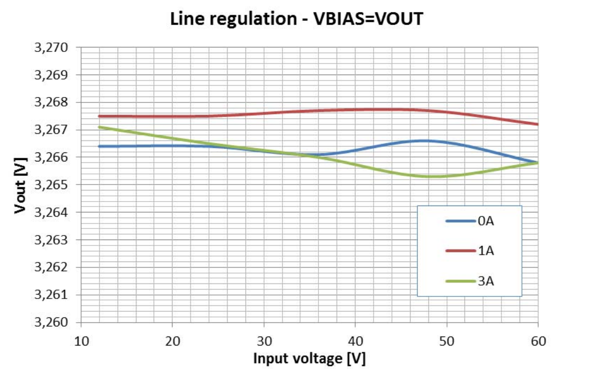


Figure 22. Line regulation. VOUT = 3.3 V, FSW = 500 kHz.



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 23. HTSSOP16 package outline

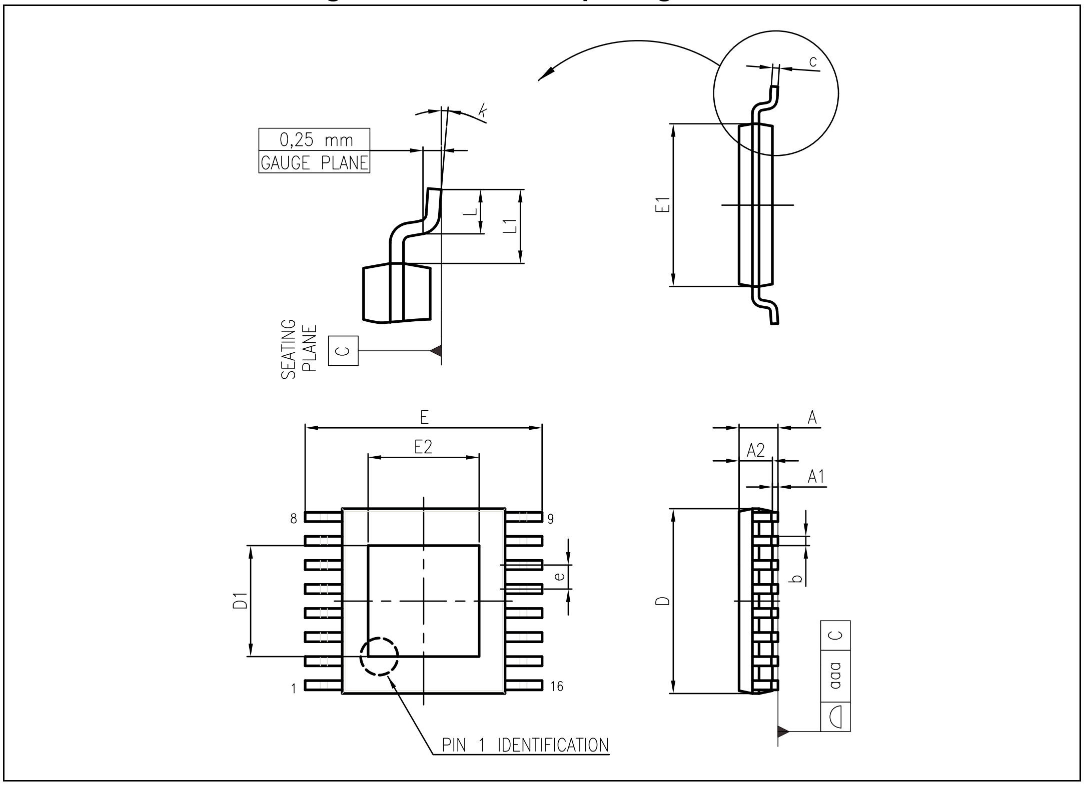


Table 8. HTSSOP16 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
D1	2.80	3.00	3.20
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.80	3.00	3.20
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
k	0.00		8.00
aaa			0.10

8 Ordering information

Table 9. Order codes

Order code	Package	Packaging
L7987	HTSSOP16	Tube
L7987TR	HTSSOP16	Tape and reel

9 Revision history

Table 10. Document revision history

Date	Revision	Changes
26-Nov-2013	1	Initial release.
10-Dec-2014	2	Updated *Section : Applications on page 1* (added “tolerant” to “Fail safe system”). Updated *Figure 2: Block diagram on page 4* (replaced by new figure). Updated *Section 3: Electrical characteristics on page 8* (updated whole *Section 3*, *Table 5: Electrical characteristics on page 8* replaced by new table, added notes *2* and *3*). Updated *Equation 13: on page 22* (replaced “ΔL_L” by “ΔI_L”). Updated *Section 6: Demonstration board on page 31* (added *Figure 17* to *Figure 22*).
04-Mar-2015	3	Updated document status to “production data”.