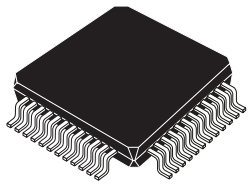
L9908

Datasheet

Automotive 3-Phase motor gate driver unit



TQFP48 (exposed pad down)

Product status link
L9908

Product summary		
Order code	Package	Packing
L9908	TQFP48 (exp. pad down)	Tray
L9908-TR		Tape&Reel

Features

- AEC-Q100 qualified
- Full ISO26262 compliant, ASIL-D systems ready
- VDH motor supply voltage range from 4.5 V to 75 V for working in single (12 V systems), double (24 V systems) and 48 V battery applications
- 3.3 V internal supply voltage generated from 5 V on VDD pin
- Digital I/O compatible to 3.3 V/5 V logics
- 6 separate N-channel FET pre-drivers:
  - dedicated source connection to each FET
  - the device can withstand -14 V to 95 V on motor connection pins
  - 0% to 100% duty cycle operation support
  - dedicated PWM input pin for each gate driver
- 3 differential high accuracy current monitors for ground referred current measurements:
  - ADC/DAC architecture
  - SPI adjustable Gain Factor and Output Offset
  - built-in error calibration
  - the device can withstand -14 V to 6 V on input sensing pins
  - SPI readable current measurement
  - 0 to 4.6 V DAC output dynamic range
- 3 real time phase voltage monitor channels:
  - SPI programmable phase voltage feedback;
  - SPI readable phase duty cycle measurement;
- 32-bit - 10 MHz SPI interface with 5-bit CRC and 1bit frame counter for internal setting, self-test and full diagnostics
- Protection and diagnostic:
  - SPI programmable VDS diagnostic and protection in on-state
  - SPI programmable Dead Time protection
  - SPI programmable Shoot-through diagnostic and protection
  - Open load, short to GND and short to battery diagnostic in off-state
  - Over-temperature diagnostic and protection with SPI programmable warning flag
  - SPI readable Tj measurement
  - Ground loss diagnostic
  - System clock monitoring
  - Power supply pins VDD, VDH, VBP over-voltage and under-voltage diagnostic
  - FET driver supply VPRE and VCP under-voltage and over-voltage diagnostic
  - SPI Window Watchdog
  - Fault status flag output

Application

- EPS – Electronic Power Steering
- HVAC Blowers – Heating, ventilation, and air conditioning
- Engine Cooling Fans
- Electronic Brake Booster
- EWP, EFP, EOP

Description

L9908 is a gate driver unit (GDU) for controlling 6 N-channel FETs for brushless motors in automotive applications.

Each one of the 3 half bridge drivers channels (HS/LS couples) can be independently configured allowing different load driving and is able to withstand -14 V to 95 V excursion on motor`s pins.

Through 6 dedicated parallel inputs the pre-driver stages can be controlled independently supporting duty cycle operations from 0% to 100% and allowing to implement all kinds of electric motor control strategy. A dedicated combination of regulators, charge pumps and bootstrap circuits allows L9908 to be suitable to operate in passenger, commercial or hybrid vehicles.

Safe operation of half bridges is ensured by shoot-through diagnosis, dead-time, short to battery, short to ground and open load detection plus a real time phase voltage monitoring.

L9908 is equipped with 3 independent high accuracy current monitor channels with SPI-configurable input differential voltage ranges for ground referenced current measurements, with 5 V/3.3 V output dynamic range compatibility.

L9908 implements diagnostics on external and internal supply, ground level, internal temperature.

A 32-bit out of frame SPI-slave interface is implemented for communication up to 10 MHz between L9908 and uC. SPI communication is safe-guarded by 5-bit CRC, 1bit frame counter, frame length check and an SPI-configurable Window Watchdog.

1 Block diagram and pin description

Figure 1. **Block diagram**

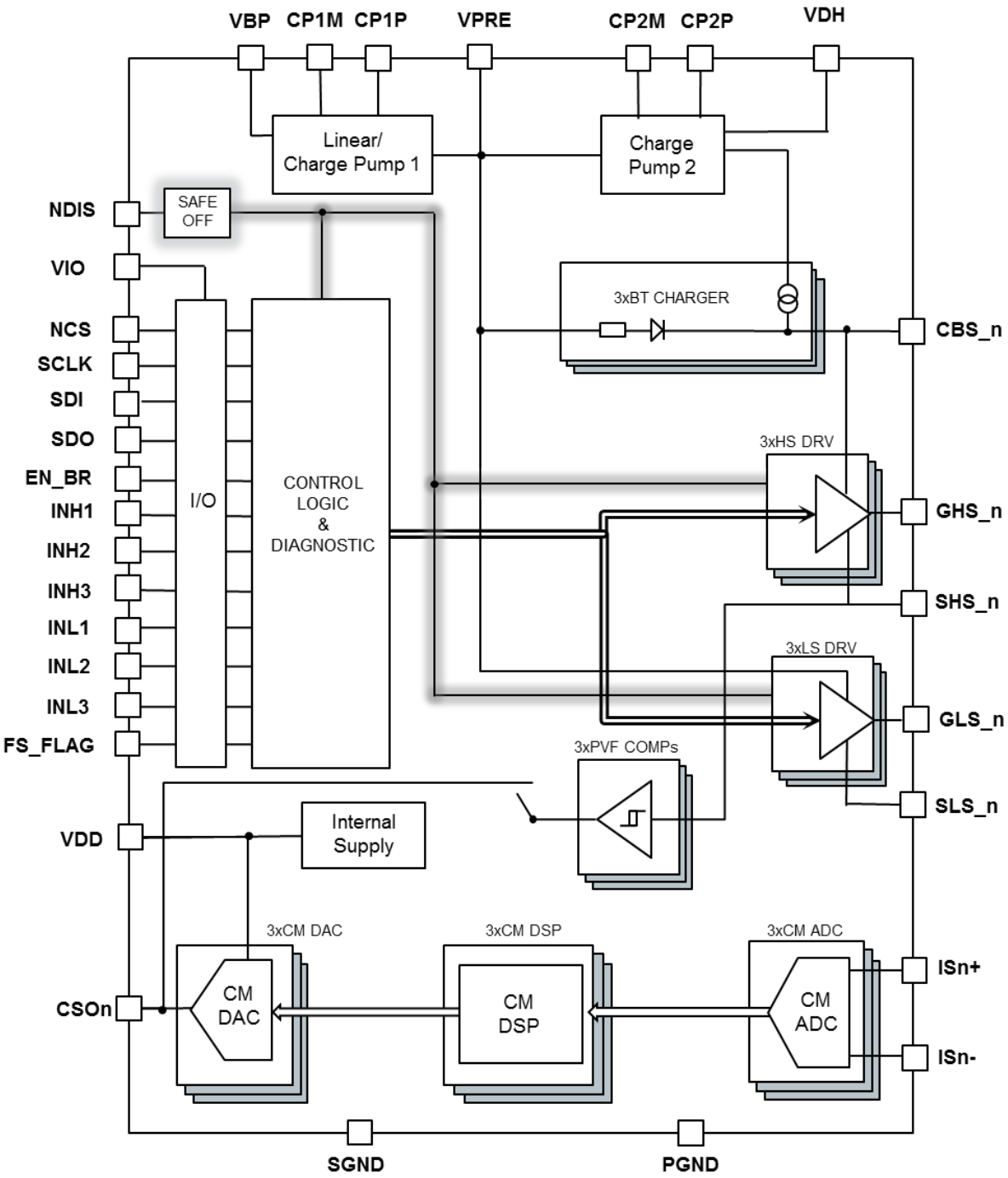
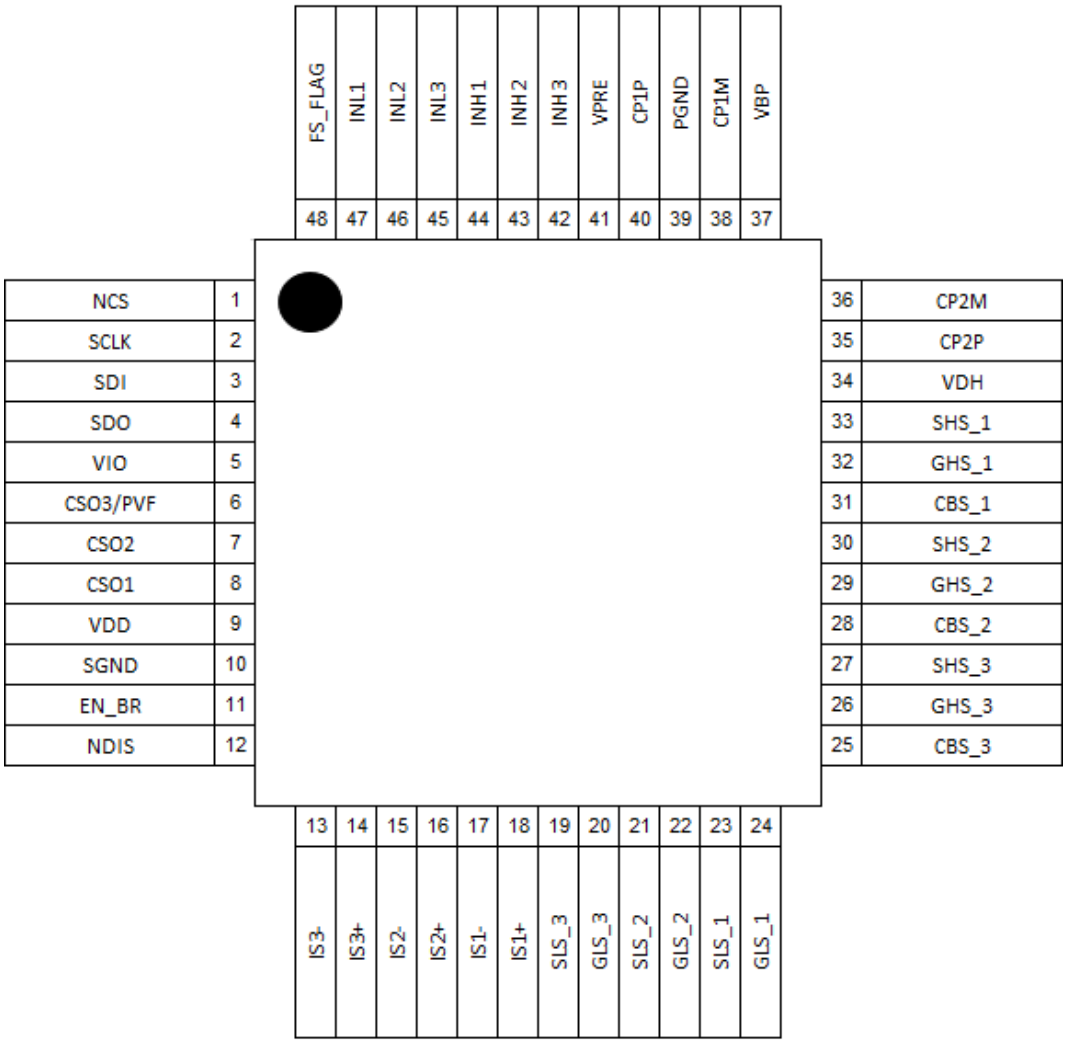


Figure 2. **Pin connection diagram (top view)**



Legenda: I = Input, O = Output, P = Power Supply, G = Ground, I/O = Input/Output

Table 1. **Pin list description**

Pin #	Pin name	Description	Pin type	Class
1	NCS	SPI Chip Select Input (Active LOW)	I	Local
2	SCLK	SPI Serial Clock Input	I	Local
3	SDI	SPI Serial Data Input	I	Local
4	SDO	SPI Serial Data Output	O	Local
5	VIO	Power supply for digital output	P	Local
6	CSO3/PVM	Current monitor 3 analog output. Phase voltage feedback output	O	Local
7	CSO2	Current monitor 2 analog output	O	Local
8	CSO1	Current monitor 1 analog output	O	Local
9	VDD	Power supply input for internal circuitry and current monitors analog output (CSOn)	P	Local
10	SGND	Signal Ground (Analog, Digital, Reference)	G	Local
11	EN_BR	Bridge Enable Input (Active HIGH)	I	Local

Pin #	Pin name	Description	Pin type	Class
12	NDIS	Safe switch-off activation Input (Active LOW)	I	Local
13	IS3-	Current monitor 3 negative input	I	Local
14	IS3+	Current monitor 3 positive input	I	Local
15	IS2-	Current monitor 2 negative input	I	Local
16	IS2+	Current monitor 2 positive input	I	Local
17	IS1-	Current monitor 1 negative input	I	Local
18	IS1+	Current monitor 1 positive input	I	Local
19	SLS_3	Source connection of LS FET, phase 3	I/O	Local
20	GLS_3	Gate connection of LS FET, phase 3	I/O	Local
21	SLS_2	Source connection of LS FET, phase 2	I/O	Local
22	GLS_2	Gate connection of LS FET, phase 2	I/O	Local
23	SLS_1	Source connection of LS FET, phase 1	I/O	Local
24	GLS_1	Gate connection of LS FET, phase 1	I/O	Local
25	CBS_3	Bootstrap capacitor of HS, phase 3	I/O	Local
26	GHS_3	Gate connection of HS FET, phase 3	I/O	Local
27	SHS_3	Source connection of HS FET, phase 3	I/O	Global
28	CBS_2	Bootstrap capacitor of HS, phase 2	I/O	Local
29	GHS_2	Gate connection of HS FET, phase 2	I/O	Local
30	SHS_2	Source connection of HS FET, phase 2	I/O	Global
31	CBS_1	Bootstrap capacitor of HS, phase 1	I/O	Local
32	GHS_1	Gate connection of HS FET, phase 1	I/O	Local
33	SHS_1	Source connection of HS FET, phase 1	I/O	Global
34	VDH	Drain connection of HS FETs	P	Global
35	CP2P	Charge Pump 2 positive input of fly capacitance	I/O	Local
36	CP2M	Charge Pump 2 negative input of fly capacitance	I/O	Local
37	VBP	Pre-regulation stage power supply	P	Global
38	CP1M	Charge Pump 1 negative input of fly capacitance	I/O	Local
39	PGND	Power Ground (Charge Pump 1 and 2)	G	Local
40	CP1P	Charge Pump 1 positive input of fly capacitance	I/O	Local
41	VPRE	Pre-regulated voltage for HS/LS Vgs driving	I/O	Local
42	INH3	PWM command for HS, phase 3 (Active HIGH)	I	Local
43	INH2	PWM command for HS, phase 2 (Active HIGH)	I	Local
44	INH1	PWM command for HS, phase 1 (Active HIGH)	I	Local
45	INL3	PWM command for LS, phase 3 (Active HIGH)	I	Local
46	INL2	PWM command for LS, phase 2 (Active HIGH)	I	Local
47	INL1	PWM command for LS, phase 1 (Active HIGH)	I	Local
48	FS_FLAG	Fault status flag output (Active LOW)	O	Local
	Exp. PAD	Cooling pad not electrically connected. Connect to GND plane on PCB		

Safety Related pin NDIS and EN_BR have the following characteristics:

Table 2. Safety related digital input pins functional partitioning

Pins	Default State	Description
NDIS	Type B – Internal Resistance Pull-down	SPI Pin (SPI communication related pin)
EN_BR	Type B – Internal Resistance Pull-down	SPI Pin (SPI communication related pin)

Table 3. NDIS and EN_BR electrical characteristics

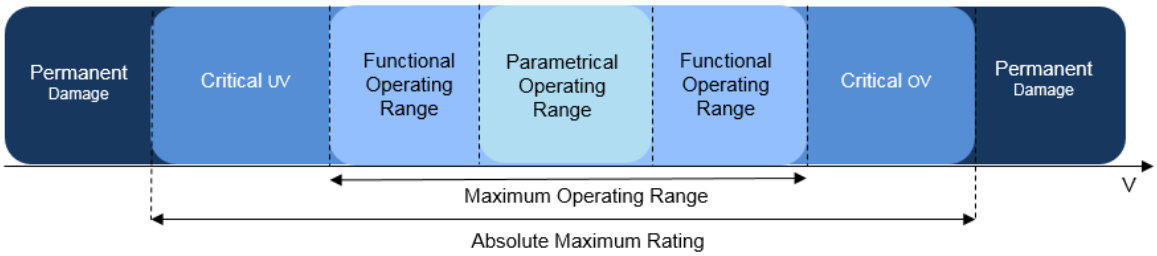
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
NDIS_ll_th	NDIS Input Low Level		-0.3	-	0.8	V	-
NDIS_hl_th	NDIS Input High Level		2	-	65	V	-
T_ndis_flt	NDIS filtering time		1	2.5	5	µs	Analog filter
NDIS_in_ipd	NDIS Pull Down Current	NDIS = VIO	-65	-40	-15	µA	-
EN_BR_ll_th	EN_BR Input Low Level		-0.3	-	0.8	V	-
EN_BR _hl_th	EN_BR Input High Level		2	-	65	V	-
T_en_br_flt	EN_BR filtering time		1	2.5	5	µs	Digital filter
EN_BR _in_ipd	EN_BR Pull Down Current	EN_BR = VIO	-65	-40	-15	µA	-

The state of Safety control pins EN_BR and NDIS is echoed into dedicated SPI readable bits **EN_BR_ECHO** and **NDIS_ECHO** in the register **GEN_STATUS2**.

2 Absolute maximum ratings

In the following section the voltage ranges of each pin are described by dividing them into three categories: Functional Operating Range, Parametrical Operating Range and Absolute maximum rating.

Figure 3. Pin voltage ranges



2.1 Maximum Operating Range (MOR)

2.1.1 Functional Operating Range

Within these operating ranges the part operates as specified in the circuit description, electrical characteristics are guaranteed only in the parametrical operating range, between these two ranges parametrical deviation may occur. The device may not operate properly if functional operating range conditions are exceeded. Once taken beyond the functional operative ratings and returned back within, the part will recover with no damage or degradation (provided that AMR range is not exceeded). All analog and digital voltages are related to the potential at signal ground SGND. All currents are assumed to be positive when current flows into the pin.

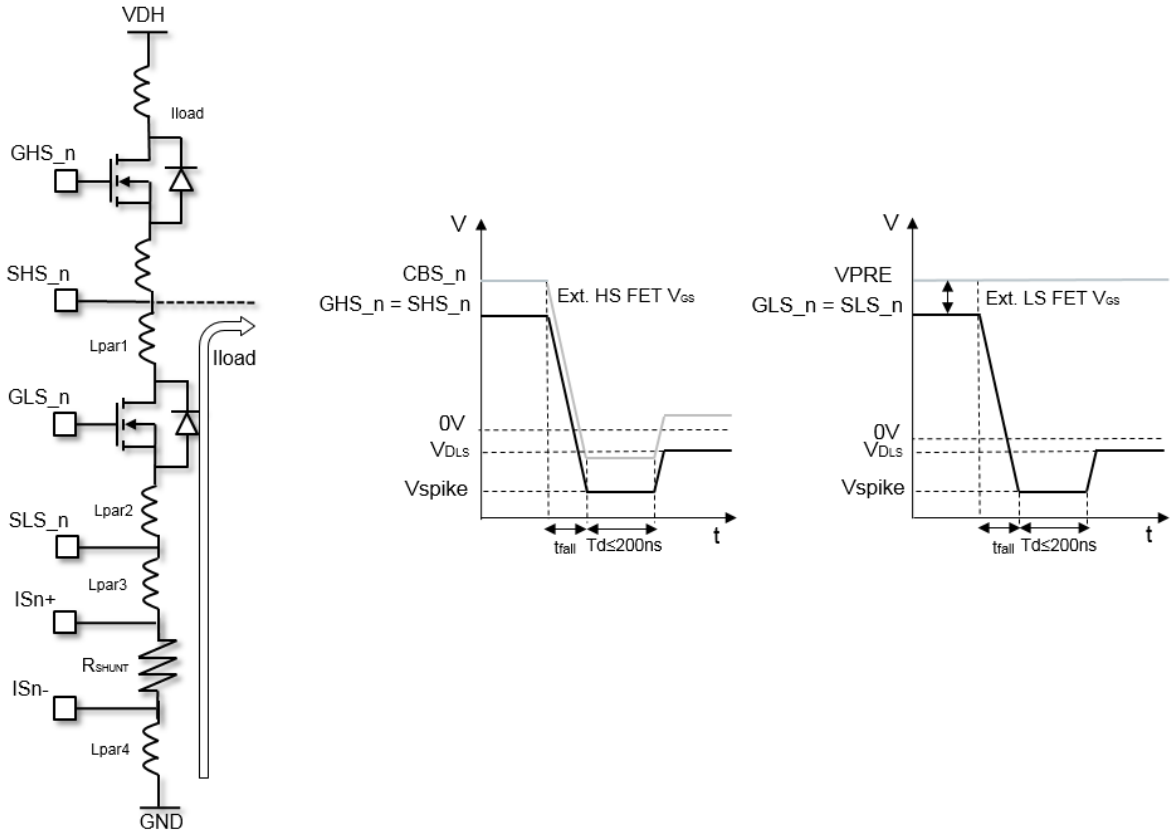
Table 4. Functional operating conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Power Supply						
VBP_MOR	VBP: voltage range	VBP UV	-	VBP OV	V	Thermally limited
VBP_MOR_PU	VBP: voltage range for power up	VBP UV + HYST	-		V	Power-Up
VDH_MOR	VDH: voltage range	VDH UV	-	VDH OV	V	-
VDH_MOR_PU	VDH: voltage range for power up	VDH UV + HYST	-		V	Power-Up
VDD_MOR	VDD: voltage range	VDD UV	-	VDD OV	V	-
VDD_MOR_PU	VDD: voltage range for power up	VDD UV + HYST	-		V	Power-Up
VIO_MOR	VIO: voltage range	2.5	-	5.5	V	-
Gate Driver Supply						
d_CP1P_CP1M_MOR	CP1P - CP1M: Charge Pump1 external capacitance terminals differential voltage	VPRE UV	-	VPRE OV	V	-
VPRE_MOR	VPRE: voltage range	VPRE UV	-	VPRE OV	V	-
d_CP2P_CP2M_MOR	CP2P – CP2M: Charge Pump2 external capacitance terminals differential voltage	VPRE UV	-	VPRE OV	V	-

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Gate Drivers						
d_CBSN_SHSN_MOR_BT1_MOR	CBS_n – SHS_n: differential voltage between CBS_n and SHS_n	VPRE UV	-	VPRE OV	V	Charge through BT charge limiter 1 only [n=1,2,3]
d_CBSN_SHSN_MOR_BT2_MOR	CBS_n – SHS_n: differential voltage between CBS_n and SHS_n	BT_lim2_vlim (MIN)	-	BT_lim2_vlim (MAX)	V	Charge through BT charge limiter 2 only [n=1,2,3]
d_GHSN_SHSN_MOR	GHS_n – SHS_n: differential voltage between GHS_n and SHS_n	0	-	CBS_n-SHS_n	V	[n=1,2,3]
SHSN_MOR	SHS_n: voltage range	-12	-	VDH +12	V	[n=1,2,3]
d_GLSN_SLSN_MOR	GLS_n – SLS_n: differential voltage between GLS_n and SLS_n	0	-	VPRE-SLS_n	V	[n=1,2,3]
d_SLSN_MOR	SLS_n: voltage range	-12	-	2	V	[n=1,2,3]
Current Monitors						
ISN_MOR	ISn+ – ISn-: differential voltage between ISn+ and IS-n	-0.3	-	0.3	V	[n=1,2,3]
ISN_MOR	ISn+/ISn-: common mode voltage range	-2	-	2	V	[n=1,2,3]
CSON_MOR	CSOn: voltage range	0	-	VDD-0.4	V	[n=1,2,3]
Digital I/O						
DO_MOR	SDO, PVM, FS_FLAG: voltage range	0	-	VIO	V	-
DI_MOR	NCS, SCLK, SDI, EN_BR, NDIS, INHn, INLn: voltage range	0	-	VIO	V	[n=1,2,3]

Note: undershoot spikes at motor`s phase (SHS_n) take place when the high side is switched off and the load current must flow through the low-side freewheeling diode.

Figure 4. **14 V pulse scenario - applicative condition**



The negative peak voltage reached during such a transition can be described by the following formula:

$$SHS_{n(peak)} = V_{d\_peak} + (L_{PAR\_TOT})\frac{dI_{LOAD}}{t_{fall}} + (R_{shunt} + R_{PAR\_TOT})I_{load} \quad (1)$$

$$SHS_{n(peak)} \approx (L_{PAR\_TOT})\frac{dI_{LOAD}}{t_{fall}} \quad (2)$$

The first term Vd_peak is the transient peak voltage of the LS FET body diode, the second is due to transient response of the parasitic inductances between SHS_n and GND while the third is related to path resistance drop. Given the maximum current conducted, the application shall limit the maximum undershoot peak voltage by minimizing the ratio:

$$\frac{L_{PAR\_TOT}}{t_{fall}} \quad (3)$$

(Ex: if Iload = 100 A then L_{PAR_TOT} = 4 nH then t_{fall} must be kept higher than 33 ns)

The above-mentioned considerations also apply to SHS_n positive pulse which takes place when the inverter is working in generator mode.

2.1.2 Parametrical Operating Range

Within these operating ranges the part operates as specified and without parameter deviations. The device may show parameters deviation if parametrical operating conditions are exceeded.

Once taken beyond the operative ratings and returned back within, the part will recover with no damage or degradation (provided that AMR range is not exceeded). All analog and digital voltages are related to the potential at signal ground SGND. All currents are assumed to be positive when current flows into the pin.

Table 5. Parametrical operating conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
Power Supply							
VBP_MOR_PAR	VBP: voltage range	-	4.5	-	36	V	-
VBP_MOR_PAR_EXT1	VBP: extended voltage range 1	t ≤ 15 min Tamb = 25°C	36	-	48	V	Jump Start Pulse
VBP_MOR_PAR_EXT2	VBP: extended voltage range 2	t ≤ 400 ms Tamb = 25°C	48	-	60	V	Load Dump Pulse
VDD_MOR_PAR_CSON	VDD: voltage range (CSOn related parameter)	-	4.85	5	5.15	V	-
VDD_MOR_PAR	VDD: voltage range	-	4. 5	5	5.5	V	-
VIO_MOR_PAR	VIO: voltage range	-	2.5	-	5.5	V	-
VPRE_MOR_PAR	VPRE: voltage range	-	7	-	15	V	-
VDH_MOR_PAR	VDH: voltage range	-	4.5	-	52	V	-
VDH_MOR_PAR_EXT1	VDH: extended voltage range 1	t ≤ 60 min Tamb = 25°C	52	-	60	V	Long Term Overvoltage
VDH_MOR_PAR_EXT2	VDH: extended voltage range 2	t ≤ 40 ms Tamb = 25°C	60	-	70	V	Transient Overvoltage

Note: All parameters are guaranteed and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

2.2 Absolute Maximum Ratings (AMR)

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. All analog and digital voltages are related to the potential at signal ground SGND. All currents are assumed to be positive when current flows into the pin.

Table 6. Absolute maximum ratings

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
Power Supply							
VBP_AMR_DC	VBP: DC voltage range	-	-0.3	-	65(1)	V	-
VBP_AMR_AC	VBP: transient voltage range	t ≤ 400 ns; IVBP ≤ 500 mA	-1	-	65(1)	V	Not subject to production test
VDH_AMR_DC	VDH: DC voltage range.		-0.3	-	75(2)	V	
VDH_AMR_AC	VDH: transient voltage range.	t ≤ 400 ns; IVDH ≤ 500 mA	-1	-	90	V	Not subject to production test
d_VDH_VBP_AMR	VDH - VBP Differential voltage between VDH and VBP	-	-65	-	75	V	-
VDD_AMR	VDD: voltage range	-	-0.3	-	20	V	-
VIO_AMR	VIO: voltage range	-	-0.3	-	20	V	-
Gate Driver Supply							
CP1M_AMR	CP1M: voltage range		-0.3	-	65	V	-

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
d_VBP_CP1M_AMR	VBP - CP1M: Charge Pump1 external differential voltage between VBP and CP1M	-	-0.3	-	65	V	-
CP1P_AMR	CP1P: voltage range	-	-0.3	-	20	V	-
d_CP1P_CP1M_AMR	CP1P - CP1M: Charge Pump1 external capacitance terminals differential voltage	-	-65	-	20	V	-
d_VBP_CP1P_AMR	VBP - CP1P: Charge Pump1 external differential voltage between VBP and CP1P	-	-20	-	65	V	-
d_VPRE_CP1P_AMR	VPRE – CP1P: Charge Pump1 external differential voltage between VPRE and CP1P	-	-0.3	-	20	V	-
VPRE_AMR	VPRE: voltage range	-	-0.3	-	20	V	-
CP2M_AMR	CP2M: voltage range	-	-0.3	-	75	V	-
d_VPRE_CP2M_AMR	VPRE – CP2M: Charge Pump2 external differential voltage between VPRE and CP2M	-	-75	-	20	V	-
CP2P_AMR	CP2P: voltage range	-	-0.3	-	95	V	-
d_CP2P_CP2M_AMR	CP2P – CP2M: Charge Pump2 external capacitance terminals differential voltage	-	-20	-	75	V	-
d_VPRE_CP2P_AMR	VPRE – CP2P: Charge Pump2 external differential voltage between VPRE and CP2P	-	-75	-	20	V	-
d_VDH_CP2P_AMR	VDH – CP2P: Charge Pump2 external differential voltage between VDH and CP2P	-	-95	-	0.3	V	-
d_VDH_VPRE_SHSN_AMR	VDH+VPRE-SHS_n: constraint on simultaneous voltage on VDH, VPRE and SHS_n/GHS_n	-	-	-	100(3)	V	[n=1,2,3] Application information
Gate Drivers							
CBS_AMR_DC_RES	CBS_n: DC voltage range in RESET	VDD < VDD UV + HYST	-0.3	-	95	V	[n=1,2,3]
CBS_AMR_DC	CBS_n: DC voltage range	VDD≥VDD UV + HYST	-7(1)	-	95	V	[n=1,2,3]
CBS_AMR_AC	CBS_n: transient voltage range	VDD ≥ VDD UV + HYST t ≤ 200 ns	-14(1)	-	95	V	[n=1,2,3] Not subject to production test
d_CBSN_CP2P_AMR	CBS_n - CP2P: differential voltage between CBS_n and CP2P terminals	-	-95	-	20	V	[n=1,2,3]
GHS_N_AMR_DC_RES	GHS_n: DC voltage range in RESET	VDD < VDD UV + HYST	-0.3	-	95	V	[n=1,2,3]
GHS_N_AMR_DC	GHS_n: DC voltage range	VDD ≥ VDD UV + HYST	-7	-	95	V	[n=1,2,3]
GHS_N_AMR_AC	GHS_n: transient voltage range	VDD ≥ VDD UV + HYST t ≤ 200 ns	-14	-	95	V	[n=1,2,3] Not subject to production test

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
SHS_N_AMR_DC_RES	SHS_n: DC voltage range in RESET	VDD < VDD UV + HYST	-0.3	-	95	V	[n=1,2,3]
SHS_N_AMR_DC	SHS_n: DC voltage range	VDD ≥ VDD UV + HYST	-7	-	75	V	[n=1,2,3]
SHS_N_AMR_AC	SHS_n: transient voltage range	VDD ≥ VDD UV + HYST t ≤ 200 ns	-14	-	95	V	[n=1,2,3] Not subject to production test
SHS_N_AMR_SR	SHS_n: transient slew rate	SR ≤ 1V/ns	-	-	20	V	[n=1,2,3] Not subject to production test
d_CBSN_GHSN_AMR	CBS_n - GHS_n: differential voltage between CBS_n and GHS_n terminals	-	-0.3	-	20	V	[n=1,2,3]
d_CBSN_SHSN_AMR	CBS_n - SHS_n: Differential voltage between CBS_n and SHS_n	-	-0.3	-	20	V	[n=1,2,3]
d_GHSN_SHSN_AMR_DC	GHS _n - SHS_n: Differential DC voltage between GHS_n and SHS_n	-	-0.3	-	20	V	[n=1,2,3]
d_GHSN_SHSN_AMR_AC	GHS _n - SHS_n: Differential transient voltage between GHS_n and SHS_n	t ≤ 200 ns; IGHS_n ≤ - 2A	-2	-	20	V	[n=1,2,3] Not subject to production test
d_VDH_SHSN_AMR_RES	VDH - SHS_n: Differential voltage between VDH and SHS_n in RESET	VDD < VDD UV + HYST	-0.3	-	95	V	-
d_VDH_SHSN_AMR	VDH - SHS_n: Differential voltage between VDH and SHS_n	VDD ≥ VDD UV + HYST	-14	-	95	V	[n=1,2,3]
GLS_N_AMR_RES	GLS_n: DC voltage range in RESET	VDD < VDD UV + HYST	-0.3	-	95	V	[n=1,2,3]
GLS_N_AMR	GLS_n: DC voltage range	VDD ≥ VDD UV + HYST	-7	-	20	V	[n=1,2,3]
GLS_N_AMR_AC	GLS_n: transient voltage range	VDD ≥ VDD UV + HYST t ≤ 200 ns	-14	-	20	V	[n=1,2,3] Not subject to production test
SLS_N_AMR_DC_RES	SLS_n: DC voltage range in RESET	VDD < VDD UV + HYST	-0.3	-	95	V	[n=1,2,3]
SLS_N_AMR_DC	SLS_n: DC voltage range	VDD ≥ VDD UV + HYST	-7	-	20	V	[n=1,2,3]
SLS_N_AMR_AC	SLS_n: transient voltage range	VDD ≥ VDD UV + HYST t ≤ 200 ns	-14	-	20	V	[n=1,2,3] Not subject to production test
d_VPRE_GLSN_AMR	VPRE - GLS_n: Differential voltage between VPRE and GLS_n	-	-0.3	-	35	V	[n=1,2,3]
d_VPRE_SLSN_AMR	VPRE - SLS_n: Differential voltage between VPRE and SLS_n	-	-0.3	-	35	V	[n=1,2,3]
d_GLSN_SLSN_AMR_DC	GLS_n - SLS_n: Differential voltage between GLS_n and SLS_n	-	0(1)	-	20	V	[n=1,2,3]

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
d_GLSN_SLSN_AMR_AC	GLS_n - SLS_n: Differential voltage between GLS_n and SLS_n	t ≤ 200 ns; IGLS_n ≤ - 2 A	-2[1]	-	20	V	[n=1,2,3] Not subject to production test
Current Monitors							
IS_AMR_DC_RES	ISn+/ISn-: DC voltage range in RESET	VDD < VDD UV + HYST	-0.3	-	20	V	[n=1,2,3]
IS_AMR_DC	ISn+/ISn-: DC common mode voltage range	VDD ≥ VDD UV + HYST	-7	-	20	V	[n=1,2,3]
IS_AMR_AC	ISn+/ISn-: transient common mode voltage range	VDD ≥ VDD UV + HYST t ≤ 200 ns	-14	-	20	V	[n=1,2,3] Not subject to production test
d_ISMPN_ISMN_AMR	ISn+ - ISn-: Differential voltage between ISn+ and ISn-	-	-5	-	5	V	[n=1,2,3]
d_VPRE_IS_AMR	VPRE - ISn+/ISn: Differential voltage between VPRE and ISn+/ISn	-	0	-	40	V	[n=1,2,3] Not subject to production test
IS_AMR_SR	ISn+/ISn-: common mode transient slew rate	SR ≤ 1V/ns	-	-	20	V	[n=1,2,3] Not subject to production test
CSON_AMR	CSOn: voltage range	-	-0.3	-	20	V	[n=1,2,3]
d_VIO_CSON_AMR	VIO – CSOn: differential voltage between VIO supply and CSOn outputs	-	-0.3	-	20	V	[n=1,2,3]
SPI Interface							
NCS_AMR	NCS: voltage range	-	-0.3	-	20	V	-
SCLK_AMR	SCLK: voltage range	-	-0.3	-	20	V	-
SDI_AMR	SDI: voltage range	-	-0.3	-	20	V	-
SDO_AMR	SDO: voltage range	-	-0.3	-	20	V	-
Digital I/O							
d_VIO_SDO_AMR	VIO – SDO: differential voltage between VIO supply and SDO outputs	-	-0.3	-	20	V	-
d_VIO_PVF_AMR	VIO – PVF: differential voltage between VIO supply and PVF outputs	-	-20	-	20	V	-
d_VIO_FSFLAG_AMR	VIO – FS_FLAG: differential voltage between VIO supply and FS_FLAG outputs	-	-0.3	-	20	V	-
PVF_AMR	PVF: voltage range	-	-0.3	-	20	V	-
FS_FLAG	FS_FLAG: voltage range	-	-0.3	-	20	V	-
INHN_AMR	INHn: voltage range	-	-0.3	-	20	V	[n=1,2,3]
INLN_AMR	INLn: voltage range	-	-0.3	-	20	V	[n=1,2,3]
EN_BR _AMR	EN_BR: voltage range	-	-0.3	-	65	V	-
NDIS _AMR	NDIS: voltage range	-	-0.3	-	65	V	-
Grounds							
GND_AMR	SGND, PGND	-	-0.6	-	0.6	V	-

1. *36 V AMR over life-time. 48 V ≥ AMR ≥ 36 V for Jump Start transient pulse E-02 as defined in LV 124 standard and AMR ≥ 48 V for Load Dump Test B transient pulse as defined in ISO 16750-2 standard.*

2. *52 V AMR over life-time. 60 V ≥ AMR ≥ 52 V for E48-01a transient pulse, AMR ≥ 60 V for E48-02 transients pulse as defined in VDA_320/LV 148 standard.*
3. *The maximum voltage drop experienced by internal structures has to be limited to 100V in order to avoid damages. The HS pre-driver stage may experience together the maximum voltage and the minimum voltage all over L9908 respectively imposed by CP2 output voltage or CBS_n and SHS_n negative pulses. HS pre-driver then must be protected by ensuring that the absolute maximum voltage on CP2 or on CBS_n never takes place simultaneously with the absolute minimum voltage on SHS_n so that: VDH * VPRE - SHS_n ≤ 100 W*

Note: Integrated protection and diagnostics are designed to prevent device damage under the fault conditions defined in the functional description. Fault conditions are considered to be out of normal operating range. Protection functions are not designed for a continuous repetitive operation.

2.3 ESD resistivity

Table 7. ESD resistivity (pin level)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
HBM_LOC_ESD	HBM (Local Pins)(1)	All pins(2)	-2	-	2	kV	Class 2
HBM_GLO_ESD	HBM (Global Pins)(1)	VBP, VDH, SHS_n	-4	-	4	kV	Class 3A
CDM _ESD	CDM (1)	All pins	-500	-	500	V	Class C3
CDM_COR_ESD	CDM (1)	Corner pins	-750	-	750	V	Class C4
LUT	Latch Up (3)	All pins	-100	-	100	mA	-

1. *According to AEC-Q100-011*
2. *Pins are all GND connected together.*
3. *According to AEC-Q100-004*

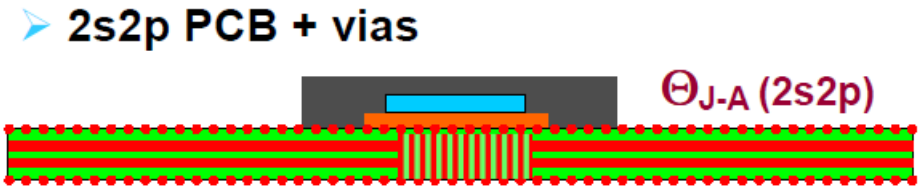
2.4 Temperature ranges and thermal data

Table 8. Temperature ranges and thermal data

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_{amb}	Operating temperature (ECU environment)	-40	-	150	°C	-
T_j(1)	Operating junction temperature	-40	-	150	°C	-
T_j	Extended operating junction temperature	-40	-	175	°C	200h over life time
T_{sto}	Storage temperature	-55	-	150	°C	
R_{thJ-A}(2)	Thermal resistance junction-to-ambient	-	31	-	°C/W	Homogeneous internal power distribution (3)
R_{Thj-cb}(2)	Thermal resistance junction-to-case-bottom	-	2.1	-	°C/W	Homogeneous internal power distribution

1. *All parameters are guaranteed and tested, in the temperature range T_j -40 ÷ 150°C unless otherwise specified. The device is still operative and functional at higher temperatures (up to T_j 175°C). Device functionality at high temperature is guaranteed by bench validation, electrical parameters are guaranteed by correlation with ATE tests at reduced temperature and adjusted limits (if needed).*
2. *Not subject to production test, guaranteed by design.*
3. *R_{thJA} value is retrieved according to Jedec JESD51-2,-5,-7 guideline with a 2s2p board.*

Figure 5. **2s2p PCB with thermal vias**



Note: In “2s2p”, the “s” suffix stands for “Signal” and the number before indicates how many PCB layers are dedicated to signal wires. The “p” suffix stands for “Power” and the number before indicates how many PCB layers are dedicated to power planes.

3 Current consumption

Table 9. Quiescent current consumption in reset mode

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
IQ_VBP1	Quiescent consumption for VBP in reset mode	VBP = 14 V, -40° ≤ T_j ≤ 25°C VDD = 0 V	-	0.5	15	µA
IQ_VBP2	Quiescent consumption for VBP in reset mode	VBP = 14 V, 25°C < T_j ≤ 150°C VDD = 0 V	-	1.3	15	µA
IQ_VBP3	Quiescent consumption for VBP in reset mode	VBP = 60 V, -40°C ≤ T_j ≤ 25°C VDD = 0 V	-	2.2	15	µA
IQ_VBP4	Quiescent consumption for VBP in reset mode	VBP = 60 V, 25°C < T_j ≤ 150°C VDD = 0 V	-	4.6	15	µA
IQ_VDH1	Quiescent consumption for VDH in reset mode	VDH = 14 V, -40°C ≤ T_j ≤ 25°C VDD = 0 V	-	0.3	15	µA
IQ_VDH2	Quiescent consumption for VDH in reset mode	VDH = 14 V, 25°C <T_j ≤ 150°C VDD = 0 V	-	1	15	µA
IQ_VDH3	Quiescent consumption for VDH in reset mode	VDH = 60 V, 40°C ≤ T_j ≤ 25°C VDD = 0 V	-	0.8	15	µA
IQ_VDH4	Quiescent consumption for VDH in reset mode	VDH = 60 V, 25°C <T^j ≤ 150°C VDD = 0 V	-	2.5	15	µA
IQ_VIO1	Quiescent consumption for VIO in reset mode	VIO = 5 V, -40°C ≤ T_j ≤ 25°C VDD = 0 V	-	5	15	µA
IQ_VIO2	Quiescent consumption for VIO in reset mode	VIO = 5 V, 25°C < T_j ≤ 150°C VDD = 0 V	-	6	15	µA

Table 10. Mean current consumptions in normal mode

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
INORMAL_VBP1	Mean Current consumption for VBP in normal mode	VBP = 14 V, -40°C ≤ T_j ≤ 25°C Default Configuration and HBn_DIS=0 INLn=INHn=0, SHS_n=0 [n=1,2,3]	-	2.5	20	mA
INORMAL_VBP2	Mean Current consumption for VBP in normal mode	VBP = 14 V, 25°C < T_j ≤ 150°C Default Configuration and HBn_DIS=0 INLn=INHn=0, SHS_n=0 [n=1,2,3]	-	2.5	20	mA
INORMAL_VBP3	Mean Current consumption for VBP in normal mode	VBP = 60 V, -40°C ≤ T_j < 25°C Default Configuration and HBn_DIS=0 INLn=INHn=0, SHS_n=0 [n=1,2,3]	-	2.5	20	mA
INORMAL_VBP4	Mean Current consumption for VBP in normal mode	VBP = 60 V, 25°C < T_j ≤ 150°C Default Configuration and HBn_DIS=0 INLn=INHn=0, SHS_n=0 [n=1,2,3]	-	2.5	20	mA

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
INORMAL_VDH1	Mean Current consumption for VDH in normal mode	VDH = 14 V, -40°C ≤ T_j ≤ 25°C Default Configuration and HBn_DIS=0 INLn=INHn=0, SHS_n=0 [n=1,2,3]	-	3.5	15	mA
INORMAL_VDH2	Mean Current consumption for VDH in normal mode	VDH = 14 V, 25°C < T_j ≤ 150°C Default Configuration and HBn_DIS=0 INLn=INHn=0, SHS_n=0 [n=1,2,3]	-	3.5	15	mA
INORMAL_VDH3	Mean Current consumption for VDH in normal mode	VDH = 60 V, -40°C ≤ T_j ≤ 25°C Default Configuration and HBn_DIS=0 INLn=INHn=0, SHS_n=0 [n=1,2,3]	-	3.5	15	mA
INORMAL_VDH4	Mean Current consumption for VDH in normal mode	VDH = 60 V, 25°C < T_j ≤ 150°C Default Configuration and HBn_DIS=0 INLn=INHn=0, SHS_n=0 [n=1,2,3]	-	3.5	15	mA
INORMAL_VDD1	Mean Current consumption for VDD in normal mode	VDD = 5.5 V, -40°C ≤ T_j ≤ 25°C Default Configuration and HBn_DIS=0 INLn=INHn=0, SHS_n=0 [n=1,2,3]	-	23	40	mA
INORMAL_VDD2	Mean Current consumption for VDD in normal mode	VDD = 5.5 V, 25°C < T_j ≤ 150°C Default Configuration and HBn_DIS=0 INLn=INHn=0, SHS_n=0 [n=1,2,3]	-	25	40	mA
INORMAL_VIO1	Mean Current consumption for VIO in normal mode	VIO = 5 V, -40°C ≤ T_j ≤ 25°C Default Configuration and HBn_DIS=0 INLn=INHn=0, SHS_n=0 [n=1,2,3]	-	2	4	mA
NORMAL_VIO2	Mean Current consumption for VIO in normal mode	VIO = 5 V, 25°C < T_j ≤ 150°C Default Configuration and HBn_DIS=0 INLn=INHn=0, SHS_n=0 [n=1,2,3]	-	2.5	4	mA

4 Functional safety

4.1 Safe states

To reach the safety requirements of the system, the following safe states are supported by L9908, with a different associated priority level:

- SAFE-OFF due to CLK1_TIME_OUT or NDIS='0'. Priority Level = 1
- SAFE-HIZ. Priority Level = 2
- SAFE-OFF due to STD Fault detection except INT_RST or Configurable fault with related FRC set as 00. Priority Level = 3
- SAFE-DIS. Priority Level = 4

In case of simultaneous safe state activation requests with different safe states required, the safe state reached by L9908 is determined by the highest priority level.

Note:
- *Priority is descending, 1 = higher priority.*
- *SAFE – OFF by NDIS assertion has the highest priority all over.*

4.1.1 SAFE-OFF

When SAFE-OFF is active the gate driver unit is disabled by forcing the three Half Bridges in a tristate mode so that VGHS_n-VSHS_n = 0 V actively, VGLS_n-VSLS_n = HIZ and by disabling the Gate Drive Supply block (CP1_EN = CP2_EN = 0).

SAFE-OFF is activated by default if the following conditions are verified:

- STD Fault detection except INT_RST
- CLK1_TIME_OUT
- Configurable fault with related FRC set as 00
- NDIS = 0

4.1.2 SAFE-DIS

When SAFE-DIS is active the gate driver unit is disabled by forcing the three Half Bridges in a tristate mode so that VGHS_n-VSHS_n and VGLS_n-VSLSn are kept tight to 0 V actively.

SAFE-DIS is activated by default if the following conditions are verified:

- VPRE UV fault detection
- Configurable fault with related FRC set as 01
- EN_BR = 0

4.1.3 SAFE-HIZ

When SAFE-HIZ is active the gate driver unit is disabled by forcing the driver output in a tristate mode so that VGHS_n-VSHS_n and VGLS_n-VSLSn = HIZ.

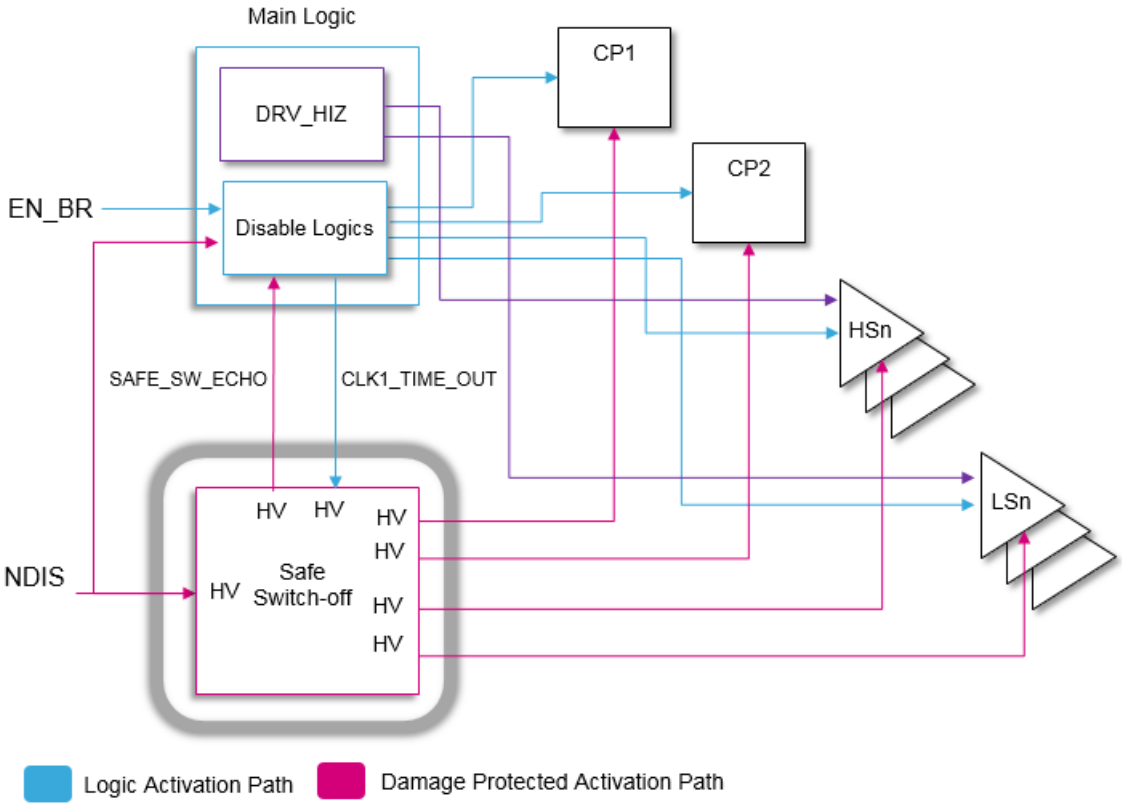
SAFE-HIZ is activated by default if the following conditions are verified:

- Fault detection which generates INT_RST
- SW_RST
- No STD faults present & HBn_DIS = 0 [n = 1,2,3] & STD DRV_HIZ = 1

4.2 Safe state activation

Depending on the safe state its activation is performed through one between two separate paths.

Figure 6. Safe states activation paths



Logic activation path: safe state activation is carried out entirely by the main logic.

This path is used to develop:

- SAFE HIZ (except if determined by CLK1_TIME_OUT)
- SAFE DIS
- SAFE OFF

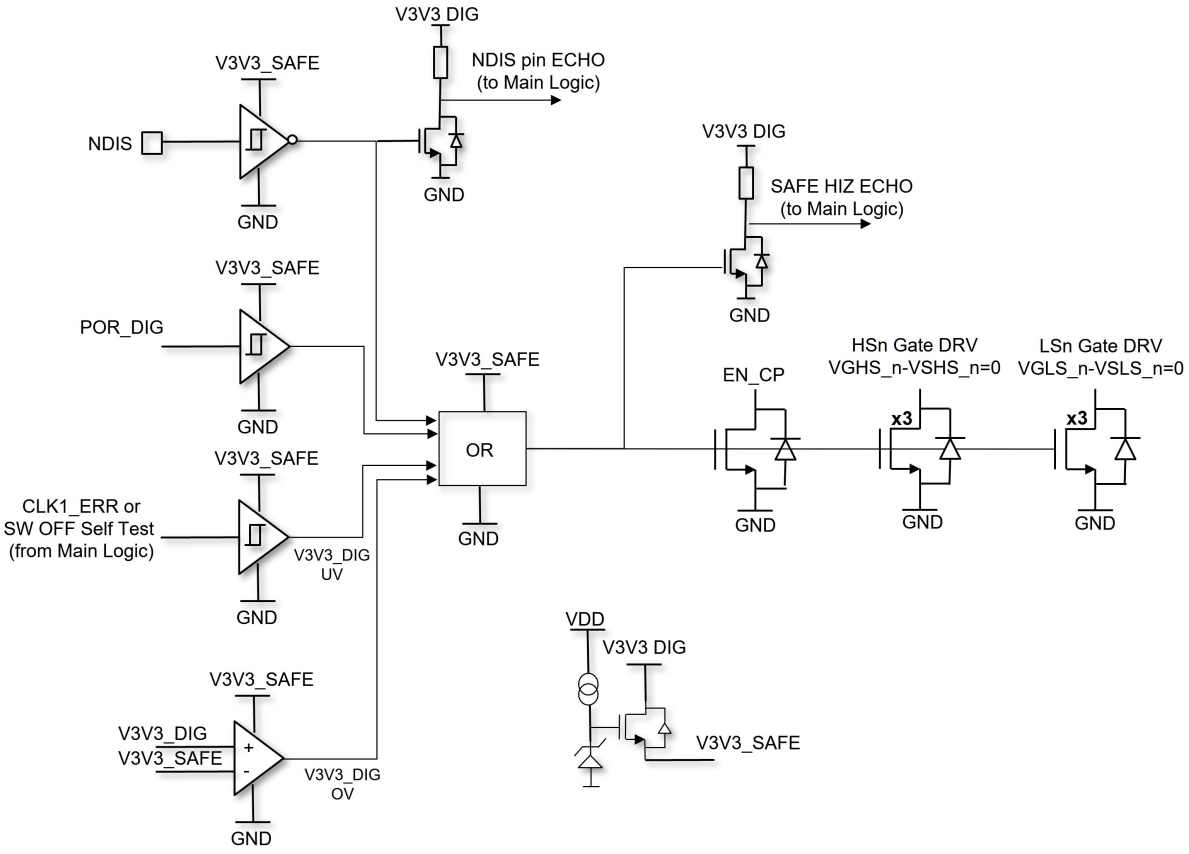
Damage protected activation path: in case of device failure where internal main logic integrity is compromised L9908 implements an isolated Safe Switch Off structure which allows to activate an isolated Safe Switch Off structure which can be activated through a separated path.

This path is used to develop:

- SAFE OFF (only if determined by NDIS = 0)
- CLK1_TIME_OUT

The Safe State activation through the damage protected path is signaled by setting the dedicated SPI read only bit SAFE_STATE (GEN_STATUS1[2]).

Figure 7. **Damage protected activation simplified structure**



5 Functional description

5.1 Internal supply

5.1.1 VDD power supply

The internal supply rails for analog and digital circuitries on L9908 are generated from the VDD pin which is the main power input. Additionally VDD is used as reference voltage for Current Measurement Analog output (CSO Buffers).

5.1.2 Internal supply monitor

Each internal supply voltage level (V3V3_ANA/DIG) is monitored by means of a dedicated UV and an OV diagnosis. Abnormal behavior on internal supply level will cause the generation of a POR (Power on Reset) event that consequently sends L9908 into a RESET state. Hysteresis on thresholds and filtering time are implemented.

If V3V3_ANA/DIG ≤ V3V3_uv_th occurs for an interval longer than T_por_htol_flt, INT_RST flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by an SPI command. POR_ANA/DIG is set low and internal reset is triggered.

If V3V3_ANA/DIG ≥ V3V3_ov_th occurs for an interval longer than T_por_htol_flt, INT_RST flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by an SPI command. POR_ ANA/DIG is set low and internal reset is triggered. OV/UV Resets related to V3V3 internal reference are represented in Figure 8.

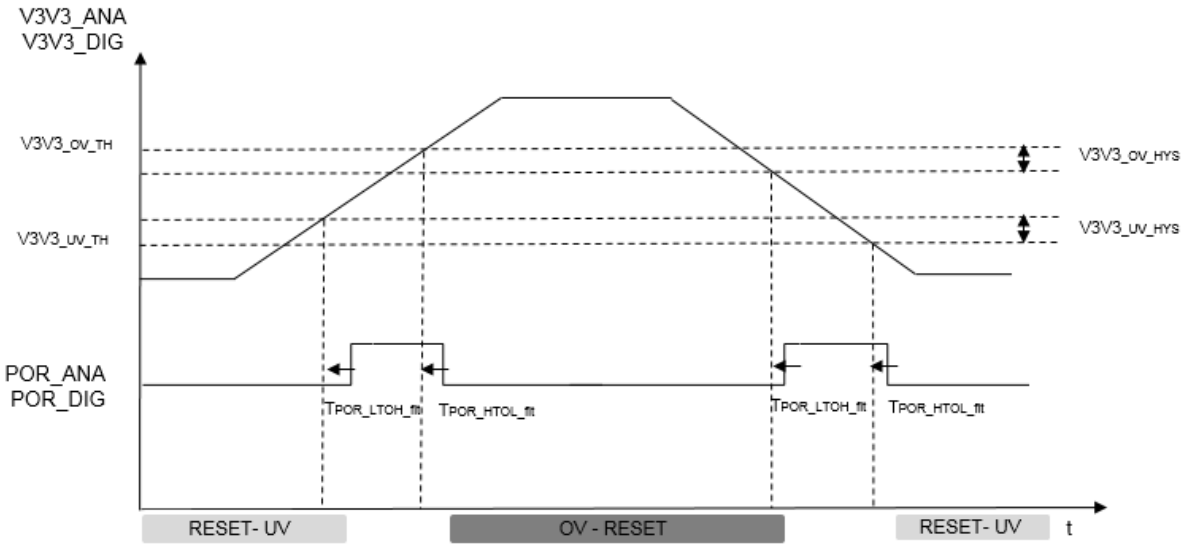
The internal supply monitor is safety relevant and then a self-check procedure is implemented.

Note: All parameters are guaranteed and tested in the voltage ranges specified in Table 5 unless otherwise specified. Where not specified parametrical operating range equals functional operating range.

Table 11. Internal power supply electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VBG_vout	Bandgap output voltage	1.188	1.2	1.212	V	-
V3V3_vout	V3V3_ANA/DIG output voltage	3.2	3.3	3.34	V	-
V3V3_uv_th	V3V3_ANA/DIG under-voltage threshold	2.65	2.73	2.93	V	Comparator output Low to High
V3V3_uv_hys	V3V3_ANA/DIG under-voltage hysteresis	35	45	56	mV	-
V3V3_ov_th	V3V3_ANA/DIG over-voltage threshold	3.6	3.7	3.9	V	Comparator output Low to High
V3V3_ov_hys	V3V3_ANA/DIG over-voltage hysteresis	-	0	-	mV	-
V3V3_pre_vout	V3V3_PRE output voltage	2.7	3.35	3.55	V	-
T_por_ltoh_flt	POR_V3V3 Low to High state filter time	3.2	4.8	7.3	µs	Analog filter
T_por_htol_flt	POR_V3V3 High to Low state filter time	5.4	8.3	13.5	µs	Analog filter

Figure 8. **Internal supply operative range**



5.1.3 VDD monitor

VDD voltage level is monitored by means of dedicated UV and an OV diagnosis. Hysteresis on thresholds and filtering time are implemented.

If VDD ≤ VDD_uv_th occurs for an interval longer than T_por_htol_flt, INT_RST flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by SPI command. POR_ANA is set low and internal reset is triggered.

If VDD ≥ VDD_ov_th occurs for an interval longer than T_vdd_ov, VDD_OV flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by SPI command.

Device's functional ranges related to VDD level are represented in Figure 9.

The operative VDD monitor is safety relevant and then a self-check procedure is implemented.

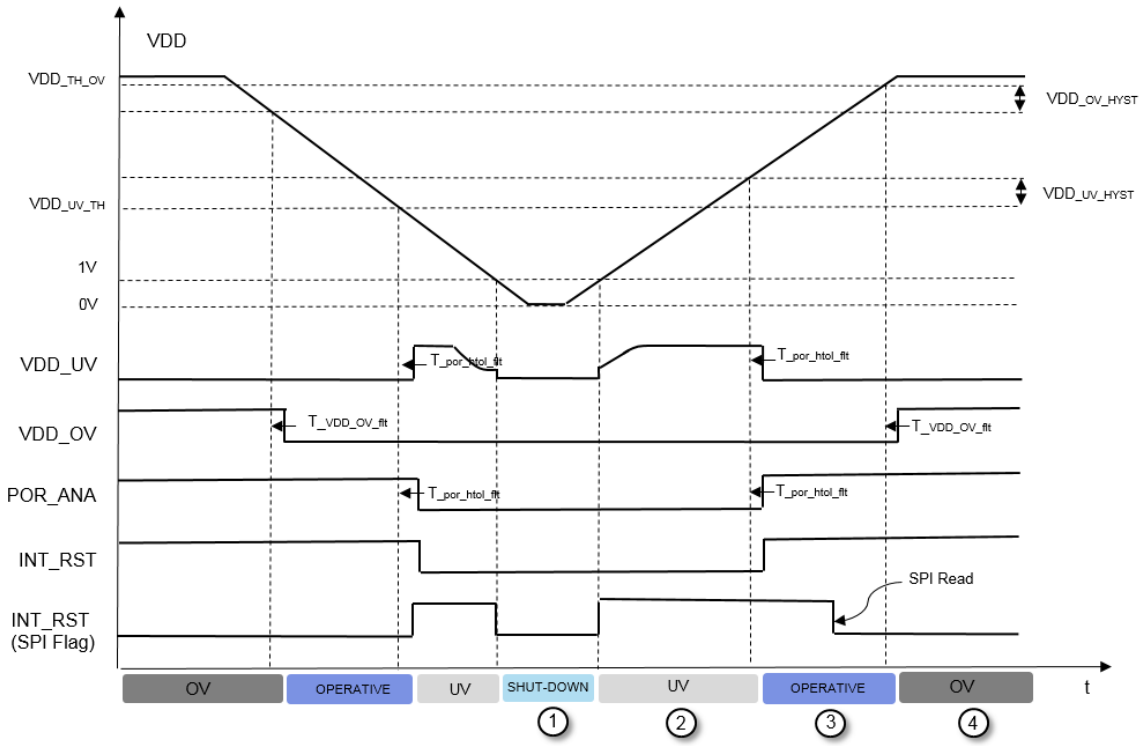
Note: All parameters are guaranteed and tested in the voltage ranges reported in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

Table 12. **VDD monitor electrical characteristics**

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD_uv_th	VDD under-voltage threshold	3.95	4.05	4.15	V	Comparator output Low to High
VDD_uv_hys	VDD under-voltage hysteresis	135	-	165	mV	
VDD_ov_th	VDD over-voltage threshold	5.5	-	6	V	Comparator output Low to High
VDD_ov_hys	VDD over-voltage hysteresis	120	170	220	mV	
T_vdd_ov_flt	VDD over-voltage detection filter time	1	-	5	µs	Digital filter

5.1.3.1 VDD functional ranges

Figure 9. **VDD functional ranges**



Where:

1. 0V ≤ VDD ≤ 1V

   L9908 is shut-down. Internal supply and reference voltage/currents levels are shutdown.

2. 1V ≤ VDD ≤ VDD_uv_th + VDD_uv_hyst

   VDD is in under-voltage and L9908 is sent into RESET mode. Internal supply and reference voltage/currents levels are degraded. Internal registers are under reset.

3. VDD_uv_th ≤ VDD ≤ VDD_ov_th

   Internal supply and reference voltage/currents are available. Internal registers are out of reset. (if no STD faults are detected and NDIS='1' the device is in NORMAL mode).

4. VDD_ov_th ≤ VDD

   VDD is in over-voltage and L9908 sent into safe state. The internal supply and reference voltage/currents are available. Internal registers are out of reset.

5.2 Internal resets (INT_RST, CFG_RST)

L9908 implements two different reset states following two different reset signals INT_RST and CFG_RST.

- INT_RST (active LOW) is the main internal reset signal; when active it resets the whole logic system.

  This signal is generated via the reset logic by supervising Internal Supply Monitor, VDD Monitor and ICM outputs: if a fault is verified the internal reset is activated.

  The internal INT_RST can be alternatively triggered through an activation key written into a dedicated SPI register SW_RESET_KEY.

Table 13. SW reset activation register

SW_RESET_KEY <7:0>	Description
0xCC	SW Reset Activation

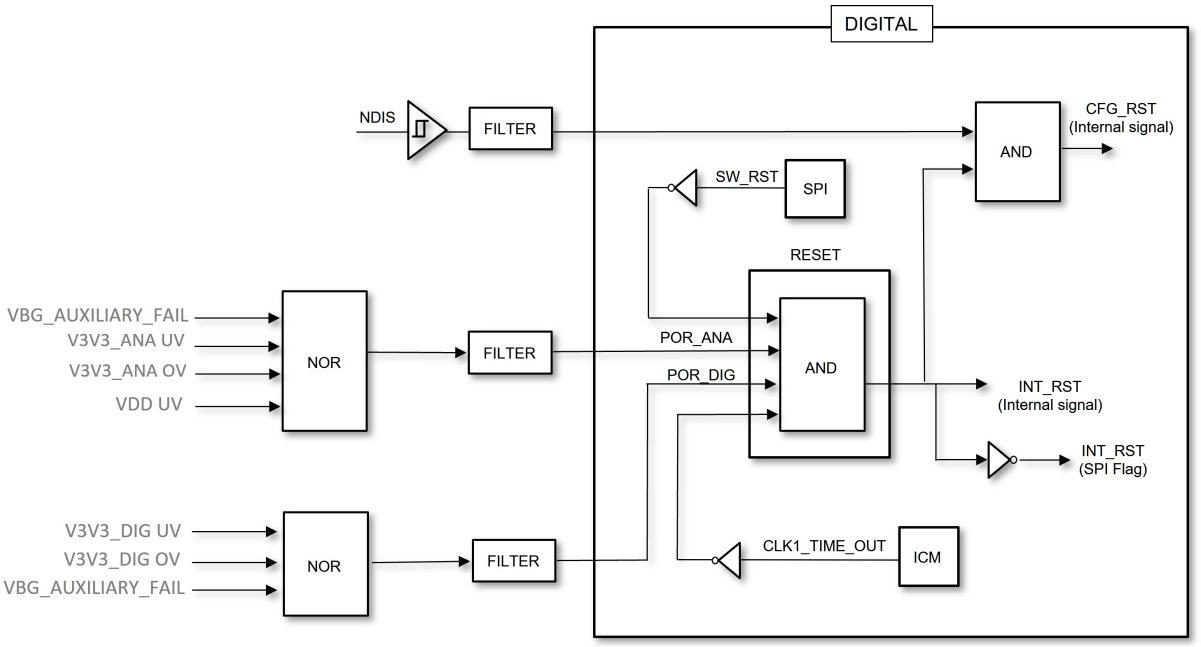
- CFG_RST (active LOW) is the reset signal configuration register.

  This signal is generated via the reset logic by supervising the NDIS pin status level: if a ‘0’ logic level is detected for a time interval greater than T_ndis_flt the reset is activated.

Table 14. Internal resets sources and filtering

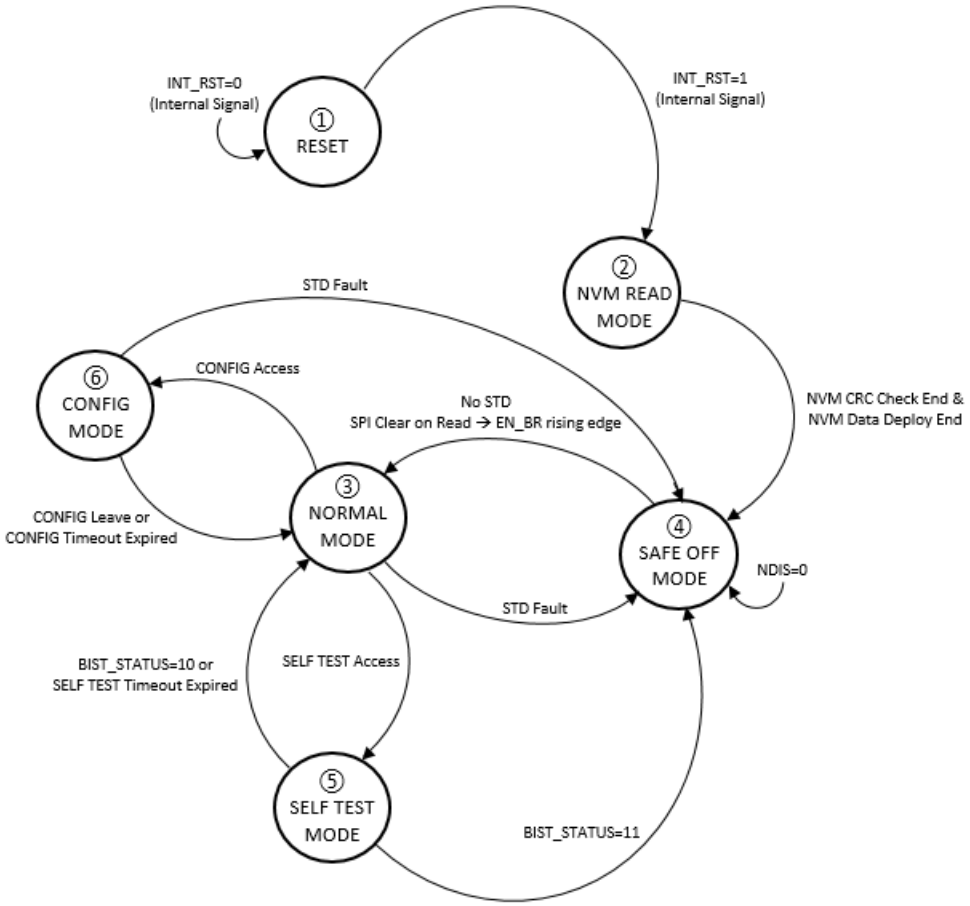
Condition	Action	Filter timer for Reset
NDIS=’0’	CFG_RST=0	T_ndis_flt
UV on V3V3_ANA	CFG_RST=0 INT_RST=0	T_por_ltoh_flt
UV on V3V3_DIG	CFG_RST=0 INT_RST=0	T_por_ltoh_flt
OV on V3V3_ANA	CFG_RST=0 INT_RST=0	T_por_ltoh_flt
OV on V3V3_DIG	CFG_RST=0 INT_RST=0	T_por_ltoh_flt
UV on BG MAIN	CFG_RST=0 INT_RST=0	T_por_ltoh_flt
UV on BG AUXILIARY	CFG_RST=0 INT_RST=0	T_por_ltoh_flt
UV on VDD	CFG_RST=0 INT_RST=0	T_por_ltoh_flt
CLK1 timeout (stuck)	CFG_RST=0 INT_RST=0	ICM Timeout
SW Reset SPI frame	CFG_RST=0 INT_RST=0	NA

Figure 10. **Internal reset logic simplified block diagram**



5.3 Device operation state machine

Figure 11. **Device operational state machine**



Where:

1. RESET MODE

   Internal supply and reference voltage/currents levels are degraded or shutdown. Main logic is under reset (INT_RST = ’0’, Internal signal). All functions are disabled:

   – Gate Driver Supply stage and Half Bridge Gate Drivers stage are shutdown (SAFE-HIZ)
   – Current Monitors chains and monitoring units are shutdown
   – SPI Read/Write operations are not available

   The device persists in this state as long as INT_RST=’0’ (Internal signal).

2. NVM READ MODE

   Internal supply and reference voltage/currents are available possibly exceeding spec parametrical ranges. Main logic is out of reset (INT_RST = ’1’, Internal signal). Main functions are disabled:

   – Gate Driver Supply stage disabled
   – Half Bridge Gate Drivers stages are in HIZ mode while LS Half Bridge Gate Drivers stages are shutdown (SAFE-HIZ)
   – Current Monitors chains and monitoring units are disabled
   – SPI Read is available while SPI Write is disabled

   In this mode a CRC check on NVM data is first performed:

   – If no CRC error is detected the NVM content is deployed into main logic register
   – If a CRC error is detected the related main logic registers are reset to default values (all ‘0’) and NVM_CRC_FAIL flag is set to ‘1’

Note: All parameters are guaranteed and tested in the voltage ranges reported in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

Table 15. Power up/down timings

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_nvm	NVM data deploy & CRC duration	-	-	2	ms	Not subject to production test

3. NORMAL MODE

   Internal supply and reference voltage/currents are available and within spec ranges. Main logic is out of reset (INT_RST = ’1’, Internal signal). Main functions:

   – Half Bridge Gate Drivers status depends on disable logic assessment (Functional or SAFE_DIS)
   – Gate Driver Supply stage status depends on configuration
   – Current Monitors chains and monitoring units status depend on configuration
   – SPI Read/Write operations are available

4. SAFE OFF MODE

   Internal supply and reference voltage/currents are available and within spec ranges. Main logic is out of reset (INT_RST = ’1’, Internal signal). Main functions:

   – Gate Driver Supply stage is disabled
   – HS and LS state are in SAFE_OFF or SAFE_HIZ depending on fault reaction as described in Table 17
   – Current Monitors chains and monitoring units status depend on configuration
   – SPI Read/Write operations are available

5. SELF TEST MODE

   Internal supply and reference voltage/currents are available and within spec ranges. Main logic is out of reset (INT_RST = ’1’, Internal signal). Main functions:

   – Gate Driver Supply stage depends on disable logic assessment
   – Half Bridge Gate Drivers are disabled (SAFE-DIS)
   – Current Monitors chains and monitoring units status depend on configuration
   – SPI Read is available while SPI Write is disabled

6. CONFIG MODE

   Internal supply and reference voltage/currents are available and within spec ranges. Main logic is out of reset (INT_RST = ’1’, Internal signal). Main functions:

   – Half Bridge Gate Drivers status depends on disable logic assessment (Functional or SAFE_DIS)
   – Gate Driver Supply stage status depends on configuration
   – Current Monitors chains and monitoring units status depend on configuration
   – SPI Read/Write operations are available

Three SPI readable flags are present to read-back the operational state machine status according to the following table:

Table 16. **Operation mode status bits**

OPERATION_MODE2	OPERATION_MODE1	OPERATION_MODE0	Description
0	0	0	RESET Mode
0	0	1	NVM Read Mode
0	1	0	SAFE OFF Mode
0	1	1	NORMAL Mode
1	0	0	CFG Mode
1	0	1	SELF TEST Mode
1	1	0	RESET Mode
1	1	1	RESET Mode

Table 17. **Device operation modes summary**

Operation Mode	Logic Core	Gate Driver Supply	HS/LS Pre-drivers	Current Monitors	Diagnosis	SPI Access
RESET	Reset	Disabled	SAFE_HIZ	Disabled	Disabled	Disabled
NVM READ	Functional	Disabled	SAFE_HIZ	Disabled	Disabled	Read
SELF TEST	Functional	As configured	SAFE_DIS	As configured	As configured	Read
SAFE OFF	Functional	Disabled	SAFE_OFF/ SAFE_HIZ	Disabled	As configured	Read/Write
CONFIG	Functional	As configured	Functional/SAFE_DIS	As configured	As configured	Read/Write
NORMAL	Functional	As configured	Functional/SAFE_DIS	As configured	As configured	Read/Write

5.4 Configuration mode

The L9908 default configuration can be modified by properly writing the SPI configuration registers.

Configuration registers are divided into three categories depending on their functional safety relevance:

- Safety Relevant Registers (SRR): the content of these registers is protected by a two-step LOCK mechanism: CONFIG mode access procedure and a masking related to Half Bridges status (EN_BR = 0 or HBn_DIS = 1 with n = 1, 2, 3). The content is then protected by a cyclic 5-bit CRC check.
- Safety Latent Registers (SLR): the content of these registers is protected by a one-step LOCK mechanism: CONFIG mode access procedure. The content has no CRC protection.
- Non-safety Registers (NSR): the content of these registers can be accessed directly in NORMAL Mode and has no CRC protection.

Correct SRR modification is safety relevant and then a CRC check on their bit is performed continuously by a dedicated state machine. CRC check is performed sequentially over the 11 bits content of shadow register, LSB first. The 5-bit CRC is calculated using the following polynomial expression over bit 5-15:

$$g(x) = x^5 + x^2 + 1 \quad (4)$$

The initial value to be used is 11111 (0x1F).

Example:

- Input word: [000.0000.0100] (0x004)
- Computed CRC: [0.1011] (0XB)
- Resulting frame: [0000.0000.1000.1011] (0X8B)

If a CRC violation on one or more SRR the SR_CRC_FAIL flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

5.4.1 Configuration mode activation

An accidental SRR and SLR change must be avoided therefore a finite state machine is implemented to access the CONFIG mode.

The CONFIG mode access state machine is composed by 2 sequential states, the passage from a state to the next one is carried out by the acknowledgment of a dedicated UNLOCK frames sequence to be written in the SPI register CFG_EN_UNLOCK (UNLOCK1 key: 0x55 → UNLOCK2 key: 0x33).

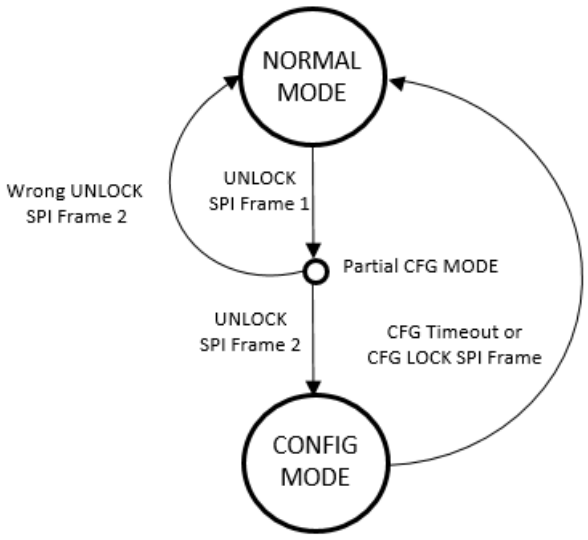
The correct completion of the CONFIG Mode procedure gives access to SLR. Access to SRR is further masked until EN_BR = 0 or HBn_DIS = 1 [n = 1, 2, 3].

Table 18. CONFIG mode activation register

CFG_EN_UNLOCK <7:0>	Description
0x55 → 0x33	CONFIG Mode Access
0xAA	CONFIG Mode Exit

Note:
- *SRR and SLR configuration will become effective the next clock cycle after the completed writing operation.*
- *Write attempts on SRR and SLR are ignored as long as the previous requirements aren`t met.*
- *Write attempts on Read Only (RO) registers are ignored, no matter if the register is NSR, SLR or SRR.*

Figure 12. CONFIG mode state machine



The configuration mode is left by a dedicated LOCK frame (LOCK key: 0xAA) to be written in the SPI register CFG_EN_UNLOCK, which confirms the written changes and locks them on writing. The configuration mode is also left automatically after the CONFIG mode time-out expiration: if no correct LOCK SPI frame is detected within T_cgf_time_out, the CONFIG mode is left.

Note: All parameters are guaranteed and tested in the voltage ranges reported in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

Table 19. CFG timeout

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_cgf_time_out	CFG Mode Time-out	-	100	-	ms	Not subject to production test

5.5 Self-test mode

A built-in self-test (BIST) procedure is implemented to check safety relevant circuitries both in digital core and in the analog monitor circuits on L9908.

The target of core logic self-test is to check the correct functionality of the Internal Clock Monitor.

The target of the analog monitor is to check the correct functionality of the comparators involved in the safety relevant monitors and of the Safety Switch Off path.

To allow a certain amount of freedom the block on which the self-test procedure runs can be configured by setting a dedicated SPI frame.

Note:
- *During Self-Test of the SW OFF path SAFE-OFF state is activated*
- *In case of BIST_STATUS = 11 (BIST check failure), the device is sent in SAFE_OFF Mode; re-engage procedure can be performed only by issuing a SW_RESET command*

Table 20. Self-test selection bits

SELF_TEST_CFG4	SELF_TEST_CFG3	SELF_TEST_CFG2	SELF_TEST_CFG1	SELF_TEST _CFG0	Description
OND LS	OND HS	Supply Monitors	SW OFF Path	Clock Monitor	
0	0	0	0	0	Self-Test Not Active
1	1	1	1	1	Self-Test Active (Defaults)

Note: Supply Monitors include: Internal Supply, VDD, VPRE, VCP, VBP, VDH and GLM.

Self-Test procedure is developed in different steps in the following order:
- Clock Monitor
- Supply Monitor & OND_LS & OND_HS
- SW OFF Path

5.5.1 Self-test activation

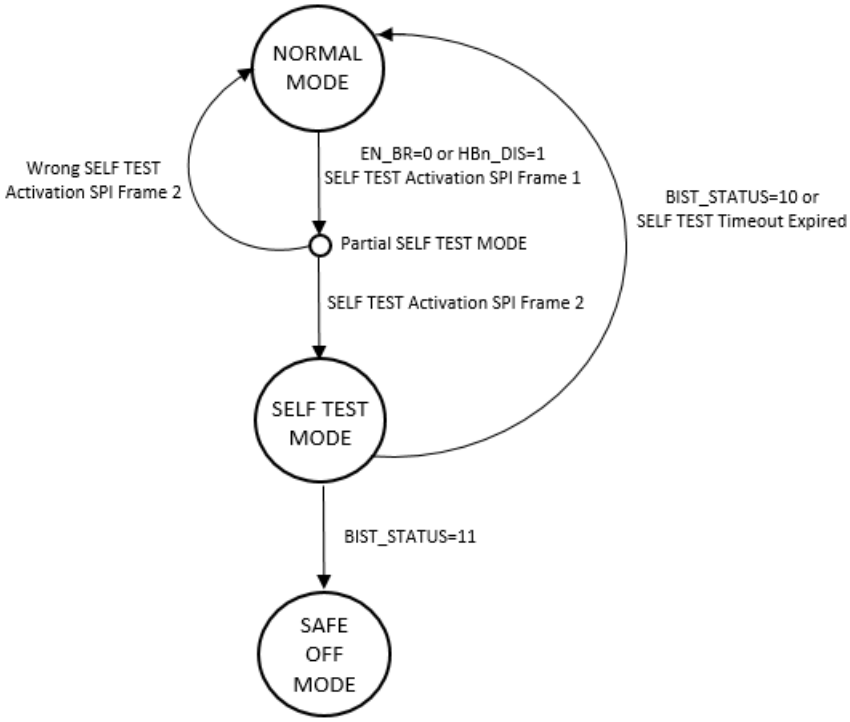
When Self-Test procedure is active, safety related analog and digital parts are under test, thus are not functional; this implies that Self-Test procedure can be activated only when no actuation is applied to half bridges: HBn_DIS = 1 [n = 1, 2, 3] or EN_BR = 0.

Accidental Self-Test procedure activation must be avoided therefore a finite state machine is implemented. The Self-Test activation state machine is composed by 2 sequential states, the passage from a state to the next one is carried out by a correct Self-Test activation SPI frame sequence to be written in the SPI register BIST_KEY (SELF-TEST1 key: 0x55 → SELF-TEST 2 key: 0x33).

Table 21. Self-test mode activation register

BIST_KEY <7:0>	Description
0x55à0x33	SELF TEST Mode Access

Figure 13. **Self-test mode state machine (NORMAL MODE)**



Note: Self-Test procedure shall be activated only when the L9908 is supplied within its Functional Operating Range otherwise the self-check may fail.

Two SPI readable flags are present in the register **GEN_STATUS1** to read-back the BIST state machine activation status according to the following table:

Table 22. **Self-test procedure status bits**

SELF_TEST_STATUS1	SELF_TEST _STATUS0	Description
0	0	SELF TEST stop
0	1	SELF TEST running
1	0	SELF TEST finished with NO Failure
1	1	SELF TEST finished with Failure

The self-test mode is left when procedure ends or after the Self-Test Time-out expiration: after accessing self-test mode a timeout is started, when the timeout expires, it is aborted.

Note: All parameters are guaranteed and tested in the voltage ranges reported in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

Table 23. **Self-test timings and timeout**

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_hwsc	Self-Test procedure duration	0.65	-	0.75	ms	Not subject to production test
T_selftest_time_out	SELF TEST Mode Time-out	0.77	0.88	0.99	ms	Not subject to production test

5.6 Fault Handling Management (FHM)

The fault set is divided into two main categories based on the required corrective actions:

- STD (Shutdown Faults): this set includes faults which are highly dangerous for the IC or the application and that needs a quick corrective action to avoid harming;
- WRN (Warnings): this set includes all those faults against which the application and the device are tolerant and the corrective action can be waived or delayed.

L9908 allows a certain degree of fault management customization a subset of available enabled faults can be configured by setting the proper FHC registers.

Table 24. Fault summary

Fault Flag	Source Diagnosis	Self-Check	Failure Reaction	Fault Description
INT_RST=1	Internal Supply Monitor	Yes	RESET	Under-voltage on V3V3_ANA
INT_RST=1	Internal Supply Monitor	Yes	RESET	Under-voltage on V3V3_DIG
INT_RST=1	Internal Supply Monitor	Yes	RESET	Over-voltage on V3V3_ANA
INT_RST=1	Internal Supply Monitor	Yes	RESET	Over-voltage on V3V3_DIG
INT_RST=1	VDD Monitor	Yes	RESET	Under-voltage on VDD
VDD_OV=1	VDD Monitor	Yes	SAFE-OFF	Over-voltage on VDD
INT_RST=1	ICM	Yes	RESET & SAFE_OFF	Main clock stuck violation
CLK1_ERR=1 CLK2_ERR=1 CLK2_TIME_OUT=1	ICM	No	Flag only (NORMAL)	Oscillators mismatch or auxiliary clock stuck violation
PGND_LOSS=1 AGND_LOSS=1 DGND_LOSS=1	GLM	Yes	Flag only (NORMAL)	Loss of power or signal grounds
OTM_SD=1	OTM	No	SAFE-OFF	Thermal shutdown
OTM_WR=1	OTM	No	Flag only (NORMAL)	Thermal warning
STDn_PWM =1 [n=1,2,3]	STD on PWM	No	Ignore overlapping PWM command	Shoot through on half bridge n (PWM input)
STDn_VGS =1 [n=1,2,3]	STD on VGS	No	Configurable	Shoot through on half bridge n (Ext. FET Vgs)
HSn_STG = 1 [n=1,2,3]	OND	Yes	Configurable	Short to ground on SHS_n
LSn_STB=1 [n=1,2,3]	OND	Yes	Configurable	Short to battery on SHS_n
HS2_OFD=1 LSn_OFD=0 [n=1,2,3]	OFD	Yes	Flag only (NORMAL)	Short to ground on one or multiple motor phase
HS2_OFD=0 LSn_OFD=1 [n=1,2,3]	OFD	Yes	Flag only (NORMAL)	Short to battery on one or multiple motor phase
HS2_OFD=0 LSn_OFD=011,101,100 [n=1,2,3]	OFD	Yes	Flag only (NORMAL)	Open connection on motor phase 1,2,3

Fault Flag	Source Diagnosis	Self-Check	Failure Reaction	Fault Description
VDH_UV=1	MBM	Yes	Configurable	Under-voltage at VDH pin
VDH_OV=1	MBM	Yes	Configurable	Over-voltage at VDH pin
VPRE_UV=1	VPRE Monitor	Yes	Auto-retry	Under-voltage at VPRE pin
VPRE_OV=1	VPRE Monitor	Yes	SAFE-OFF	Over-voltage at VPRE pin
VCP_UV=1	VCP Monitor	Yes	Flag only (NORMAL)	Under-voltage at CP2 output
VCP_OV=1	VCP Monitor	Yes	Flag only (NORMAL)	Over-voltage at CP2 output
VBP_UV=1	VBP Monitor	Yes	Configurable	Under-voltage at VBP pin
VBP_OV=1	VBP Monitor	Yes	Configurable	Over-voltage at VBP pin
WDT_DATA_fail=1	WDT	NA	SAFE-OFF	Watchdog reset failure
WDT_OVF_fail=1	WDT	NA	SAFE-OFF	Watchdog time-out failure
SPI_ERR=1	SPI CRC Check	NA	Ignore Frame	SPI CRC Check failure
SPI_ERR=1	SPI FC Check	NA	Ignore Frame	SPI FC Check failure
SPI_ERR=1	SPI Clock Counter Check	NA	Ignore Frame	SPI Clock Counter Check failure
NVM_CRC_FAIL=1	NVM Data CRC Check	NA	SAFE-OFF Load default values	NVM Data CRC Check
CFG_CRC_FAIL=1	SRR Data CRC Check	NA	SAFE-OFF	SRR Data CRC Check
BIST_STATUS=11	BIST	NA	SAFE-OFF	BIST Failure

5.6.1 FHC registers

The L9908 default FHM configuration can be modified by properly writing the FHC configuration registers through the CONFIG mode. FHC are considered as SRR.

5.6.1.1 Fault Reaction Configuration (FRC)

For each one of the fault listed in Table 24 two configuration bits allow to define whether the corrective action shall be automatically developed by the device itself or it can be waived.

Table 25. Fault Reaction Configuration bits

<FLT_REF>_REACT_CFG1	<FLT_REF>_REACT_CFG0	Description
0	0	Full SW Off – disable all HB drivers and CPs, device goes in SAFE-OFF mode (Default)(1)
0	1	Reduced Operation Mode – disable failing HB only, device remains in NORMAL mode(2)
1	0	Flag only – down-rate fault to simple warning, device remains in NORMAL mode(3)
1	1	Flag only – down-rate fault to simple warning, device remains in NORMAL mode(3)

1. *Fault danger for the application is considered high, the corrective action shall be taken as soon as it is detected by the device itself by disabling all half bridges and charge pumps.*
2. *Fault danger for the application is considered high, the corrective action shall be taken as soon as it is detected by the device itself by disabling only the half bridge on which the fault is present still allowing a reduced performance operation.*
3. *Fault danger for the application is considered low, the fault can be ignored with no corrective action applied nor internal or external.*

The following table details the Fault Reaction Configurations available for the different Fault events.

Table 26. Internal Managed Faults reaction details

Fault Flag	Device Fault	Half Bridge Fault	FRC Available
STD_VGS_n=1	-	X	(1)(2)(3)
HSn_STG = 1	-	X	(1)(2)(3)
LSn_STG=1	-	X	(1)(2)(3)
VDH_UV=1	X	-	(1)(3)
VDH_OV=1	X	-	(1)(3)
VBP_UV=1	X	-	(1)(3)
VBP_OV=1	X	-	(1)(3)

1. *Fault danger for the application is considered high, the corrective action shall be taken as soon as it is detected by the device itself by disabling all half bridges and charge pumps.*
2. *Fault danger for the application is considered high, the corrective action shall be taken as soon as it is detected by the device itself by disabling only the half bridge on which the fault is present still allowing a reduced performance operation.*
3. *Fault danger for the application is considered low, the fault can be ignored with no corrective action applied nor internal or external.*

Note:
- *While other configurations are available for all FHC faults the configuration 01 is available only on a limited subset. In Faults that don't support such a FRC the configuration 01 is reserved.*
- *For VDH_UV, VDH_OV, VBP_UV, VBP_OV and CFG_CRC_FAIL the configuration 01 has the same effect as configuration 10 and 11.*

5.6.1.2 *Fault Output Redirection (FOR)*

L9908 implements a double source of fault signaling by pin FS_FLAG and by a dedicated SPI field present in every frame.

FS_FLAG output can be configured in push-pull mode or in open-drain mode by means of the following SPI bit:

Table 27. Fault output redirection configuration bit

FS_FLAG_CFG	Description
0	Push-pull (Default)
1	Open-drain

The pin FS_FLAG is asserted LOW and the IC ERR flag is set to ‘1’ if a STD fault is detected which has been configured to be redirected externally via <FLT_REF>_REDIRECT_CFG.

The pin FS_FLAG is asserted HIGH and IC ERR flag is set to ‘10’ when the STD failure condition disappears.

Table 28. IC ERR status bits

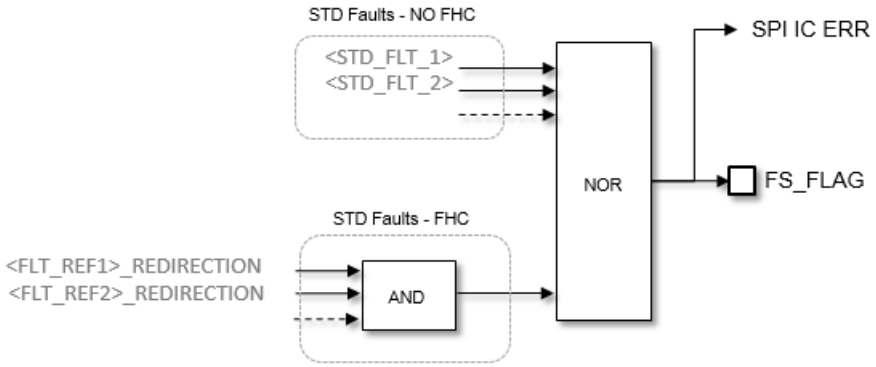
IC ERR1	IC ERR0	Description
0	0	NO STD Fault (Default)
0	1	NO STD Fault
1	0	NO STD Fault
1	1	STD Fault

In CONFIG mode a dedicated configuration bit is present for each one of the configurable reaction faults to mask output redirection as follows:

Table 29. **Fault output redirection configuration bit**

<FLT_REF>_REDIRECT_CFG	Description
0	Fault redirected on FS_FLAG/IC ERR (Default)
1	Fault redirection masked

Figure 14. **Fault output redirection logic simplified block diagram**



5.6.2 Fault reaction scenarios

Here below are described the scenarios of each different fault case separately.

In case multiple faults take place at the same time the following priority in reaction is used:

- STD fault
- Auto-retry
- Reduced operation mode
- WRN fault

5.6.2.1 Shutdown faults

When a shutdown fault is detected, the related SPI flag is set to ‘1’, the IC ERR bits in the SPI FRAME are set to ‘11’ and the FS_FLAG is asserted low.

Disable logic reacts by establishing SAFE_OFF mode: all the three half bridges are disabled, with VGHS_n-VSHS_n = 0 V and VGLS_n-VSLSn = 0V [n = 1, 2, 3]. Gate Drive Supply block is disabled (SPI configuration bit HBn_DIS, CP1_EN and CP2_EN remain set as previously configured).

The SAFE_OFF mode can be left when all the following conditions are met in the following sequence:

1. STD fault is removed;
2. STD fault flag is cleared on read (action required by Application SW);
3. EN_BR is asserted low for at least T_clear and then asserted back high (action required by Application SW).

Figure 15. **Shutdown fault - Transient fault timing diagram**

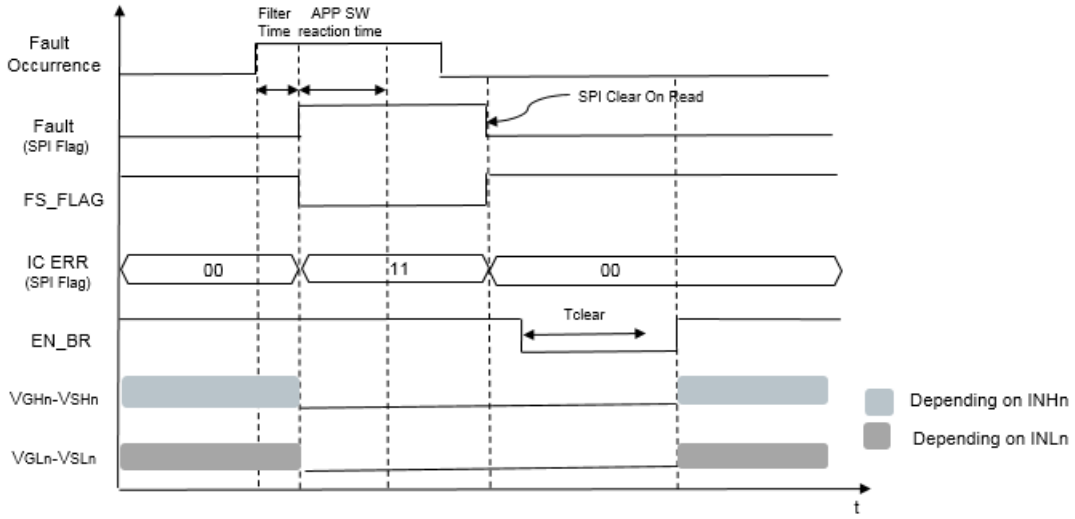


Figure 16. **Shutdown fault - Permanent fault timing diagram**

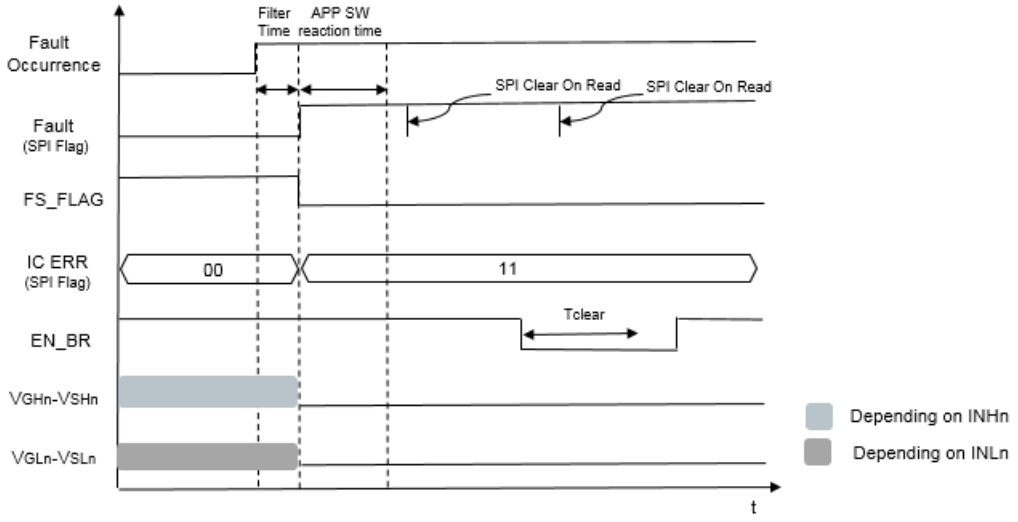


Table 30. **EN_BR minimum t_off time**

Symbol	Parameter	Min	Typ	Max	Unit	Notes
EN_BR_tclear	Minimum time interval to assert low value on EN_BR	2.5	-	-	µs	Not subject to production test

Note: All parameters are guaranteed, and tested, in the voltage ranges specified above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

Note:
- *In case of BIST_STATUS=11 (BIST check failure) the device sent in SAFE_OFF Mode, re-engage procedure can be performed only by issuing a SW_REST command.*
- *In case of WDT_OVF_fail = 1 or WDT_DATA_fail = 1 (WDT failure) the device sent in SAFE_OFF Mode, re-engage procedure can be performed only by issuing a WDT_RST or a SW_REST command.*

5.6.2.2 *Auto-retry faults*

When an auto-retry fault is detected the related SPI flag is set to ‘1’, the IC ERR bits in SPI FRAME are set to ‘11’ and the FS_FLAG is asserted low.

Disable logic reacts disabling all the three half bridges in a tristate mode so that VGHS_n-VSHS_n = 0 V and VGLS_n-VSLSn = 0 V [n = 1, 2, 3]. State machine remains in NORMAL mode (SPI configuration bit HBn_DIS remains set as previously configured).

Safe condition is left when all the following conditions are met in the following sequence:

1. Autoretry fault is removed;
2. Autoretry fault flag is cleared on read (action required by Application SW)
3. SPI bit HBn_ACK [n = 1,2,3] is set '0' and then set back to '1' (action required by Application SW).

Figure 17. Auto-retry faults - Transient fault timing diagram

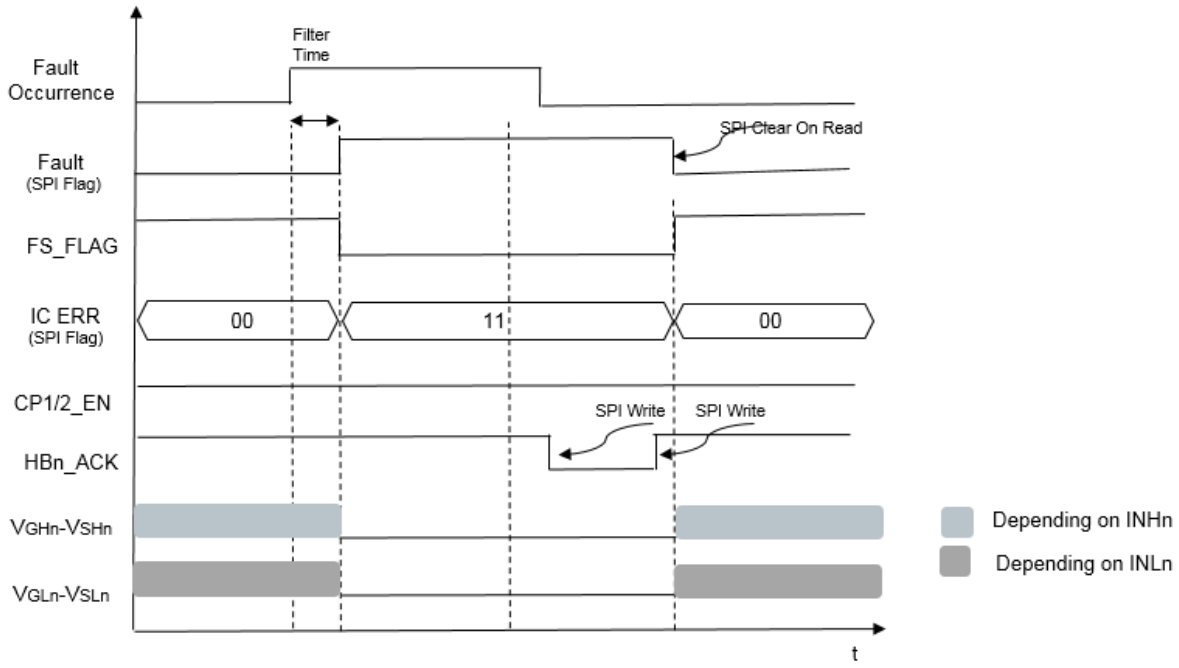
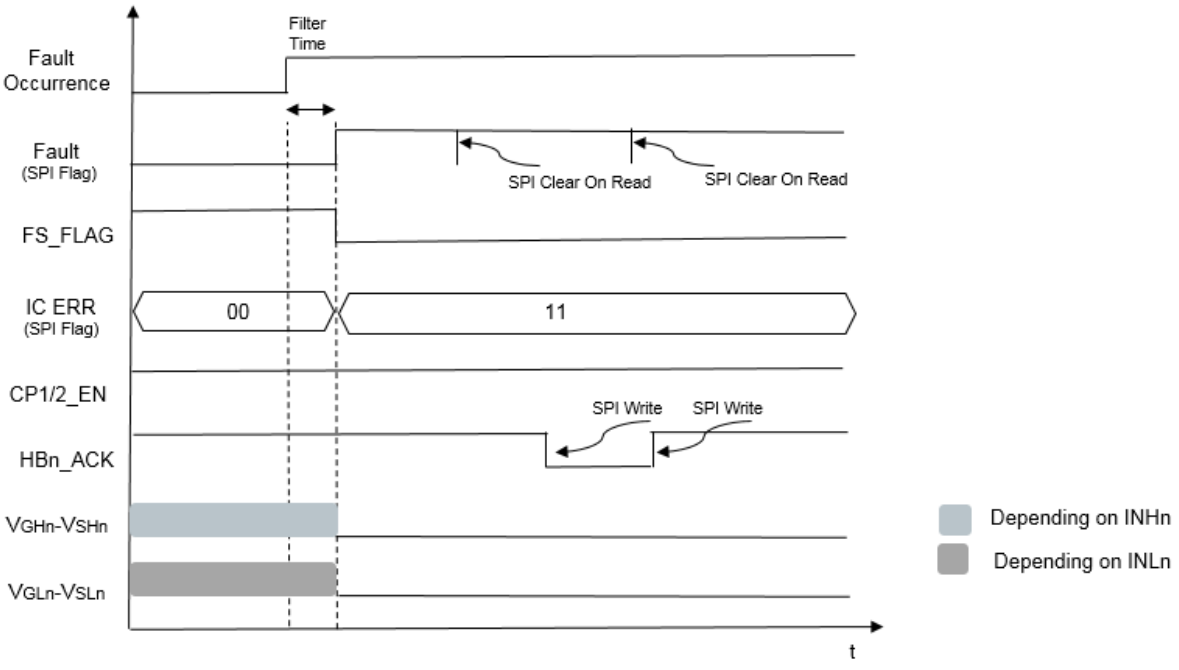


Figure 18. Auto-retry faults - Permanent fault timing diagram



5.6.2.3 *Reduced operation faults*

When a reduced operation fault is detected the related SPI flag is set to ‘1’, the IC ERR bits in SPI FRAME are set to ‘11’ and the FS_FLAG is asserted low.

Disable logic reacts forcing the failing half bridge only in a disable mode so that VGHS_n-VSHS_n = 0 V and VGLS_n-VSLSn = 0 V [n → failing HB] (SPI configuration bit HBn_DIS remains set as previously configured).

Safe condition is left when all the following conditions are met in the following sequence:

1. Reduced Operation fault is removed;
2. Reduced Operation fault flag is cleared on read (action required by Application SW);
3. SPI bit HBn_ACK [n = 1,2,3] is set ‘0’ and then set back to ‘1’ (action required by Application SW).

Note: Since HBn_ACK is a Safety Latent Register (SLR) it is required to access correctly the CONFIG MODE in order to conclude correctly the recovery flow.

Figure 19. Reduced operation fault - Transient fault timing diagram

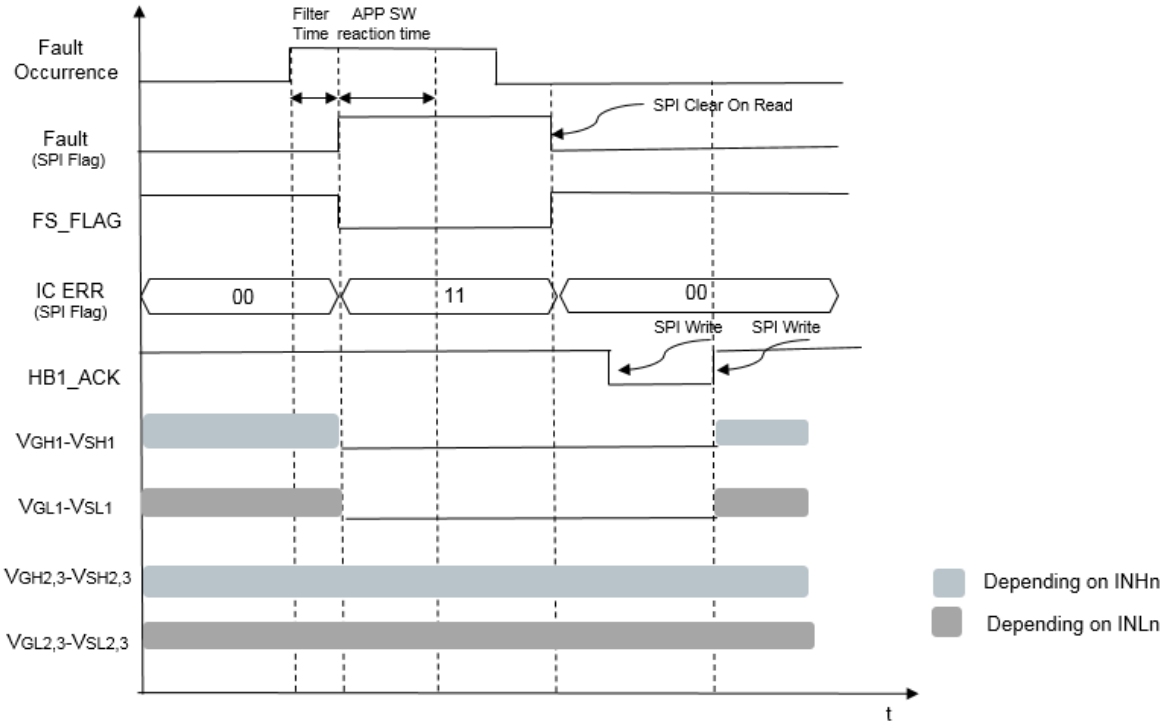
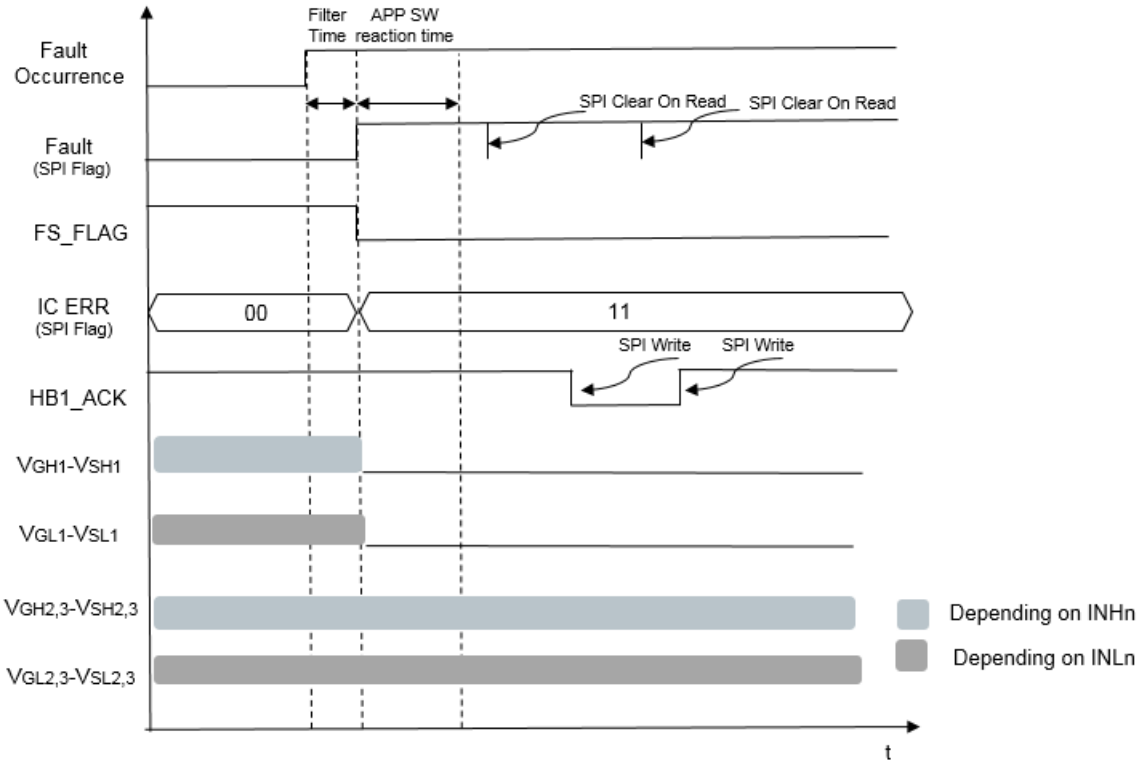


Figure 20. **Reduced operation fault - Permanent fault timing diagram**



5.6.2.4 *Warnings*

When a warning fault is detected the related SPI flag is set to ‘1’, the IC ERR bits in SPI FRAME are left to ‘00’ and the FS_FLAG is left asserted high.

Disable logic performs no corrective action (SPI configuration bit HBn_DIS remains set as previously configured).

Figure 21. **Warning - Transient fault timing diagram**

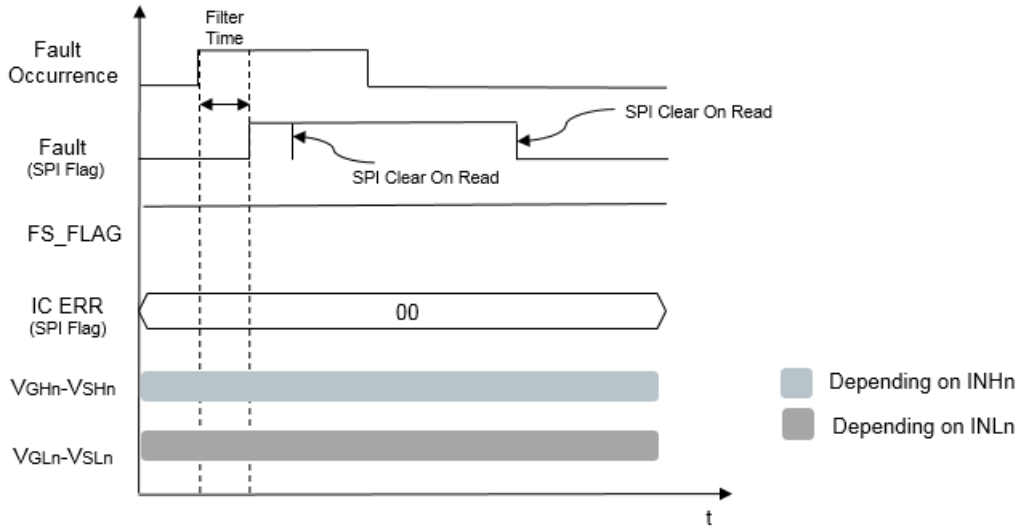
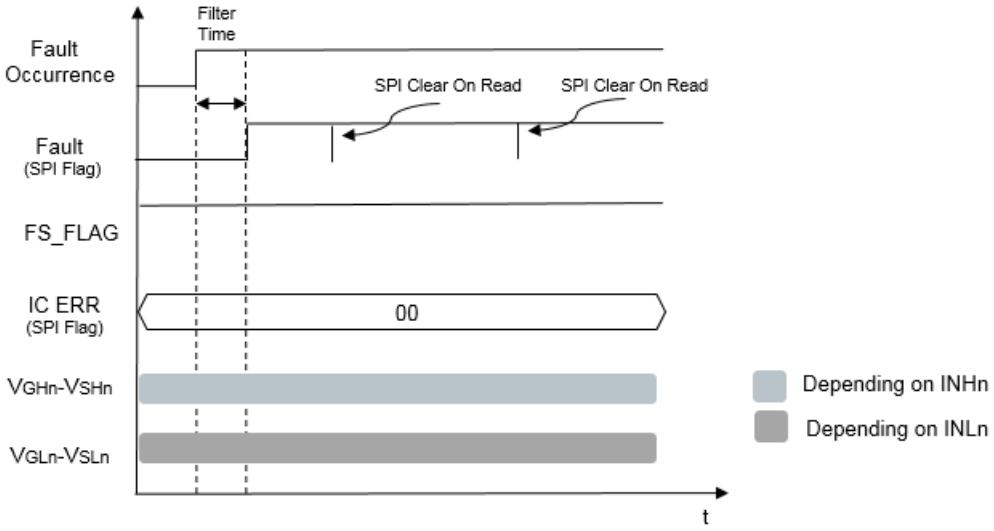


Figure 22. **Warning - Permanent fault timing diagram**



5.6.3 Half bridges disable logic

The enabling/disabling operation of the n-th Half Bridges is managed by a dedicated combinatory disable logic which constantly processes the following disable sources:

- HBn_DIS SPI configuration register status
- EN_BR pin status
- STD faults detection
- VPRE UV fault detection
- NDIS pin state
- Configurable reaction faults detection with related FRC set as 00 or 01

The status of the n-th disable n-th half bridge is echoed into dedicated SPI readable registers: HBn_EN_ECHO [n = 1, 2, 3].

5.6.4 Gate driver supply enable logic

The enabling/disabling operation of the Gate Driver supply unit (CP1 and CP2) is managed by a dedicated combinatory disable logic which constantly processes the following disable sources:

- **CP1_DIS** & **CP2_DIS SPI** bits status (within register **SAFETY_RELEVANT3**)
- STD faults detection
- NDIS pin status
- Configurable reaction faults detection with related FRC set as 00

The status of the n-th charge pump is echoed into dedicated SPI signals **CPn_EN_ECHO** [n = 1,2,3], within register **GEN_STATUS3**.

5.7 Power-Up sequences

The recommended power UP sequence should be aligned to the following flowchart.

Figure 23. Power-Up diagram

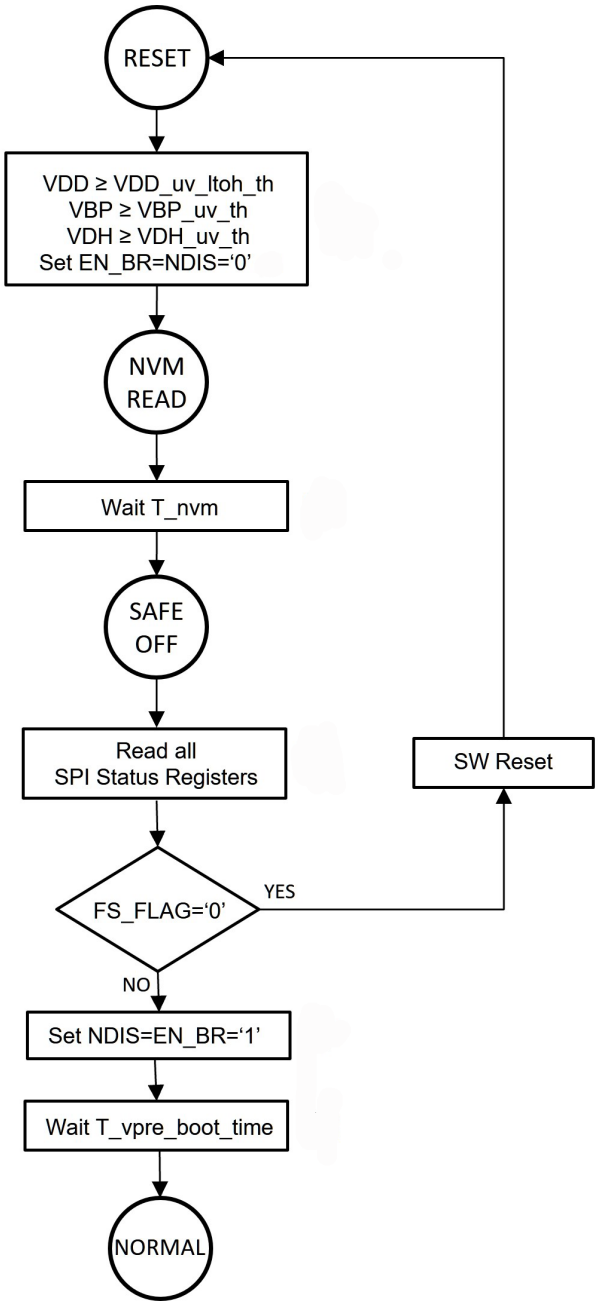
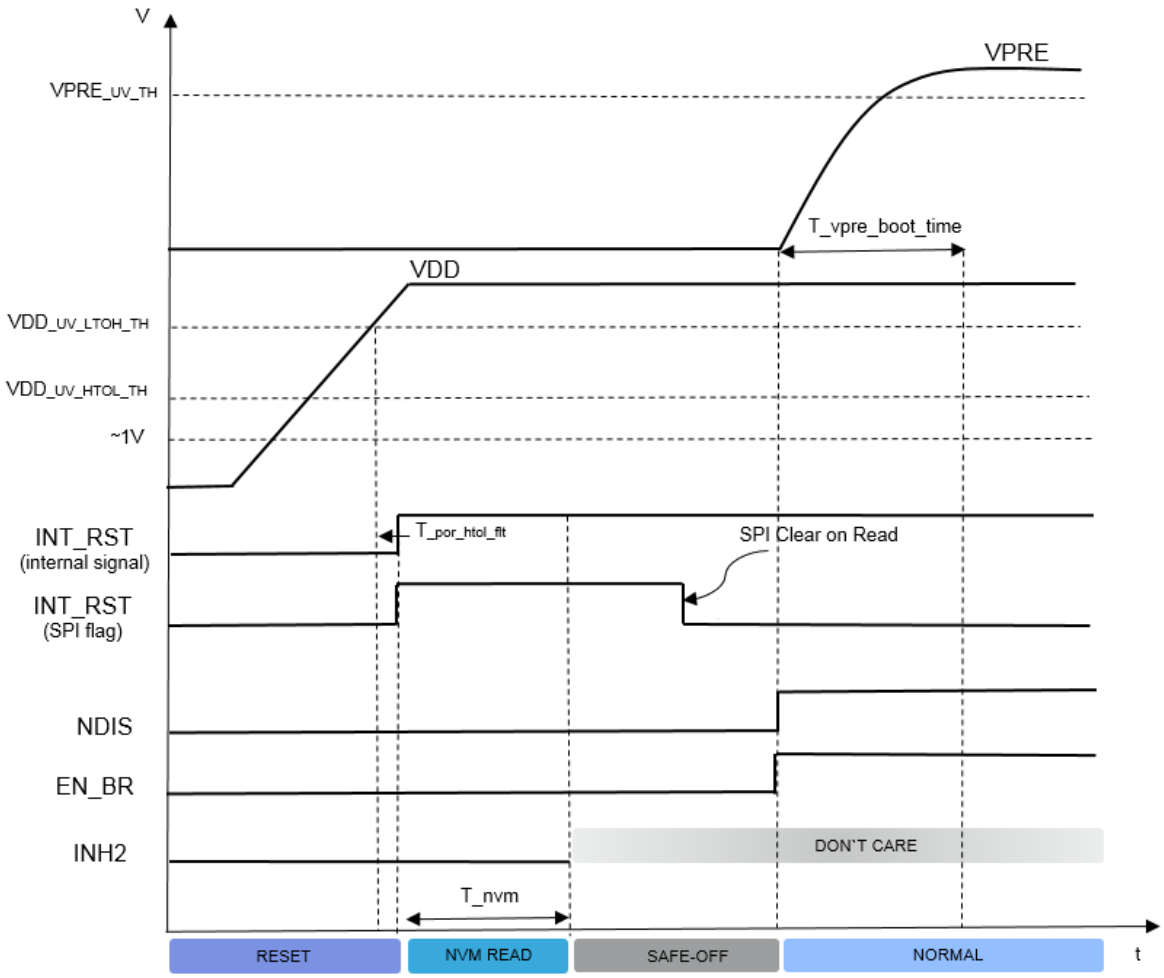


Figure 24. **Recommended Power-Up sequence**



5.8 Digital I/O

5.8.1 VIO power supply

The VIO power supply is a dedicated power input designed to supply the Digital Output circuitry. The voltage level applied to VIO will reflect directly onto digital output level allowing compliance with major digital I/O standards (5 V, 3.3 V).

5.8.2 Digital Input (DI)

Digital input pins on L9908 are used to transfer digital communications coming from an external source and supply domain to the internal logic and it's related to a 3.3 V domain.

Table 31. **Digital input pins functional partitioning**

Pins	Default State	Description
SCLK	Type A – Internal Current Pull-down	SPI Pin (SPI communication related pin)
SDI	Type A – Internal Current Pull-down	SPI Pin (SPI communication related pin)
NCS	Type C – Internal Current Pull-up	SPI Pin (SPI communication related pin)

Pins	Default State	Description
INHn, INLn [1,2,3]	Type A – Internal Current Pull-down	Control Loop Pins (Gate Driver control related pins)

Table 32. Digital input electrical characteristics (Control Loop Pins)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
DI_in_hl_th	High input voltage range	-	2.0	-	VIO+0.3	V	-
DI_in_ll_th	Low input voltage range	-	-0.3	-	0.65	V	-
DI_in_hys	Input voltage hysteresis	-	120	300	570	mV	-
SPI_DI_in_ipu	Pull up current	Pin = GND	15	40	65	µA	Type C
DI_in_ipd	Pull down current	Pin = VIO	-65	-40	-15	µA	Type A
DI_in_rpd	Pull down resistance	-	50	135	220	kΩ	Type B
DI_in_cap	Input capacitance	-	-	-	10	pF	Not subject to production test

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

The state of the PWM control pins INHn/INLn is echoed into dedicated SPI readable bits: **INHn_ECHO** and **INLn_ECHO** [n = 1, 2, 3], within the register **GEN_STATUS2**.

5.8.3 Digital Output (DO)

Digital output pins on L9908 are used to transfer an internal digital information to an external user whose domain is defined by the VIO voltage.

Depending on the information carried these pins can be divided into three categories:

Table 33. Digital output pins functional partitioning

Pins	Description
SDO	SPI Pin (SPI communication related pin)
CSO3/PVF	CSA phase 3 analog output/Phase voltage comparator output feedback
FS_FLAG	Fault Handling Pin (Fault flag output pin)

The digital output pin interface is developed by an HV push-pull output stage supplied by VIO and a driving stage supplied by the internal V3V3_DIG reference.

Table 34. Digital output electrical characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DO_in_hl	High output voltage	Iload = 1 mA	VIO-0.215	-	VIO	V
DO_in_ll	Low output voltage	Iload = -1 mA	0	-	0.2	V
T_do_rt	Output rise time	Cload = 120 pF From 10% to 70%	-	-	35	ns
T_do_ft	Output fall time	Cload = 120 pF From 10% to 70%	-	-	35	ns

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

5.9 Internal clock

Table 35. Internal clock electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
CLK_freq	System Clock Frequency	CLK_SSM_EN = 0	-	20	-	MHz
CLK_freq_acc	System Clock Frequency Accuracy	CLK_SSM_EN = 0	-5	-	+5	%

5.9.1 Spread Spectrum Modulation (SSM)

L9908 clocks generator implements a frequency modulation (Spread Spectrum Modulation) feature to reduce the main logic and Charge Pumps emissions around the main frequency by spreading the power spectrum over a larger frequency range.

Table 36. Clock spread spectrum electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
SSM_spreading	Spread Spectrum Modulation spreading range	1	3	5	%	Not subject to production test
SSM_freq	Spread Spectrum Modulating frequency	-	156.25		kHz	Not subject to production test

Note: All parameters are guaranteed and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

The clock spread spectrum modulation function can be enabled by the dedicated SPI bit **CLK_SSM_EN** in the register **GEN_CFG1** as follows:

Table 37. Clock spread spectrum enable bit

CLK_SSM_EN	Description
0	Clock SSM Disabled (Default)
1	Clock SSM Enabled

Note: When the clock spread spectrum is enabled the internal digital timings are affected by a timing jitter equal to the selected spread spectrum spreading range.

5.9.2 Internal Clock Monitor (ICM)

The correct operation and the precision of the internal synchronization signal are safety relevant and therefore L9908 implements a monitoring unit to detect abnormal deviation of the clock signal frequency. The monitoring unit is based on the use of two oscillators and two monitor chains (a Main one and an Auxiliary one) to avoid common-cause failures.

Each monitor chain compares the other clock period, the first one samples CLK1 by means of CLK2 and the second one samples CLK2 by means of CLK1.

If TCLK1 ≥ ICM_timeout_th: the flag INT_RST and CLK1_TIME_OUT are set.

If TCLK2 ≥ ICM_timeout_th: the flag CLK2_TIME_OUT is set.

The error flags remain set until the failure condition is removed and the flags are cleared by the SPI command. The correct level of clock monitor is safety relevant and then a self-check procedure is implemented on its monitor.

Table 38. Internal clock monitor electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
ICM_err_th	ICM frequency mismatch threshold accuracy	24	30	36	%	Application information
ICM_timeout_th	ICM timeout accuracy	30	50	70	us	Application information

Note: If no oscillator clock is available, the SPI data processing cannot work properly: L9908 delivers always the latest answer.

5.10 Motor Battery Monitor (MBM)

L9908 implements a monitoring unit on the voltage level of the motor`s battery through the pin VDH with the purpose of detecting over-voltage events that can harm the device and under-voltage events that can prevent a correct motor driving. Hysteresis on thresholds and filtering time are implemented.

If VDH ≤ VDH_uv_th occurs for an interval longer than T_vdh_uv_flt filtering time, VDH_UV flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

If VDH ≥ VDH_ov_th occurs for an interval longer than T_vdh_ov_flt filtering time, VDH_OV flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

The correct level of motor`s battery stage monitor is safety relevant and then a self-check procedure is implemented on its monitor.

The under-voltage thresholds VDH_uv_th can be configured by dedicated SPI bits as follows:

Table 39. Motor battery monitor UV threshold configuration bits

VDH_UV_CFG1	VDH_UV_CFG0	Description
0	0	12 V Systems (Defaults)
0	1	24 V Systems
1	0	48 V Systems
1	1	VDH UV Disabled

The over-voltage threshold VDH_ov_th can be configured by dedicated SPI bits as follows:

Table 40. Motor battery monitor OV threshold configuration bits

VDH_OV_CFG2	VDH_OV_CFG1	VDH_OV_CFG0	Description
0	0	0	12 V Systems 1
0	0	1	12 V Systems 2
0	1	0	24 V Systems 1
0	1	1	24 V Systems 2
1	0	0	48 V Systems 1
1	0	1	48 V Systems 2
1	1	0	48 V Systems 3
1	1	1	48 V Systems 4 (Defaults)

The filter time on under/over voltage diagnosis T_vdh_uv_flt/ T_vdh_ov_flt can be configured by dedicated SPI bits as follows:

Table 41. Motor battery monitor filtering configuration bits

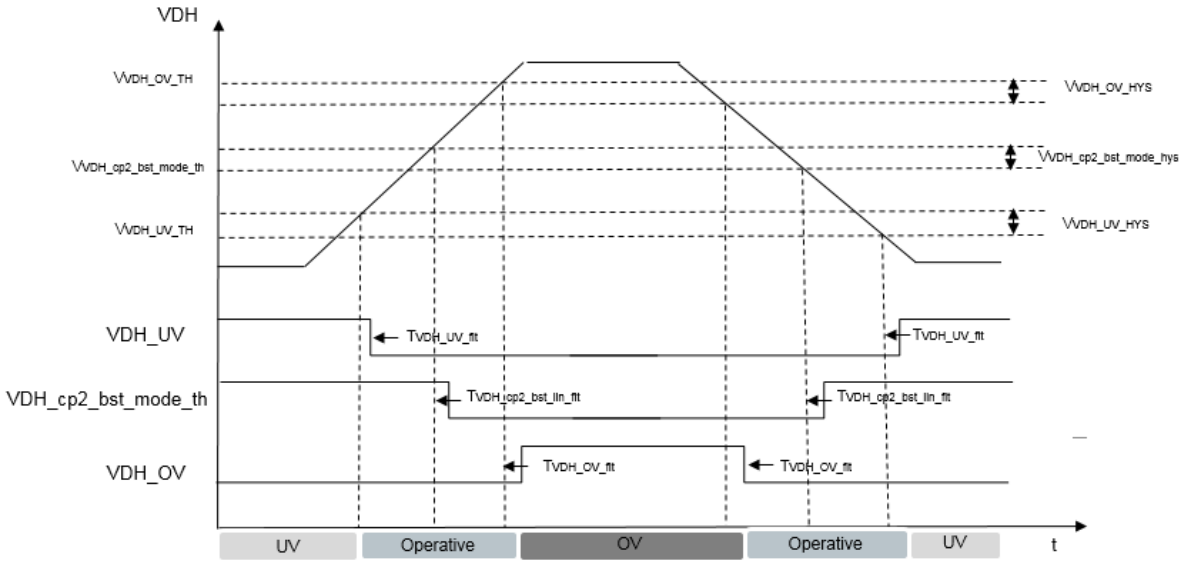
VDH_FLT_CFG1	VDH_FLT_CFG0	Description
0	0	12.25 µs (Defaults)
0	1	25 µs
1	0	50 µs
1	1	100 µs

Table 42. Motor battery monitor electrical characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
VDH_cp2_bst_mode_th	CP2 boost mode enable threshold	-	10.3	10.6	10.9	V	Comparator output Low to High
VDH_cp2_bst_mode_hys	CP2 boost mode enable hysteresis	-	0.95	1.05	1.1	V	-
VDH_cp2_bst_mode_flt	CP2 boost mode enable detection filter time	-	100	200	300	ns	Analog Filter
VDH_uv_th_12v	VDH under-voltage threshold (12 V systems)	-	4	4.25	4.5	V	Comparator output Low to High
VDH_uv_th_24v	VDH under-voltage threshold (24 V systems)	-	7.8	8.4	9	V	Comparator output Low to High
VDH_uv_th_48v	VDH under-voltage threshold (48 V systems)	-	17.3	18.65	20	V	Comparator output Low to High
VDH_uv_hys	VDH under-voltage hysteresis	-	90	150	250	mV	-
VDH_ov_th1_12v	VDH over-voltage threshold (12 V systems 1)	-	18.11	18.67	19.23	V	Comparator output Low to High
V_ov_th2_12v	VDH over-voltage threshold (12 V systems 2)	-	27.16	28	28.84	V	Comparator output Low to High
VDH_ov_th1_24v	VDH over-voltage threshold (24 V systems 1)	-	36.22	37.34	38.46	V	Comparator output Low to High
VDH_ov_th2_24v	VDH over-voltage threshold (24 V systems 2)	-	50.3	51.86	53.41	V	Comparator output Low to High
VDH_ov_th1_48v	VDH over-voltage threshold (48 V systems 1)	-	56.34	58.08	59.82	V	Comparator output Low to High
VDH_ov_th2_48v	VDH over-voltage threshold (48 V systems 2)	-	60.36	62.23	64.09	V	Comparator output Low to High
VDH_ov_th3_48v	VDH over-voltage threshold (48 V systems 3)	-	65.39	67.41	69.43	V	Comparator output Low to High
VDH_ov_th4_48v	VDH over-voltage threshold (48 V systems 4)	-	70.42	72.6	74.78	V	Comparator output Low to High
VDH_ov_hys	VDH over-voltage hysteresis	-	0.8	1.15	1.85	V	-
VDH_tflt_acc	VDH Fault Detection Filter Time accuracy	CLK_SSM_EN = 0	-15	-	15	%	-

Note: All parameters are guaranteed and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

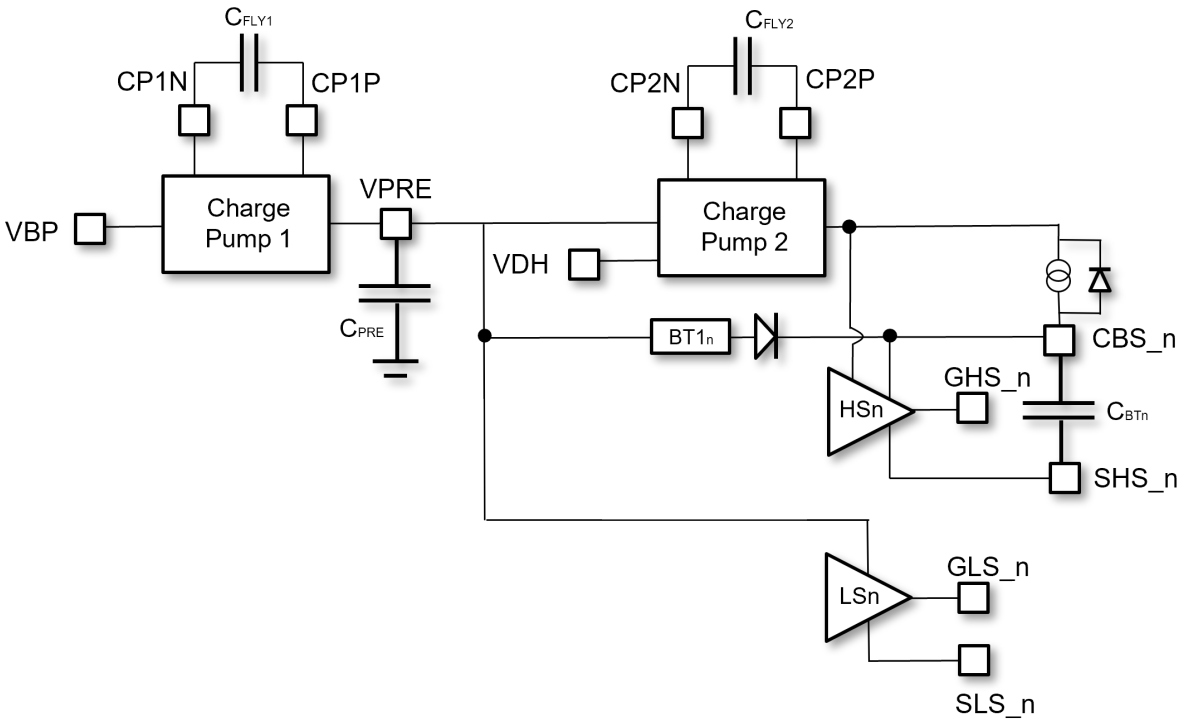
Figure 25. **VDH operative range**



5.11 Gate driver supply

The Ext. FET gate drivers supply on L9908 is developed by the cascaded connection of a pre-regulation stage and a supply distribution stage.

Figure 26. **Ext. FET gate supply simplified block diagram**



5.11.1 Pre-regulation stage

The pre-regulator stage has the purpose to generate an intermediate supply rail to be used as a reference level for the Ext. FET ON driving. This function is carried out by a current-limited Single Stage 2-Phases Dickson charge pump with external capacitance.

Charge Pump1 can be disabled by the dedicated SPI bit **CP1_DIS** within the **SAFETY_RELEVANT3** register, as follows:

Table 43. Charge pump 1 enable bit

CP1_DIS	Description
0	Charge Pump 1 Enabled (Default)
1	Charge Pump 1 Disabled

Table 44. Pre-regulation stage electrical characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
CP1_iout1	Charge Pump1 external Load Current for no VPRE_UV	5.5 V ≤ VBP < 8 V CFLY1 = 1 µF CPRE = 4.7 µF	-	-	40	mA	-
CP1_iout2	Charge Pump1 external Load Current for no VPRE_UV	8 V ≤ VBP CFLY1 = 1 µF CPRE = 4.7 µF	-	-	55	mA	-
CP1_vout1	Charge Pump1 Output Voltage	4.5 V ≤ VB = < 5.5 V Iload ≤24 mA CFLY1 = 1 µF CPRE = 4.7 µF	5.8	-	13	V	(1)
CP1_vout2	Charge Pump1 Output Voltage	5.5 V ≤ VBP < 11 V Iload = 24 mA CFLY1 = 1 µF CPRE = 4.7 µF	8	-	13	V	(1)
CP1_vout3	Charge Pump1 Output Voltage	11 V ≤ VBP Iload = 36 mA CFLY1 = 1 µF CPRE = 4.7 µF	11	12	13	V	(1)
CP1_freq	Charge Pump1 Frequency	-	180	200	220	kHz	Not subject to production test
VPRE_boot_time	VPRE boot time at high battery (VBP & VDH > 10 V)	Iload ≤ 0 mA CFLY1 = 1 µF CPRE = 4.7 µF 0 V ≤ VPRE ≤ 7 V	0.2	-	0.5	ms	-
VPRE_boot_time	VPRE boot time at low battery (VBP & VDH < 10 V)	Iload ≤ 0 mA CFLY1 = 1 µF CPRE = 4.7 µF 0 V ≤ VPRE ≤ 7 V	0.5	-	1	ms	-

1. *Iload is the total external current out sink form VPRE equivalent to a gate charge load: Iload = (# of switching FETs) * fPWM * QgTOT.*

Note: All parameters are guaranteed and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

5.11.2 VBP monitor

VBP voltage level is monitored be means of the dedicated UV and OV diagnosis. Hysteresis on thresholds and filtering time is implemented.

If VBP ≤ VBP_uv_th occurs for an interval longer than T_vbp_uv_flt filtering time, the VBP_UV flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

If VBP ≥ VBP_ov_th occurs for an interval longer than T_vbp_ov_flt filtering time, the VBP_OV flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

The correct operation VBP Level monitor is safety relevant and then a self-check procedure is implemented.

The under-voltage threshold VBP_uv_th can be configured by dedicated SPI bits within the **SAFETY_RELEVANT3** register as follows:

Table 45. VBP monitor UV threshold configuration bits

VBP_UV_CFG1	VBP_UV_CFG0	Description
0	0	12 V Systems (Defaults)
0	1	24 V Systems
1	0	48 V Systems
1	1	VBP UV Disabled

The over-voltage threshold VBP_ov_th can be configured by dedicated SPI bits within the **SAFETY_RELEVANT2** register as follows:

Table 46. VBP monitor OV threshold configuration bits

VBP_OV_CFG1	VBP_OV_CFG0	Description
0	0	12 V Systems 1
0	1	12 V Systems 2
1	0	24 V Systems 1
1	1	24 V Systems 2 (Defaults)

The filter time on under/over voltage diagnosis T_vbp_uv_flt/ T_vbp_ov_flt can be configured by dedicated SPI bits within the **SAFETY_RELEVANT3** register as follows:

Table 47. VBP monitor filtering configuration bits

VBP_FLT_CFG1	VBP_FLT_CFG0	Description
0	0	12.25 µs (Defaults)
0	1	25 µs
1	0	50 µs
1	1	100 µs

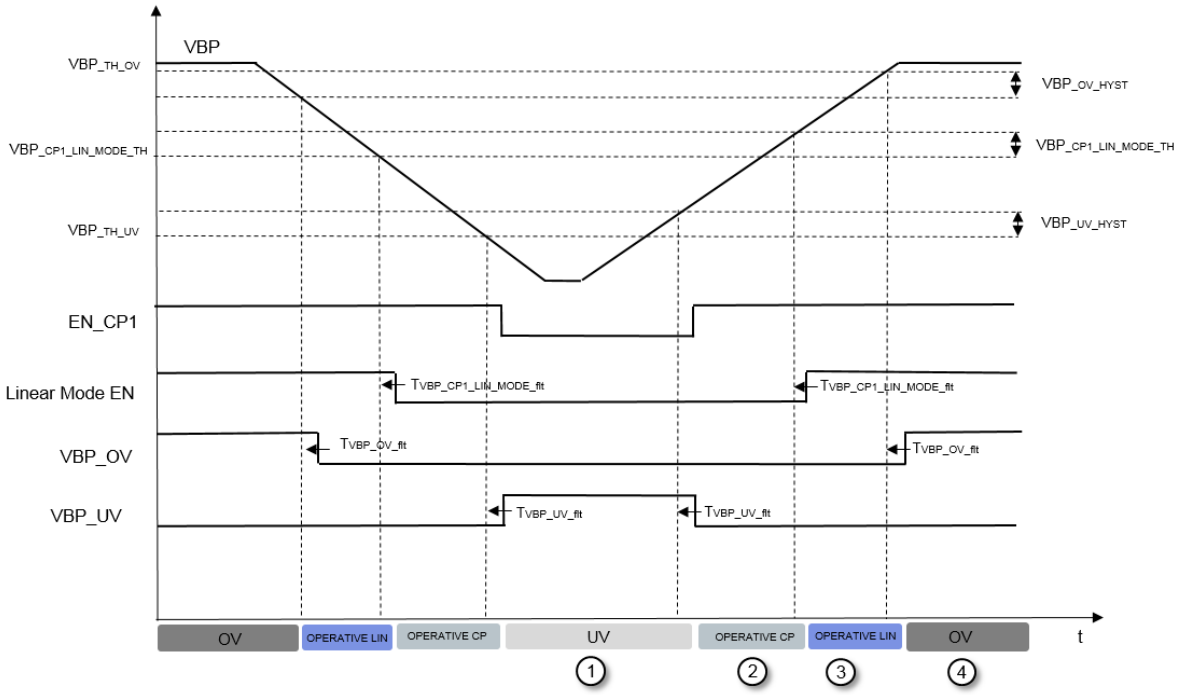
Table 48. VBP monitor electrical characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
VBP_cp1_lin_mode_th	CP1 linear mode enable threshold	-	10.3	10.6	10.9	V	Comparator output Low to High
VBP_cp1_lin_mode_hys	CP1 linear mode enable hysteresis	-	0.95	1.05	1.1	V	-
VBP_cp1_lin_mode_flt	CP1 linear mode enable detection filter time	-	100	200	300	ns	Digital filter
VBP_uv_th_12v	VBP under-voltage threshold (12 V systems)	-	4	4.25	4.5	V	Comparator output Low to High
VBP_uv_th_24v	VBP under-voltage threshold (24 V systems)	-	7.8	8.4	9	V	Comparator output Low to High
VBP_uv_th_48v	VBP under-voltage threshold (48 V systems)	-	17.3	18.65	20	V	Comparator output Low to High
VBP_uv_hys	VBP under-voltage hysteresis	-	90	150	250	mV	-
VBP_ov_th1_12v	VBP over-voltage threshold (12 V systems 1)	-	18.11	18.67	19.23	V	Comparator output Low to High
VBP_ov_th2_12v	VBP over r-voltage threshold (12 V systems 2)	-	27.16	28	28.84	V	Comparator output Low to High
VBP_ov_th1_24v	VBP over-voltage threshold (24 V systems 1)	-	36.22	37.34	38.46	V	Comparator output Low to High
VBP_ov_th2_24v	VBP over-voltage threshold (24 V systems 2)	-	50.3	51.86	53.41	V	Comparator output Low to High
VBP_ov_hys	VBP over-voltage hysteresis	-	0.8	1.15	1.6	V	-
VBP_tflt_acc	VBP Fault Detection Filter Time accuracy	CLK_SSM_EN = 0	-15	-	15	%	Digital filter

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

5.11.2.1 *VBP functional ranges*

Figure 27. **VBP functional ranges**



Where:

1. VBP ≤ VBP_uv _th

   VBP is in under-voltage and L9908 is sent into the operating mode defined into the FMC registers. If set as IMF a VBP UV event automatically sets CP1_EN = 0 bit, thus disabling the CP1 stage. If set to EMF, protection mechanism is let to µC.

2. VBP_uv_th ≤ VBP ≤ VBP_cp1_lin_mode_th

   L9908 is in NORMAL Mode (operative), CP1 regulates the target voltage on VPRE by working in charge pump mode.

3. VBP_cp1_lin_mode_th ≤ VBP ≤ VBP_ov_th

   L9908 is in NORMAL Mode (operative), CP1 regulates the target voltage on VPRE by working in linear regulator mode.

4. VBP ≥ VBP_ov_th

   VBP is in over-voltage and L9908 is sent into the operating mode defined into FMC registers.

5.11.3 VPRE monitor

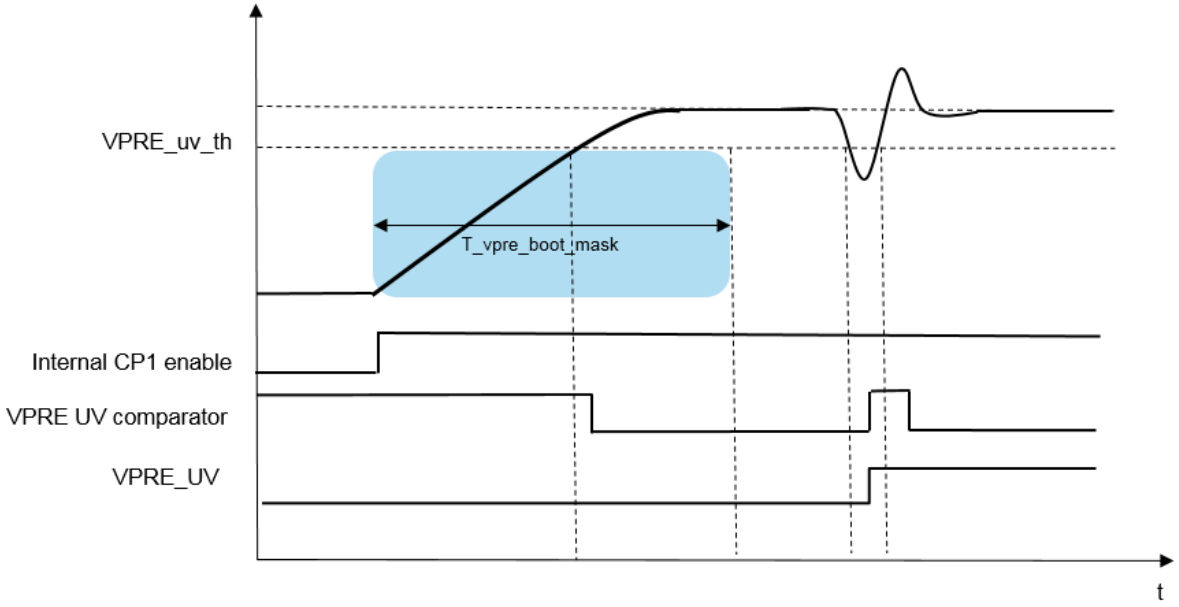
VPRE voltage level is monitored by means of dedicated UV and an OV diagnosis. Hysteresis on thresholds and filtering time is implemented.

If VPRE ≤ VPRE_uv_th occurs for an interval longer than T_vpre_uv_flt filtering time, the VPRE_UV flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

If VPRE ≥ VPRE_ov_th occurs for an interval longer than T_vpre_ov_flt the VPRE_OV flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command. The correct operation Pre-Regulator stage monitor is safety relevant and then a self-check procedure is implemented.

To avoid UV/OV detection during power up phase VPRE monitor comparators are masked for a T_vpre_boot_mask filtering time, starting from each low to high transition of the internal CP1 enabling command.

Figure 28. **VPRE monitor boot masking**



Note: The total external capacitance applied to VPRE should be selected in order to allow a VPRE boot time always lower than VPRE boot time masking. This means that the maximum total capacitance shall be:

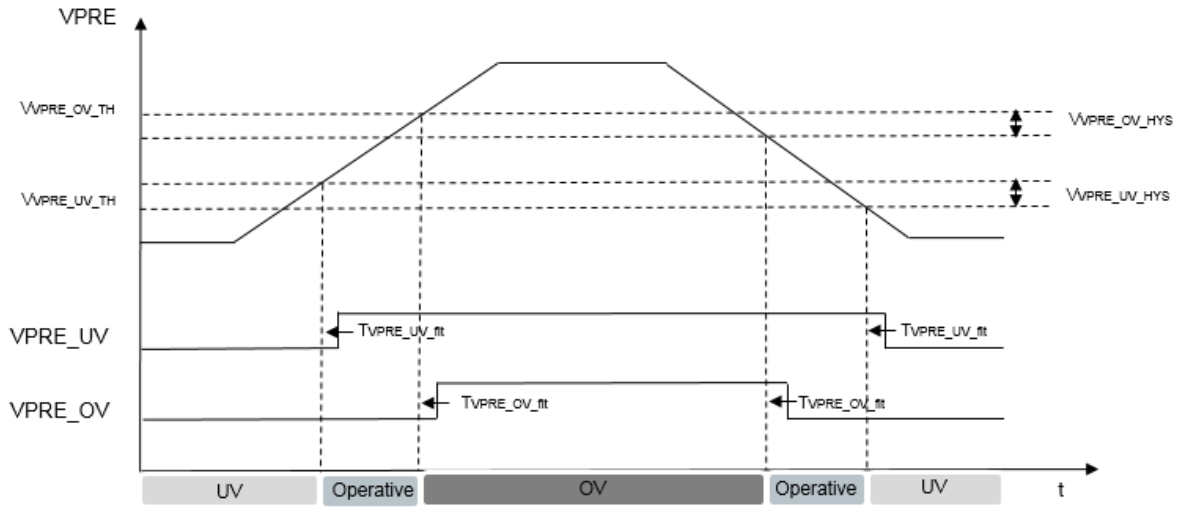
$$C_{VPRE\_tot} \leq \frac{CP1_{iout\_\min}}{CP1_{vout\_\max}} T_{vpre\_boot\_mask\_\min} = 7.192\,\mu F \quad (5)$$

Table 49. **VPRE Monitor electrical characteristics**

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VPRE_uv_th	VPRE under-voltage threshold	6.4	6.7	7	V	Comparator output Low to High
VPRE_uv_hys	VPRE under-voltage hysteresis	100	-	200	mV	-
T_vpre_uv_flt	VPRE under-voltage detection filter time	1	-	5	µs	Digital filter
VPRE_ov_th	VPRE over-voltage threshold	14.5	15.5	16.5	V	Comparator output Low to High
VPRE_ov_hys	VPRE over-voltage hysteresis	100	-	250	mV	-
T_vpre_ov_flt	VPRE over-voltage detection filter time	1	-	5	µs	Digital filter
T_vpre_boot_mask	VPRE boot masking time	1.7	2	2.3	ms	-

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

Figure 29. **VPRE operative ranges**



5.11.4 Supply distribution stage

The supply distribution stage has the purpose to properly deliver the pre-regulated supply to LS and HS driver.

- LS drivers are directly supplied by the VPRE voltage itself as it is referenced to GND and already conditioned to fit the Ext. FET Vgs range for a correct driving. Supply distribution stage is then absent for LS drivers.
- HS drivers cannot use directly VPRE voltage as they need this voltage to be translated above VDH for a correct Ext. FET driving. Supply distribution stage for each HS driver is then composed by the cooperation of bootstrap circuits and a dedicated Single Stage 2-Phases Dickson charge pump with external capacitance.

Charge Pump 2 (CP2) and Bootstrap Limiter 2 (BT2)

The purpose of CP2 is to guarantee a stable Vgs on HS FET during 100% (full-on) operations and to support the bootstrap supply in “high” duty cycle PWM mode by recovering the static consumption of the three HS pre-drivers in ON condition.

To carry out this function CP2 structure generates a VDH+VPRE voltage onto the internal line VCP by means of a current-limited Single Stage 2-Phases Dickson charge pump with external capacitance (the tank capacitance function of this stage is developed by the bootstrap capacitance itself).

When VDH < VDH_cp2_bst_mode_th the CP2 will use VPRE as input in both phases, resulting in an output voltage equal to 2*VPRE.

Charge Pump2 can be Disabled by a dedicated SPI bit **CP2_DIS** within the register **SAFETY_RELEVANT3** as follows:

Table 50. **Charge pump 2 enable bit**

CP2_DIS	Description
0	Charge Pump 2 Enabled (Default)
1	Charge Pump 2 Disabled

Table 51. **Charge pump 2 electrical characteristics**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
CP2_iout1	Total Charge Pump2 Load Current	5.5 V ≤ VBP ≤ CP1_lin_mode_th CFLY2 = 1 µF SHS_n = VDH INHn = 1	-	-	10	mA	[n = 1,2,3]

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
CP2_iout2	Charge Pump2 Load Current	CP1_lin_mode_th < VBP ≤ 60 V CFLY2 = 1 µF SHS_n = VDH INHn = 1	-	-	10	mA	[n = 1,2,3]
CP2_vout1	Charge Pump2 output voltage at CBS_n-SHS-n	5.5 V ≤ VBP ≤ CP1_lin_mode_th CFLY2 = 1 µF SHS_n = VDH INHn = 1	8	-	-	V	[n = 1,2,3]
CP2_vout2	Charge Pump2 output voltage at CBS_n-SHS-n	CP1_lin_mode_th < VBP ≤ 60 V CFLY2 = 1 µF SHS_n = VDH INHn = 1	8	-	-	V	[n = 1,2,3]
CP2_freq	Charge Pump2 Frequency	-	-	400	-	kHz	Not subject to production test
BT_lim2_ilim	BT Charge Limiter2 limitation current	SHS_n = VDH INHn = 1	-8	-	-1	mA	[n = 1,2,3]
BT_lim2_vlim	BT Charge Limiter2 limitation voltage	SHS_n = 0 BT1_DIS = 1	7	10	14	V	[n = 1,2,3]
CBT_boot_time_HB	CBT boot time at high battery (VBP & VDH > 10V)	SHS_n = 0 CBT = 1 µF CBS_n 0 V to 7 V	0.25	-	0.5	ms	[n=1,2,3]
CBT_boot_time_LB	CBT boot time at low battery (VBP & VDH < 10V)	SHS_n = 0 CBT = 1 µF CBS_n 0 V to 7 V	0.5	-	1	ms	[n=1,2,3]

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

Bootstrap capacitance and Bootstrap Limiter 1 (BT1)

Bootstrap capacitance has the purpose of delivering the charge required for the external HS FET turn on translating its voltage level over VDH.

These capacitances are charged from the C_VPRE through BT1n circuitries during the n-th half bridge (1-D)*Tpwm interval (where Tpwm is the PWM period and D is the half bridge duty cycle).

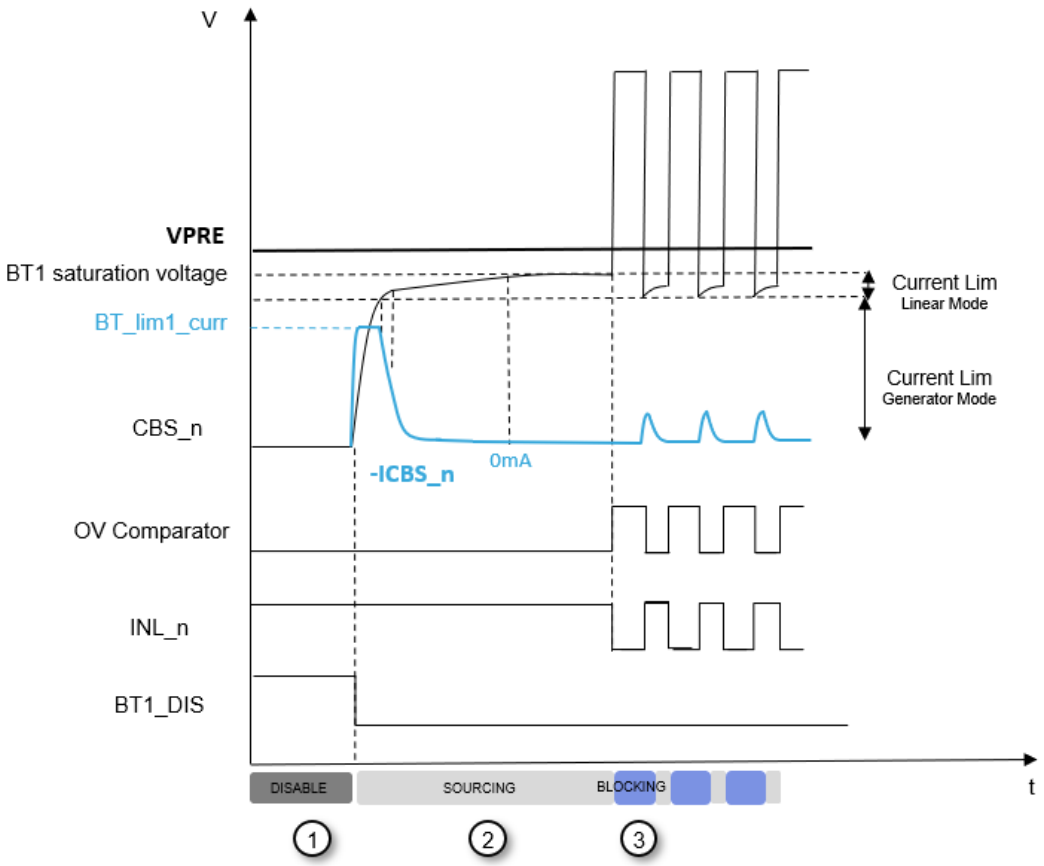
BT1 develops this function by ensuring at the same time a current limitation to avoid in-rush current when CBS are depleted and an over-voltage protection during HS turn-on phases and related voltage swing.

If Bootstrap Limiter 1 is disabled the charging path from VPRE is interrupted and bootstrap capacitors must be charge by other means, e.g. from CP2. Bootstrap Limiter 1 can be disabled by the dedicated SPI bit **BT1_DIS** within the register **GEN_CFG3** as follows:

Table 52. Bootstrap limiter 1 disable bit

BT1_DIS	Description
0	Bootstrap Limiter 1 Enabled (Default)
1	Bootstrap Limiter 1 Disabled

Figure 30. **BT1 behavior timing diagram**



Where:

1. BT1_DIS = '1'

   BT1 is disabled and the direct connection from VPRE to CBS_n is opened, the current flow is prevented.

2. CBS_n – VPRE ≥ BT_lim1_ov_ltoh_th

   BT1 is enabled and CBS_n voltage is lower than the overvoltage threshold. Direct connection from VPRE to CBS_n is established and the current flow is controlled according to the current limiting feature:

   – As long as VPRE-CBS_n drop voltage is higher than the saturation mode threshold (~1.3 V) the current sourced is almost constant and equal to BT_lim1_curr;

   – When the VPRE-CBS_n drop voltage falls below the saturation threshold the output stage enters the linear operation and its behavior is assimilable to a resistance with value BT1_lim_res.

   If the CBS_n voltage increases the BT1_lim_res increase until the BT_lim1_sat_drop is reached and the sourced current falls to 0 mA.

3. CBS_n – VPRE ≥ BT_lim1_ov_htol_th

   BT1 is enabled and CBS_n voltage is higher than the overvoltage threshold. An overvoltage is detected and the connection from CBS_n to VPRE is opened to prevent the reverse current flow.

Table 53. **Bootstrap Limiter 1 electrical characteristics**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
BT_lim1_res	BT Charge Limiter1 limitation resistance	VPRE-CBS_n ≤ 1.3 V	90	120	150	Ω	Linear Mode [n = 1,2,3](1)
BT_lim1_curr	BT Charge Limiter1 limitation current	CBS_n = 0 V	79	118	160	mA	Generator Mode [n = 1,2,3]

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
BT_lim1_sat_drop	BT Charge Limiter1 VRE-CBS_n drop voltage for ICBS_n = 0 mA	CBS_n = Open	335	490	535	mV	[n = 1,2,3]

1. *Not subject to production test. This is an equivalent resistance, its value shall be used for bootstrap charge timings estimation only.*

5.11.5 VCP monitor

VCP voltage level is monitored by means of the dedicated UV and OV diagnosis. Hysteresis on thresholds and filtering time is implemented.

If VCP ≤ VCP_uv_th occurs for an interval longer than T_vcp_uv_flt filtering time, the VCP_UV flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

If VCP ≥ VCP_ov_th occurs for an interval longer than T_vcp_ov_flt filtering time, the VCP_OV flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

To avoid UV detection during power up VCP monitor comparators are masked for a T_vcp_boot_mask filtering time, starting from each low to high transition of the internal CP1 enabling command.

Figure 31. VCP UV boot masking

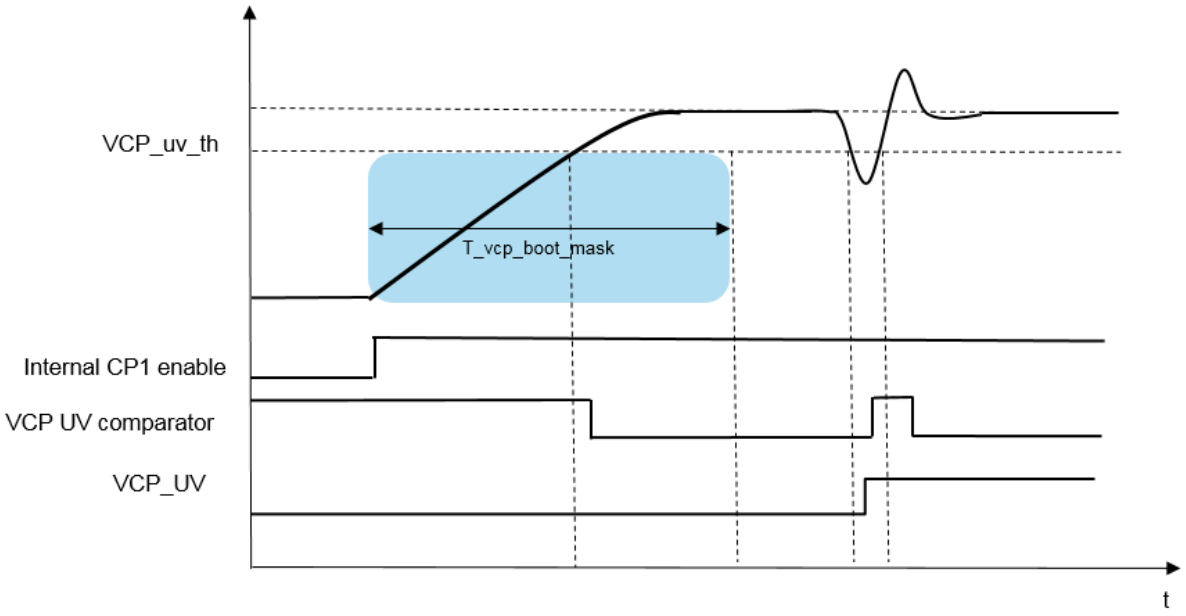
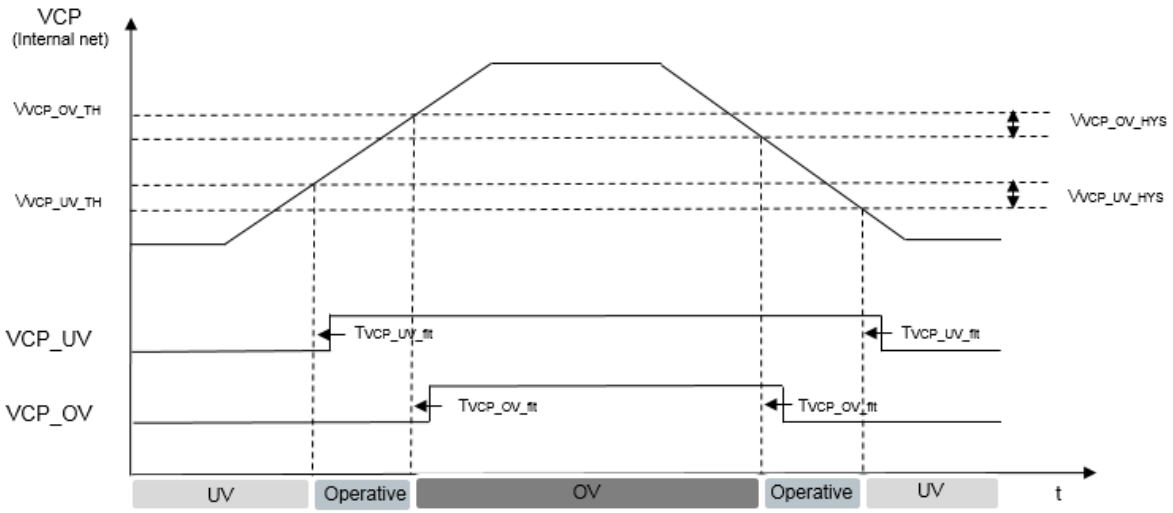


Table 54. VCP Monitor electrical characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
VCP_uv_th	VCP-VDH under-voltage threshold	-	4.5	5.1	5.8	V	Comparator output Low to High
VCP_uv_hys	VCP under-voltage hysteresis	-	200	300	400	mV	-
T_vcp_uv_flt	VCP under-voltage detection filter time	CLK_SSM_EN = 0	10	-	15	µs	Digital filter guaranteed through scan pattern
VCP_ov_th	VCP-VDH over-voltage threshold	-	15.8	17.6	19.5	V	Comparator output Low to High
VCP_ov_hys	VCP over-voltage hysteresis	-	50	325	500	mV	-
T_vcp_ov_flt	VCP over-voltage detection filter time	CLK_SSM_EN = 0	10	-	15	µs	Digital filter guaranteed through scan pattern
T_vcp_boot_mask	VCP boot masking time	-	1.7	2	2.3	ms	-

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

Figure 32. VCP operative range



5.12 Half bridges gate drivers

The core feature of L9908 is represented by the three identical and independent gate pre-driver stages to drive three inverter`s half bridges. Each half bridge pre-driver is composed by a floating current controlled LS and HS pre-driver couple.

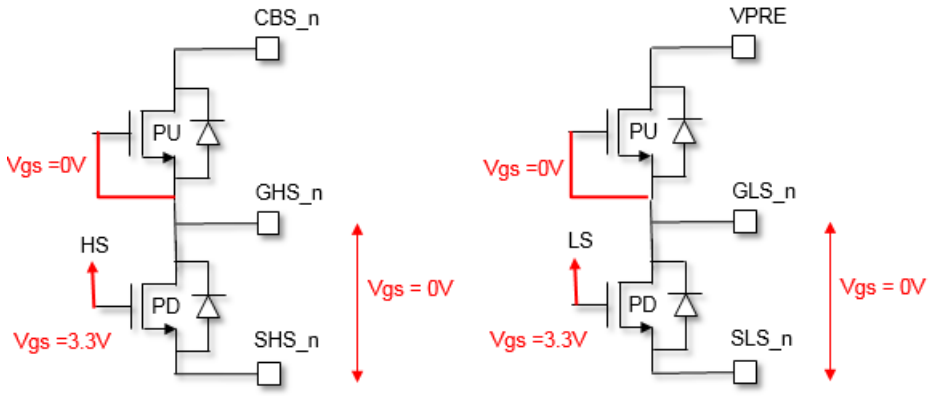
The specific n-th half bridge driver can be disabled by the dedicated SPI bit **HBn_DIS, n = [1,2,3]**, within the register **GEN_CFG4** as follows:

Table 55. n-th Half Bridge pre-drivers disable mode bit

HBn_DIS	Description
0	n-th HS/LS drivers is enabled (Default)
1	n-th HS/LS drivers is disabled

When disabled the n-th half bridge driver's internal HS/LS PU stages are off while the internal HS/LS PD are on resulting in a VGHS_n-VSHS_n = 0 V and VGLS_n-VSLS_n = 0 V.

Figure 33. Pre-drivers Disable mode behavior



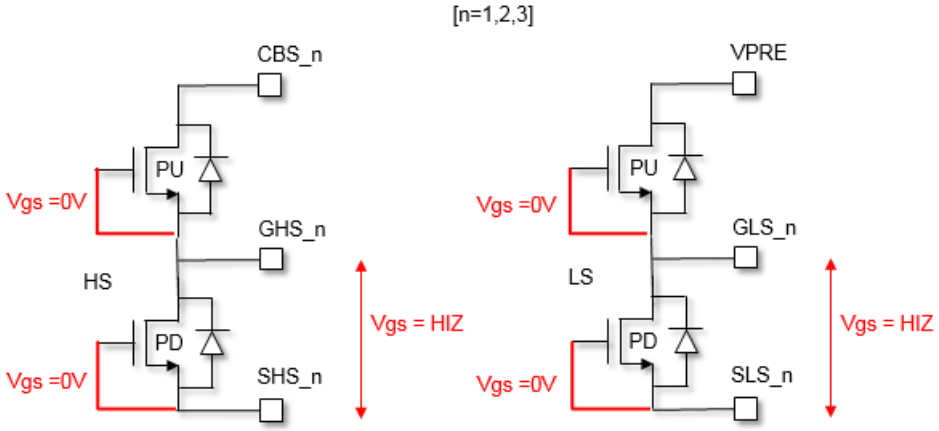
All drivers can be set in high impedance state by the dedicated SPI bit **DRV_HIZ** within the register **GEN_CFG4** as follows:

Table 56. Pre-drivers HIZ mode enable bit

DRV_HIZ	Description
0	Pre-drivers in NO high impedance
1	Pre-drivers in high impedance (Default)

When in HIZ mode the half bridge driver's internal HS/LS PU and PD stages are both off resulting in a VGHS_n-VSHS_n = HIZ and VGLS_n-VSLS_n = HIZ.

Figure 34. **Pre-drivers HIZ mode behavior**



The behavior of the driver depending on the DRV_HIZ and HBn_DIS setting reflects the following truth table:

Table 57. **Pre-drivers behavior truth table**

DRV_HIZ	HBn_DIS	Description
0	0	Pre-driver enabled
0	1	Pre-driver disabled
1	0	Pre-driver in high impedance (Default)
1	1	Pre-driver disabled

Note: above described condition in Disable or HIZ conditions are valid for LS drivers as long as VPRE ≥ 2.6 V and for HS as long as VDH ≥ 2.6 V. If these conditions do not hold despite the configuration the drivers are automatically in HIZ mode and the ext. FET Vgs is not driven actively.

Table 58. **Pre-driver timings**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
DRV_pwm_freq	PWM Frequency	-	-	20	-	kHz	Consumption Limited(1)
DRV_pwm_dc	HS Duty Cycle in PWM mode	-	0	-	100	%	Not subject to production test(2)
DRV_hs_on_dly	HS Pre-driver switch ON total propagation delay (T_logic_+T_hs_on_dly)	Rload = 2 kΩ INHn*0.5 to GHS_n*0.1 SHS_n = 0 V [n = 1,2,3]	170	-	400	ns	-
DRV_hs_off_dly	HS Pre-driver switch OFF total propagation delay (T_logic_+T_hs_off_dly)	Rload = 2 kΩ INHn*0.5- GHS_n*0.9 SHS_n = 0 V [n = 1,2,3]	170	-	400	ns	-
DRV_ls_on_dly	LS Pre-driver switch ON total propagation delay (T_logic_+T_ls_on_dly)	Rload = 2 kΩ INLn*0.5 to GLS_n*0.1 [n = 1,2,3]	170	-	400	ns	-

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
DRV_ls_off_dly	LS Pre-driver switch OFF total propagation delay (T_logic_+T_ls_off_dly)	Rload = 2 kΩ INLn*0.5 to GLS_n*0.9 [n = 1,2,3]	170	-	400	ns	-
DRV_on_dly_match	Pre-drivers switch ON propagation delay matching (phase to phase)	-	0	-	75	ns	-
DRV_off_dly_match	Pre-drivers switch OFF propagation delay matching (phase to phase)	-	0	-	75	ns	-
DRV_hs_trise	HS Pre-driver rise time	Cload = 33 nF GHS_n 1 V to 7 V SHS_n = 0 V [n = 1,2,3]	50	-	300	ns	-
DRV_hs_tfall	HS Pre-driver fall time	Cload = 33 nF GHS_n 1 V to 7 V SHS_n = 0 V [n = 1,2,3]	50	-	300	ns	-
DRV_ls_trise	LS Pre-driver rise time	Cload = 33 nF GLS_n 1 V to 7 V [n = 1,2,3]	50	-	250	ns	-
DRV_ls_tfall	LS Pre-driver fall time	Cload = 33 nF GLS_n 1 V to 7 V [n = 1,2,3]	50	-	250	ns	-
DRV_on_dly_match	Pre-drivers rise time matching (phase to phase)	-	0	-	20	ns	-
DRV_on_dly_match	Pre-drivers fall time matching (phase to phase)	-	0	-	20	ns	-

1. *The maximum allowed frequency is retrieved from the maximum average allowed current consumption from VPRE: Where: N is the number of Ext. FETs and Qg is the FET`s gate charge. So that if for example Qg = 150 nC the maximum fpwm allowed is close to 60 kHz (being Iload_max = 55 mA).*
2. *This D.C. limitation shall be adopted to guarantee the minimum Vgs on HS FETs over the whole battery operative range.*

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

Figure 35. Pre-drivers delay characteristics

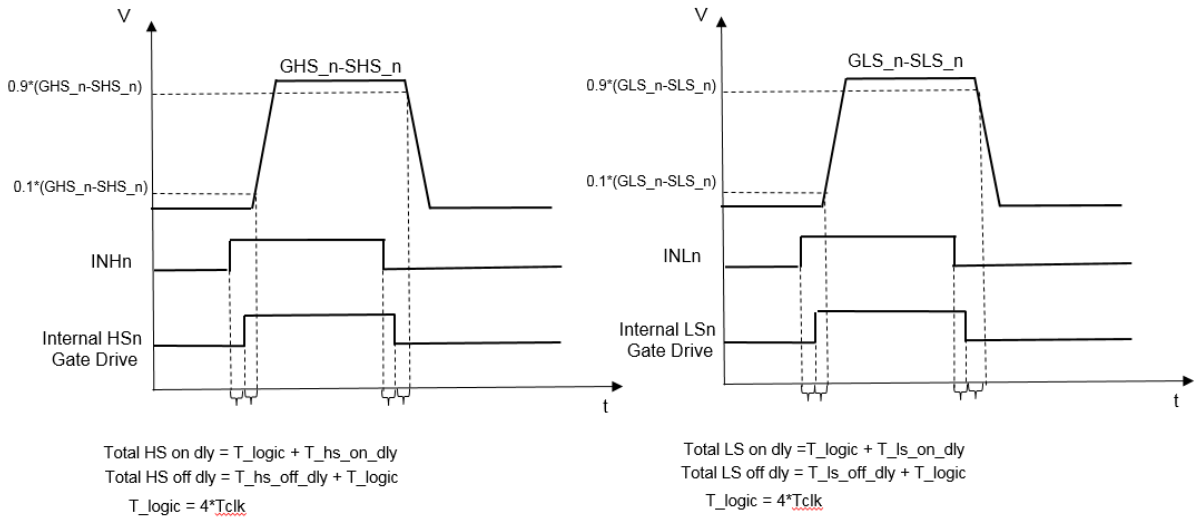


Figure 36. **Pre-drivers rise/fall time characteristics**

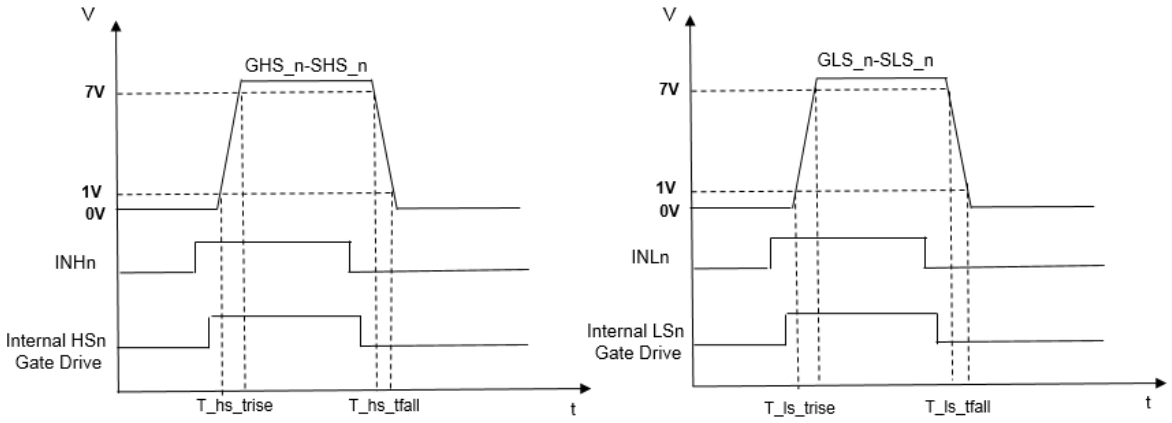


Table 59. **Pre-drivers electrical characteristics**

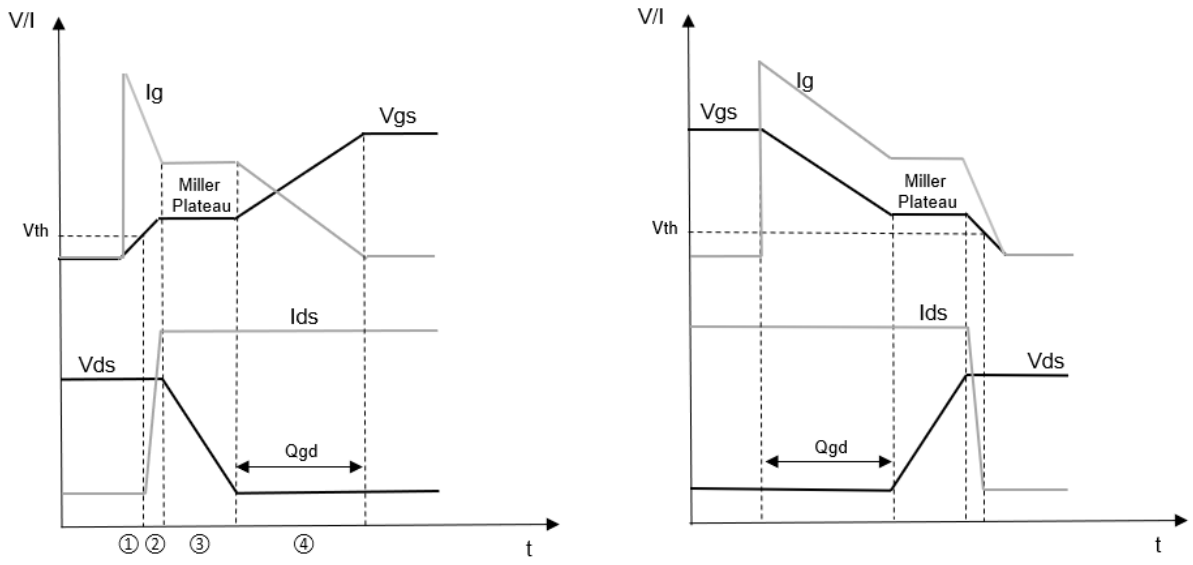
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
DRV_hs_pu_iout	HS Pre-driver pull up Gate Current	VGHS_S – VSHS_n = 0 V [n = 1,2,3]	1	2.2	-	A	Not subject to production test
DRV_hs_pd_iout	HS Pre-driver pull down Gate Current	VGHS_S – VSHS_n = 10 V [n = 1,2,3]	1	2.2	-	A	Not subject to production test
DRV_ls_pu_iout	LS Pre-driver pull up Gate Current	VGLS_S – VSLS_n = 0 V [n = 1,2,3]	1	2.2	-	A	Not subject to production test
DRV_ls_pd_iout1	LS Pre-driver pull down Gate Current	VGLS_S – VSLS_n = 0 V [n = 1,2,3]	1	2.2	-	A	Not subject to production test
DRV_hs_iout_match	HS Pre-drivers switch ON/OFF current matching (driver to driver)	-	-	-	1	%	-
DRV_ls_iout_match	LS Pre-drivers switch ON/OFF current matching (driver to driver)	-	-	-	1	%	-
DRV_hs_iout_onoff_match	HS Pre-drivers switch ON/OFF current matching (pull up to pull down)	-	-	-	1	%	-
DRV_ls_iout_onoff_match	LS Pre-drivers switch ON/OFF current matching (pull up to pull down)	-	-	-	1	%	-
DRV_hs_vout_ll	HS Pre-driver Low Level output voltage (GHS_n-SHS_n)	IGHS_n = 4 mA INHn = 0 SHS_n = 0 V [n = 1,2,3]	-	-	130	mV	-
DRV_hs_vout_ll_match	HS Pre-driver Low Level output voltage matching	-	-15	-	15	mV	-
DRV_hs_rpd	HS Pre-driver output resistance at low state	IGHS_n = 4 mA INHn = 0 SHS_n = 0 V	0.85	1.15	1.95	Ω	-

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
		[n = 1,2,3]					
DRV_ls_vout_ll	LS Pre-driver Low Level output voltage (GLS_n-SLS_n)	IGLS_n = 4 mA INLn = 0 SLS_n = 0 V [n = 1,2,3]	-	-	200	mV	-
DRV_ls_vout_ll_match	LS Pre-driver Low Level output voltage matching (GLS_n-SLS_n)	-	-15	-	15	mV	-
DRV_ls_rpd	LS Pre-driver output resistance at low state	IGLS_n = 4 mA INLn = 0 SLS_n = 0 V [n = 1,2,3]	0.85	1.15	1.95	Ω	-
DRV_ vout_ll_passive	Passive output voltage clamping (GHS_n-SHS_n, GLS_n-SLS_n)	DRV_HIZ = 1 IGATE = 5 µA SHS_n = SLS_n = 0 V [n = 1,2,3]	-	-	2	V	-
DRV_hs_vout_hl	HS Pre-driver High Level output voltage	IGHS_n = 4 mA INHn = 1 [n = 1,2,3]	7	-	12	V	-
DRV_hs_vout_hl_match	HS Pre-driver High Level output voltage matching	-	-	-	1	%	-
DRV_hs_rpu	HS Pre-driver output resistance at high state	IGHS_n = 4 mA INHn = 1 [n = 1,2,3]	0.85	1.15	1.95	Ω	-
DRV_ls_vout_hl	LS Pre-driver High Level output voltage	IGLS_n = 4 mA INLn = 1 [n = 1,2,3]	7	-	12	V	-
DRV_ls_vout_hl_match	LS Pre-driver High Level output voltage matching	-	-	-	1	%	-
DRV_ls_rpu	LS Pre-driver output resistance at high state	IGLS_n = 4 mA INLn = 1 [n = 1,2,3]	1.35	1.7	3.55	Ω	-
DRV_iout_reverse	Pre-driver reverse output current	GHS_n-SHS_n = -0.6 V GLS_n-SLS_n = -0.6 V [n = 1,2,3]	1	-	-	A	Not subject to production test

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

Note: Given the standard Ext. FET model, the currents and voltages behavior at its terminals at Turn-on/off can be described by the following piece-wise linear diagram.

Figure 37. **Ext. FET Turn-on/off simplified behavior**



Where:

1. The gate-source voltage (VGS) ramps up according to the time constant formed by the FET gate resistance (Rg) and input capacitance (Ciss)
2. Once the VGS reaches the threshold voltage (Vth) the current through the device starts to ramp up. The channel is supporting the full-load current and the drain-source voltage (VDS) starts decaying.
3. The VDS falls continuously to its on-state value while the VGS stays approximately constant (Miller Plateau) as well as the gate current.
4. The VGS ramps up to the value applied by the driver. This additional gate voltage fully enhances the FET channel and reaches the full RdsON.

Turn-off is the reverse of turn-on process. During turn-off, the Miller Plateau indicates the start of the rise of the VDS and the voltage of the Miller Plateau will represent the minimum required VGS to sustain the load current.

While a precise value of FET`s VDS slew rates at turn-on/off requires simulations including FET and GDU model plus the board and package parasitic details a first order approximations can be used to estimate this value.

The key parameter required for the estimation is the peak current the driver can source/sink to the Ext. FET gate terminal during the turn-on/off process, so the FET VDS rise/fall time can then be approximated by:

$$t_{rise} = \frac{Q_{gd}}{I_{DRV\_SOURCE\_PEAK}} \quad (6)$$

$$t_{fall} = \frac{Q_{gd}}{I_{DRV\_SINK\_PEAK}} \quad (7)$$

Where Qgd is the Ext. FET gate-drain charge and Idrv_source/sink_peak are the predrivers Pull-up/Pull-down current. Driver peak current should not be confused with drivers Average Current which is the average current the driver is delivering over full FET switching period i.e.

$$I_{DRV\_AVERAGE} = Q_g f_{sw} \quad (8)$$

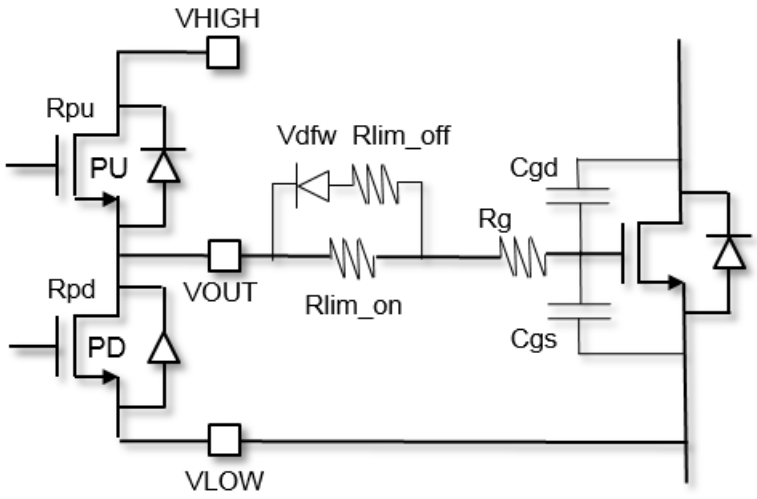
Where Qg is the Ext. FET total gate charge and fsw is the predriver switching frequency.

Output peak current limitation

Since pre-drivers output current is not programmable the peak level can be reduced by means of an external series resistances in order to achieve the following goals:

- dump ringing due to parasitic inductances/capacitances;
- dump ringing due to high voltage/current switching dv/dt, di/dt, and Ext. FET's body-diode reverse recovery charge;
- optimize the switching losses;
- reduce electromagnetic interference (EMI).

Figure 38. **Pre-driver peak output current limitation circuit**



The maximum PU/PD peak output currents can be estimated as follows:

$$I_{OUT\_PU\_PK} = MIN\left(DRV\_pu\_iout, \frac{V_{HIGH}}{R_{\lim\_on} + R_{PU} + R_g}\right) \quad (9)$$

$$I_{OUT\_PD\_PK} = MIN\left(DRV\_pu\_iout, \frac{V_{HIGH} - V_{dfw}}{R_{\lim\_on} \parallel R_{\lim\_off} + R_{PD} + R_g}\right) \quad (10)$$

Where: Vhigh is the driver`s output stage supply, Vdfw is the external diode forward voltage, Rg is the Ext. FET series gate resistance, and Rlim_on/off are the external limitation resistances.

Example: if Rg = 1.6 Ω, Vdfw = 0.75 V, VHIGH = 10 V to have maximum peak current below 0.8 A the external resistance shall be:

$$I_{OUT\_PU\_PK} = \frac{10V}{R_{\lim\_on} + 1.15\Omega + 1.6\Omega} = 0.8A \rightarrow \left(R_{\lim\_on} + 2.75\Omega\right) \approx 12.5\Omega \quad (11)$$
$$\rightarrow R_{\lim\_on} \approx 9.75\Omega$$

$$I_{OUT\_PD\_PK} = \frac{10V - 0.75V}{R_{\lim\_on} \parallel R_{\lim\_off} + 1.15\Omega + 1.6\Omega} = 0.8A \rightarrow \left(R_{\lim\_on} \parallel R_{\lim\_off} \right. \quad (12)$$
$$\left. + 2.75\Omega\right) \approx 11.56\Omega \rightarrow 9.75\Omega \parallel R_{\lim\_off} \approx 8.81\Omega \rightarrow R_{\lim\_on} \approx 4.63\Omega$$

5.12.1 Ext. FET VGS monitor

The correct functionality of each six pre-drivers is monitored by a dedicated comparator that senses the difference between Gate and Source terminals of the Ext. FET.

If GHS_n-SHS_n (GLS_n-SLS_n) ≥ VGS_TH + VGS_uv_hys occurs for an interval longer than T_vgs_flt the VGS comparator output goes to 0 and the HSn_OFF (LSn_OFF) flag is reset. The Ext FET is considered turned-on.

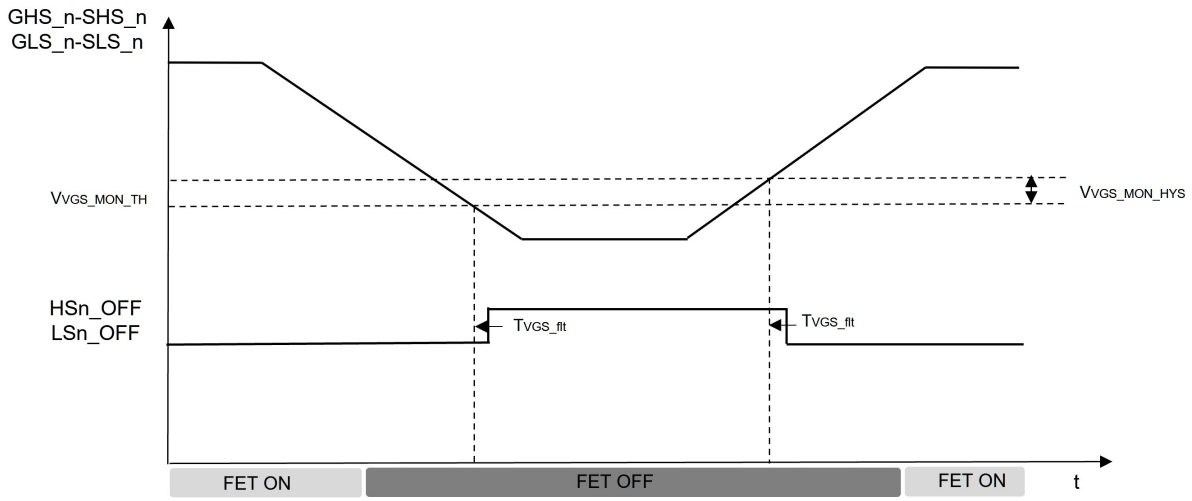
If GHS_n-SHS_n (GLS_n-SLS_n) ≤ VGS_TH occurs for an interval longer than T_vgs_flt the VGS comparator output goes to 1 and the HSn_OFF (LSn_OFF) flag is set. The Ext FET is considered turned-off.

Table 60. **VGS monitor electrical characteristics**

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VGS_mon_th	VGS monitor threshold	2	2.5	3	V	-
VGS_uv_hys	VGS monitor hysteresis	60	-	200	mV	-
T_vgs_uv_flt	VGS monitor detection filter time	200	230	300	ns	Analog filter

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

Figure 39. **VGS Monitor operative ranges**



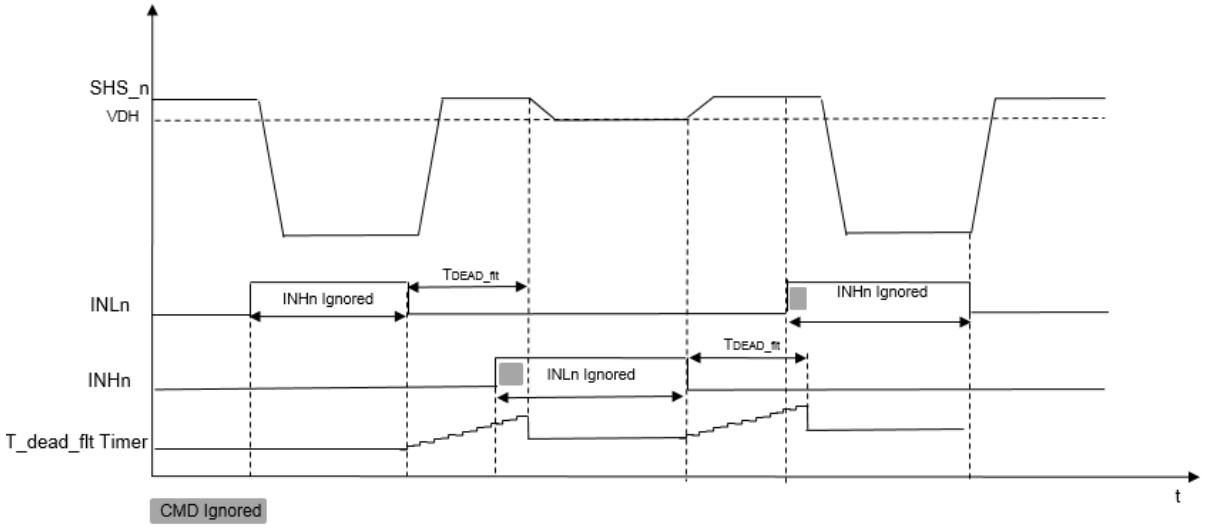
5.12.2 Dead Time Protection (DTP)

The prevention of cross-conduction due to HSn/LSn ON-phase overlap is in principle under the responsibility of the uC driving the PWM pins INHn/INLn. However, a built-in dead time protection is available.

When the main logic processes a falling edge event on INHn/INLn it starts a programmable masking time interval T_dead_flt during which the rising edges on the opposite signal (INLn/INHn respectively) are ignored.

In general a rising edge on INHn/INLn is processed only during the condition INHn=INLn= 0 and if such a condition hold for at least a T_dead_flt.

Figure 40. **Dead Time Protection functional operation**



The T_dead_flt configuration can be set by the dedicated SPI signal **DTP_CFG** within the register **GEN_CFG1** as follows:

Table 61. **Dead Time Protection configuration bits**

DTP_CFG2	DTP_CFG1	DTP_CFG0	Description
0	0	0	0us – DTP Disabled
0	0	1	0.25 µs

DTP_CFG2	DTP_CFG1	DTP_CFG0	Description
0	1	0	0.35 µs
0	1	1	0.5 µs
1	0	0	1 µs – Default
1	0	1	1.5 µs
1	1	0	2 µs
1	1	1	4 µs

Table 62. Dead Time Protection accuracy

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DTP_tflt_acc	Dead Time Filter accuracy	CLK_SSM_EN = 0	-15		15	%

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

5.12.3 Shoot-Through Protection (STP)

Independently of the activation of DTP, L9908 implements a monitoring unit to detect the dangerous condition when HS and LS of the same half bridge are driven on at the same time. The diagnosis is performed at two levels: on the devices PWM inputs from uC (INHn/INLn) and on the Ext. FET Vgs; this allows a diagnosis coverage both on external and internal shoot-through faults.

The first diagnosis level consists in a dedicated digital counter for each half bridge PWM inputs (INHn/INLn couple) set/reset by the logic AND between INHn and INLn and integrates the time interval where the INHn and the INLn are high together.

If INHn=INLn='1' occurs for an interval longer than T_stp_pwm_flt the flag STP_PWM_n is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

In addition to STP, an interlocking protection function on INHn and INLn is implemented: when the main logic processes a rising edge event on INHn/INLn a masking on the opposite signal (INLn/INHn respectively) is applied for the entire duration of the INHn/INLn on pulse. During this interval any rising edge on the opposite signal is ignored. In case INHn/INLn rising edge is synchronous then INLn has the priority.

The interlocking protection is always active and cannot be disabled.

Figure 41. Interlocking protection on PWM inputs: functional operation

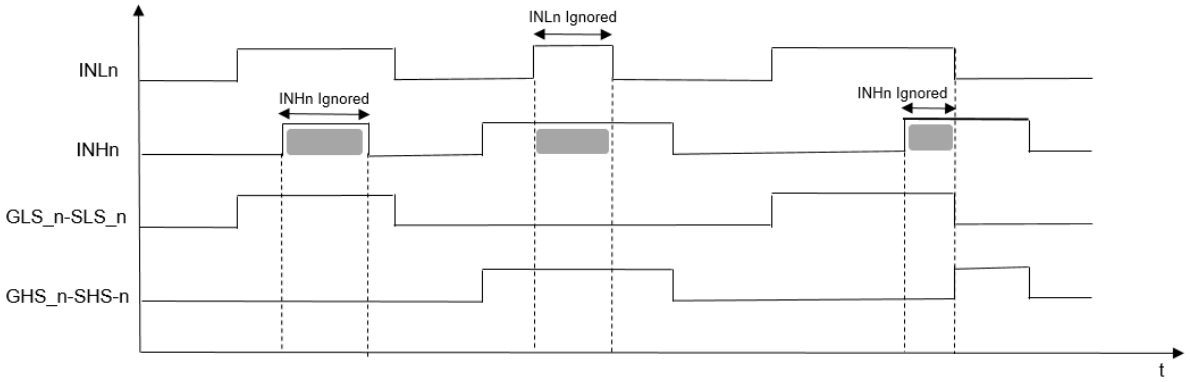
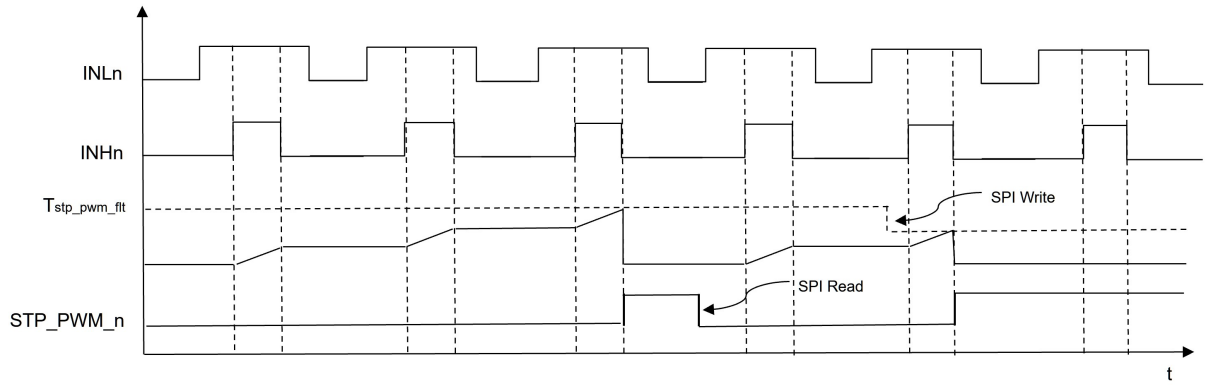


Figure 42. **Shoot-Through diagnosis on PWM inputs: functional operation**

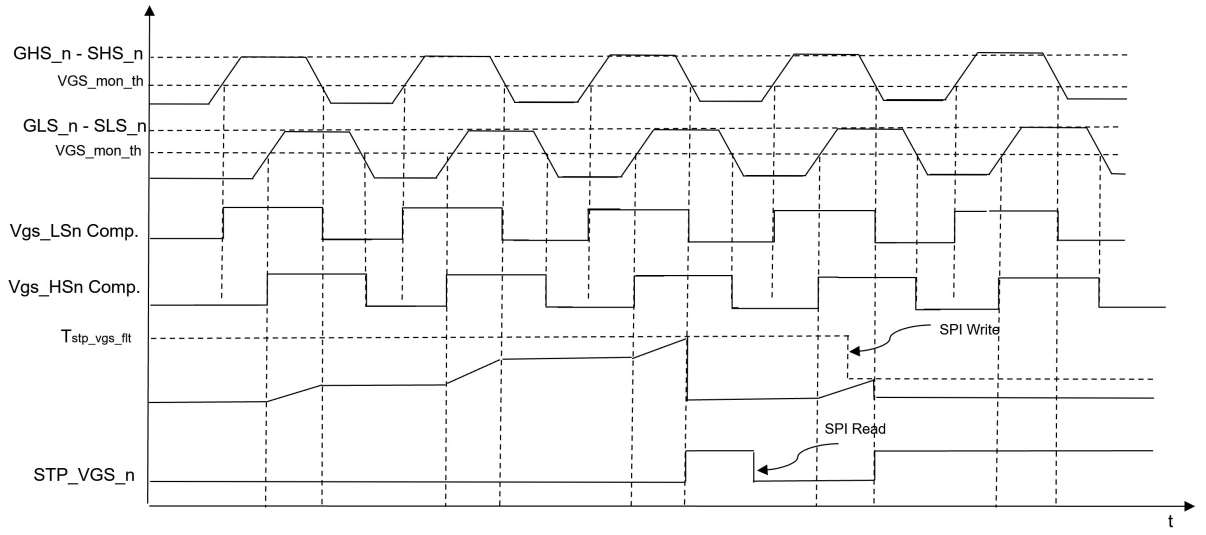


Note: PWM STD Filter integrates INHn/INLn timing overlap on multiple PWM periods, in this way STD Fault on PWM inputs can be detected also in case minimum timing overlaps are spread over multiple and not adjacent periods.

The second diagnosis level consists in a dedicated digital counter for each half bridge (HS/LS couple) set/reset by the logic NOR of the HS/LS VGS comparators and integrates the time interval where the HS and the LS are on together.

If HSn_OFF=LSn_OFF='0' occurs for an interval longer than T_stp_vgs_flt the flag STP_VGS_n is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

Figure 43. **Shoot-through protection on Ext. FET Vgs functional operation**



Note: VGS STD Filter integrates Vgs_LSn/Vgs_HSn timing overlap on multiple PWM periods, in this way STD Fault on Ext. FET Vgs can be detected also in case minimum timing overlaps are spread over multiple and not adjacent periods.

The STD diagnosis can be disabled on the single half bridge by a dedicated SPI bit as follows:

Table 63. **Shoot-Through Protection on PWM inputs enable bit**

STPn_PWM_DIS	Description
0	Shoot-through protection on PWM input enabled (Default)
1	Shoot-through protection on PWM input disabled

Table 64. **Shoot-Through Protection on Ext. FET VGS enable bit**

STPn_VGS_DIS	Description
0	Shoot-through protection on FET Vgs enabled (Default)
1	Shoot-through protection on FET Vgs disabled

The T_stp_flt configuration for the n-th pre-driver can be set by a dedicated SPI bit as follows:

Table 65. **Shoot-Through Protection on PWM inputs filtering configuration bits**

STPn_PWM_CFG1	STPn_PWM_CFG0	Description
0	0	0.2 µs (Defaults)
0	1	0.5 µs
1	0	1 µs
1	1	1.5 µs

Table 66. **Shoot-Through Protection on Ext. FET VGS filtering configuration bits**

STPn_VGS_CFG1	STPn_VGS_CFG0	Description
0	0	0.2 µs (Defaults)
0	1	0.5 µs
1	0	1 µs
1	1	1.5 µs

Table 67. **Shoot-Through Protection accuracy**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
STP_pwm_tflt_acc	PWM Shoot-through Filter Time accuracy	CLK_SSM_EN = 0	-10	-	10	%
STP_vgs_tflt_acc	VGS Shoot-through Filter Time accuracy	CLK_SSM_EN = 0	-10	-	10	%

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

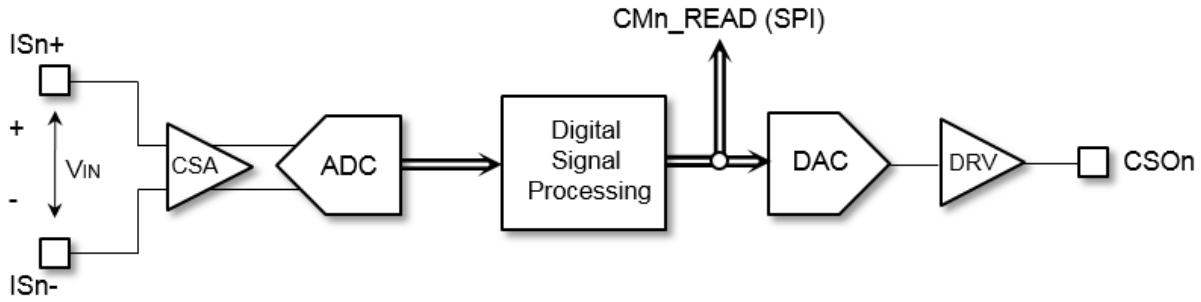
5.13 Current monitors

L9908 implements three identical and independent current monitor channels.

The motor current converted by an external shunts resistance into a differential voltage VIN is measured through the input pins Isn+ and Isn- (VIN = Isn+ - Isn-).

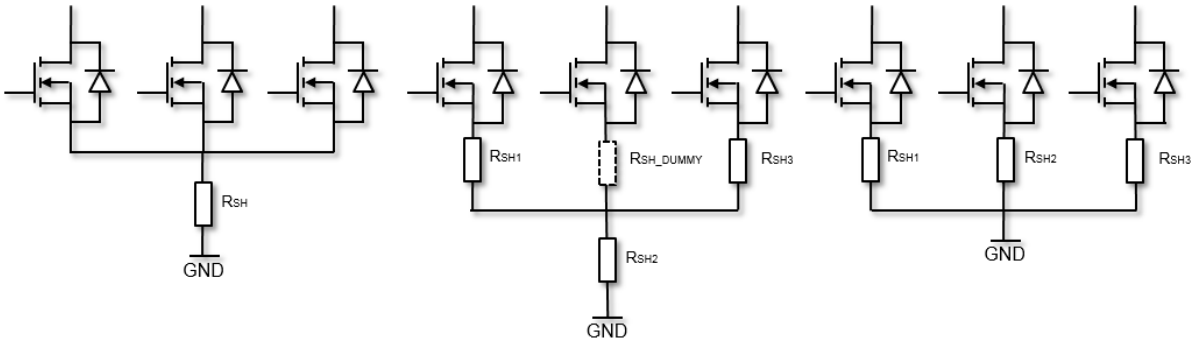
A current sense amplifier (CSA) is used to amplify the ground referenced differential voltages then converted via an internal 11-bit ADC. The current information is made available either in digital form through SPI register readout or reconverted in analog form through an 11-bit DAC at CSO_n pin.

Figure 44. **n-th Current Monitor Channel simplified block diagram**



Each current monitor channel can be used to measure positive or negative motor current flow through single (DC Link) or multiple (Single Leg) shunts system configurations.

Figure 45. **External Shunts Configurations a) DC-Link, b) 2xSingle Leg + DC-Link, c) 3xSingle Leg**



The specific n-th current monitor channel can be disabled by a dedicated SPI bit in the SAFETY_RELEVANT2 register, as follows:

Table 68. **n-th Current Monitor Channel enable bit**

CSn_DIS	Description
0	n-th current monitor enabled (Default)
1	n-th current monitor disabled

When disabled, the n-th input current measurement structure is set in low consumption mode, the related DSP logic is reset and the output stage is set into high impedance state.

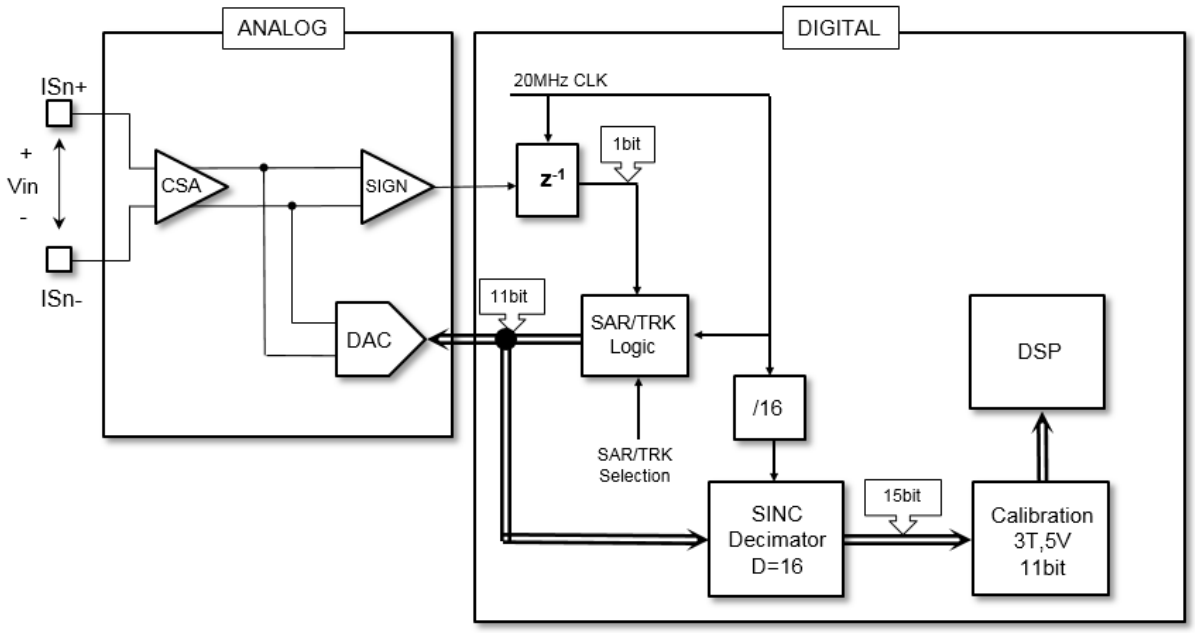
The current monitor channel consists of three main parts:

- A/D Conversion;
- Digital Signal Processing;
- D/A Conversion.

5.13.1 A/D conversion

The A/D conversion part is composed by a floating differential amplifier (CSA) that feeds an 11bits ADC.

Figure 46. **A/D Conversion simplified block diagram**



The differential transconductance amplifier measures the voltage across the external shunt cancelling errors due to voltage drop across the stray resistances and the offsets between the external and internal ground.

The cascaded ADC compares the differential current output from CSA with the output of an 11bit (1bit sign+10bit module) differential current steering DAC thus converting the current information in an 11 binary-coded word clocked at 20 MHz.

The DAC LSB can be configured separately for each current monitor channel by means of dedicated SPI bits in order to adjust the current monitor input range to the ADC input range as follows:

Table 69. **Current Monitor input range configuration bit**

Input Range	CSMn_IN_RANGE_CFG2	CSMn_IN_RANGE_CFG1	CSMn_IN_RANGE_CFG0	Description
0	0	0	0	VIN_MAX = ± 7 mV
1	0	0	1	VIN _MAX = ±18 mV
2	0	1	0	VIN _MAX = ±36 mV
3	0	1	1	VIN_MAX = ±90 mV
4	1	0	0	VIN_MAX = ±160 mV
5	1	0	1	VIN_MAX = ±300 mV (Default)
-	1	1	0	Reserved
-	1	1	1	Reserved

V_{IN_MAX} is the input range for which all parameters are guaranteed. Input Full Scale range is actually larger (to allow some headroom for calibration purposes), and can be calculated multiplying CM input ADC LSB (indicated in Table 70) values by 2^{11}-1.

To increase the signal to noise ratio, a successive digital process section filters the raw conversion by means of a SINC Decimation filter with a decimation factor of 16. The output digital information is then available in a 15bit length word.

Table 70. Current Monitor Input characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
Current Monitor Input							
CM_in_range_diff	CM differential voltage input range	CSMn_IN_RANGE_CFG = 000 CSMn_IN_RANGE_CFG = 001 CSMn_IN_RANGE_CFG = 010 CSMn_IN_RANGE_CFG = 010 CSMn_IN_RANGE_CFG = 011 CSMn_IN_RANGE_CFG = 100	-7 -18 -36 -90 -160 -300	-	7 18 36 90 160 300	mV	Application information(1)(2)
CM_in_range_cm	CM common mode voltage input range	-	-2	-	2	V	Application information(2)
CM_in_ic1	CM input current	ISn+ = ISn- = -2 V	-210	-25	-0.23	mA	-
CM_in_ic2	CM input current	ISn+ = ISn- = +2 V	-310	-270	-230	uA	-
CM_in_cm_res1	CM input common mode resistance	ISn+ = ISn- = -2 V	9.5	-	-	Ω	Application Information
CM_in_cm_res2	CM input common mode resistance	ISn+ = ISn- = +2 V	6.5	-	-	kΩ	Application Information
CM_in_dm_res	CM input differential mode resistance	CSMn_IN_RANGE_CFG = 000 CSMn_IN_RANGE_CFG = 001 CSMn_IN_RANGE_CFG = 010 CSMn_IN_RANGE_CFG = 010 CSMn_IN_RANGE_CFG = 011 CSMn_IN_RANGE_CFG = 100	-	0.283 0.566 1.132 2.831 5.096 9.06	-	kΩ	Application Information
Current Monitor Input Resolution							
CM_in_resolution	CM input ADC resolution	-	-	11	-	bits	Application Information
CM_in_lsb	CM input ADC LSB	CSMn_IN_RANGE_CFG = 000 CSMn_IN_RANGE_CFG = 001 CSMn_IN_RANGE_CFG = 010 CSMn_IN_RANGE_CFG = 010 CSMn_IN_RANGE_CFG = 011 CSMn_IN_RANGE_CFG = 100	-	10.05 20.11 40.28 100.7 181.27 322.26	-	µV	Application information
Current Monitor Input Accuracy							
CM_in_gain_err	CM ADC Gain Error	-	-2	-	2	%	All input ranges(3)(4)
CM_in_offset_err	CM ADC Input Referred Offset Error	CSMn_IN_RANGE_CFG = 000 CSMn_IN_RANGE_CFG = 001 CSMn_IN_RANGE_CFG = 010 CSMn_IN_RANGE_CFG = 010 CSMn_IN_RANGE_CFG = 011	-2 -2 -2 -2 -3	-	2 2 2 2 3	mV	(4)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
		CSMn_IN_RANGE_CFG = 100	-6		6		
Current Monitor Input Dynamic Characteristics							
CM_in_gain_toggling	CM CSA transition time gain toggling	-	-	26	-	Tclk	Application Information
CM_in_overload_recovery	Overload Recovery Time	-	-	36	-	Tclk	Application Information
CM_in_sr	CM ADC sample rate	-	-	20	-	MHz	Application information
CM_in_rise_fall_sr	CM Input Differential Rise/Fall Time	trise, tfall	16	-	-	Tclk	Application Information
CM_in_pulse_sr	CM Input Differential Slew Rate	(V2 - V1)/tpulse	-	-	1LSB/ Tclk	mV/ µs	Application Information
CM_in_pulse_time	CM Input Differential pulse length	tpulse	TSYNC + 10Tclk	-	-	µs	Application Information

1. *Offset free differential input range.*
2. *VIN may exceed CM_in_range_diff up to the absolute maximum ratings. However, it will saturate the A/D dynamic range.*
3. *Ex. 1*
   - *CSMn_IN_RANGE_CFG:011 → CM_in_range_diff = ±90 mV*
   - *FSR = 180 mV*
   - *|ISn+ - ISn-| = 20 mV → ±20 mV*2% = ±0.4 mV*

   Ex.2
   - *CSMn_IN_RANGE_CFG:100 → CM_in_range_diff = ±160 mV*
   - *FSR = 320 mV*
   - *|ISn+ - ISn-| = 150 mV → ±150 mV*2% = ±3 mV*
4. *ADC conversion total error can be retrieved for each differential input range as follows:*
   - *CM_in_total_error = CM_in_gain_err + CM_in_offset_err*
   - *Ex1*
     - *CM_in_range_diff = ±90 mV*
     - *|ISn+ - ISn-| = 70 mV*

   *Total ADC conversion error = ±2 mV ± (2%*70 mV) = ±2 mV ±1.4 mV. The value read by SPI will range between 70 mV-(2 mV + 1.4 mV) and 70 mV + (2 mV + 1.4 mV), which is 70 mV ± 34LSB. i.e. CSn_READ = 0x2B7 ± 0x22*

Figure 47. Current Monitor input dynamic timings

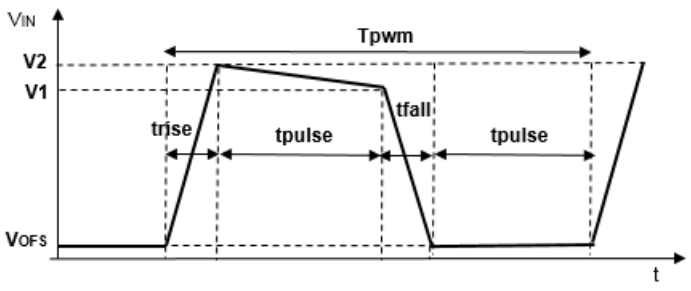


Figure 48. **Current monitor input CMRR - Positive Common Mode input voltage**

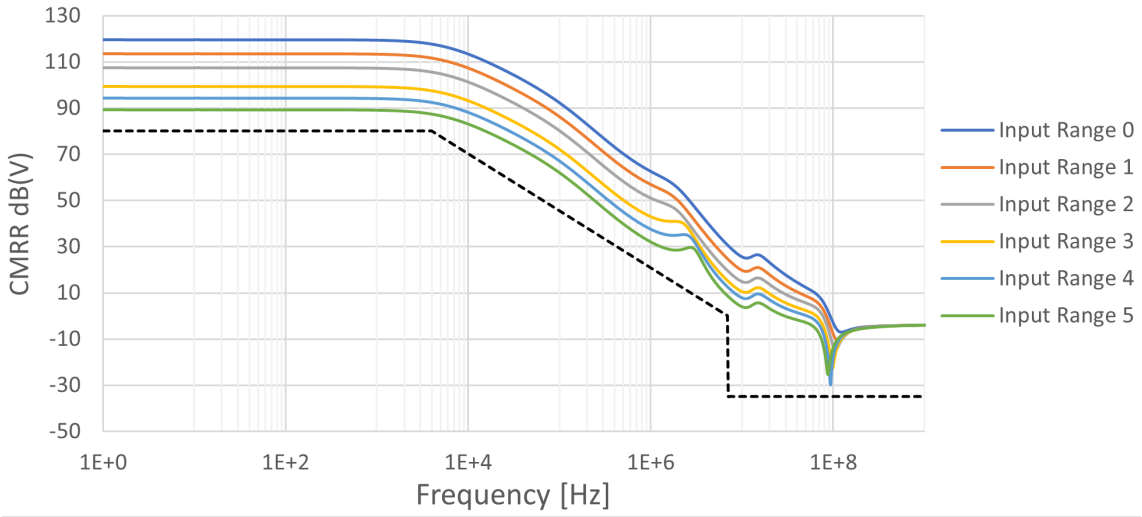
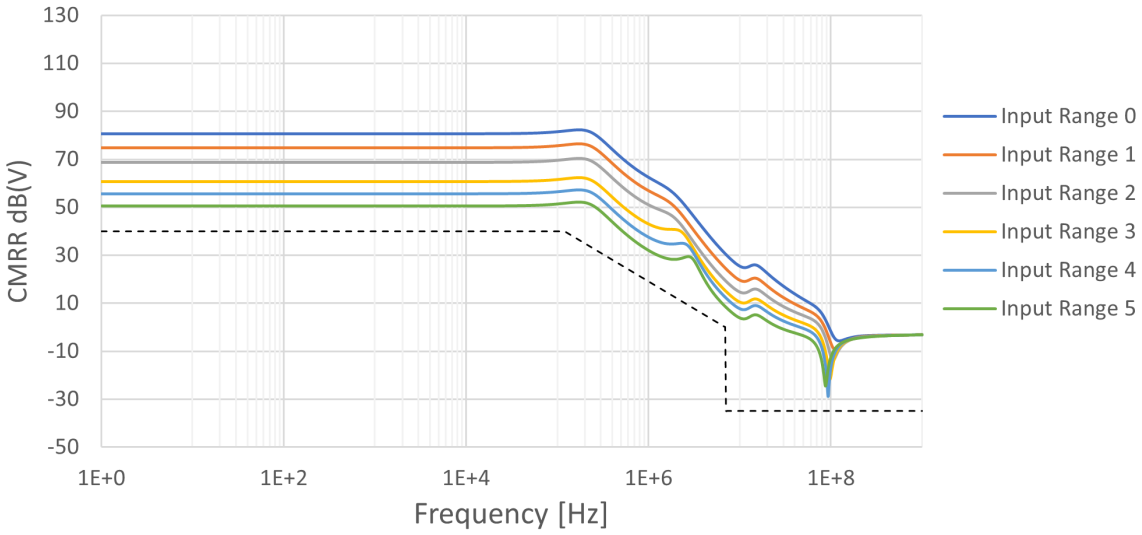


Figure 49. **Current monitor input CMRR - Negative Common Mode input voltage**



$$CMRRn = -20\log\left(\frac{\sqrt{CSOn_{RF\_RMS}^2 + CSOn_{DC}^2}}{Vin_{RF\_RMS}}\right) \quad (13)$$

Where:

CSOn_rf_rms = output voltage RMS calculated taking into account only the AC component of the output voltage on the n-th CSO output.

CSOn_dc = Output DC shift (with respect to the reference value with zero AC component).

Vin_rf_rms = input voltage RMS calculated taking into account only the AC component of the input voltage on n-th CM input (Vin = IS + -IS-).

Example:CSOn = 200 mV (reference value without RF applied) CSOn_DC_RF = 160 mV (DC output value with RF applied) Vin_pp = 4 Vpp -> Vin_RMS = 1.4 Vrms (applied RMS RF level) CSOn_ac = 0 (i.e. no ripple at current measurement output).

CMRR = 30.88 dB

$$CMRRn = -20\log\left(\frac{\sqrt{(0)_{AC_{RMS}}^2 + (-0.04)_{DC}^2}}{1.4}\right) = 30.88\,dB(V) \quad (14)$$

5.13.1.1 *Conversion triggering logic*

In order to improve the effectiveness of the A/D conversion and maximize the dynamic performances the current monitor ADC implements two different conversion algorithms:

- Up/Down TRK algorithm is active while SAR is disabled. TRK logic increments/decrements by 1LSB each clock cycle the DAC input depending on the sign comparator assessment. This algorithm is able to guarantee a high conversion accuracy but along with a limited input slew rate given by 1LSB/Tclk;
- SAR algorithm is active while TRK is disabled. SAR logic increments/decrements by $2^{10}/2^{N}$at each *N* clock cycle. This algorithm is effective in the fast changing signal but lacks in accuracy.

A/D conversion default algorithm is TRK; SAR conversion algorithm is launched by triggering logic assessment.

Conversion triggering logic assessment follows two different criteria:

- Command Edge Triggering;
- Auto-triggering.

Note: As long as enabled, each n-th A/D continuously converts input voltage into digital words: the conversion triggering only defines how SAR and TRK algorithms interleave to get the most accurate current conversion.

5.13.1.1.1 Command edge triggering

Command Edge Triggering criteria relies on ACT function: when the value stored in ACTn register equals the value configured in the TSYNCn register, a trigger pulse is generated and the SAR conversion is performed.

SAR conversion is launched at the same time on all current monitors, synchronously.

The n-th ACT to be used for sampling reference can be configured by means of the following bits:

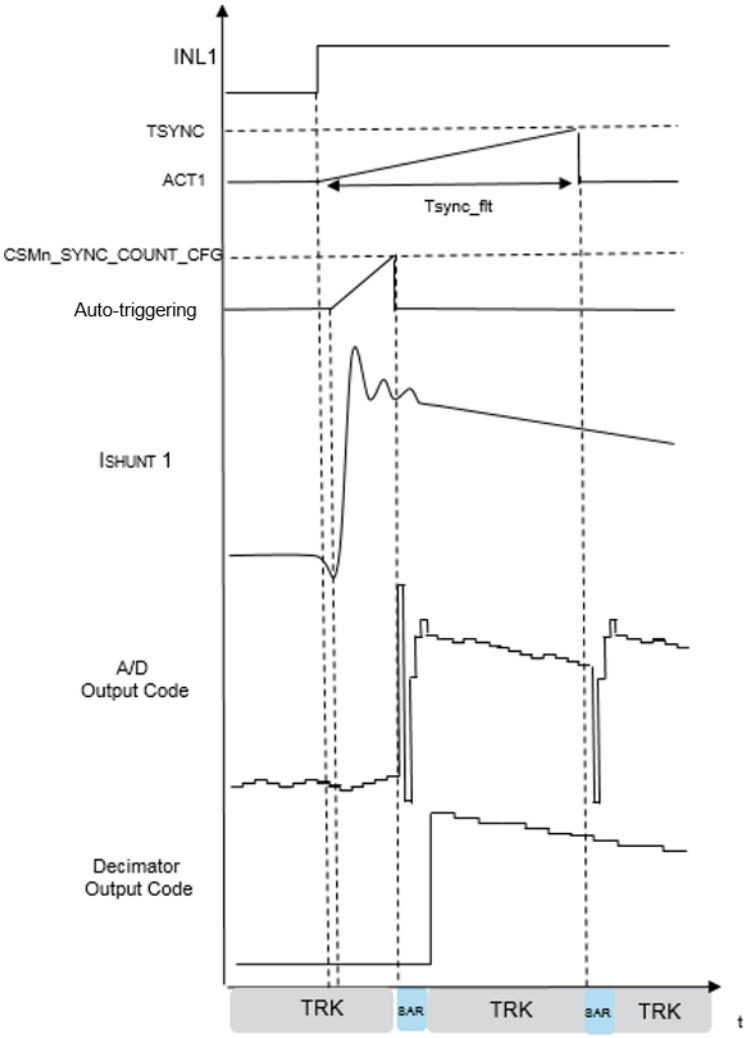
Table 71. Command edge triggering configuration bits

CSM_SSPV_PH_CFG1	CSM_SSPV_PH_CFG0	Description
0	0	No synchronization
0	1	TSYNC based on Phase 1 (Default)
1	0	TSYNC based on Phase 2
1	1	TSYNC based on Phase 3

Note:

- *When CSM_SSPV_PH_CFG is set 00 the value output on CSOn and stored in CSn_READ correspond to the last sample value when CSM_SSPV_PH_CFG ≠ 00.*
- *When CSM_SSPV_PH_CFG = 01 ACT1 is used for the comparison*
- *When CSM_SSPV_PH_CFG = 10 ACT2 is used for the comparison*
- *When CSM_SSPV_PH_CFG = 11 ACT3 is used for the comparison*

Figure 50. **Command edge triggering timing diagram**



The Tsync_flt can be set separately for each phase by the SPI signal TSYNCn_CFG<10:0> in the register CHn_CFG3, so that:

$$T_{SYNCn} = \Delta_{LSB\_TSYNC} \times TSYNCn\_CFG[10:0] \quad (15)$$

Being:

$$\Delta_{LSB\_TSYNC} = \Delta_{ACT\_lsb} \quad (16)$$

Where: Δ_{ACT_lsb} is the ACT quantization step (see Table 98).

5.13.1.1.2 Auto-triggering

Auto-triggering criteria relies on an internal counter which counts the number of clock cycles in which the Sign comparator has the same sign. When the counted value equals the value configured in the CSMn_SYNC_COUNT_CFG register a trigger pulse is generated and the SAR conversion is performed.

SAR conversion is launched independently on each current monitor, asynchronously.

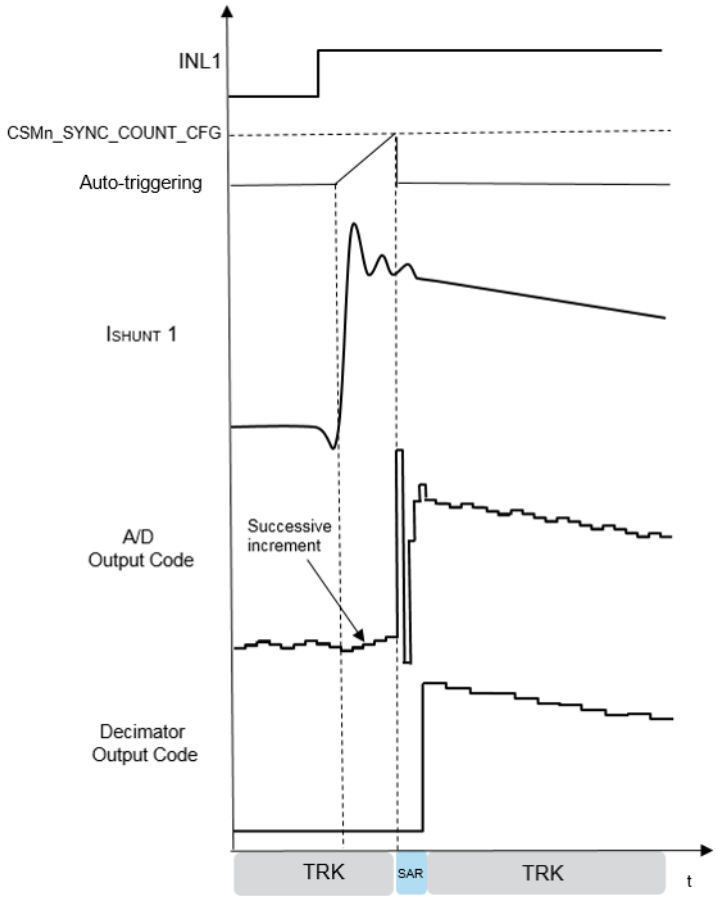
Note: Auto-triggering is always active and cannot be disabled. Its purpose is to allow A/D to promptly react in front of input voltage sharp transitions also in case Command Edge Triggering is not enabled.

SR Counter threshold can be programmed for the single current monitor through the following SPI bits:

Table 72. **Synchronization counter configuration bits**

CSMn_SYNC_COUNT_CFG1	CSMn_SYNC_COUNT_CFG0	Description
0	0	16 Tclk (Default)
0	1	24 Tclk
1	0	32 Tclk
1	1	40 Tclk

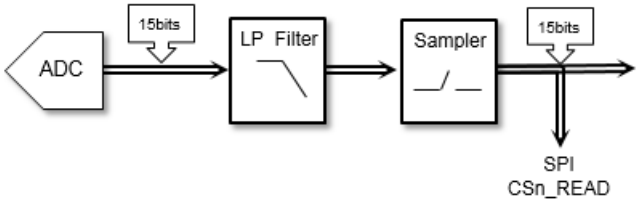
Figure 51. **Auto-triggering timing diagram**



5.13.2 Digital signal processing

The signal processing consists in a series of operations performed on the converted current information in the digital domain.

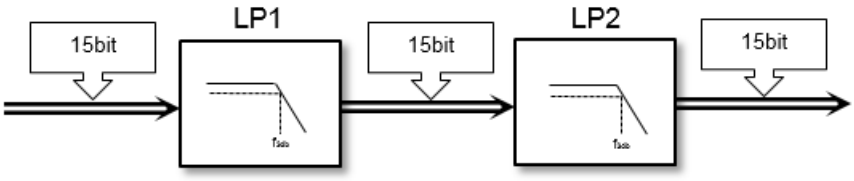
Figure 52. **Digital signal processing simplified block diagram**



5.13.2.1 *Low-pass filtering*

The first operation performed is a 2nd order low-pass filtering on the raw ADC data accomplished by two cascaded single pole filters with the same cut-off frequency.

Figure 53. Digital LP filtering simplified block diagram



The filter`s cut-off frequency can be configured through SPI as follows (setting is common for the three phases):

Table 73. Current monitors LP filtering configuration bits

CSM_LP_CFG2	CSM_LP_CFG1	CSM_LP_CFG0	Description
0	0	0	No filtering (Default)
0	0	1	91 kHz
0	1	0	37 kHz
0	1	1	17 kHz
1	0	0	8 kHz
1	0	1	4 kHz
1	1	0	2 kHz
1	1	1	1 kHz

5.13.2.2 *Conversion sampling*

Current monitor`s DSP allows two kinds of data flow toward the SPI register (digital format) and to D/A (analog format):

- Free running;
- Track & Hold

Note: Conversion sampling affects NO A/D operation whatsoever. Conversion sampling logic only defines how SPI reg. and D/A output values have to be updated.

5.13.2.2.1 Free running

In Free Running mode the CSn_READ SPI registers and the CSOn voltage are continuously updated as soon as A/D output words are available.

Free Running mode is enabled configuring signal CSM_SAMPLE_CFG = 000 in the register CHn_CFG2.

Note: In the following timing diagrams, N-th A/D Out value corresponds to the SAR conversion value.

Figure 54. **Free running sampling timing diagram - non-zero current + auto-triggering**

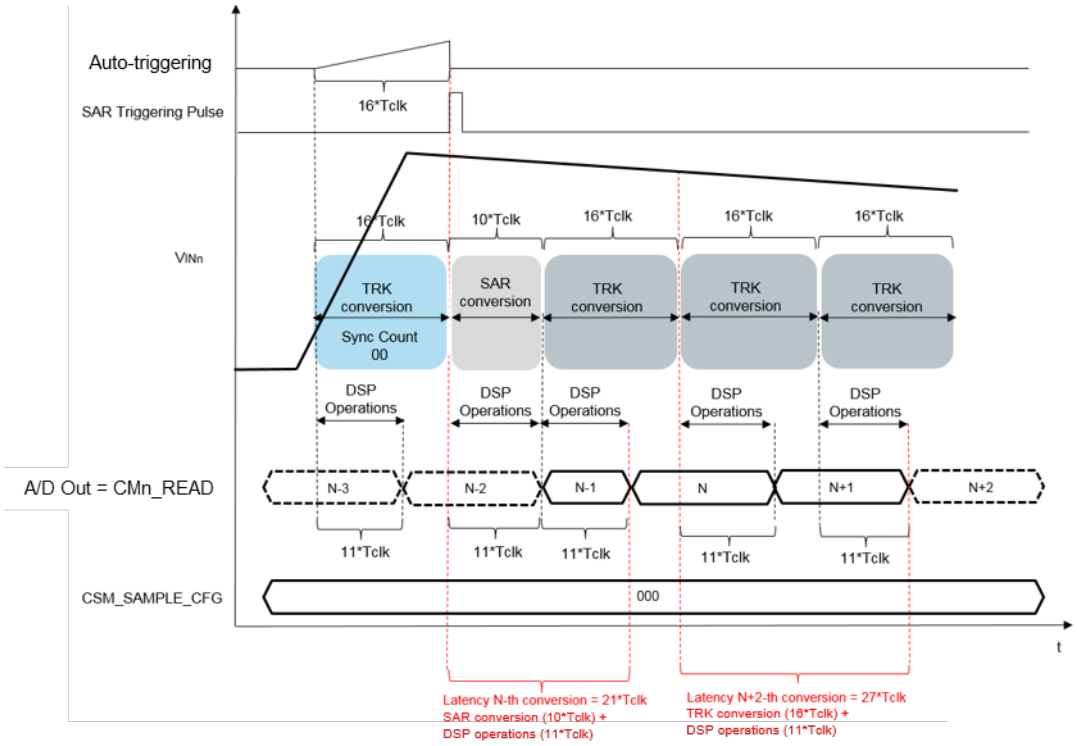


Figure 55. **Free running sampling timing diagram - non-zero current + auto-triggering, latency to CSOn**

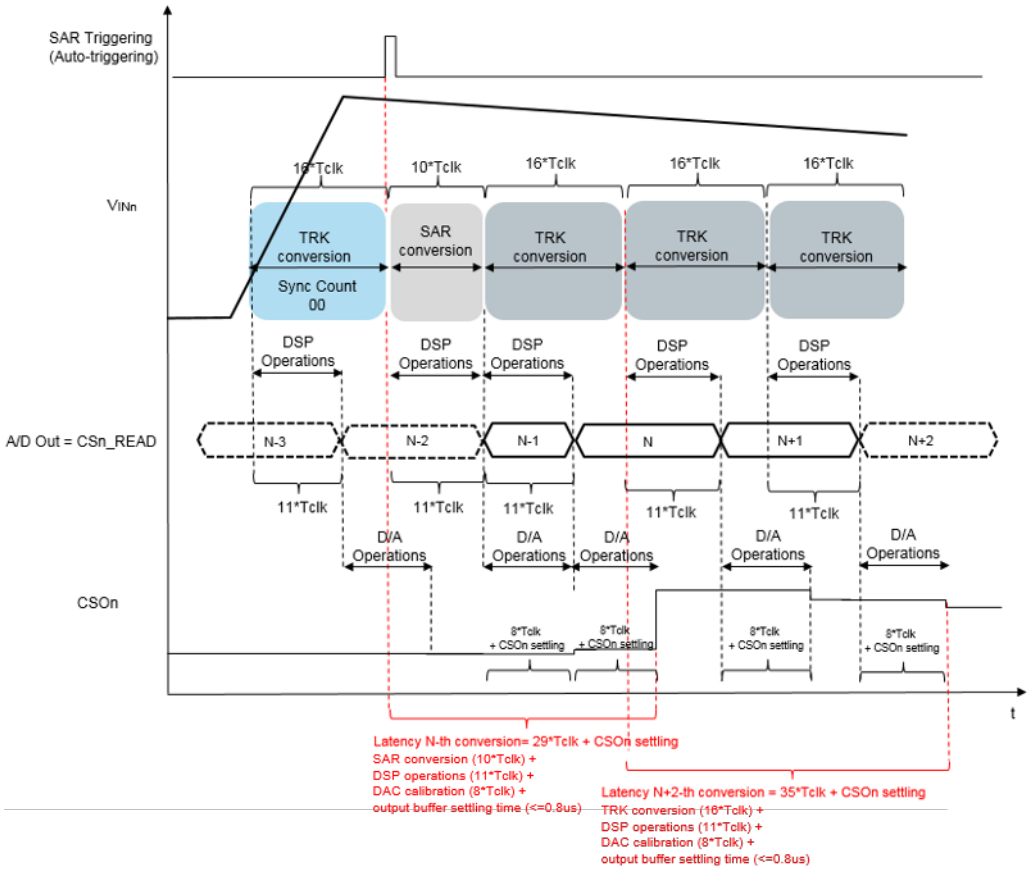


Figure 56. **Free running sampling timing diagram - non-zero current + command edge-triggering**

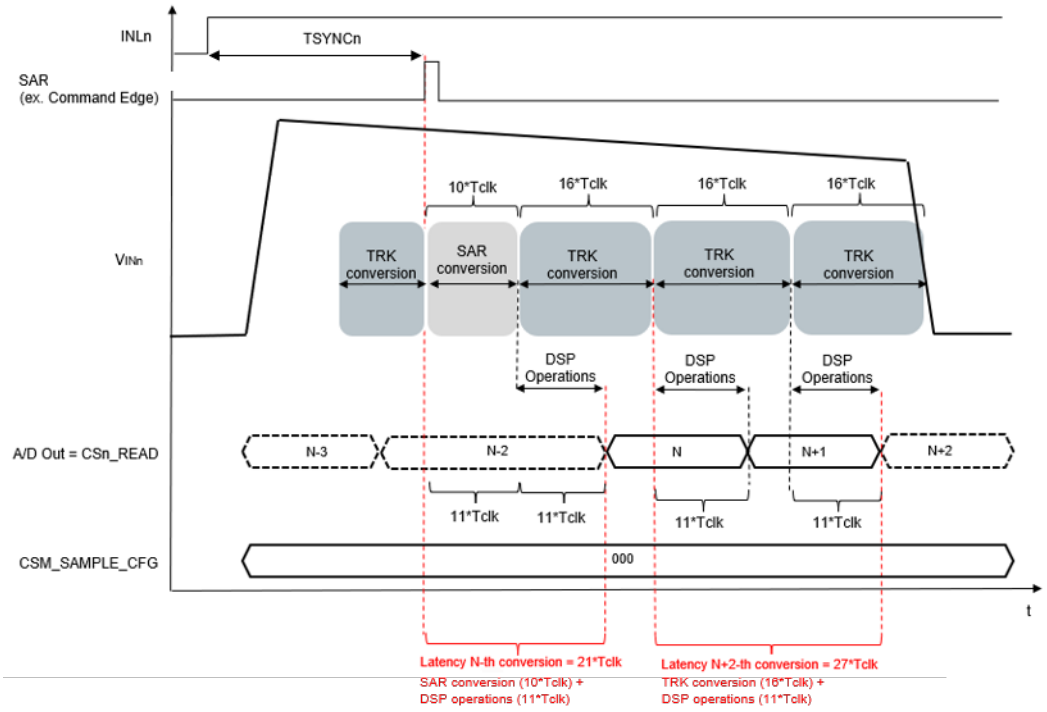


Figure 57. **Free running sampling timing diagram - zero current (offset) + auto-triggering**

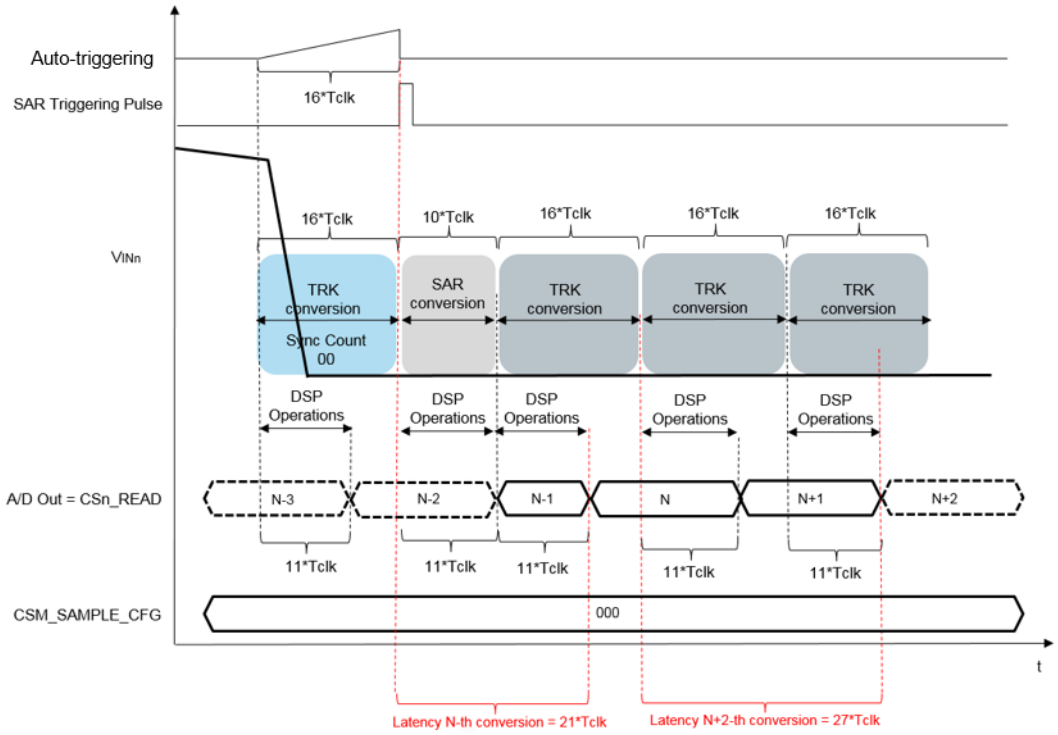
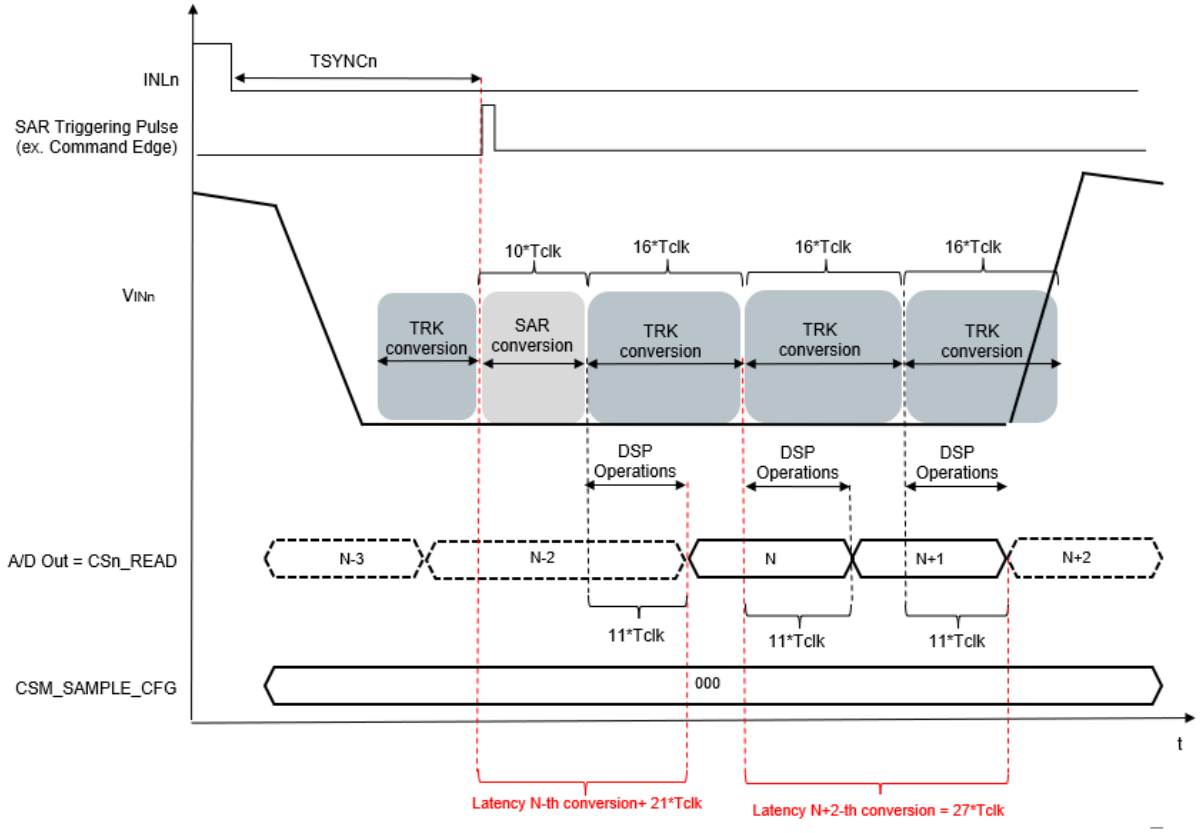


Figure 58. **Free running sampling timing diagram - zero current (offset) + command edge-triggering**



5.13.2.2.2 Track and hold

In Track and Hold mode the CMn_READ SPI registers and the CSOn voltage track the A/D output starting from the SAR Triggering Pulse and hold the n-th conversion specified in the CSM_SAMPLE_CFG register.

As a consequence, this kind of sampling method is useful along with a command edge triggering. It turns out that if no Command Edge is present (ex. INLn rising/falling) the CMn_READ SPI registers and the CSOn voltage display the last written value.

All A/D output words [phase 1, 2, 3] are tracked and sampled at the same time, synchronously.

The n-th data conversion after the SAR triggering to be hold can be configured by means of the following bits:

Table 74. **Current monitors sampling configuration bits**

CSMn_SAMPLE_CFG3	CSMn_SAMPLE_CFG1	CSMn_SAMPLE_CFG0	Description
0	0	0	Free running – No T&H (Default)
0	0	1	T&H 1st data conversion from triggering
0	1	0	T&H 2nd data conversion from triggering
0	1	1	T&H 3rd data conversion from triggering
1	0	0	T&H 4th data conversion from triggering
1	0	1	T&H 5th data conversion from triggering
1	1	0	T&H 6th data conversion from triggering
1	1	1	T&H 7th data conversion from triggering

Note: CSM_SAMPLE_CFG and CSM_SSPV_PH_CFG configurations can be separately configured with no internal gating.

This way all the following configurations are allowed to take place in principle:

1. *Auto-Triggering only (NO Command Edge) + Free Running*
2. *Auto-Triggering only (NO Command Edge) + T&H*
3. *Command Edge Triggering + Free Running*
4. *Command Edge Triggering + T&H*

In scenario 2) CMn_READ and CSOn value won't be updated and the value displayed reflects the last valid value or the default non valid value as ever been captured.

This possibility in case not specifically needed by application shall be avoided by the application SW itself.

Note: In the following timing diagrams, N-th A/D Out value corresponds to the SAR conversion value.

Figure 59. T&H sampling timing diagram - non-zero current + auto-triggering

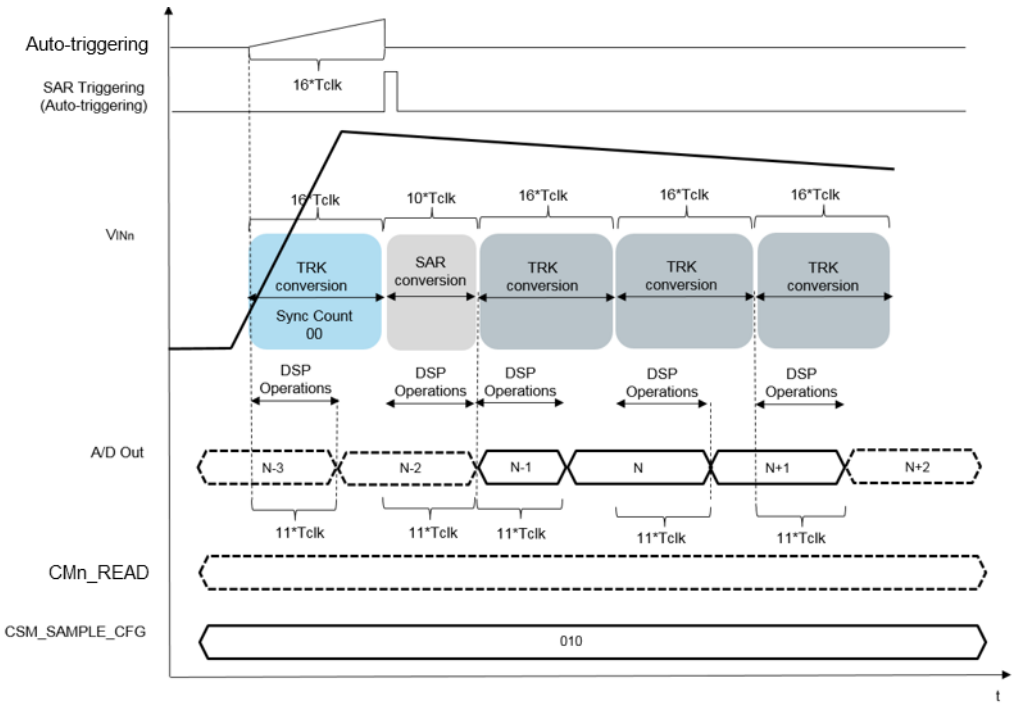


Figure 60. **T&H sampling timing diagram - zero current (offset) + auto-triggering**

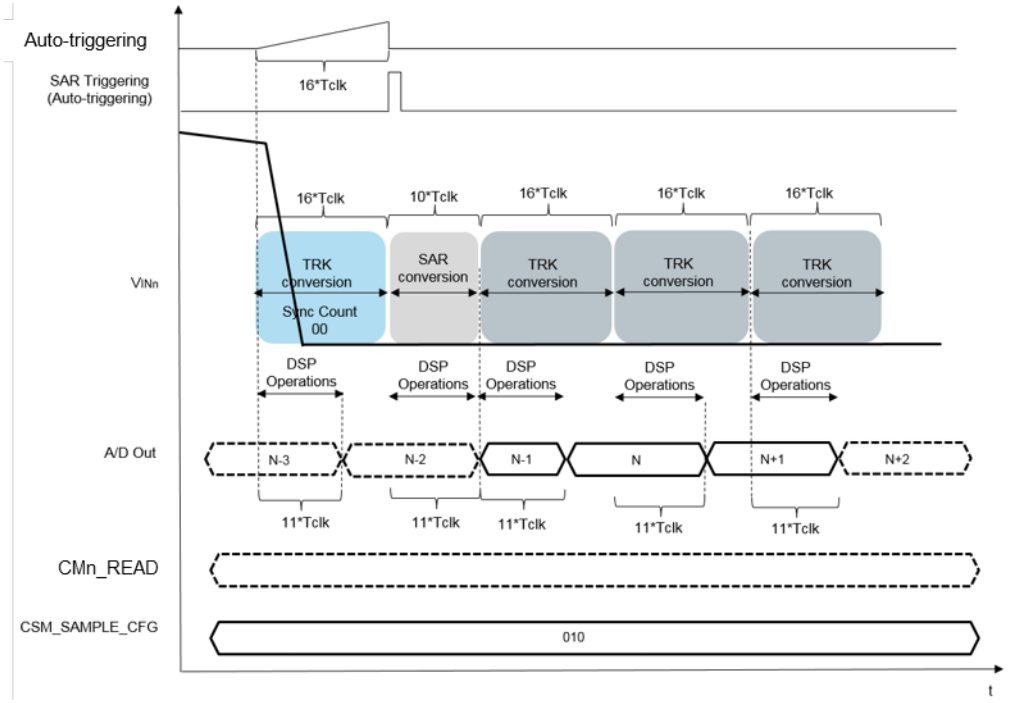


Figure 61. **T&H sampling timing diagram - non-zero current + command edge-triggering**

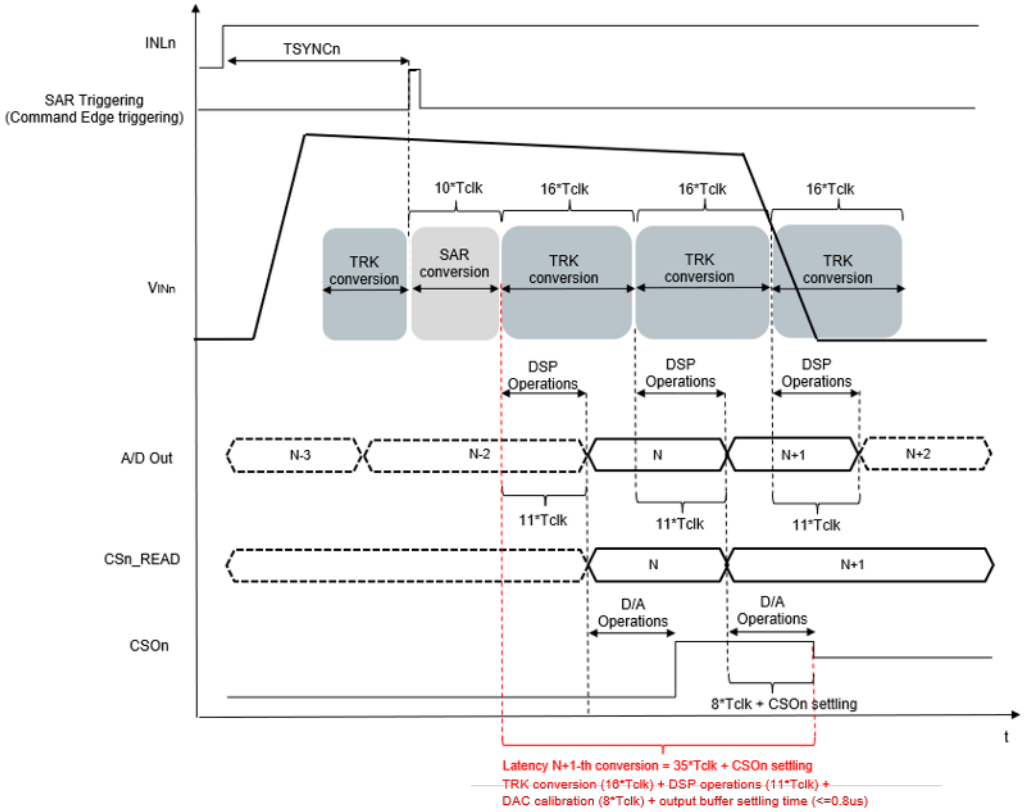
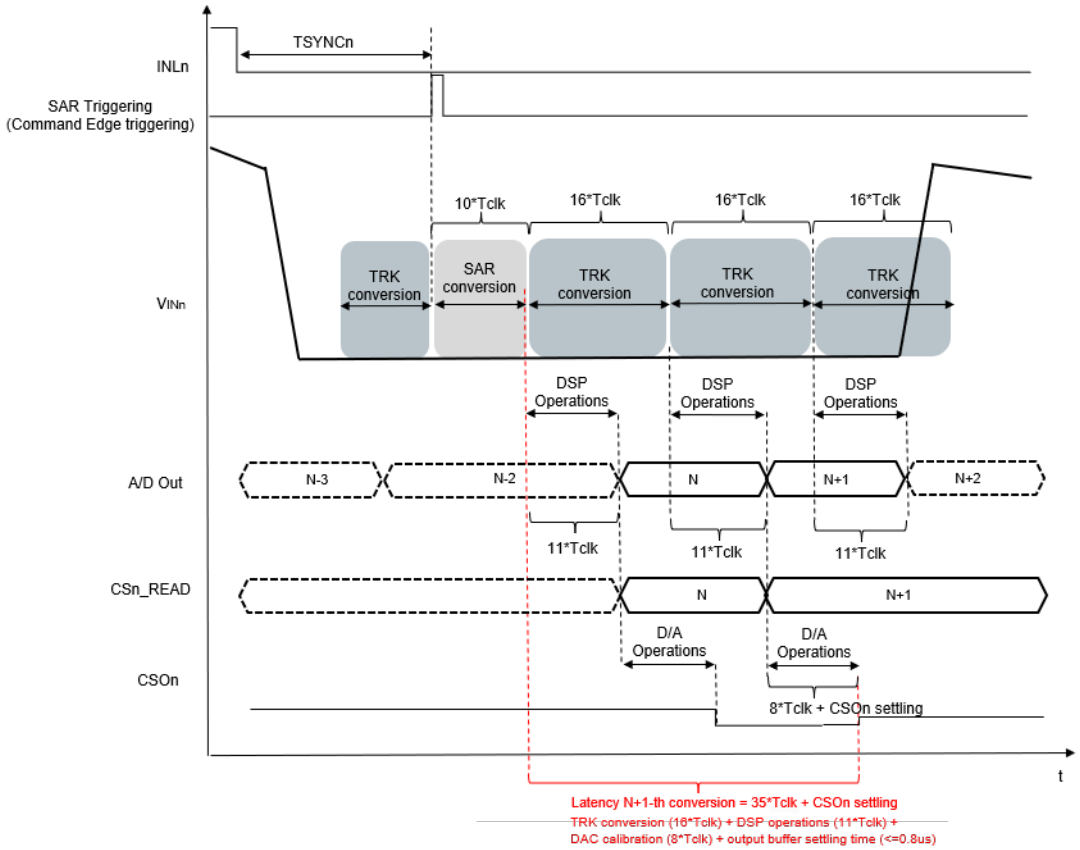


Figure 62. **T&H sampling timing diagram - zero current (offset) + command edge-triggering**



5.13.2.3 *Digital format current information*

The current measurement is available in digital format right after the T&H block and can be read through a dedicated SPI signal (CMn_READ in CHn_STATUS2 register).

Current Measurement reconstruction formula

Internal conversion data read-out via CMn_READ registers:

$$I_{LOAD}{}^{R}shunt = \Delta_{CM\_in\_LSB\_15bit} \times {}^{D}CMn\_READ \quad (17)$$

Where: D_{CMn_READ} is the digital word stored in C_{Mn_READ} and $\Delta_{CM\_in\_LSB\_15bit}$ is the input ADC quantization step re-defined as follows:

$$\Delta_{CM\_in\_LSB\_15bit} = \frac{CM\ input\ ADC\ LSB}{2^4} \quad (18)$$

Table 75. **Digital format current information LSB**

VCM_MAX	ΔCM_in_LSB_15bit
±7 mV	0.628 µV
±18 mV	1.256 µV
±36 mV	2.517 µV
±90 mV	6.293 µV
±160 mV	11.329 µV
±300 mV	20.141 µV

D_{CMn_READ} coding in two`s complement.

Example:

D_{CMn_READ} = 101100011110101 (binary) → - 9995 (decimal)

CS_INRANGE_CFG = 011 (CM input ADC range +/-90 mV)

I_{LOAD} R_{SHUNT} = - 9995 *6.293 µV = -62.898 mV

Latency associated to digital format current information update (SPI) in auto-triggering mode can be retrieved in the following table.

Table 76. Current monitors A/D auto-triggering latency

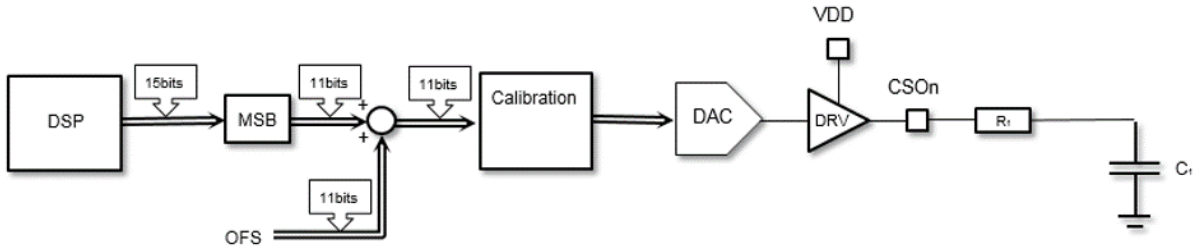
Symbol	Parameter	Min	Typ	Max	Unit	Notes
CM_in_latency	CM Input latency	31 39 47 55	-	37 45 53 61	Tclk	Application information(1)

1. *CSMn_SYNC_COUNT_CFG1 (16/24/32/40 Tclk) + SAR (10 Tclk) + DSP (5 to 11 Tclk).*

5.13.3 D/A conversion

After DSP operations digital conversion is forwarded to an analog output channel which provides the processed current information to the analog domain.

Figure 63. D/A conversion simplified block diagram



In order to better fit dynamic range and maximize the output S/N with respect to the externally connected microcontroller A/D, two successive digital operations are performed.

First is the truncation from signed 15 bits to signed 11 bits.

The current measurement coded in a signed 15-bit word is firstly converted to a signed 11-bit word by taking the 11MSB.

Second is Shift and Rescale (sign removal and offset adding).

From the resulting processed word the 11MSB without sign are taken and a fixed selectable offset OFS is added (shift).

The shift amount for the specific channel can be configured by means of dedicated SPI bits in order to adjust the current monitor output range to the µC ADC input range as follows:

Table 77. Current monitors output offset configuration bits

CSMn_OFS1	CSMn_OFS0	Description
0	0	0LSB DAC
0	1	90LSB DAC
1	0	1024LSB DAC
1	1	1024LSB DAC (Default)

Note:

- *00 and 01 configurations are intended to be used when the current to be read is only positive (DC-LINK configuration)*
- *10 and 11 configurations should be used when the current to be read is either positive or negative (Single Leg)*

The 11-bits unsigned word feeds a cascaded of a 10-bit resistive string DAC and a Voltage Buffer that converts the digital code into the corresponding analog signal referred to the full scale voltage.

DRV gain can be configured by means of dedicated SPI bits in order to adjust the current monitor output range to the µC ADC input range as follows:

Table 78. Current monitors output gain configuration

CSM_OUT_RANGE_CFG	Description
0	VCSO = 3.3 V (Default)
1	VCSO = 5 V

To ensure output signal stability, a RC low-pass filter is recommended on CSOn pins; refer to Section 6 Application circuit and the related Section 6.3 Bill of materials for details.

Table 79. Current monitor`s analog output characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
Current Monitor Analog Output							
CM_out_range_max	CSOn output range max	Iload = 250 µA	-	-	0.11	V	-
CM_out_range_min	CSOn output range min	Iload = -250 µA CSMn_OUT_RANGE_CFG = 1 CSMn_OUT_RANGE_CFG = 0	4.8 3.28	-	VDD 3.32	V	-
Current Monitor Analog Output Resolution							
CM_out__dac_res	CM DAC resolution	-	-	11	-	bits	Design Information
CM_out_dac_lsb	CM DAC LSB	-	-	2.441 1.611	-	mV	Design Information
Current Monitor Analog Output Dynamic Characteristics							
CM_out_dac_data_rate	CM DAC sample rate	-	-	1.25	-	MHz	Application information
CM_out_dac_pos_st1	CM DAC positive settling time 1	23 to 1023 LSB transition RLP = 1 kΩ CLP = 270 pF	-	-	0.8	µs	-
CM_out_dac_pos_st2	CM DAC positive settling time 2	1023 to 2048 LSB Transition RLP = 1 kΩ CLP = 270 pF	-	-	0.8	µs	-
CM_out_dac_neg_st1	CM DAC negative settling time 1	2048 to 1023 LSB transition RLP = 1 kΩ CLP = 270 pF	-	-	0.8	µs	-
CM_out_dac_neg_st2	CM DAC negative settling time 2	1023 to 23 LSB Transition RLP = 1 kΩ CLP = 270 pF	-	-	0.8	µs	-

5.13.3.1 *Analog format current information*

Current Measurement reconstruction formula at CSO_n pin is the following:

$$I_{LOAD}R_{shunt} = \left(\frac{V_{CSO\_n}}{\Delta_{CM\_out\_LSB}} - OFS\right)\Delta_{CM\_in\_LSB} \quad (19)$$

Where: V_{CSO_n} is the voltage at pin CSO_n, OFS is the selected shift value, R_{SHUNT} is the shunt resistance value, $\Delta_{CM\_in\_LSB}$ is the input ADC quantization step, defined in Table 75, and $\Delta_{CM\_out\_LSB}$ is D/A quantization step, available in Table 79 (parameter name: T CM_out_dac_lsb).

Example:

- VCSO_n = 1 V
- CSMn_OFS = 1024LSB
- CSM_OUT_RANGE_CFG = 0
- CSM_OUT_RANGE_CFG = 0
- CS_INRANGE_CFG = 011 (CM input ADC range +/-90 mV)
- ILOAD*RSHUNT = (1/1.611 mV - 1024)*100.7 µV = -40.609 mV

Latency associated to analog format current information update in auto-triggering mode can be retrieved in the following table.

Table 80. Current monitors A/D - D/A auto-triggering latency

Symbol	Parameter	Min	Typ	Max	Unit	Notes
CM_latency	CM latency	33 41 49 57	-	45 53 61 69	Tclk	Application information(1)

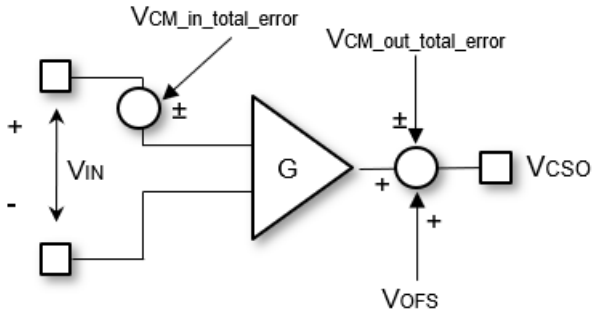
1. *CSMn_SYNC_COUNT_CFG1 (16/24/32/40 Tclk) + SAR (10 Tclk) + DSP (7 to 19 Tclk)*

Note: Please note that values indicated in Table 80 refers to ADC & DSP section only. CSO buffer settling time should be added to retrieve the full chain settling time at CSOn.

5.13.4 Current monitor A/D - D/A chain

When Current Measurement is evaluated at CSOn pins, the full A/D-D/A chain is exploited and the structure can be assimilated to a voltage amplifying stage, which can be represented as in the following picture, and the corresponding Input/Output transfer function:

Figure 64. A/D-D/A chain accuracy block diagram



$$V_{CSO} = V_{IN}G \pm V_{CM\_in\_total\_error}G + V_{OFS} \pm V_{CM\_out\_total\_error} \quad (20)$$

CSM chain gain values are summarized in the following table.

Table 81. **CSM gain**

CSM input range FULL SCALE	GAIN output range: 0-5V	GAIN output range: 0-3.3V
±7 mV	242.8856	160.2985
±18 mV	121.3824	80.1094
±36 mV	60.60079	39.99503
±90 mV	24.24032	15.99801
±160 mV	13.4661	8.887295
±300 mV	7.574629	4.999069

Gain is calculated as the ratio between CSO output range (either 3.3 V or 5 V) and the input Full Scale range. Values in Table 81 are valid only in case OFS = 1024 lsb. OFS = 0 lsb and OFS = 90 lsb have to be used in case of DC-link configuration; in this case input voltage can be only positive and gain values of Table 81 must be multiplied by 2.

Total error:

The CM A/D – D/A Chain total error contribution is given by:

Table 82. **Current monitor A/D - D/A total error**

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Current Monitor Accuracy						
CM_gain_err	CM Gain Error	-2	-	2	%	(1) All input ranges
CM_offset_err	CM Offset Error	-2 -2 -2 -2 -3 -6	-	2 2 2 2 3 6	mV	(1) Each value refers to the corresponding CM differential voltage input range

1. *Ex.*
   - *Vin = ISn+ - ISn- = -70 mV*
   - *CM_in_range_diff = ±90 mV*
   - *CM_out_range = 3.3 V*
   - *CSM_OFS = 1024*
   - *VOFS = 1024*1.611 mV = 1.65 V*
   - *G = 15.99801*
   - *V_CM_total_error = ±2 mV ± (2%*70 mV) = ±2 mV ±1.4 mV = ±3.4 mV*
   - *Vout (ideal) = 1.65 V-70 mV*15.99801 = 530 mV*
   - *Vout (minimum) = Vout (ideal) – (3.40 mV*15.99801) = 475.60 mV*
   - *Vout (maximum) = Vout (ideal) + (3.40 mV*15.99801) = 584.39 mV*

Noise Performance

Table 83. **Current monitor chain noise performance**

Symbol	Parameter	Min	Typ	Max	Unit	Notes
CM_noise_performance	CM integrated output noise voltage	-	9.7 4.5 2.6	-	mV (RMS)	Application information(1)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
			1.4 1.2 1.2			

1. *Measurement setup: Tj = 25ºC IS+n = IS-n, RLP = 1 kΩ; CLP = 270 pF; VOFS = 2.5 V. Measured after low pass filter.*

5.14 Off State Diagnosis (OFD)

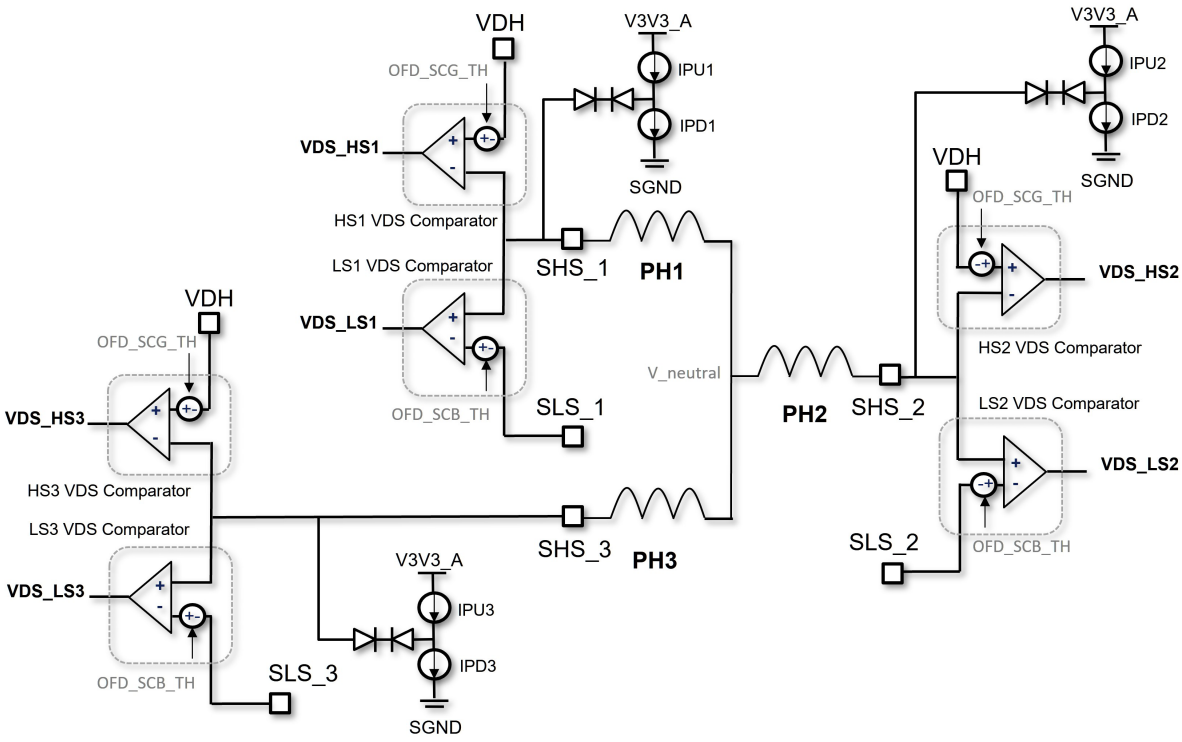
L9908 implements a monitoring unit to detect failure condition affecting the load during the half bridges tristate condition (VGHn - VSHn = 0 V and VGLn - VSLn = 0 V).

Load Failure Mode Detection:

- Open load at one of the SHS_n terminals;
- Short-circuit to ground at one or multiple SHS_n terminals;
- Short-circuit to battery at one or multiple SHS_n terminals.

Each error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

Figure 65. OFF State Diagnosis simplified block diagram



The off state diagnosis unit is composed by a multiple force stage and a multiple monitor stage.

The force stage has the purpose of driving the state of each SHS_n terminal into a predetermined voltage condition, any deviation from this condition is then detected by the monitor stage and interpreted as a faulty condition.

Force stage is composed by a protected controlled pull-up/pull-down current source for each phase respectively towards V3V3_A and SGND.

Monitor stage is composed by the LS VDS and the HS VDS comparators which compare the n-th phase voltage with respectively OFD_SCB_TH and OFD_SCG_TH fixed thresholds.

The n-th phase OFD unit can be enabled/disabled by dedicated SPI bits as follows:

Table 84. OFD enable bits

OFDn_EN1	OFDn_EN0	Description
0	0	Off State Diagnosis disabled (Default)
0	1	Pull-up current enabled, Pull-down current disabled
1	0	Pull-down current enabled, Pull-up current disabled
1	1	Off State Diagnosis disabled

The OFD is automatically enabled when OFD_EN bit is set and INLn/INHn = 0 [n = 1,2,3]. Once enabled, the OFD circuit is stopped as soon as a 0 → 1 transition of INHn/INLn is detected.

Depending on the external load condition, the OFD configuration and detection shall follow the next table:

Table 85. OFD fault detection table

Condition	OFD_EN[1:0]	Error Flag	Description
3-Phase OFD [Three phase load]	OFD1 = 10 OFD2 = 01 OFD3 = 10	HS2_OFD = X(1) LS1_OFD = 0 LS2_OFD = 0 LS3_OFD = 0	Short to ground on one or multiple motor phase
		HS2_OFD = 0 LS1_OFD = 1 LS2_OFD = 1 LS3_OFD = 1	Short to battery on one or multiple motor phase
		HS2_OFD = X(1) LS1_OFD = 0 LS2_OFD = 1 LS3_OFD = 1	Open connection on motor phase 1 (SHS_1)
		HS2_OFD = X(1) LS1_OFD = 0 LS2_OFD = 1 LS3_OFD = 0	Open connection on motor phase 2 (SHS_2)
		HS2_OFD = X(1) LS1_OFD = 1 LS2_OFD = 1 LS3_OFD = 0	Open connection on motor phase 3 (SHS_3)
		HS2_OFD = 1 LS1_OFD = 1 LS2_OFD = 1 LS3_OFD = 1	No Fault

1. *X = don't care.*

Note:

- *The OFD circuit can detect a SCB or SCG condition affecting the three phases in general, due to the low DC resistance of the motor it cannot identify at which phase the failure is present.*
- *Correct functionality of OFD is based on a current mismatch between pull-up and pull-down current. In case of additional external pull-up/down contribution the following inequation must be satisfied:*

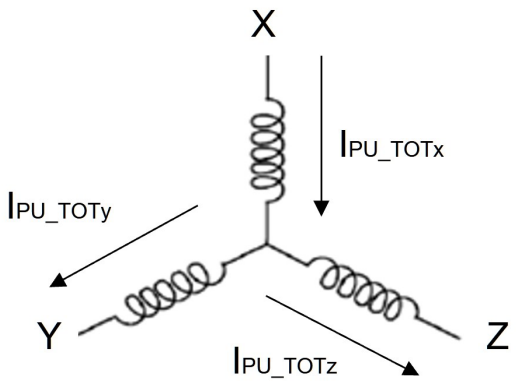
$$I_{PU\_TOTx} > I_{PD\_TOT\_PHy} + I_{PD\_TOT\_PHz} \quad (21)$$

Where:

Ipu_totx is the equivalent pull-up current injected into the phase x (assuming phase x being configured as OFD_EN = 01)

Ipd_toty and Ipd_totz are the equivalent pull-down currents injected respectively into the phase y and z (assuming phase y and z being configured as OFD_EN = 10)

Figure 66. OFD currents in motor phases



Blanking and Filtering

To avoid false error detections during the diagnosis settling time and to increase noise robustness, the OSD implements a two-step digital filtering: an Up/Down counter of length equal to T_ofd_flt on the comparator`s output filters out the high frequency noise while a blanking time masks the filters output by a programmable delay time T_ofd_blank.

Figure 67. OFD enabling and masking time start - IPU example

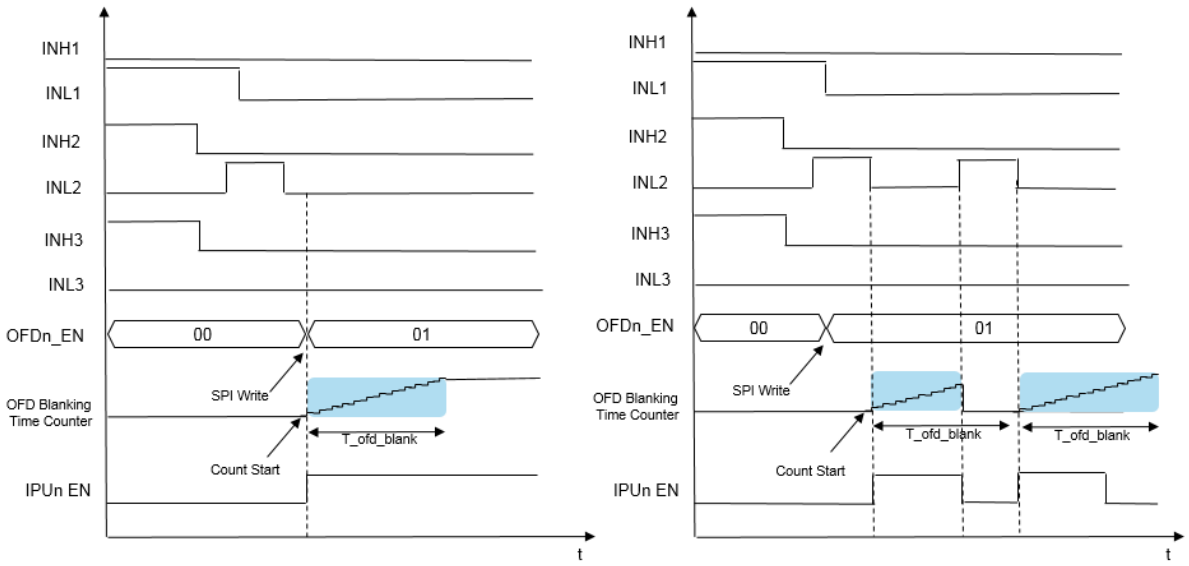


Figure 68. **OFD Masking and deglitch filtering - LSn_OFD Example**

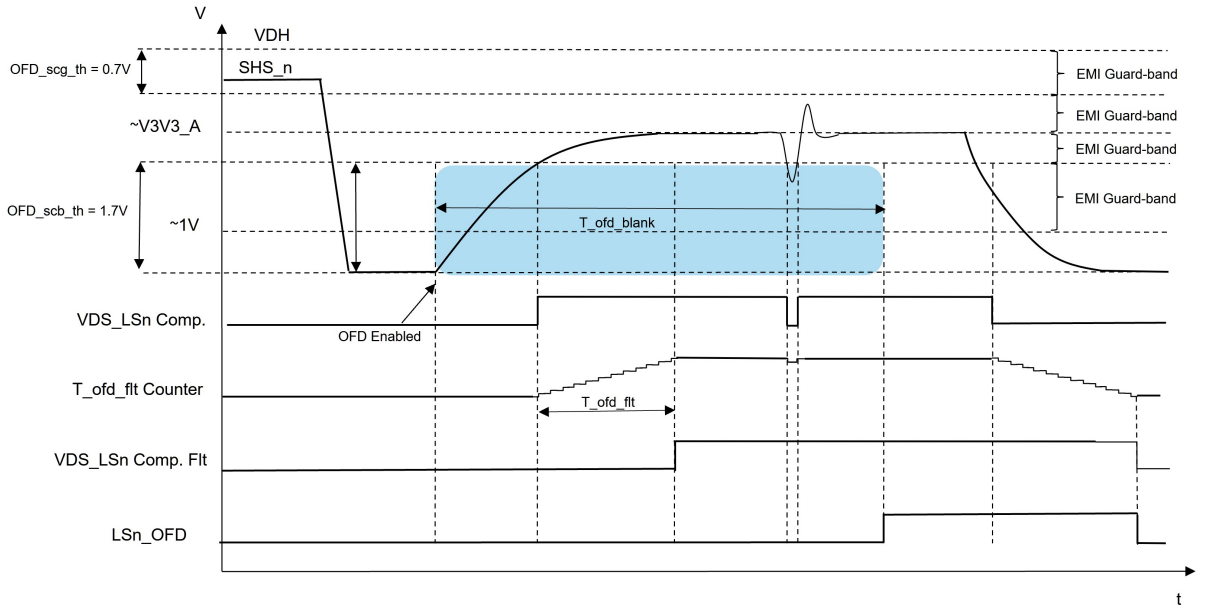
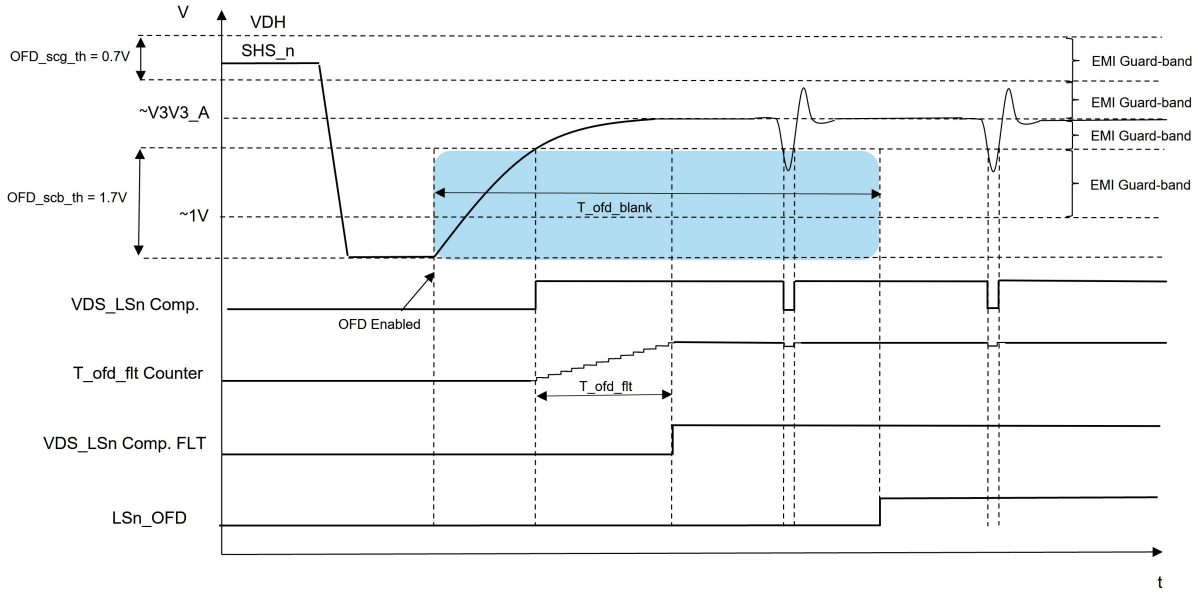


Figure 69. **OFD Masking and deglitch filtering - LSn_OFD Example with multiple glitches**



The T_ofd_blank can be configured by dedicated SPI bits as follows:

Table 86. **OFD blanking time configuration bits**

OFD_BLANK1	OFD_BLANK0	Description
0	0	T_ofd_blank = 10 ms
0	1	T_ofd_blank = 25 ms
1	0	T_ofd_blank = 50 ms (Default)
1	1	T_ofd_blank = 100 ms

Note: The application software must configure T_ofd_blank to ensure that the motor is not running and the phases are not energized. For some applications the maximum available T_ofd_blank configuration could be too short, the application SW then shall enable the OFD circuit with an additional delay after disabling the bridge drivers.

Table 87. OFD electrical characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
OFD_rvef	OFD phase reference voltage in with no fault	OFDn_EN = 01 OFDi,j_EN = 10	2	2.7	3.1	V	-
OFD_vpd_ol	OFD open load voltage in pd mode	OFDn_EN = 10 SHS_n = No Load	-	-	0.9	V	-
OFD_ipu	OFD pull up current capability	OFDn_EN = 01	2.25	-	3.3	mA	-
OFD_ipd	OFD pull down current capability	OFDn_EN = 10	0.6	0.75	0.9	mA	It includes ILEAK contribution
OFD_scb_th	OFD_SCB detection threshold	-	-	SLS_n+1.7	-	V	Not subject to production test
OFD_scg_th	OFD_SCG detection threshold	-	-	VDH-0.7	-	V	Not subject to production test
T_ofd_flt	OFD Fault detection filter time	-	85	100	115	µs	Digital filter
T_ofd_blank_acc	OFD Blanking Time accuracy	CLK_SSM_EN = 0	-15	-	15	%	-

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

5.15 On State Diagnosis (OND)

L9908 implements a monitoring unit to detect failure condition affecting the load during the half bridges ON state by monitoring the voltage drain-source drop across the Ext. FET.

The ON state diagnosis unit is composed by a dedicated VDS comparator for each HS and LS Ext. FET that constantly monitors the voltage drop during FET`s ON state.

ON State Load Failure Mode Detection:

- Short-circuit to ground at one SHS_n terminals → HSn_STG flag is set to 1
- Short-circuit to battery at one SHS_n terminals → LSn_STB flag is set to 1

The ON state diagnosis can be disabled by a dedicated SPI bit as follows:

Table 88. OND enable bits

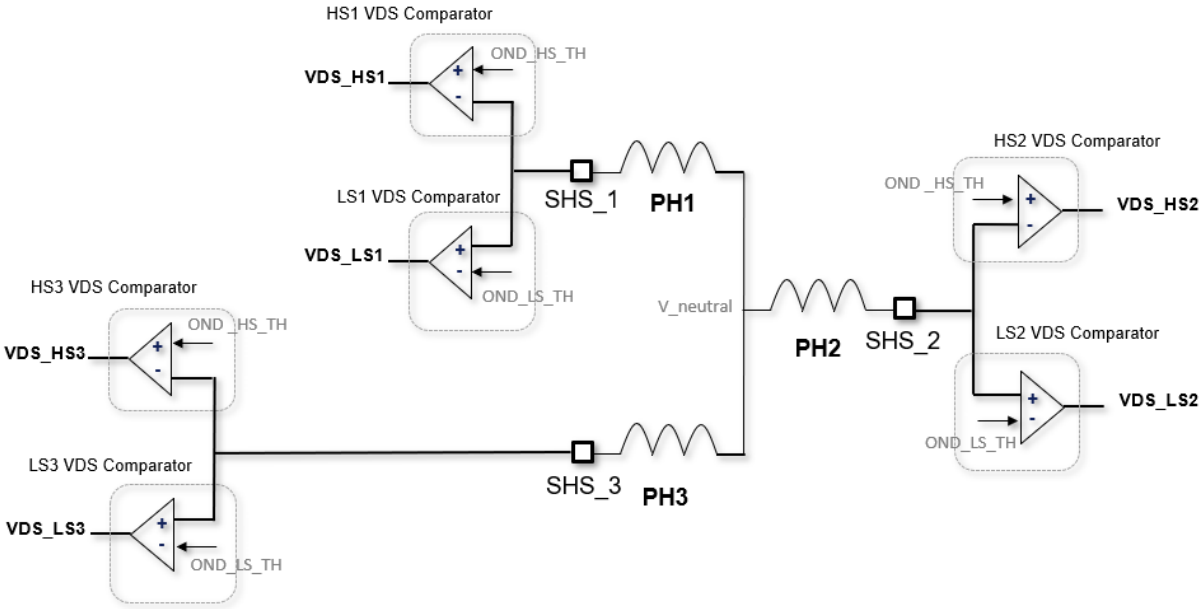
ONDn_DIS	Description
0	ON State diagnosis enabled on n-th HS and LS (Default)
1	ON State diagnosis disabled on n-th HS and LS

When the OND monitoring is disabled while having the fault flag set, the flag will not be cleared until SPI read.

If VDH-SHS_n ≥ V_ond_hs_th occurs for an interval longer than T_ond_flt filter time, the HSn_STG flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

If SHS_n-SLSn ≥ V_ond_ls_th occurs for an interval longer than T_ond_flt filter time, the LSn_STB flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

Figure 70. **ON State Diagnosis simplified block diagram**



Threshold configuration

The reference thresholds for the OND unit V_ond_th are generated through two 6-bit Current Steering DAC, one for HS and one for LS FETs.

Diagnosis thresholds can be configured through dedicated SPI bits as follows:

$$V_{OND\_TH\_HS} = \Delta_{LSB} \times VDS\_HS\_TH[5:0] \quad (22)$$

$$V_{OND\_TH\_LS} = \Delta_{LSB} \times VDS\_LS\_TH[5:0] \quad (23)$$

Where: ΔLSB is the minimum voltage step and VDS_HS_TH/VDS_LS_TH [5:0] in the register GEN_CFG2 there are the dedicated SPI configuration bits.

Default value is VDS_HS_TH = VDS_LS_TH = 0x00. The default code equals the first non-zero code 0x01 which corresponds to a Vond_hs_th = 1LSB = 27 mV

Blanking and Filtering

The OND fault detection is based on the correlation between Vds voltage with the current conducted through ohm`s law; it turns out that a correct detection can be performed only when Ext. FET is in full RdsON mode.

In order to prevent spurious short circuit detections due to an internal circuit voltage compression, the n-th OND monitor circuit is masked by the VDH UV diagnosis assertion. During a VDH UV condition OND fault detection is always prevented.

In order to prevent spurious short circuit detections due to a non-linear operation region, the n-th OND monitor circuit is masked according to the internal n-th gate drive signal:

- masking is removed after a programmable blanking time T_ond_blank from gate drive signal rising edge;
- masking is re-activated soon after gate drive signal falling edge.

The T_ond_blank can be configured by dedicated SPI bits as follows:

Table 89. **OND blanking time configuration bits**

OND_BLANK2	OND_BLANK1	OND_BLANK0	Description
0	0	0	T_ond_blank = 0.7 µs
0	0	1	T_ond_blank = 1 µs
0	1	0	T_ond_blank = 1.5 µs (Default)
0	1	1	T_ond_blank = 2 µs
1	0	0	T_ond_blank = 2.5 µs

OND_BLANK2	OND_BLANK1	OND_BLANK0	Description
1	0	1	T_ond_blank = 3.5 µs
1	1	0	T_ond_blank = 5 µs
1	1	1	T_ond_blank = 8 µs

Note: The PWM ON time must be longer than T_ond_blank, else way the short circuit condition cannot be detected.

In order to remove glitches and increase the detection capability of the system also at low Duty Cycles a cascaded filtering is introduced. Filtering action is developed by a digital up/down counter, incrementing the count at fault present and decrementing it at fault absent cumulating detections all over PWM cycles.

The T_ond_flt can be configured by dedicated SPI bits as follows:

Table 90. OND filtering time configuration bits

OND_FLT1	OND_FLT0	Description
0	0	T_ond_flt= 1 µs
0	1	T_ond_flt = 2.5 µs
1	0	T_ond_flt = 4 µs (Default)
1	1	T_ond_flt = 8 µs

Figure 71. OND blanking and filtering (VDS_LSn example), multiple fault

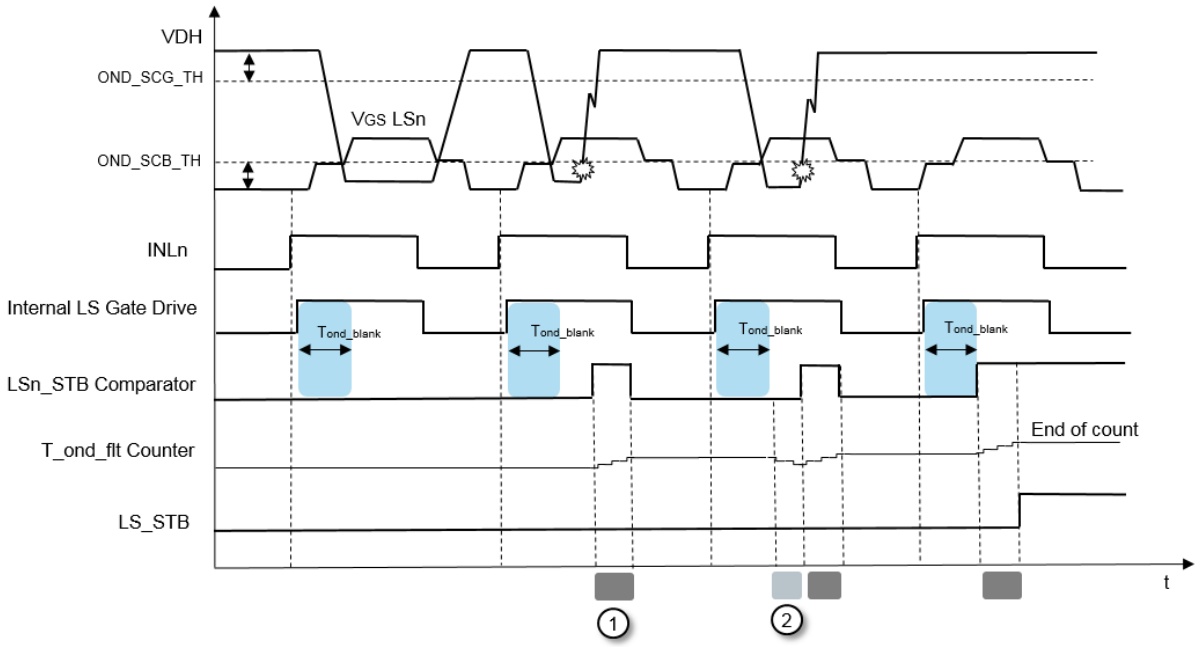
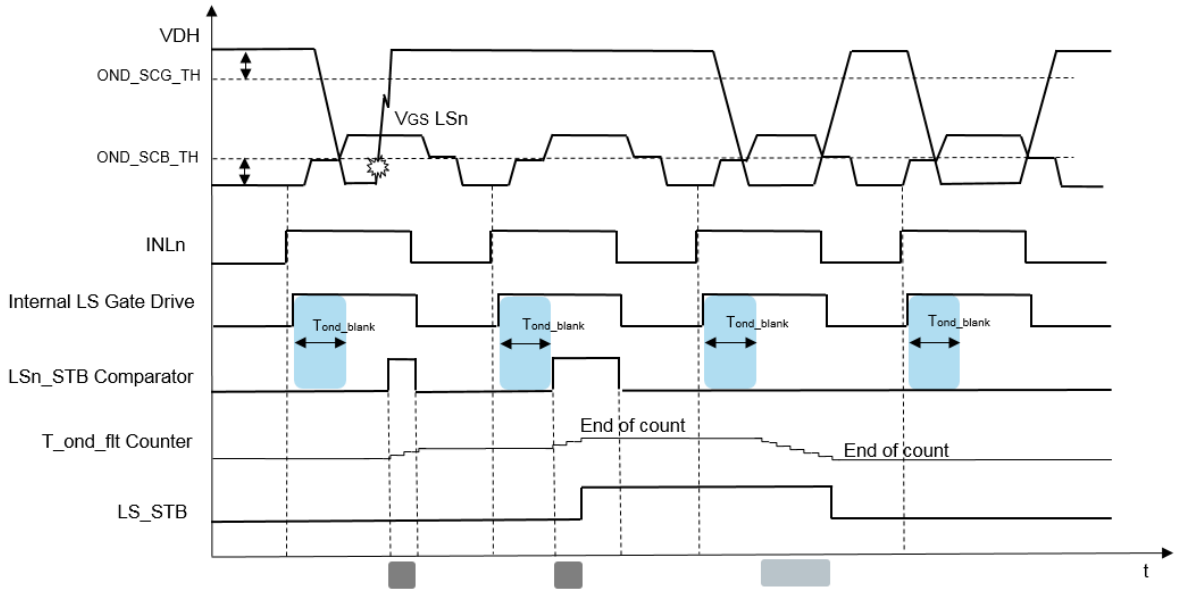


Figure 72. **OND blanking and filtering (VDS_LSn example), single fault**



Where:

1. LSn gate drive rising edge → T_ond_blank is elapsed comparator output masking is released; VSLn-VSHn > VDS_ond_th → LSn_STB comparator output is set to 1;T_ond_flt counter +1; LSn gate drive falling edge → comparator output masking is enabled → T_ond_flt counter freeze.
2. LSn gate drive rising edge → T_ond_blank is elapsed comparator output masking is released; VSLn-VSHn < VDS_ond_th → LSn_STB comparator output is set to 0; T_ond_flt counter -1; LSn gate drive falling edge → comparator output masking is enabled → T_ond_flt counter freeze.

The correct operation OND stage is safety relevant and then a self-check procedure is implemented.

Table 91. **OND electrical characteristics**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
OND_th_lsb	VDS monitoring threshold step	-	-	27	-	mV	Not subject to production test
OND_th_acc1	VDS monitoring thresholds accuracy 1	0.594 V < VDH SHS_n < 1.7 V 0.594 V < SHS_n-SLS_n < 1.7 V	-4.5	-	4.5	%	16x < VDS_HS/LH_TH < 3Fx
OND_th_acc2	VDS monitoring thresholds accuracy 2	0.324 V < VDH-SHS_n < 0.594 V 0.324 V < SHS_n-SLS_n < 0.594 V	-6	-	6	%	Cx < VDS_HS/LH_TH < 16x
OND_th_acc3	VDS monitoring thresholds accuracy 3	0.162 V < VDH-SHS_n < 0.324 V 0.162 V < SHS_n-SLS_n < 0.324 V	-10	-	10	%	6x < VDS_HS/LH_TH < Cx
OND_th_acc4	VDS monitoring thresholds accuracy 4	0.081 V < VDH-SHS_n < 0.162 V 0.081 V < SHS_n-SLS_n < 0.162 V	-15	-	15	%	4x < VDS_HS/LH_TH < 6x

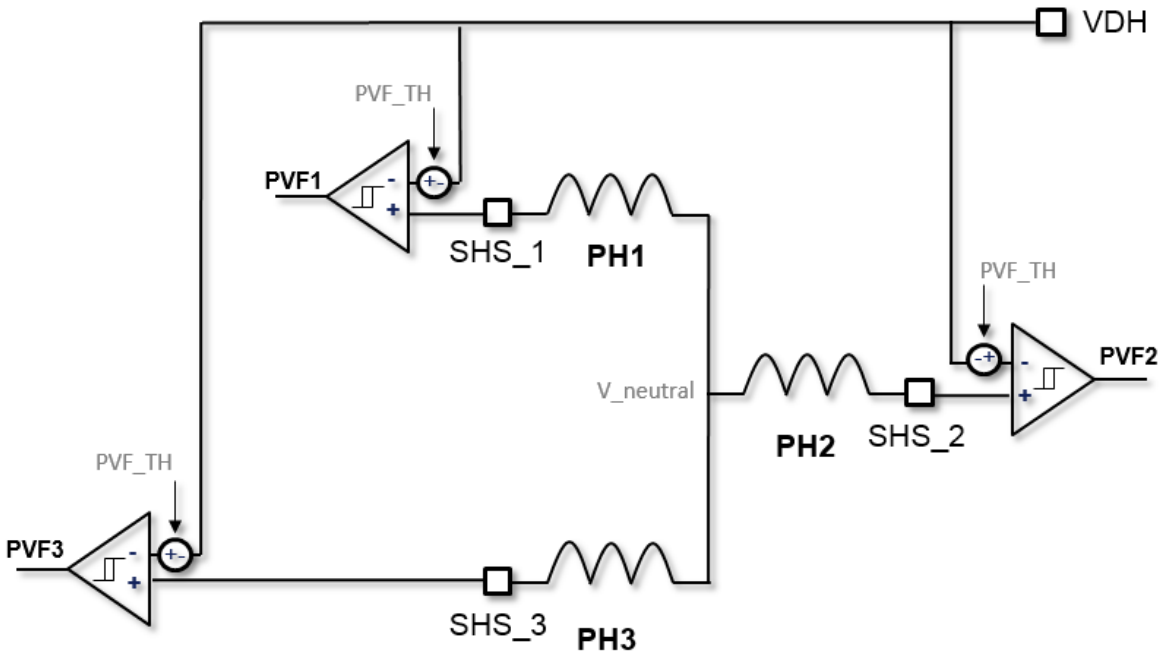
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
OND_th_acc5	VDS monitoring thresholds accuracy 5	VDH-SHS_n ≤ 0.081 V SHS_n-SLS_n ≤ 0.081 V	-12	-	12	mV	0x < VDS_HS/LH_TH < 3x
T_ond_flt_acc	OND Filtering Time accuracy	CLK_SSM_EN = 0	-15	-	15	%	-
T_ond_blank_acc	OND Blanking Time accuracy	CLK_SSM_EN = 0	-15	-	15	%	-

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

5.16 Phase Voltage Feedback (PVF)

L9908 implements three symmetric hysteretic comparators to monitor the level each motor phase voltage. This function allows a real time feedback on half bridges behavior in terms of phase voltage level and transition timing and actual phase's duty cycle.

Figure 73. Off State Diagnosis block diagram



Each phase voltage comparator converts the output phase voltage into a digital signal by comparing it against a threshold proportional to VDH voltage so that:

VDH-SHS_n ≥ PVFn_th_h: PVFn is set to 1.

VDH-SHS_n ≤ PVFn_th_l: PVFn is set to 0.

PVFn_th_h and PVFn_th_l are referred to as a specific percentage of the VDH voltage and can be configured by **PVF_TH_CFG** bits in the register **GEN_CFG4**, as follows:

Table 92. PVF threshold selection bits

PVF_TH_CFG	Description
0	VPVF_TH_H = VDH*0.75 (Default) VPVF_TH_L = VDH*0.25

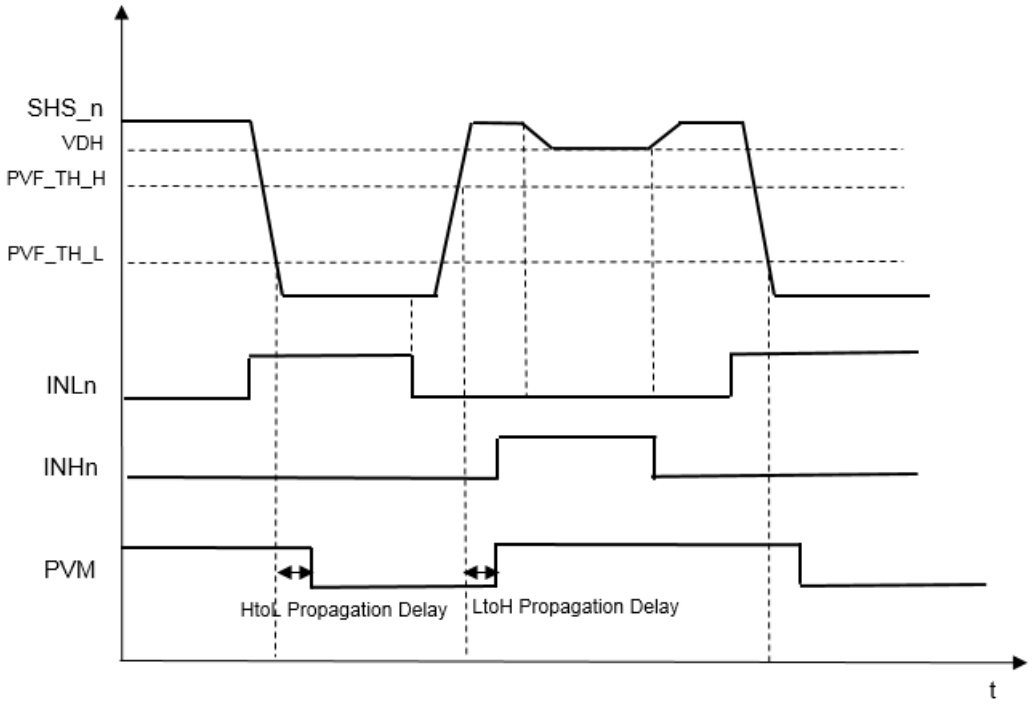
PVF_TH_CFG	Description
1	VPVF_TH_H = VDH*0.6 VPVF_TH_L = VDH*0.4

Table 93. PVF electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
PPVF_th_acc	PVF thresholds accuracy	-6.5	-	6.5	%	-
PPVF_th_match	PVF thresholds matching	-8	-	8	%	-
PPVF_htol_dly	PVF high to low propagation delay	-	-	200	ns	-
PPVF_ltoh_dly	PVF low to high propagation delay	-	-	200	ns	-
PPVF_dly_match	PVF propagation delay matching (phase vs. phase)	-	10	30	ns	-
PPVF_htol_ltoh_dly_match	PVF propagation delay matching (single phase - rise to fall)	-	20	35	ns	-

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

Figure 74. Phase voltage feedback behavior



The state of PVF comparators is echoed into dedicated SPI readable registers PVFn_ECHO, in the register GEN_STATUS3.

To save pin-count the phase comparator outputs are multiplexed to one single output pin CSO3/PVM.

The selection of which phase comparators output can be configured by means of a dedicated SPI bit set as follows:

Table 94. **PVF output redirection selection bit**

PVF_OUT_CFG0	PVF_OUT_CFG0	Description
0	0	PVF1 xor PVF2 xor PVF3 is output (Default)
0	1	PVF1 is output
1	0	PVF2 is output
1	1	PVF3 is output

5.16.1 CSO3 - PVF multiplexing

For pin saving purpose PVF and CSO3 outputs are multiplexed on the same pin and can be selected by CSO3_DIS bit in the register SAFETY_RELEVANT2:

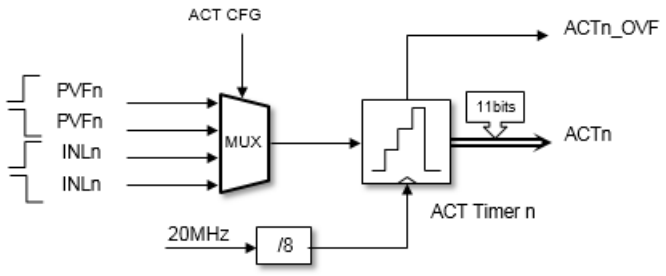
Table 95. **CSO3-PVFn output multiplexing selection bits**

CSO3_DIS	Description
0	CSO3/PVM pin used a CM3 output (Default)
1	CSO3/PVM pin used a PVFn output

5.17 Actuation Timers (ACT)

L9908 implements an additional built-in feature which measures cycle by cycle the on or the off time windows applied to each phase either on INLn or on PVFn signals. This feature is performed by three dedicated 11-bit accumulators which count the number of clock cycles (CLK/8) fitting the time window.

Figure 75. **Actuation Timer simplified block diagram**

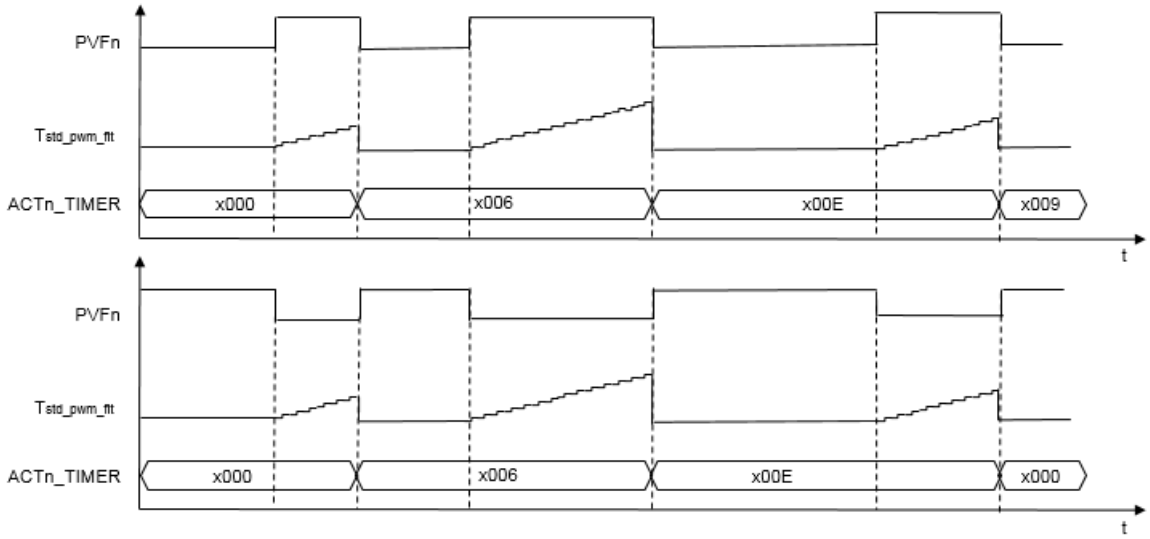


To allow the maximum flexibility against the time window to be measured, either positive or negative, timers can be configured by a proper SPI bit set to be run in negative or positive polarity so that the time is triggered respectively by the falling or the rising of the reference signal and stopped by the opposite edge.

Table 96. **Actuation Timers configuration bits**

ACT_CFG1	ACT_CFG0	Description
0	0	PVF Negative Polarity (Default)
0	1	PVF Positive Polarity
1	0	INL Negative Polarity
1	1	INL Positive Polarity

Figure 76. **Actuation Timers timing diagram on ACT (positive & negative polarity)**



The content of the count is stored into a dedicated 11bit SPI read-only register ACTn.

Reconstruction formula:

$$T_{ON-OFF} = \Delta_{ACT\_LSB} \times D_{ACTn} \quad (24)$$

Where: D_{ACTn} is the digital word stored in ACTn and Δ_{ACT_LSB} is the ACT counter quantization step.

Example:

DACTn = 10001010101 (binary) à 1109 (decimal)

ACT_CFG = 01

TON_PVF = 1109 *0.4 µs = 443.6 us ±50 ns

In case the measured time window will exceed the maximum count allowed the counter overflow is flagged by setting to '1' a dedicated SPI read-only register ACTn_OVF.

Note: when ACT overflow condition is reached on n-th counter the ACTn value keeps the full-scale value until another counting window is started or the disabling of ACT function.

The ACT function can be enabled according to the following SPI bits:

Table 97. **Actuation Timers enable bits**

ACT_EN	Description
0	ACT Disabled (Default)
1	ACT Enabled

Table 98. **Actuation Timers electrical characteristics**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
ACT_res	ACT resolution	-	-	11	-	bits	Not subject to production test
ACT_lsb	ACT LSB	-	-	0.4	-	µs	Not subject to production test
ACT_in_acc	ACT accuracy	CLK_SSM_EN = 0	-50	-	50	µs	Not subject to production test

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

Note: Internal counter is a 14-bit counter with LSB equal to 50 ns. ACT readout and TSYNC configuration however are available only through the internal counter 11MSB.

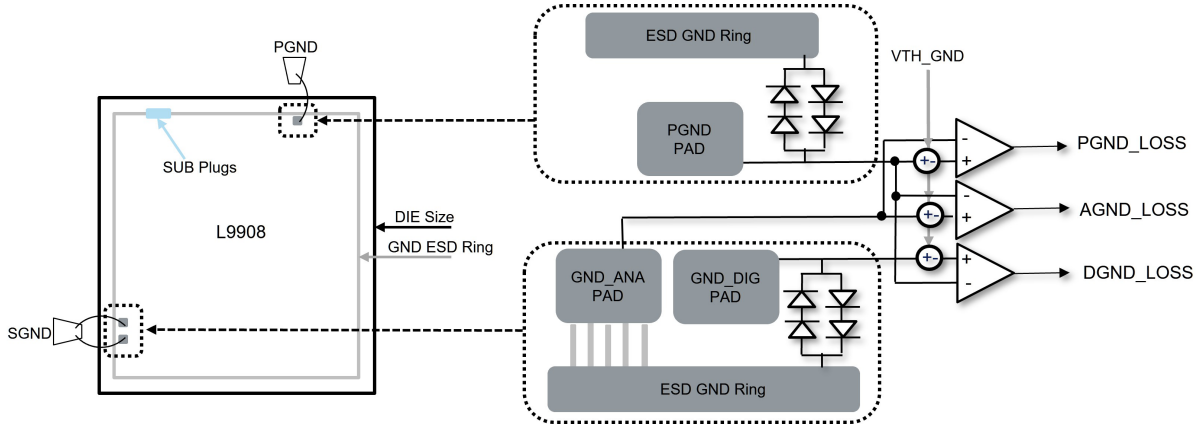
5.18 Ground Loss Monitor (GLM)

L9908 implements two ground reference pins, a Power Ground (PGND) dedicated as reference for the noisy, high power gate supply circuitry (CP1, CP2) and a Signal Ground (SGND) dedicated to the low power internal analog/digital circuitry.

For EMI robustness the GND pin is internally split in two GND reference PADs: GND_ANA (ground reference for analog circuitry supplied from V3V3_ANA) and GND_DIG (ground reference for digital circuitry supplied by V3V3_DIG), GND_ANA is connected to the ESD GND ring by means of a direct metal connection and bias the substrate through SUB Plugs placed all around IC border.

GND_ANA and PGND are connected to the ESD GND by means of a standard ESD protection for ground pins composed by a double couple of anti-parallel LV diodes.

Figure 77. Ground pins inter-connection



L9908 implements a monitoring unit to detect disconnection affecting ground references.

If VPGND-VGND_ANA ≥ VTH_GND occurs for an interval longer than T_glm_loss_flt filtering time, the PGND_LOSS flag is set.

If VGND_DIG-VGND_ANA ≥ VTH_GND occurs for an interval longer than T_glm_loss_flt filtering time, the DGND_LOSS flag is set.

If VGND_DIG-VPGND ≥ VTH_GND occurs for an interval longer than T_glm_loss_flt filtering time, the AGND_LOSS flag is set.

The correct operation Ground Loss Monitor stage is safety relevant and then a self-check procedure is implemented.

Table 99. GLM electrical characteristics

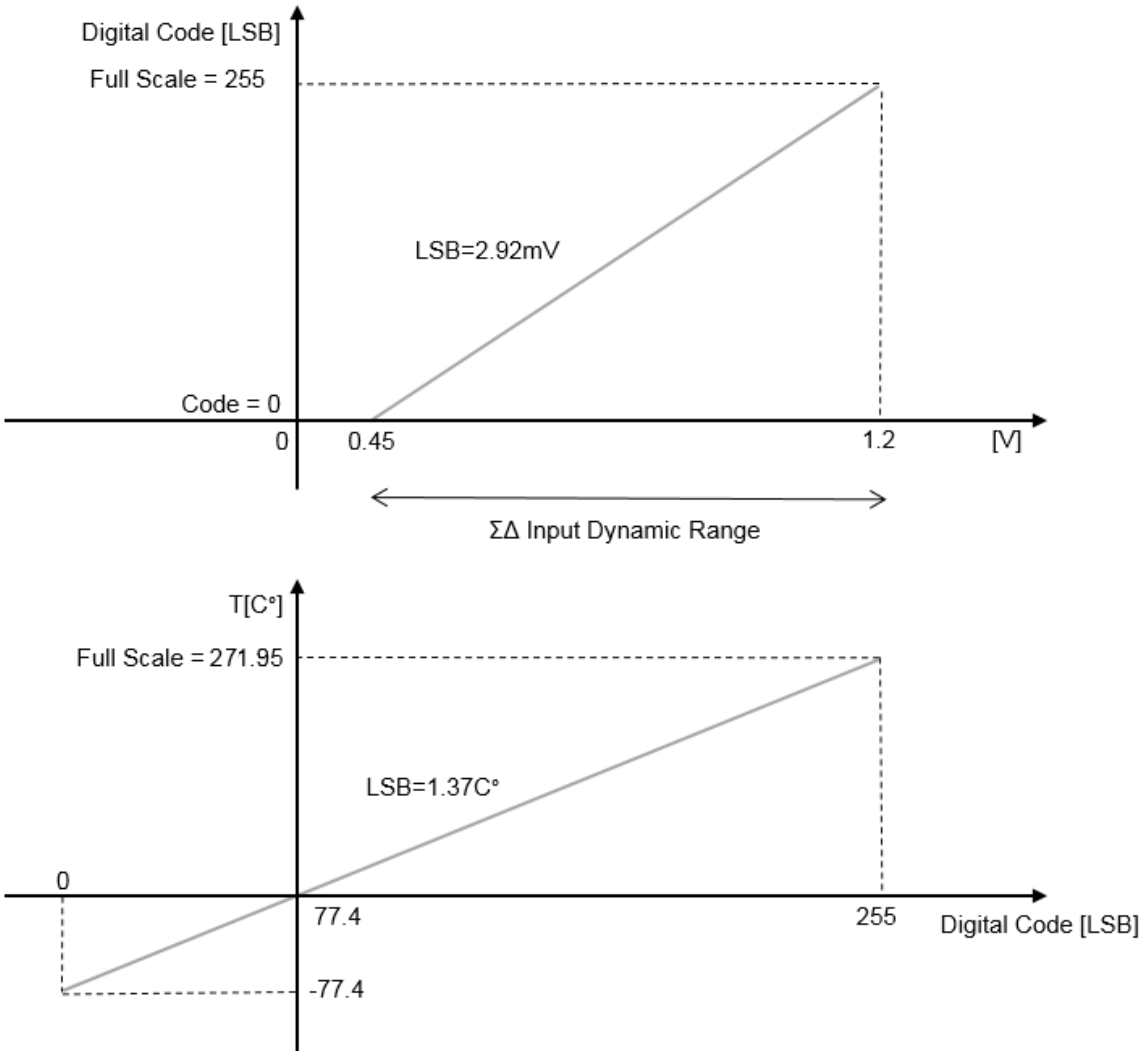
Symbol	Parameter	Min	Typ	Max	Unit	Notes
GLM_th	GLM detection threshold VTH_GND	0.24	0.4	0.55	V	-
T_glm_loss_flt	GLM filter time	1	1.25	1.5	ms	Digital Filter

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

5.19 Temperature Monitor (OTM)

L9908 implements a monitoring unit of the average junction temperature able to detect excessive over-heating conditions affecting the device.

Figure 78. **Temperature monitor ADC characteristics**



The temperature measurement data are stored in a dedicated register and can be retrieved by SPI readout of TEMP_READ in the register GEN_TEMP_STATUS.

The temperature can be retrieved by the following formula:

$$T_j[^\circ C] = (1.37^\circ C \times D_{TEMP\_READ}) - 77.4^\circ C \quad (25)$$

Where: DTEMP_READ is the digital word stored in TEMP_READ.

The digitized temperature information is compared by two hysteresis comparators with selectable threshold based on the following scheme:

If DTEMP ≥ DTEMP_WR_TH occurs for an interval longer than T_otm_wr_flt filtering time, the OTM_WR flag is set. The error flag remains set until the failure condition is removed.

If DTEMP ≥ DTEMP_SD_TH (= 185deg.) occurs for an interval longer than T_otm_sd_flt filtering time, the OTM_SD flag is set. The error flag remains set until the failure condition is removed and the flag is cleared by the SPI command.

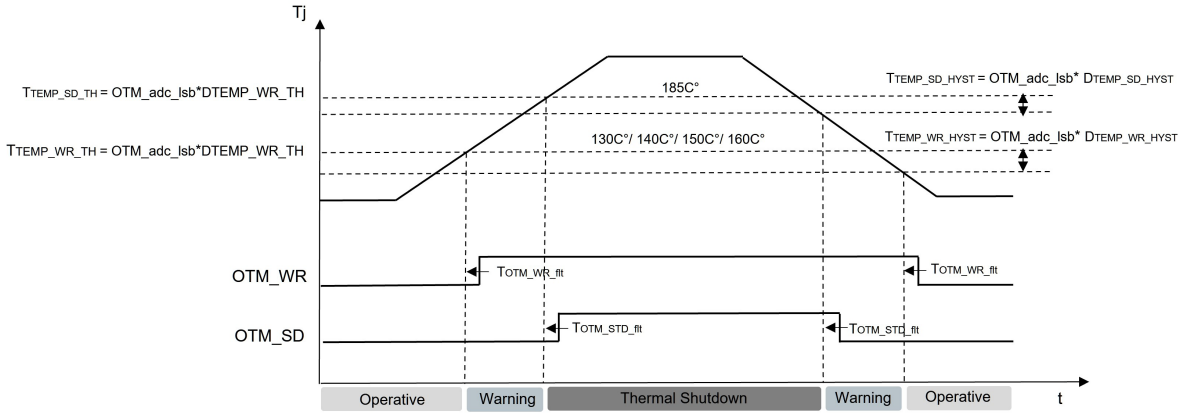
The thermal Warning threshold can be configured by the following SPI bit sets:

Table 100. **Thermal warning configuration bits**

TWN_CFG1	TWN_CFG0	Description
0	0	130 deg.

TWN_CFG1	TWN_CFG0	Description
0	1	140 deg. (Default)
1	0	150 deg.
1	1	160 deg.

Figure 79. Junction temperature ranges



Temperature Range: Parametrical/Functional Range

L9908 is in NORMAL mode: Gate Driver Supply is active, Half Bridge Gate Drivers stage is enabled, monitoring units are enabled and SPI registers are out of reset. No damage affects L9908 and no wrong operation takes place. All static and dynamic parameters stay within specification limits.

Temperature Range: Critical OT Range

L9908 is set into SAFE- OFF mode: Gate Driver Supply is disabled, Half Bridge Gate Drivers stage is disabled. No damage affects L9908 and no wrong operation takes place. Static and dynamic parameters may deviate from specification limits.

Exposure to critical OT conditions for extended periods may affect device reliability.

Table 101. OTM electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
OTM_th	OTM detection threshold hysteresis	5	10	15	°C	Not subject to production test
T_otm_wr_flt	Thermal Warning filter time	10	20	30	µs	Digital Filter
T_otm_sd_flt	Thermal Shutdown filter time	7	13	17.5	µs	Digital Filter
OTM_readout_res	OTM Readout Resolution	-	8	-	-	Not subject to production test
OTM_readout_lsb	OTM Readout LSB	-	1.37	-	°C	Not subject to production test
OTM_acc	OTM ADC conversion accuracy	-5	-	5	°C	Temperature Read out accuracy
OTM-sr	OTM ADC sample rate	-	-	1	kHz	Not subject to production test
T_otm_start_up	OTM ADC start up time	-	-	3	ms	Not subject to production test

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

5.20 Serial Peripheral Interface (SPI)

L9908 implements a standard 4-pin Serial Peripheral Interface (SPI) to access both IC configuration and diagnosis/status registers up to 10 MHz Baud Rate (up/down-stream).

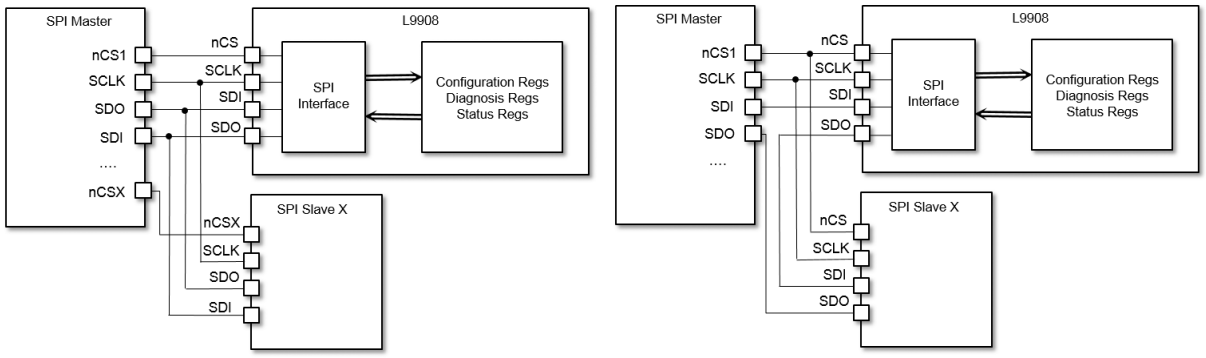
5.20.1 Protocol description

L9908 implement a SPI-slave interface based on a 32-bit protocol.

This slave interface then always requires a SPI-master device (ex. uC) which is responsible to generate the selection and the synchronization signals (NCS, SCLK) necessary to the data transmission.

The interface supports star mode connections along with other SPI-slave devices while it does not support daisy-chain mode connections (input data aren`t transmitted directly to output port).

Figure 80. SPI connection modes "a" star connection (supported) "b" daisy-chain connection (not supported)



The data exchange has an out-of-frame structure: each MISO output frame is related to the previously transmitted MOSI frame.

SPI-master can directly verify if the previous frame has been received and processed correctly.

NCS pin (chip select) is used by the SPI-master to enable/disable the data communication. Communication starts with the NCS falling edge while is stopped with the NCS rising edge. As long as NCS is high any transition at the SCLK and SDI pins (including glitches) is ignored and SDO is forced into a high impedance state.

SCLK pin (Synchronous Serial Clock) is used by the SPI-master to synchronize the data communication. Each correct communication shall contain 32 SCLK pulses.

At each SCLK rising edge SDI and SDO data are updated respectively by SPI-master and L9908 (shift), at each SCLK falling edge SDI and SDO data are sampled respectively by L9908 and SPI-master (capture). SCLK has to be low during NCS transition.

SDI pin (Serial Data Input) is used by the SPI-master to deliver the 32-bit input frame to L9908. In MOSI communication the first bit expected is MSB while the last is LSB.

SDO pin (Serial Data Output) is used by L9908 to transmit the 32-bit data output. In MISO communication the first bit transmitted is MSB while the last is LSB.

Figure 81. SPI timing diagram

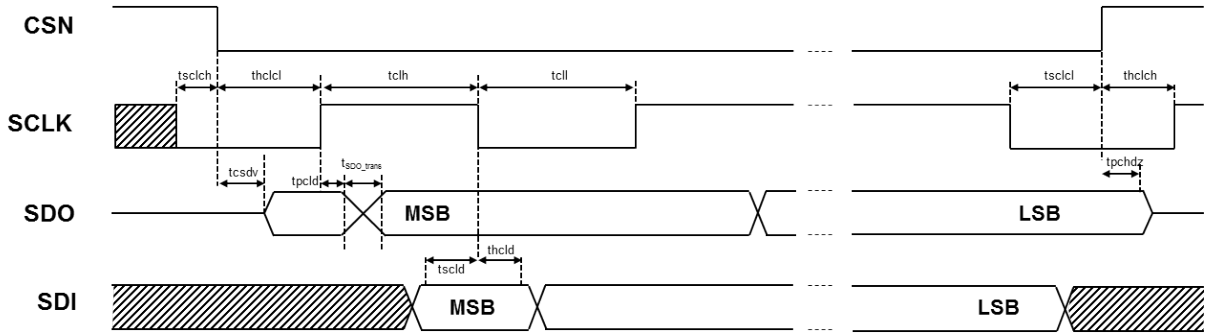


Table 102. SPI timing characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SPI_fclk	Transfer Frequency	50% duty cycle(1)	-	10	10.2	MHz

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SPI_tpcld_tsdo_trans	Propagation delay	SCLK to data at SDO is valid Cload_max = 200 pF Including parasitics	-	-	100	ns
SPI_tcsdv	NCS=LOW to data at SDO active	Cload_max = 200 pF Inlcuding parasitics	-	-	200	ns
SPI_tpchdz	NCS L/H to SDO at high impedance	Cload_max = 200 pF Including parasitics	-	-	200	ns
SPI_tsclch	SCLK before NCS low	(2)	50	-	-	ns
SPI_thclcl	SCLK change L/H after NCS=LOW	(2)	130	-	-	ns
SPI_tsclcl	SCLK low before NCS high	(2)	50	-	-	ns
SPI_thclch	SCLK high after NCS high	(2)	50	-	-	ns
SPI_tscld	SDI input setup time	(2)	20	-	-	ns
SPI_thcld	SDI input hold time	(2)	-	-	20	ns
SPI_tonNCS	NCS min. high time	(2)	650	-	-	ns
SPI_tclh	Minimum Time SCLK=HIGH	(2)	45	-	-	ns
SPI_tcll	Minimum Time SCLK=LOW	(2)	45	-	-	ns
SPI_Cin	Input pin capacitance	(2)	-	-	30	pF
SPI_Cout_hiz	MISO output pin capacitance in tri-state	(2)	-	-	50	pF

1. *SPI max frequency may be less depending on the total capacitive load or MCU timing requirements.*
2. *Not subject to production test, guaranteed by design.*

Note: All parameters are guaranteed, and tested, in the voltage ranges reported above in Table 5 unless otherwise specified. Where not specified the parametrical operating range equals the functional operating range.

5.20.2 Frame description

The 32-bit SPI frames content is divided as follows:

Table 103. MOSI - SPI frame description

Bit	31	30-23	22	21	20-5	4-0
MOSI	R/W	ADDRESS	RSV/TM	FC	DATA WRITE	CRC

MOSI Stream:

[31] R/W Flag. Selects if the current operation is a read (0) operation or write (1) operation.

[30-23] SPI register address

[22] Test Mode Flag

[21] Frame Counter

[20-5] Data Write

[4-0] CRC checksum generated by SPI-master

Table 104. MISO - SPI frame description

Bit	31	30-29	28-21	20-5	4-0
MISO	SPI ERR	IC ERR	ADDRESS FB	DATA READ	CRC

MISO Stream:

[31] SPI Error Flag. Provide information related to the previous stream.

[30-29] IC Error Flag. Provide information related to IC high level error.

[28-21] SPI register address feedback. Last received valid frame address feedback.

[20-5] Data Read. Data contents of SPI register addressed by last received valid frame.

[4-0] CRC checksum generated by SPI-slave

5.20.2.1 *Write-Read operations*

1st Frame: Write Access to R/W Register X

As the NCS rising edge is detected, if it is valid, the command is processed and the R/W register X is updated with data Y. After the register X is updated correctly the output buffer is updated as well.

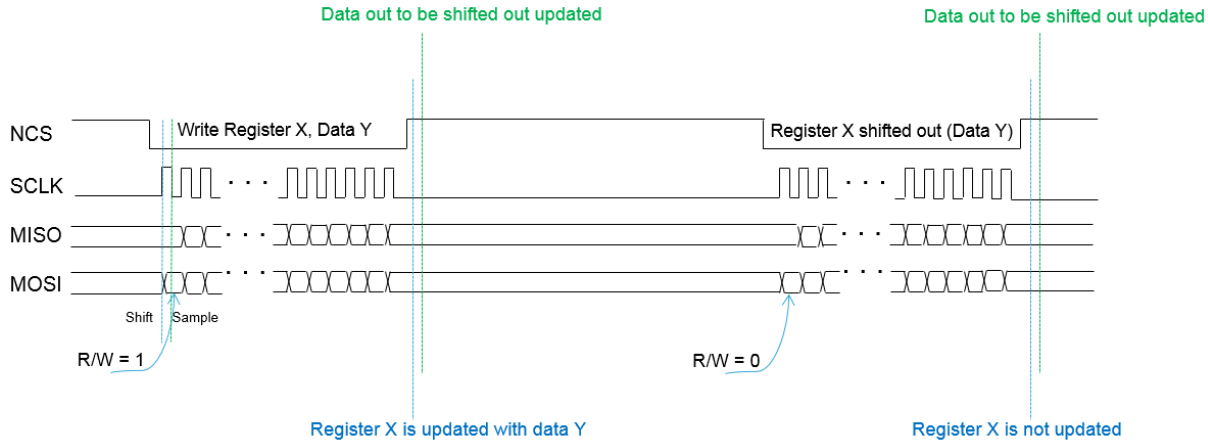
2nd Frame: Read Access

As the NCS falling edge is detected, the register X with data Y is started being shifted out on MISO bus. The X register data remains unchanged as R/W bit is zero, the following MISO frame will be updated with the same data.

The first SPI frame after an internal reset (i.e. INT_RST) will have a fixed content:

- IC_ERR and SPI_ERR flag all 0
- Address Feedback all = 0
- Data all = 0

Figure 82. **SPI Write-Read operation**



5.20.2.2 *Read-Read operations*

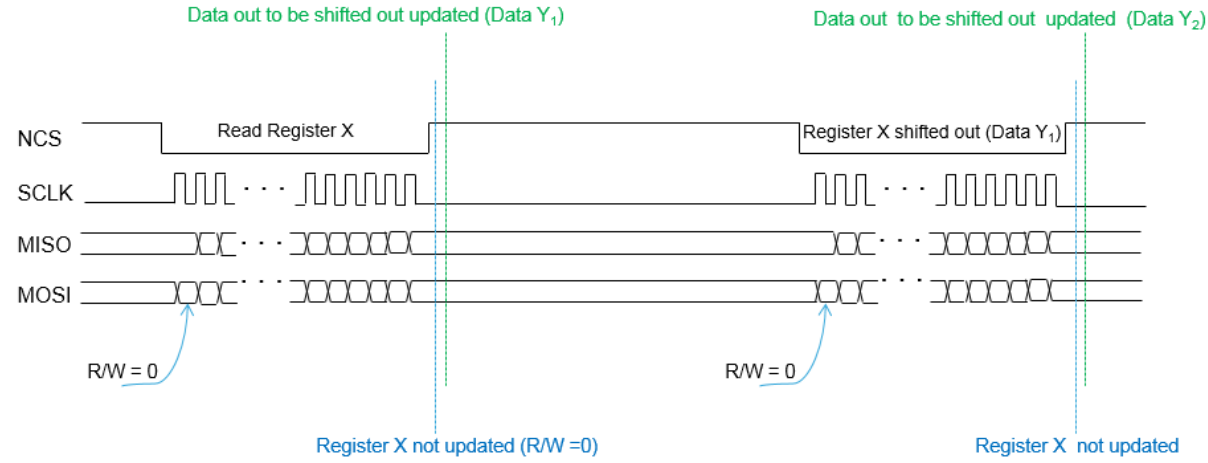
1st Frame: Read Access to Register X

As the NCS rising edge is detected, if it is valid, the command is processed but the R/W register X register data remains unchanged as R/W bit is zero and the output buffer is updated with data Y1.

2nd Frame: Read Access to Register X

As the NCS falling edge is detected, the register X with data Y1 is started being shifted out on MISO bus. The X register data remains unchanged as R/W bit is zero, the following MISO frame will be updated with the data Y2.

Figure 83. **SPI Read-Read operation**



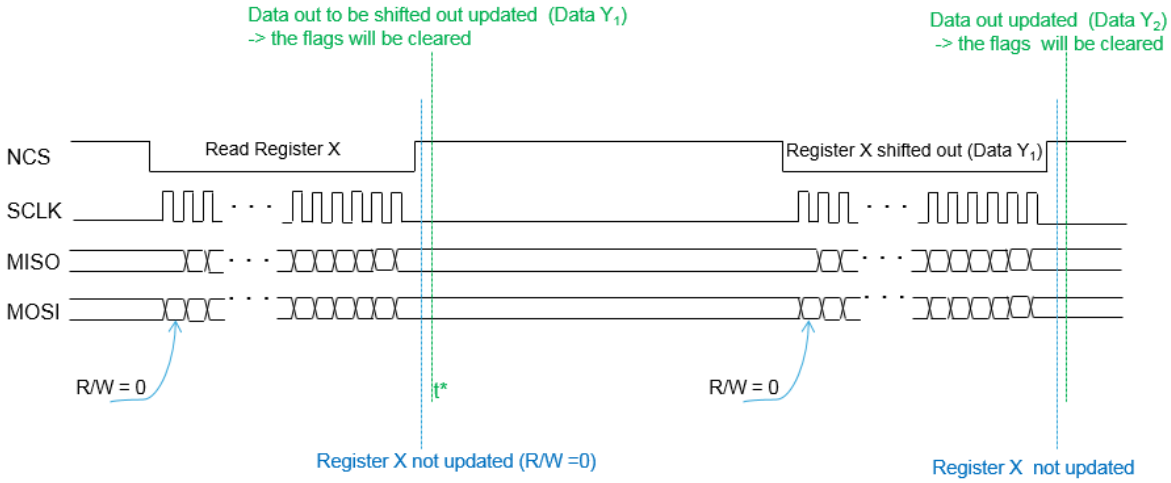
5.20.2.3 *Clear on Read Operations*

1st Frame: Read Access to Register X

As the NCS rising edge is detected, if it is valid, the command is processed but the R/W register X register data remains unchanged as R/W bit is zero and the output buffer is updated with data Y1. After the output buffer is updated correctly the X register flags are cleared.

2nd Frame: Read Access to Register X As NCS falling edge is detected, the register X with data Y1 is started being shifted out on MISO bus.

Figure 84. SPI Clear on Read operation



5.20.3 Frame monitoring

Correct SPI communication is safety relevant and then the following safety mechanism is implemented.

Cyclic Redundancy Check (CRC)

MISO/MOSI SPI data are protected with a 5-bit CRC using the following polynomial expression:

$$G(x) = x^5 + x^2 + 1 \quad (26)$$

The initial value to be used is 11111 (0x1F).

CRC is calculated over bit 5-31 except bit 21 (Hamming distance of 3 over 26 bit data), MSB First.

Example:

Read register 0x4A command (data = 0)

Frame: [0 0100:1010 0 0 0000:0000:0000:0000 10001] (0x25000011)

Frame: [0 0100:1010 0 1 0000:0000:0000:0000 10001] (0x25200011)

CRC is 10001 independently on FC value.

Write 0xABCD to register 0xC7 command

Frame: [1 1100:0111 0 0 1010:1011:1100:1101 11000] (0xE39579B8)

Frame: [1 1100:0111 0 1 1010:1011:1100:1101 11000] (0xE3B579B8)

CRC is 11000b independently on FC value.

Frame Counter Check (FC)

A 1-bit frame counter is transmitted by the SPI-master within every MOSI frame to support the detection of failures in the communication channel (ex. corrupted or missing frames). The initial value to be used is 0.

Clock Counter Check

L9908 implements two separate clock counters for the rising and the falling edges of SCLK clock to check the length of the MOSI frame to be equal to 32. The clock counters reset is generated from the detection of a rising edge of NCS.

5.20.4 Error handling

In case of an error either regarding the SPI word length (clock counter), frame counter bit value (FC) or wrong CRC check, the SPI_ERR bit is set to ‘1’ and the frame is ignored by L9908. The SPI error bit always refers to the previous SPI frame.

The register SPI_CMM_FAULT contains specific bits indicating which SPI fault occurred on the previous frame. After reading, register value will be reset. Refer to the next section for details.

5.20.5 Register description

Legenda:

Safety Description:

- NSR = Non-safety Relevant Register
- SLR = Safety Latent Register
- SSR = Safety Relevant Register

Operation Type:

- RW = Read/Write
- RO = Read Only
- CR = Clear on Read

Reset Source:

- A = INT_RST
- B = INT_RST || CFG_RST
- D = INT_RST (excluded CLK1_TIMEOUT)

Table 105. CHIPID

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CHIPID	0x0	UNUSED_9	RO	15	1	0x0	B

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
NSR		UNUSED_8	RO	14	1	0x0	B
		UNUSED_7	RO	13	1	0x0	B
		UNUSED_6	RO	12	1	0x0	B
		UNUSED_5	RO	11	1	0x0	B
		UNUSED_4	RO	10	1	0x0	B
		UNUSED_3	RO	9	1	0x0	B
		UNUSED_2	RO	8	1	0x0	B
		UNUSED_1	RO	7	1	0x0	B
		UNUSED_0	RO	6	1	0x0	B
		METAL_ID	RO	3	3	0x0	B
		SILICON_ID	RO	0	3	0x1	B

Table 106. GEN_CFG1

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
GEN_CFG1	0x2	WDT_EN 0: Watchdog disabled (Default) 1: Watchdog enabled	RW	15	1	0x0	B
SLR		CLK_SSM_EN 0: Clock SSM Disabled (Default) 1: Clock SSM Enabled	RW	14	1	0x0	B
		CSM_OUT_RANGE_CFG	RW	13	1	0x0	B
		CSM_SSPV_PH_CFG 00: No synchronization 01: TSYNC based on Phase 1 (Default) 10: TSYNC based on Phase 2 11: TSYNC based on Phase 3	RW	11	2	0x01	B
		CSM_LP_CFG 000: No filtering (Default) 001: 91kHz 010: 37kHz 011: 17kHz 100: 8kHz 101: 4kHz 110: 2kHz 111: 1kHz	RW	8	3	0x0	B
		DTP_CFG 000: 0us - DTP Disabled 001: 0.25us 010: 0.35us 011: 0.5us 100: 1us - Default 101: 1.5us	RW	5	3	0x2	B

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
SLR		110: 2us 111: 4us					
		SR_CRC_FAIL_REDIRECT_CFG	RW	4	1	0x0	B
		VBP_OV_REDIRECT_CFG 0: Fault redirected on FS_FLAG/IC ERR (Default) 1: Fault redirection masked	RW	3	1	0x0	B
		VBP_UV_REDIRECT_CFG 0: Fault redirected on FS_FLAG/IC ERR (Default) 1: Fault redirection masked	RW	2	1	0x0	B
		VDH_OV_REDIRECT_CFG 0: Fault redirected on FS_FLAG/IC ERR (Default) 1: Fault redirection masked	RW	1	1	0x0	B
		VDH_UV_REDIRECT_CFG 0: Fault redirected on FS_FLAG/IC ERR (Default) 1: Fault redirection masked	RW	0	1	0x0	B

Table 107. GEN_CFG2

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
GEN_CFG2	0x3	ACT_CFG 00: PVF Negative Polarity (Default) 01: PVF Positive Polarity 10: INL Negative Polarity 11: INL Positive Polarity	RW	14	2	0x0	B
SLR		OFD_BLANK 00: T_ofd_blank = 10ms 01: T_ofd_blank = 25ms 10: T_ofd_blank = 50ms (Default) 11: T_ofd_blank = 100ms	RW	12	2	0x2	B
		VDS_HS_TH	RW	6	6	0x0	B
		VDS_LS_TH	RW	0	6	0x0	B

Table 108. GE_CFG3

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
GEN_CFG3	0x4	TWN_CFG 00: 130deg. 01: 140deg. (Default) 10: 150deg. 11: 160deg.	RW	14	2	0x1	B
SLR		STP3_VGS_DIS 0: Shoot-through protection on FET Vgs enabled (Default)	RW	13	1	0x0	B

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
SLR		1: Shoot-through protection on FET Vgs disabled					
		STP2_VGS_DIS 0: Shoot-through protection on FET Vgs enabled (Default) 1: Shoot-through protection on FET Vgs disabled	RW	12	1	0x0	B
		STP1_VGS_DIS 0: Shoot-through protection on FET Vgs enabled (Default) 1: Shoot-through protection on FET Vgs disabled	RW	11	1	0x0	B
		STP3_PWM_DIS 0: Shoot-through protection on PWM input enabled (Default) 1: Shoot-through protection on PWM input disabled	RW	10	1	0x0	B
		STP2_PWM_DIS 0: Shoot-through protection on PWM input enabled (Default) 1: Shoot-through protection on PWM input disabled	RW	9	1	0x0	B
		STP1_PWM_DIS 0: Shoot-through protection on PWM input enabled (Default) 1: Shoot-through protection on PWM input disabled	RW	8	1	0x0	B
		UNUSED_0	RW	6	2	0x0	B
		BT1_DIS 0: Bootstrap Limiter 1 Enabled (Default) 1: Bootstrap Limiter 1 Disabled	RW	5	1	0x0	B
		OND_FLT 00: T_ond_flt = 1 µs 01: T_ond_flt = 2.5 µs 10: T_ond_flt = 4 µs (Default) 11: T_ond_flt = 8 µs	RW	3	2	0x2	B
		OND_BLANK 000: T_ond_blank = 0.7u 001: T_ond_blank = 1 µs 010: T_ond_blank = 1.5 µs (Default) 011: T_ond_blank = 2 µs 100: T_ond_blank = 2.5 µs 101: T_ond_blank = 3.5 µs 110: T_ond_blank = 5 µs 111: T_ond_blank = 8 µs	RW	0	3	0x2	B

Table 109. GEN_CFG4

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
GEN_CFG4	0x5	PVF_OUT_CFG	RW	14	2	0x0	B

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
		00: PVF1 xor PVF2 xor PVF3 is output (Default) 01: PVF1 is output 10: PVF2 is output 11: PVF3 is output					
SLR		PVF_TH_CFG 0: VPVF_TH_H = VDH*0.75 (Default) VPVF_TH_L = VDH*0.25 1: VPVF_TH_H = VDH*0.6 VPVF_TH_L = VDH*0.4	RW	13	1	0x0	B
		UNUSED_0	RW	12	1	0x0	B
		DRV_HIZ 0: Pre-drivers in NO high impedance 1: Pre-drivers in high impedance (Default)	RW	11	1	0x1	B
		SELF_TEST_CFG4 0: OND LS Self-Test Not Active 1: OND LS Self-Test Active (Default) SELF_TEST_CFG3 0: OND HS Self-Test Not Active 1: OND HS Self-Test Active (Default) SELF_TEST_CFG2 0: Supply Monitors Self-Test Not Active 1: Supply Monitors Self-Test Active (Default) SELF_TEST_CFG1 0: SW Off Path Self-Test Not Active 1: SW Off Path Self-Test Active (Default) SELF_TEST_CFG0 0: Clock Monitor Self-Test Not Active 1: Clock Monitor Self-Test Active (Default)	RW	6	5	0x1F	B
		HB3_ACK	RW	5	1	0x1	B
		HB2_ACK	RW	4	1	0x1	B
		HB1_ACK	RW	3	1	0x1	B
		HB3_DIS 0: 3rd HS/LS drivers is enabled (Default) 1: 3rd HS/LS drivers is disabled	RW	2	1	0x0	B
		HB2_DIS 0: 2nd HS/LS drivers is enabled (Default) 1: 2nd HS/LS drivers is disabled	RW	1	1	0x0	B
		HB1_DIS 0: 1st HS/LS drivers is enabled (Default) 1: 1st HS/LS drivers is disabled	RW	0	1	0x0	B

Table 110. **GEN_STATUS1**

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
GEN_STATUS1	0x6	AGND_LOSS	CR	15	1	0x0	A
NSR		DGND_LOSS	CR	14	1	0x0	A
		PGND_LOSS	CR	13	1	0x0	A
		NVM_CRC_FAIL	RO	12	1	0x0	A
		VDD_OV	CR	11	1	0x0	A
		SELF_TEST_STATUS	RO	9	2	0x0	D
		SR_CRC_FAIL	CR	8	1	0x0	A
		CLK2_ERR	CR	7	1	0x0	A
		UNUSED_0	RO	6	1	0x0	A
		CLK1_ERR	CR	5	1	0x0	A
		CLK2_TIMEOUT	CR	4	1	0x0	A
		CLK1_TIMEOUT	CR	3	1	0x0	D
		SAFE_STATE	RO	2	1	0x1	A
		CFG_RST	CR	1	1	0x1	B
		INT_RST	CR	0	1	0x1	A

Table 111. **GEN_STATUS2**

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
GEN_STATUS2	0x7	INL3_ECHO	RO	15	1	0x0	A
NSR		INL2_ECHO	RO	14	1	0x0	A
		INL1_ECHO	RO	13	1	0x0	A
		INH3_ECHO	RO	12	1	0x0	A
		INH2_ECHO	RO	11	1	0x0	A
		INH1_ECHO	RO	10	1	0x0	A
		NDIS_ECHO	RO	9	1	0x1	A
		EN_BR_ECHO	RO	8	1	0x0	A
		VBP_OV	CR	7	1	0x0	A
		VBP_UV	CR	6	1	0x0	A
		VDH_OV	CR	5	1	0x0	A
		VDH_UV	CR	4	1	0x0	A
		VCP_OV	CR	3	1	0x0	A
		VCP_UV	CR	2	1	0x0	A
		VPRE_OV	CR	1	1	0x0	A
		VPRE_UV	CR	0	1	0x0	A

Table 112. **GEN_STATUS3**

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
GEN_STATUS3	0x8	UNUSED_4	RO	15	1	0x0	A
NSR		UNUSED_3	RO	14	1	0x0	A

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
NSR		CP2_EN_ECHO	RO	13	1	0x1	A
		CP1_EN_ECHO	RO	12	1	0x1	A
		HB3_EN_ECHO	RO	11	1	0x1	A
		HB2_EN_ECHO	RO	10	1	0x1	A
		HB1_EN_ECHO	RO	9	1	0x1	A
		UNUSED_0	RO	6	3	0x0	A
		OPERATION_MODE 000: RESET Mode 001: NVM Read Mode 010: SAFE OFF Mode 011: NORMAL Mode 100: CFG Mode 101: SELF TEST Mode 110: RESET Mode 111: RESET Mode	RO	3	3	0x0	A
		PVF3_ECHO	RO	2	1	0x0	A
		PVF2_ECHO	RO	1	1	0x0	A
		PVF1_ECHO	RO	0	1	0x0	A

Table 113. GEN_TEMP_STATUS

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
GEN_TEMP_STATUS	0x9	UNUSED_5	RO	15	1	0x0	A
NSR		UNUSED_4	RO	14	1	0x0	A
		UNUSED_3	RO	13	1	0x0	A
		UNUSED_2	RO	12	1	0x0	A
		UNUSED_1	RO	11	1	0x0	A
		UNUSED_0	RO	10	1	0x0	A
		OTM_SD	CR	9	1	0x0	A
		OTM_WR	CR	8	1	0x0	A
		TEMP_READ	RO	0	8	0x0	A

Table 114. SW_RESET

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
SW_RESET	0xA	UNUSED_7	RO	15	1	0x0	A
NSR		UNUSED_6	RO	14	1	0x0	A
		UNUSED_5	RO	13	1	0x0	A
		UNUSED_4	RO	12	1	0x0	A
		UNUSED_3	RO	11	1	0x0	A
		UNUSED_2	RO	10	1	0x0	A
		UNUSED_1	RO	9	1	0x0	A
		UNUSED_0	RO	8	1	0x0	A

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
NSR		SW_RESET_KEY 0xCC: SW Reset Activation	RW	0	8	0x0	A

Table 115. WDT_CFG_CMD

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
WDT_CFG_CMD	0xB	UNUSED_2	RO	15	1	0x0	A
NSR		UNUSED_1	RO	14	1	0x0	A
		WDT_RESET 00: NO Reset 01: NO Reset (Default) 10: Reset 11: NO Reset	RW	12	2	0x1	A
		WDT_FAIL_COUNT_CFG 00: 1 01: 1 10: 2 11: 3 (Default)	RW	10	2	0x3	A
		WDT_OVF_CFG 00: 11.26 ms 01: 22.52 ms (Default) 10: 45.04 ms 11: 90.11 ms	RW	8	2	0x1	A
		WDT_GRAY	RO	4	4	0x0	A
		WDT_BINARY	RW	0	4	0x0	A

Table 116. WDT_STATUS

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
WDT_STATUS	0xC	UNUSED_4	RO	15	1	0x0	A
NSR		UNUSED_3	RO	14	1	0x0	A
		UNUSED_2	RO	13	1	0x0	A
		UNUSED_1	RO	12	1	0x0	A
		UNUSED_0	RO	11	1	0x0	A
		WDT_FAIL_COUNT_STATUS	RO	9	2	0x0	A
		WDT_OVF_STATUS	RO	3	6	0x0	A
		WD_ON_STATUS	RO	2	1	0x0	A
		WDT_DATA_FAIL	RO	1	1	0x0	A
		WDT_OVF_FAIL	RO	0	1	0x0	A

Table 117. BIST_KEY

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
BIST_KEY	0xD	UNUSED_7	RO	15	1	0x0	B

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
NSR		UNUSED_6	RO	14	1	0x0	B
		UNUSED_5	RO	13	1	0x0	B
		UNUSED_4	RO	12	1	0x0	B
		UNUSED_3	RO	11	1	0x0	B
		UNUSED_2	RO	10	1	0x0	B
		UNUSED_1	RO	9	1	0x0	B
		UNUSED_0	RO	8	1	0x0	B
		BIST_KEY 0x55 --> 0x33 SELF TEST Mode Access	RW	0	8	0x0	B

Table 118. CFG_EN_UNLOCK

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CFG_EN_UNLOCK	0xE	UNUSED_7	RO	15	1	0x0	B
NSR		UNUSED_6	RO	14	1	0x0	B
		UNUSED_5	RO	13	1	0x0	B
		UNUSED_4	RO	12	1	0x0	B
		UNUSED_3	RO	11	1	0x0	B
		UNUSED_2	RO	10	1	0x0	B
		UNUSED_1	RO	9	1	0x0	B
		UNUSED_0	RO	8	1	0x0	B
		CFG_EN_UNLOCK 0x55 --> 0x33: CONFIG Mode Access 0xAA: CONFIG Mode Exit	RW	0	8	0x0	B

Table 119. SAFETY_RELEVANT1

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
SAFETY_RELEVANT1	0x10	FS_FLAG_CFG 0: Push-pull (Default) 1: Open-drain	RW	15	1	0x0	B
SSR		UNUSED_0	RW	13	2	0x0	B
		VBP_OV_REACT_CFG 00: Full SW Off – disable all HB drivers and CPs, device is sent in SAFE-OFF mode (Default) 01: Reduced Operation Mode – disable failing HB only, device remains in NORMAL mode 10: Flag only – down-rate fault to simple warning, device remains in NORMAL mode 11: Flag only – down-rate fault to simple warning, device remains in NORMAL mode	RW	11	2	0x0	B
		VBP_UV_REACT_CFG	RW	9	2	0x0	B

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
SSR		VDH_OV_REACT_CFG	RW	7	2	0x0	B
		VDH_UV_REACT_CFG	RW	5	2	0x0	B
		CRC	RW	0	5	0x17	B

Table 120. SAFETY_RELEVANT2

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
SAFETY_RELEVANT2	0x11	CSO3_DIS 0: CSO3/PVM pin used a CM3 output (Default) 1: CSO3/PVM pin used a PVFn output	RW	15	1	0x0	B
SSR		CS3_DIS 0: current monitor enabled (Default) 1: current monitor disabled	RW	14	1	0x0	B
		CS2_DIS 0: current monitor enabled (Default) 1: current monitor disabled	RW	13	1	0x0	B
		CS1_DIS 0: current monitor enabled (Default) 1: current monitor disabled	RW	12	1	0x0	B
		VDH_FLT_CFG 00: 12.25 µs (Defaults) 01: 25 µs 10: 50 µs 11: 100 µs	RW	10	2	0x0	B
		VDH_OV_CFG 000: 12 V Systems 1 001: 12 V Systems 2 010: 24 V Systems 1 011: 24 V Systems 2 100: 48 V Systems 1 101: 48 V Systems 2 110: 48 V Systems 3 111: 48 V Systems 4 (Defaults)	RW	7	3	0x7	B
		VDH_UV_CFG 00: 12 V Systems (Defaults) 01: 24 V Systems 10: 48 V Systems 11: VDH UV Disabled	RW	5	2	0x0	B
		CRC	RW	0	5	0x17	B

Table 121. **SAFETY_RELEVANT3**

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
SAFETY_RELEVANT3	0x12	CP2_DIS 0: Charge Pump 2 Enabled (Default) 1: Charge Pump 2 Disabled	RW	15	1	0x0	B
SSR		CP1_DIS 0: Charge Pump 1 Enabled (Default) 1: Charge Pump 1 Disabled	RW	14	1	0x0	B
		UNUSED_2	RW	13	1	0x0	B
		UNUSED_1	RW	12	1	0x0	B
		UNUSED_0	RW	11	1	0x0	B
		VBP_FLT_CFG 00: 12.25 µs (Defaults) 01: 25 µs 10: 50 µs 11: 100 µs	RW	9	2	0x0	B
		VBP_OV_CFG 00: 12 V Systems 1 01: 12 V Systems 2 10: 24 V Systems 1 11: 24 V Systems 2 (Defaults)	RW	7	2	0x0	B
		VBP_UV_CFG 00: 12 V Systems (Defaults) 01: 24 V Systems 10: 48 V Systems 11: VBP UV Disabled	RW	5	2	0x0	B
		CRC	RW	0	5	0x17	B

Table 122. **CH1_STATUS1**

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH1_STATUS1	0x20	UNUSED_7	RO	15	1	0x0	A
NSR		UNUSED_6	RO	14	1	0x0	A
		UNUSED_5	RO	13	1	0x0	A
		UNUSED_4	RO	12	1	0x0	A
		UNUSED_3	RO	11	1	0x0	A
		UNUSED_2	RO	10	1	0x0	A
		LS1_OFF	RO	9	1	0x0	A
		HS1_OFF	RO	8	1	0x0	A
		LS1_STB	CR	7	1	0x0	A
		HS1_STG	CR	6	1	0x0	A
		LS1_OFD	RO	5	1	0x0	A
		HS1_OFD	RO	4	1	0x0	A
		UNUSED_1	CR	3	1	0x0	A

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
NSR		STP_VGS_1	CR	2	1	0x0	A
		STP_PWM_1	CR	1	1	0x0	A
		UNUSED_0	RO	0	1	0x0	A

Table 123. CH1_STATUS2

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH1_STATUS2	0x21	UNUSED_0	RO	15	1	0x0	A
NSR		CM1_READ	RO	0	15	0x0	A

Table 124. CH1_CFG1

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH1_CFG1	0x22	UNUSED_1	RW	11	5	0x0	B
SLR		OFD1_EN 00: Off State Diagnosis disabled (Default) 01: Pull-up current enabled, Pull-down current disabled 10: Pull-down current enabled, Pull-up current disabled 11: Off State Diagnosis disabled	RW	9	2	0x0	B
		OND1_DIS 0: ON State diagnosis enabled on HS and LS (Default) 1: ON State diagnosis disabled on HS and LS	RW	8	1	0x0	B
		LS1_STB_REDIRECT_CFG 0: Fault redirected on FS_FLAG/IC ERR (Default) 1: Fault redirection masked	RW	7	1	0x0	B
		HS1_STG_REDIRECT_CFG 0: Fault redirected on FS_FLAG/IC ERR (Default) 1: Fault redirection masked	RW	6	1	0x0	B
		UNUSED_0	RO	15	1	0x0	A
		STP_VGS_1_REDIRECT_CFG 0: Fault redirected on FS_FLAG/IC ERR (Default) 1: Fault redirection masked	RW	4	1	0x0	B
		STP1_VGS_CFG 00: 0.2 µs (Defaults) 01: 0.5 µs 10: 1 µs 11: 1.5 µs	RW	2	2	0x0	B
		STP1_PWM_CFG 00: 0.2 µs (Defaults) 01: 0.5 µs 10: 1 µs 11: 1.5 µs	RW	0	2	0x0	B

Table 125. **CH1_CFG2**

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH1_CFG2	0x23	UNUSED	RW	11	5	0x0	B
SLR		CSM1_SYNC_COUNT_CFG 00: 16Tclk (Default) 01: 24Tclk 10: 32Tclk 11: 40Tclk	RW	9	2	0x0	B
		UNUSED_0	RW	8	1	0x0	B
		CSM1_SAMPLE_CFG 000: Free running – No T&H (Default) 001: T&H 1st data conversion from triggering 010: T&H 2nd data conversion from triggering 011: T&H 3rd data conversion from triggering 100: T&H 4th data conversion from triggering 101: T&H 5th data conversion from triggering 110: T&H 6th data conversion from triggering 111: T&H 7th data conversion from triggering	RW	5	3	0x0	B
		CSM1_IN_RANGE_CFG 000: VIN_MAX = ±7 mV 001: VIN _MAX =±18 mV 010: VIN _MAX =±36 mV 011: VIN_MAX = ±90 mV 100: VIN_MAX = ±160 mV 101: VIN_MAX = ±300 mV (Default) 110: Reserved 111: Reserved	RW	2	3	0x5	B
		CSM1_OFS 00: 0LSB DAC 01: 90LSB DAC 10: 1024LSB DAC 11: 1024LSB DAC (Default)	RW	0	2	0x3	B

Table 126. **CH1_CFG3**

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH1_CFG3	0x24	UNUSED_3	RW	15	1	0x0	B
NSR		UNUSED_2	RW	14	1	0x0	B
		UNUSED_1	RW	13	1	0x0	B
		UNUSED_0	RW	12	1	0x0	B
		ACT1_EN 0: ACT Disabled (Default) 1: ACT Enabled	RW	11	1	0x0	B
		TSYNC1_CFG	RW	0	11	0x0	B

Table 127. **CH1_SAFETY_RELEVANT**

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH1_SAFETY_RELEVANT	0x25	UNUSED_4	RW	15	1	0x0	B
SRR		UNUSED_3	RW	14	1	0x0	B
		UNUSED_2	RW	13	1	0x0	B
		STP_VGS_1_REACT_CFG 00: Full SW Off – disable all HB drivers and CPs, device is sent in SAFE-OFF mode (Default) 01: Reduced Operation Mode – disable failing HB only, device is remain in NORMAL mode 10: Flag only – down-rate fault to simple warning, device is remain in NORMAL mode 11: Flag only – down-rate fault to simple warning, device is remain in NORMAL mode	RW	11	2	0x0	B
		UNUSED_1	RW	10	1	0x0	B
		UNUSED_0	RW	9	1	0x0	B
		LS1_STB_REACT_CFG	RW	7	2	0x0	B
		HS1_STG_REACT_CFG	RW	5	2	0x0	B
		CRC	RW	0	5	0x17	B

Table 128. **CH1_ACT**

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH1_ACT	0x26	UNUSED_3	RO	15	1	0x0	A
NSR		UNUSED_2	RO	14	1	0x0	A
		UNUSED_1	RO	13	1	0x0	A
		UNUSED_0	RO	12	1	0x0	A
		ACT1_OVF	RO	11	1	0x0	A
		ACT1	RO	0	11	0x0	A

Table 129. **CH2_STATUS1**

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH2_STATUS1	0x28	UNUSED_7	RO	15	1	0x0	A
NSR		UNUSED_6	RO	14	1	0x0	A
		UNUSED_5	RO	13	1	0x0	A
		UNUSED_4	RO	12	1	0x0	A
		UNUSED_3	RO	11	1	0x0	A
		UNUSED_2	RO	10	1	0x0	A
		LS2_OFF	RO	9	1	0x0	A
		HS2_OFF	RO	8	1	0x0	A
		LS2_STB	CR	7	1	0x0	A

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
NSR		HS2_STG	CR	6	1	0x0	A
		LS2_OFD	RO	5	1	0x0	A
		HS2_OFD	RO	4	1	0x0	A
		UNUSED_1	CR	3	1	0x0	A
		STP_VGS_2	CR	2	1	0x0	A
		STP_PWM_2	CR	1	1	0x0	A
		UNUSED_0	RO	0	1	0x0	A

Table 130. CH2_STATUS2

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH2_STATUS2	0x29	UNUSED_0	RO	15	1	0x0	A
NSR		CM2_READ	RO	0	15	0x0	A

Table 131. CH2_CFG1

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH2_CFG1	0x2A	UNUSED_1	RW	11	5	0x0	B
SLR		OFD2_EN 00: Off State Diagnosis disabled (Default) 01: Pull-up current enabled, Pull-down current disabled 10: Pull-down current enabled, Pull-up current disabled 11: Off State Diagnosis disabled	RW	9	2	0x0	B
		OND2_DIS 0: ON State diagnosis enabled on HS and LS (Default) 1: ON State diagnosis disabled on HS and LS	RW	8	1	0x0	B
		LS2_STB_REDIRECT_CFG 0: Fault redirected on FS_FLAG/IC ERR (Default) 1: Fault redirection masked	RW	7	1	0x0	B
		HS2_STG_REDIRECT_CFG 0: Fault redirected on FS_FLAG/IC ERR (Default) 1: Fault redirection masked	RW	6	1	0x0	B
		UNUSED_0	RO	15	1	0x0	A
		STP_VGS_2_REDIRECT_CFG 0: Fault redirected on FS_FLAG/IC ERR (Default) 1: Fault redirection masked	RW	4	1	0x0	B
		STP2_VGS_CFG 00: 0.2 µs (Defaults) 01: 0.5 µs 10: 1 µs 11: 1.5 µs	RW	2	2	0x0	B
		STP2_PWM_CFG 00: 0.2 µs (Defaults)	RW	0	2	0x0	B

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
SLR		01: 0.5 µs 10: 1 µs 11: 1.5 µs					

Table 132. CH2_CFG2

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH2_CFG2	0x2B	UNUSED	RW	11	5	0x0	B
SLR		CSM2_SYNC_COUNT_CFG 00: 16Tclk (Default) 01: 24Tclk 10: 32Tclk 11: 40Tclk	RW	9	2	0x0	B
		UNUSED_0	RW	8	1	0x0	B
		CSM2_SAMPLE_CFG 000: Free running – No T&H (Default) 001: T&H 1st data conversion from triggering 010: T&H 2nd data conversion from triggering 011: T&H 3rd data conversion from triggering 100: T&H 4th data conversion from triggering 101: T&H 5th data conversion from triggering 110: T&H 6th data conversion from triggering 111: T&H 7th data conversion from triggering	RW	5	3	0x0	B
		CSM2_IN_RANGE_CFG 000: VIN_MAX = ±7mV 001: VIN _MAX = ±18 mV 010: VIN _MAX = ±36 mV 011: VIN_MAX = ±90 mV 100: VIN_MAX = ±160 mV 101: VIN_MAX = ±300 mV (Default) 110: Reserved 111: Reserved	RW	2	3	0x5	B
		CSM2_OFS 00: 0LSB DAC 01: 90LSB DAC 10: 1024LSB DAC 11: 1024LSB DAC (Default)	RW	0	2	0x3	B

Table 133. CH2_CFG3

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH2_CFG3	0x2C	UNUSED_3	RW	15	1	0x0	B
NSR		UNUSED_2	RW	14	1	0x0	B

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
NSR		UNUSED_1	RW	13	1	0x0	B
		UNUSED_0	RW	12	1	0x0	B
		ACT2_EN 0: ACT Disabled (Default) 1: ACT Enabled	RW	11	1	0x0	B
		TSYNC2_CFG	RW	0	11	0x0	B

Table 134. CH2_SAFETY_RELEVANT

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH2_SAFETY_RELEVANT	0x2D	UNUSED_4	RW	15	1	0x0	B
SRR		UNUSED_3	RW	14	1	0x0	B
		UNUSED_2	RW	13	1	0x0	B
		STP_VGS_2_REACT_CFG 00: Full SW Off – disable all HB drivers and CPs, device is sent in SAFE-OFF mode (Default) 01: Reduced Operation Mode – disable failing HB only, device remains in NORMAL mode 10: Flag only – down-rate fault to simple warning, device remains in NORMAL mode 11: Flag only – down-rate fault to simple warning, device remains in NORMAL mode	RW	11	2	0x0	B
		UNUSED_1	RW	10	1	0x0	B
		UNUSED_0	RW	9	1	0x0	B
		LS2_STB_REACT_CFG	RW	7	2	0x0	B
		HS2_STG_REACT_CFG	RW	5	2	0x0	B
		CRC	RW	0	5	0x17	B

Table 135. CH2_ACT

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH2_ACT	0x2E	UNUSED_3	RO	15	1	0x0	A
NSR		UNUSED_2	RO	14	1	0x0	A
		UNUSED_1	RO	13	1	0x0	A
		UNUSED_0	RO	12	1	0x0	A
		ACT2_OVF	RO	11	1	0x0	A
		ACT2	RO	0	11	0x0	A

Table 136. CH3_STATUS1

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH3_STATUS1	0x30	UNUSED_7	RO	15	1	0x0	A

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
NSR		UNUSED_6	RO	14	1	0x0	A
		UNUSED_5	RO	13	1	0x0	A
		UNUSED_4	RO	12	1	0x0	A
		UNUSED_3	RO	11	1	0x0	A
		UNUSED_2	RO	10	1	0x0	A
		LS3_OFF	RO	9	1	0x0	A
		HS3_OFF	RO	8	1	0x0	A
		LS3_STB	CR	7	1	0x0	A
		HS3_STG	CR	6	1	0x0	A
		LS3_OFD	RO	5	1	0x0	A
		HS3_OFD	RO	4	1	0x0	A
		UNUSED_1	CR	3	1	0x0	A
		STP_VGS_3	CR	2	1	0x0	A
		STP_PWM_3	CR	1	1	0x0	A
		UNUSED_0	RO	0	1	0x0	A

Table 137. CH3_STATUS2

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH3_STATUS2	0x31	UNUSED_0	RO	15	1	0x0	A
NSR		CM3_READ	RO	0	15	0x0	A

Table 138. CH3_CFG1

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH3_CFG1	0x32	UNUSED_1	RW	11	5	0x0	B
SLR		OFD3_EN 00: Off State Diagnosis disabled (Default) 01: Pull-up current enabled, Pull-down current disabled 10: Pull-down current enabled, Pull-up current disabled 11: Off State Diagnosis disabled	RW	9	2	0x0	B
		OND3_DIS 0: ON State diagnosis enabled on HS and LS (Default) 1: ON State diagnosis disabled on HS and LS	RW	8	1	0x0	B
		LS3_STB_REDIRECT_CFG 0: Fault redirected on FS_FLAG/IC ERR (Default) 1: Fault redirection masked	RW	7	1	0x0	B
		HS3_STG_REDIRECT_CFG 0: Fault redirected on FS_FLAG/IC ERR (Default) 1: Fault redirection masked	RW	6	1	0x0	B
		UNUSED_0	RO	15	1	0x0	A
		STP_VGS_3_REDIRECT_CFG	RW	4	1	0x0	B

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
SLR		0: Fault redirected on FS_FLAG/IC ERR (Default) 1: Fault redirection masked					
		STP3_VGS_CFG 00: 0.2 µs (Defaults) 01: 0.5 µs 10: 1 µs 11: 1.5 µs	RW	2	2	0x0	B
		STP3_PWM_CFG 00: 0.2 µs (Defaults) 01: 0.5 µs 10: 1 µs 11: 1.5 µs	RW	0	2	0x0	B

Table 139. CH3_CFG2

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH3_CFG2	0x33	UNUSED	RW	11	5	0x0	B
SLR		CSM3_SYNC_COUNT_CFG 00: 16Tclk (Default) 01: 24Tclk 10: 32Tclk 11: 40Tclk	RW	9	2	0x0	B
		UNUSED_0	RW	8	1	0x0	B
		CSM3_SAMPLE_CFG 000: Free running – No T&H (Default) 001: T&H 1st data conversion from triggering 010: T&H 2nd data conversion from triggering 011: T&H 3rd data conversion from triggering 100: T&H 4th data conversion from triggering 101: T&H 5th data conversion from triggering 110: T&H 6th data conversion from triggering 111: T&H 7th data conversion from triggering	RW	5	3	0x0	B
		CSM3_IN_RANGE_CFG 000: VIN_MAX = ±7 mV 001: VIN _MAX = ±18 mV 010: VIN _MAX = ±36 mV 011: VIN_MAX = ±90 mV 100: VIN_MAX = ±160 mV 101: VIN_MAX = ±300 mV (Default) 110: Reserved 111: Reserved	RW	2	3	0x5	B
		CSM3_OFS 00: 0LSB DAC	RW	0	2	0x3	B

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
SLR		01: 90LSB DAC 10: 1024LSB DAC 11: 1024LSB DAC (Default)					
		0	0	0	0	0	0

Table 140. CH3_CFG3

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH3_CFG3	0x34	UNUSED_3	RW	15	1	0x0	B
NSR		UNUSED_2	RW	14	1	0x0	B
		UNUSED_1	RW	13	1	0x0	B
		UNUSED_0	RW	12	1	0x0	B
		ACT3_EN 0: ACT Disabled (Default) 1: ACT Enabled	RW	11	1	0x0	B
		TSYNC3_CFG	RW	0	11	0x0	B

Table 141. CH3_SAFETY_RELEVANT

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH3_SAFETY_RELEVANT	0x35	UNUSED_4	RW	15	1	0x0	B
SRR		UNUSED_3	RW	14	1	0x0	B
		UNUSED_2	RW	13	1	0x0	B
		STP_VGS_3_REACT_CFG 00: Full SW Off – disable all HB drivers and CPs, device is sent in SAFE-OFF mode (Default) 01: Reduced Operation Mode – disable failing HB only, device remains in NORMAL mode 10: Flag only – down-rate fault to simple warning, device remains in NORMAL mode 11: Flag only – down-rate fault to simple warning, device remains in NORMAL mode	RW	11	2	0x0	B
		UNUSED_1	RW	10	1	0x0	B
		UNUSED_0	RW	9	1	0x0	B
		LS3_STB_REACT_CFG	RW	7	2	0x0	B
		HS3_STG_REACT_CFG	RW	5	2	0x0	B
		CRC	RW	0	5	0x17	B

Table 142. **CH3_ACT**

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
CH3_ACT	0x36	UNUSED_3	RO	15	1	0x0	A
NSR		UNUSED_2	RO	14	1	0x0	A
		UNUSED_1	RO	13	1	0x0	A
		UNUSED_0	RO	12	1	0x0	A
		ACT3_OVF	RO	11	1	0x0	A
		ACT3	RO	0	11	0x0	A

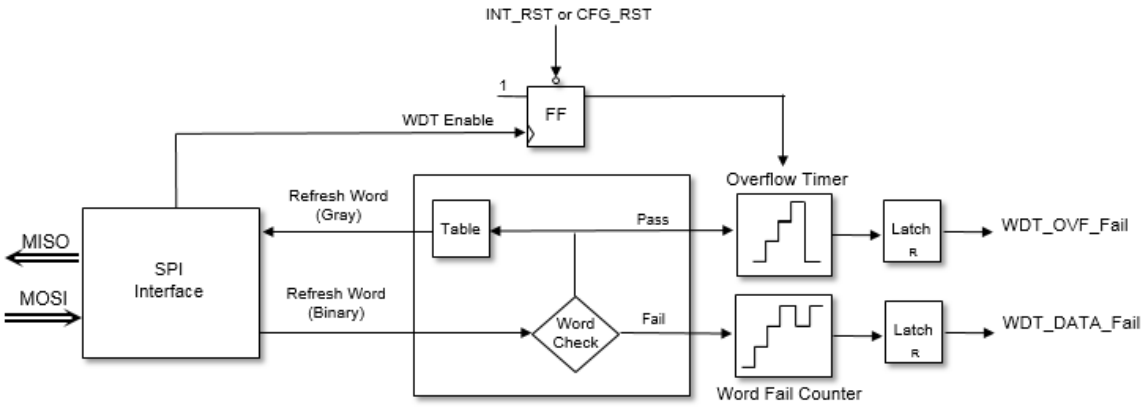
Table 143. **SPI_CMM_FAULT**

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Reset
SPI_CMM_FAULT	0xFD	UNUSED_11	RO	15	1	0x0	A
NSR		UNUSED_10	RO	14	1	0x0	A
		UNUSED_9	RO	13	1	0x0	A
		FCNTERR Wrong Frame Counter bit	CR	12	1	0x0	A
		CRCERR Wrong CRC check value	CR	11	1	0x0	A
		SHORTERR Previous SPI frame length<32 bit	CR	10	1	0x0	A
		LONGERR Previous SPI frame length>32 bit	CR	9	1	0x0	A
		UNUSED_8	RO	8	1	0x0	A
		UNUSED_7	RO	7	1	0x0	A
		UNUSED_6	RO	6	1	0x0	A
		UNUSED_5	RO	5	1	0x0	A
		UNUSED_4	RO	4	1	0x0	A
		UNUSED_3	RO	3	1	0x0	A
		UNUSED_2	RO	2	1	0x0	A
		UNUSED_1	RO	1	1	0x0	A
		UNUSED_0	RO	0	1	0x0	A

5.21 Window Watchdog Timer (WTD)

L9908 implements a watchdog timer function to ensure a safe SPI communication with µC in case of corrupted or lost SPI communication.

Figure 85. **Watchdog Timer simplified block diagram**



Watchdog timer function can be enabled by the SPI signal WDT_EN in the register GEN_CFG1:

Table 144. **Watchdog enable bit**

WDT_EN	Description
0	Watchdog disabled (Default)
1	Watchdog enabled

Once enabled, WDT_EN can be reset to disable only by INT_RST = 0 or CFG_RST = 0.

Activation status of WDT is also stored in the SPI read only register WD_ON_STATUS: WD_ON_STATUS = 0 WDT is not active, WD_ON_STATUS = 1 WDT is active.

As soon as the watchdog is enabled the overflow counter is started thus defining the available refresh window Twdt_ovf which length is defined by the SPI register WDT_OVF_CFG.

Table 145. **Watchdog configuration table for WDT overflow timer**

WDT_OVF_CFG1	WDT_OVF_CFG0	Description
0	0	11.26 ms
0	1	22.52 ms (Default)
1	0	45.04 ms
1	1	90.11 ms

The WDT overflow counter status can be accessed through the dedicated SPI read only register WDT_OVF_STATUS.

The counter value in seconds can be retrieved by the following reconstruction formula:

$$T_{WTD\_OVF-STATUS} = \Delta_{WTD\_OVF\_LSB} \times D_{WTD\_OVF\_STATUS} \quad (27)$$

Where: D_{WDT_OVF} is the digital word stored in WDT_OVF_STATUS and $\Delta_{WDT\_OVF\_LSB}$ is the counter LSB as defined in Table 146.

Table 146. **WDT overflow timer LSB**

WDT_OVF_CFG	Description
00	0.2048 ms
01	0.4096 ms (Default)
10	0.8192 ms

WDT_OVF_CFG	Description
11	1.6384 ms

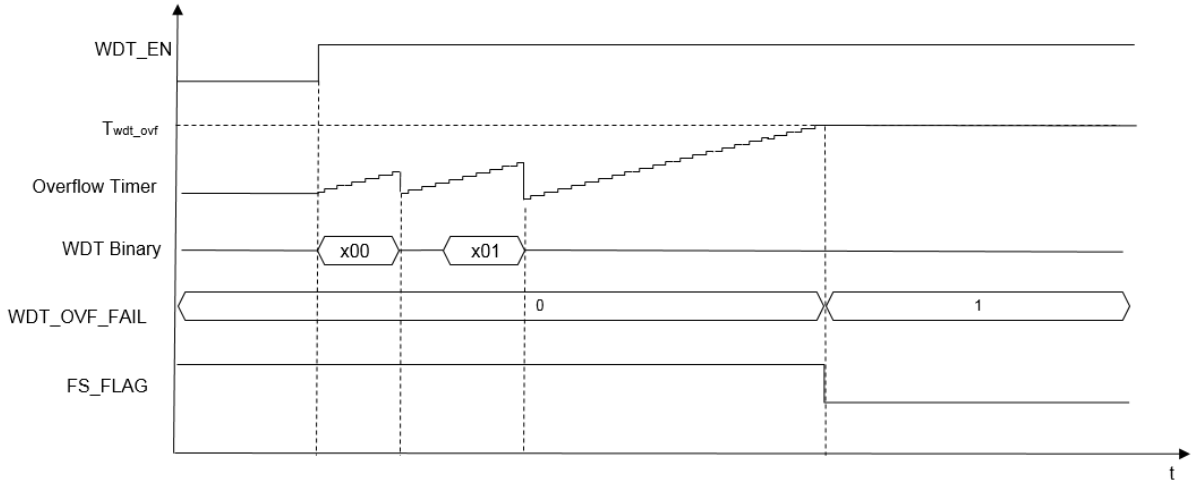
Reprogramming of WDT_OVF_CFG configuration is possible only while WDT_EN = 0

Table 147. WDT overflow counter accuracy

Symbol	Parameter	Min	Typ	Max	Unit
WDT_ovf_acc	WDT overflow counter accuracy	-10	-	10	%

Within this window the watchdog expects a refresh pulse to reset the overflow counter and restart a new window: if refresh is missed before the overflow counter is elapsed the error flag WDT_OVF_Fail is set and L9908 is sent to safe state. The flag remains set until the WDT is reset by the SPI command or re-enabled after a power-on sequence.

Figure 86. WDT Operation – Overflow timer failure



The refresh of the overflow counter has to be performed by the uC through a dedicated SPI frame including the 4-bit watchdog refresh command. The watchdog circuitry compares the received watchdog refresh command with an internal look-up table and answers with a corresponding 4-bit Gray code in the next SPI MISO frame.

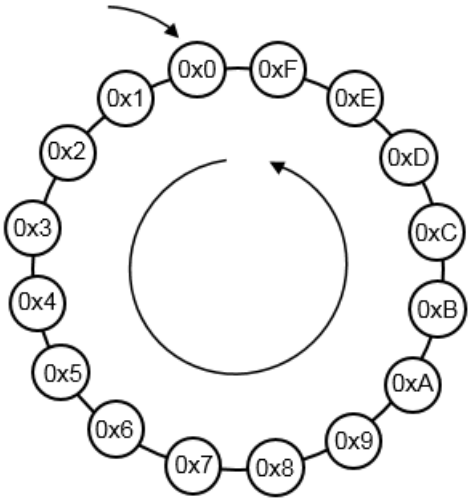
Table 148. Watchdog Binary to Gray answer conversion

Binary (µC) → Gray (L9908)	Binary → (µC) → Gray (L9908)	Binary (µC) → Gray (L9908)	Binary (µC) → Gray (L9908)
0x0 (0000) → 0x0 (0000)	0x4 (0100) → 0x6 (0110)	0x8 (1000) → 0xC (1100)	0xC (1100) → 0xA (1010)
0x1 (0001) → 0x1 (0001)	0x5 (0101) → 0x7 (0111)	0x9 (1001) → 0xD (1101)	0xD (1101) → 0xB (1011)
0x2 (0010) → 0x3 (0011)	0x6 (0110) → 0x5 (0101)	0xA (1010) → 0xF (1111)	0xE (1110) → 0x9 (1001)
0x3 (0011) → 0x2 (0010)	0x7 (0111) → 0x4 (0100)	0xB (1011) → 0xE (1110)	0xF (1111) → 0x8 (1000)

The expected watchdog command order starts with number 0x0 (0000) and is incremented by 1 at each refresh window if the command is correctly interpreted and no failure is detected.

Once command number 0xF (1111) is reached the sequence restarts with number 0x0 (0000).

Figure 87. **Watchdog command order sequence**



In case of a wrong WDT data command (command different from the expected sequence order), the watchdog word fail counter is incremented by 1. With the next valid watchdog data command the fail counter is decreased by 1. If the failure counter reaches the failure limit defined in the SPI register WDT_FAIL_COUNT_CFG the watchdog fail flag WDT_DATA_fail is set and L9908 is sent to safe state.

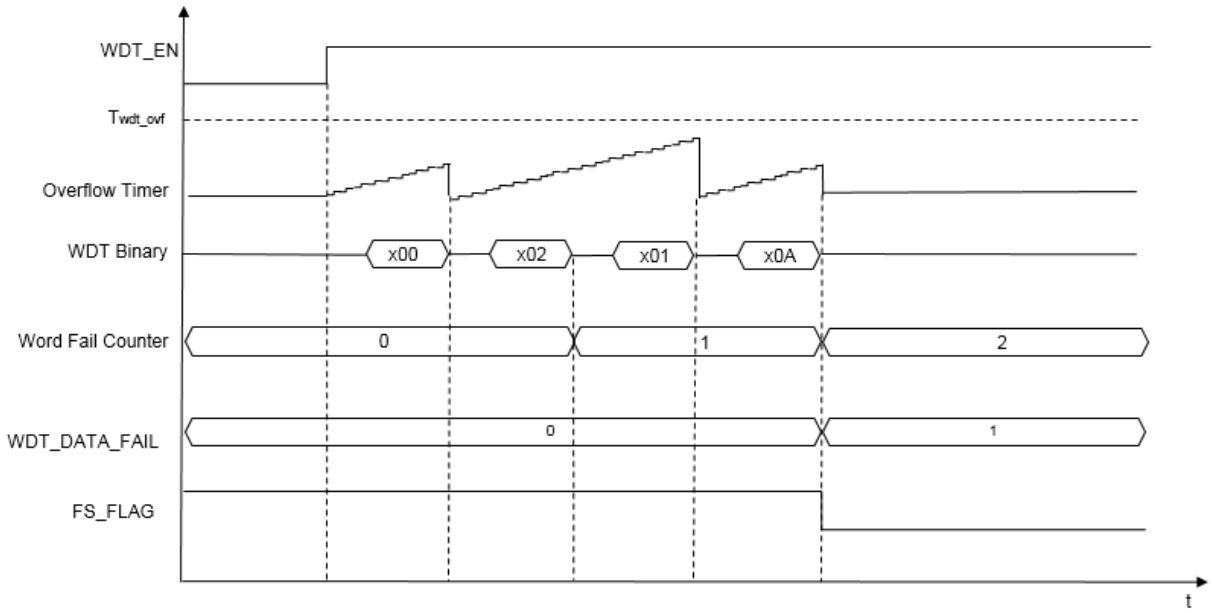
The fail counter limit can be programmed by the following SPI bit set:

Table 149. **Watchdog configuration table for WDT data fail counter**

WDT_FAIL_COUNT_CFG1	WDT_FAIL_COUNT_CFG0	Description
0	0	1
0	1	1
1	0	2
1	1	3 (Default)

The information about the number of encountered WDT data failures is stored in the dedicated SPI register WDT_FAIL_COUNT_STATUS.

Figure 88. **WDT Operation – Word sequence failure**



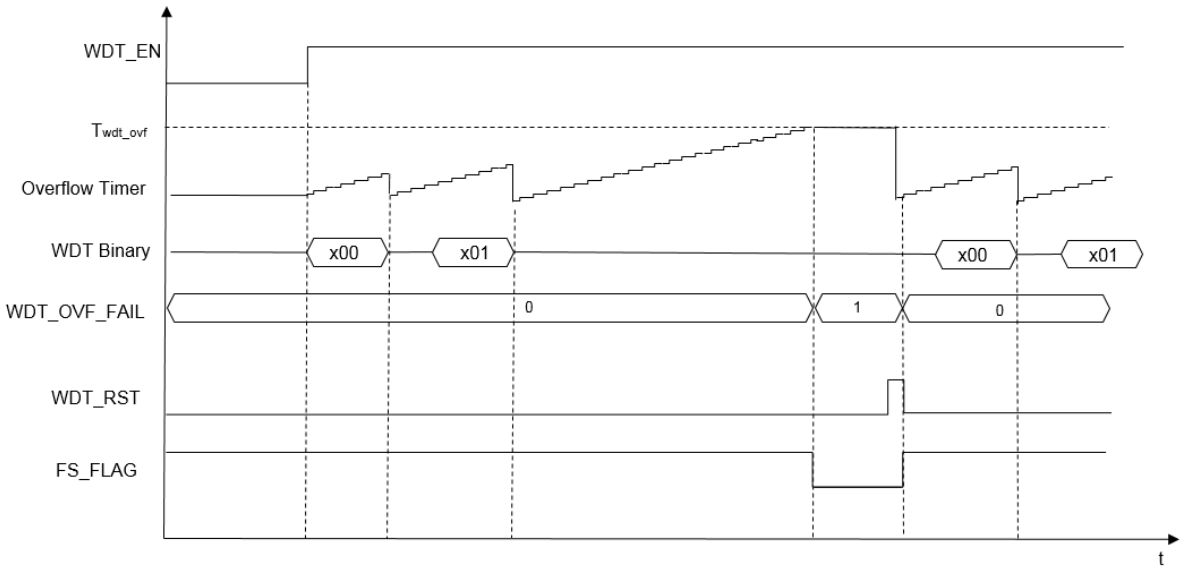
In case of failure (WDT_OVF_fail =1 or WDT_DATA_fail =1) the WDT can be reset by setting to10 the SPI register command WDT_RESET.

Table 150. **Watchdog RESET bits**

WDT_RST1	WDT_RST0	Description
0	0	NO Reset
0	1	NO Reset (Default)
1	0	Reset
1	1	NO Reset

Note: This command is processed by the logic only if a failure is detected (WDT_OVF_fail = 1 or WDT_DATA_fail = 1). The WDT_RESET doesn't reset the WDT_EN bit but only the error flag: µC needs to refresh the WDT properly afterwards.

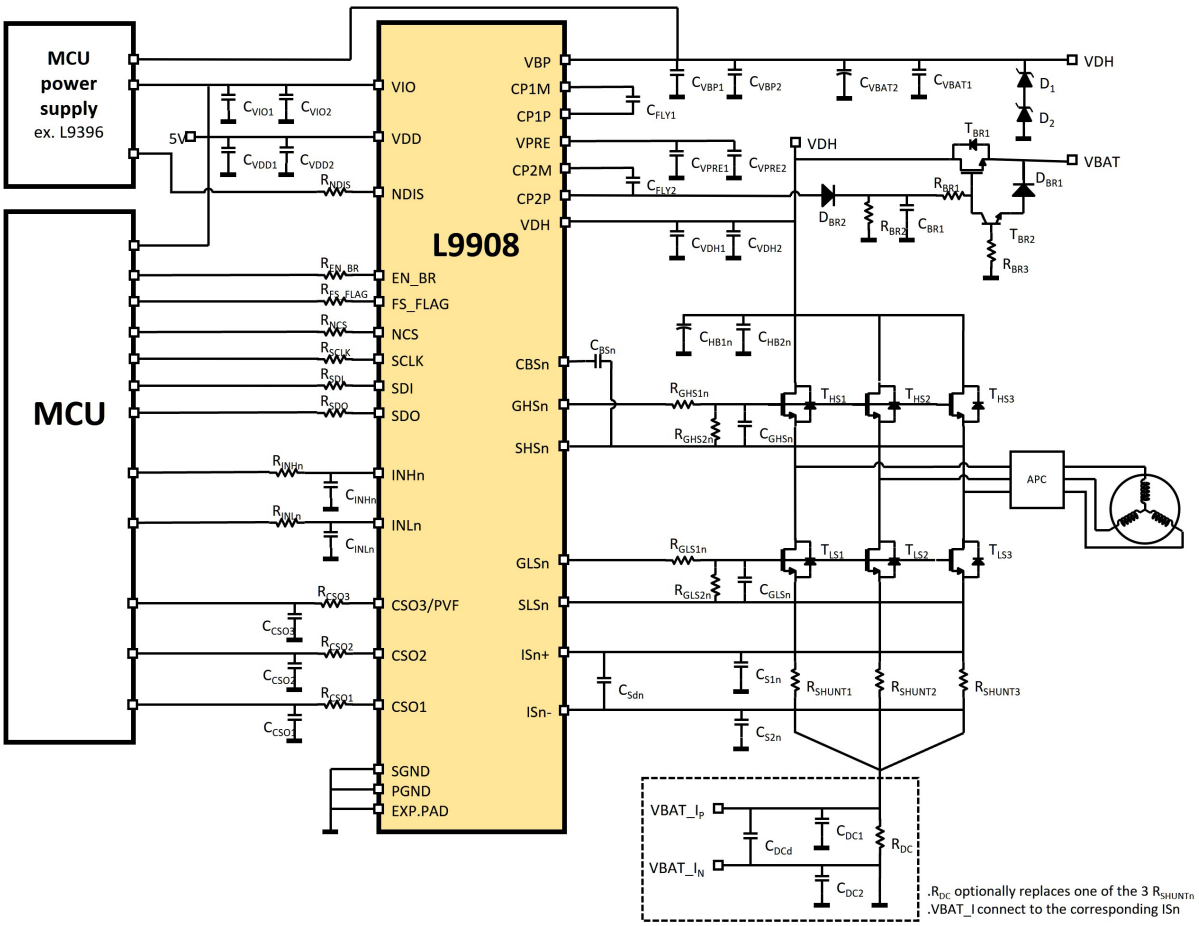
Figure 89. **WDT Operation – WDT Reset after overflow timer failure**



6 Application circuit

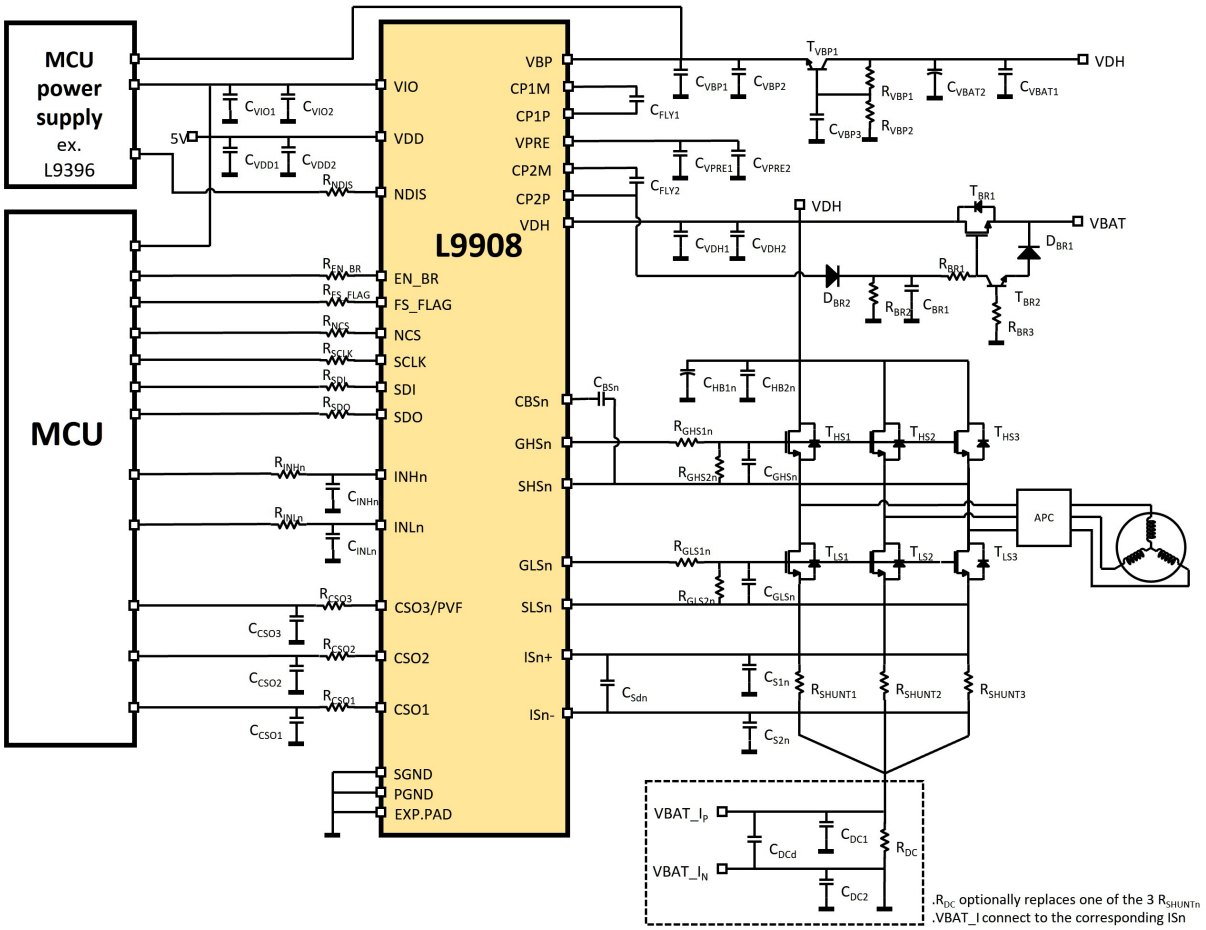
6.1 12 V/24 V systems

Figure 90. **Application circuit, 12 V/24 V systems**



6.2 48 V systems

Figure 91. **Application circuit, 48 V systems**



6.3 Bill of materials

The following table summarizes the suggested BOM for both systems shown on Figure 90 and Figure 91.

Table 151. **Application circuit - BOM**

Component	Min	Typ	Max	Unit	Minimum requirement			Comment
					12 V systems	24 V systems	48 V systems	
C_{BR1}	-	390	-	nF	50 V	100 V		-
C_{BSn}	-	1	-	µF	25 V			-
C_{CSO1}	-	220	-	pF	6.3 V			With $R_{CSO1,2,3}$, is mandatory for CSO signal stability
C_{CSO2}	-	220	-	pF	6.3 V			
C_{CSO3}	-	220	-	pF	6.3 V			
C_{DC1}	-	10	-	nF	6.3 V			Max tolerance ±5% to be mounted close to R_{DC}
C_{DC2}	-	10	-	nF	6.3 V			Max tolerance ±5% to be mounted close to R_{DC}
C_{DCd}	-	220	-	nF	6.3 V			To be mounted close to pin

Component	Min	Typ	Max	Unit	Minimum requirement			Comment
					12 V systems	24 V systems	48 V systems	
C_{FLY1}	-	1	-	µF	50 V	100 V		-
C_{FLY2}	-	1	-	µF	50 V	100 V		-
C_{GHSn}	-	-	-		16 V			Optional
C_{GLSn}	-	-	-		16 V			Optional
C_{HB1n}	-	100	-	nF	50 V	100 V		-
C_{HB2n}	-	220	-	µF	50 V	100 V		-
C_{INHn}	-	10	-	pF	6.3 V			Optional
C_{INLn}	-	10	-	pF	6.3 V			Optional
C_{S1n}	-	10	-	nF	6.3 V			Max tolerance ±5% to be mounted close to R_{SHUNTn}
C_{S2n}	-	10	-	nF	6.3 V			Max tolerance ±5% to be mounted close to R_{SHUNTn}
C_{Sdn}	-	220	-	nF	6.3 V			To be mounted close to pin
C_{VBAT1}	-	100	-	nF	50 V	100 V		-
C_{VBAT2}	-	10	-	µF	50 V	100 V		-
C_{VBP1}	-	1	-	µF	50 V	100 V	16 V	-
C_{VBP2}	-	100	-	nF	50 V	100 V	16 V	To be mounted close to pin
C_{VBP3}	-	100	-	nF	n.a.		50 V	-
C_{VDD1}	-	1	-	µF	6.3 V			-
C_{VDD2}	-	100	-	nF	6.3 V			To be mounted close to pin
C_{VDH1}	-	100	-	nF	50 V	100 V		To be mounted close to pin
C_{VDH2}	-	1	-	µF	50 V	100 V		-
C_{VIO1}	-	1	-	µF	6.3 V			-
C_{VIO2}	-	100	-	nF	6.3 V			To be mounted close to pin
C_{VPRE1}	-	4.7	6.8	µF	16 V			Max tolerance ±20%
C_{VPRE1}	-	4.7	6.8	µF	n.a.	16 V		Max tolerance ±20%
C_{VPRE2}	-	100	-	nF	16 V			To be mounted close to pin
D_1	-	-	-		SMA6T39AY	SMA6T56AY	n.a.	-
D_2	-	-	-		Short	SMA6T6V7AY		-
D_{BR1}	-	-	-	-	STPS3L60			-
D_{BR2}	-	-	-	-	STPS0520Z			-
R_{VBP1}	-	22	-	kΩ	-			-
R_{VBP2}	-	22	-	kΩ	-			-
R_{BR1}	-	1	-	kΩ	-			-
R_{BR2}	-	39	-	kΩ	-			-
R_{BR3}	-	22	-	kΩ	-			-
R_{CSO1}	-	1	-	kΩ	-			With $C_{CSO1,2,3}$, is mandatory for CSO signal stability
R_{CSO2}	-	1	-	kΩ	-			

Component	Min	Typ	Max	Unit	Minimum requirement			Comment
					12 V systems	24 V systems	48 V systems	
R_{CSO3}	-	1	-	kΩ	-			With $C_{CSO1,2,3}$, is mandatory for CSO signal stability
R_{DC}	-	4	-	mΩ	WSL10204L000FEA			-
R_{EN_BR}	-	100	-	Ω	-			Optional
R_{FS_FLAG}	-	100	-	Ω	-			Optional
R_{GHS1n}	-	47	-	Ω	-			-
R_{GHS2n}	-	100	-	kΩ	-			-
R_{GLS1n}	-	47	-	Ω	-			-
R_{GLS2n}	-	100	-	kΩ	-			-
R_{INHn}	-	100	-	Ω	-			Optional
R_{INLn}	-	100	-	Ω	-			Optional
R_{NCS}	-	100	-	Ω	-			Optional
R_{NDIS}	-	100	-	Ω	-			Optional
R_{SCLK}	-	100	-	Ω	-			Optional
R_{SDI}	-	100	-	Ω	-			Optional
R_{SDO}	-	100	-	Ω	-			Optional
R_{SHUNTn}	-	4	-	mΩ	WSL10204L000FEA			-
T_{BR1}	-	-	-	-	STL225N6F7AG	STH275N8F7		-
T_{BR2}	-	-	-	-	BCP56-16			-
T_{VBP1}	-	-	-	-	BCP56-16			-
T_{HSn}	-	-	-	-	STL225N6F7AG	STD105N10F7AG		-
T_{LSn}	-	-	-	-	STL225N6F7AG	STD105N10F7AG		-

6.4 Layout guidelines

The following layout guidelines apply to any of the above shown application circuits.

- Three separated bulk capacitors CHB1 should be used - one per half bridge.
- Three separated ceramic capacitors CHB2 should be used - one per half bridge.
- Each of the 3 bulk capacitors CHB1 and each of the 3 ceramic capacitors CHB2 should be assigned to one of the half bridges and should be placed very close to it.
- The components within one half bridge should be placed close to each other to reduce stray inductance to a minimum: high-side MOSFET, low-side MOSFET, bulk capacitor CHB1, ceramic capacitor CHB2 and the shunt resistor RSHUNT form a loop that should be as small and tight as possible. The traces should be short and wide.
- The three half bridges can be separated; however, when there is one common GND referenced shunt resistor (RDC) for the three half bridges the sources of all low-side MOSFETs should be close to each other and close to the common shunt resistor.
- Additional R-C snubber circuits can be placed to attenuate/suppress oscillations during switching of the MOSFETs, there may be one or two snubber circuits per half bridge and components must be low inductive in terms of routing and packaging (ceramic capacitors).
- The exposed pad on the backside of the package shall be connected to GND.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 TQFP48 (7x7x1 mm exp. pad down) package information

Figure 92. **TQFP48 (7x7x1 mm exp. pad down) package outline**

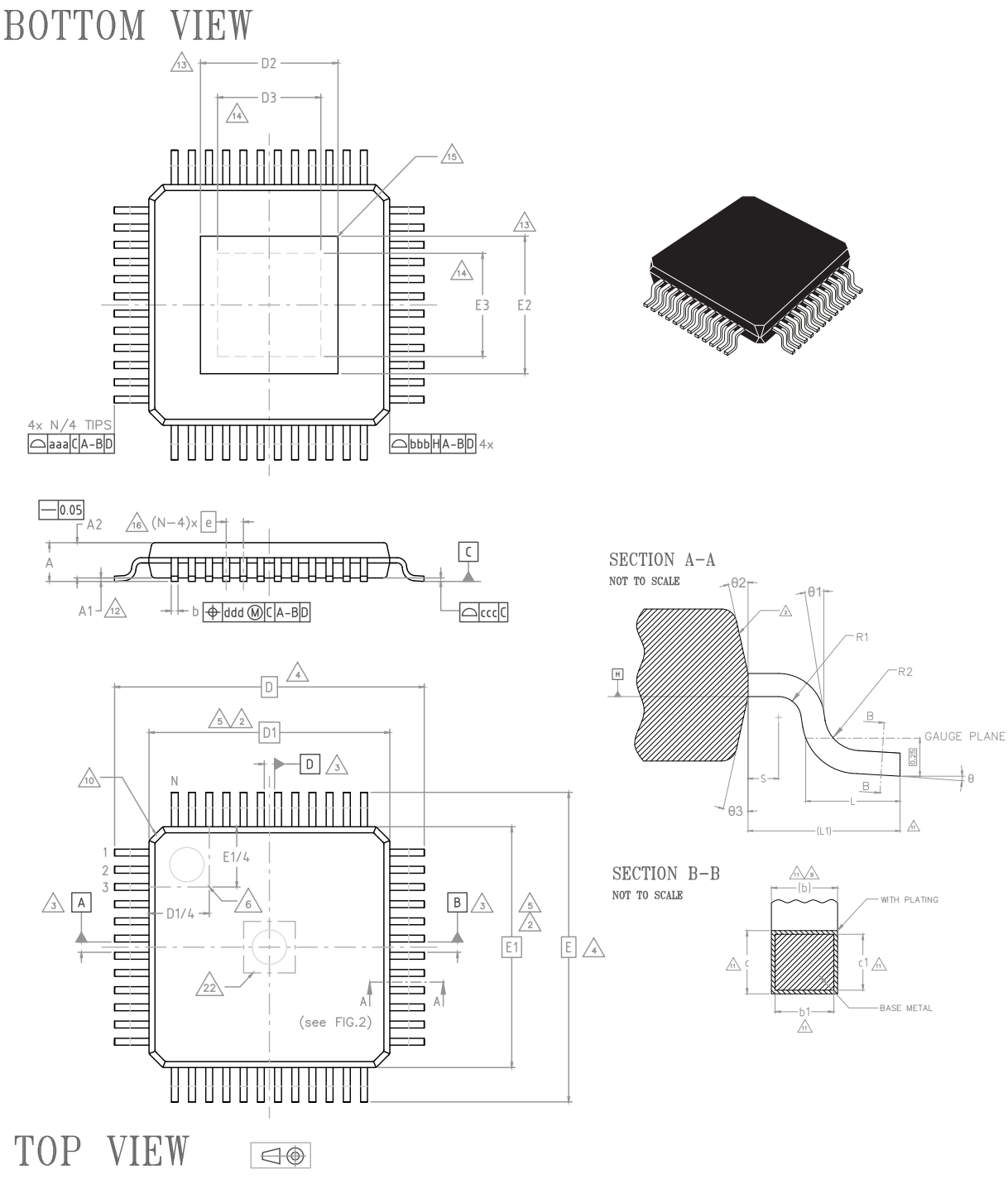
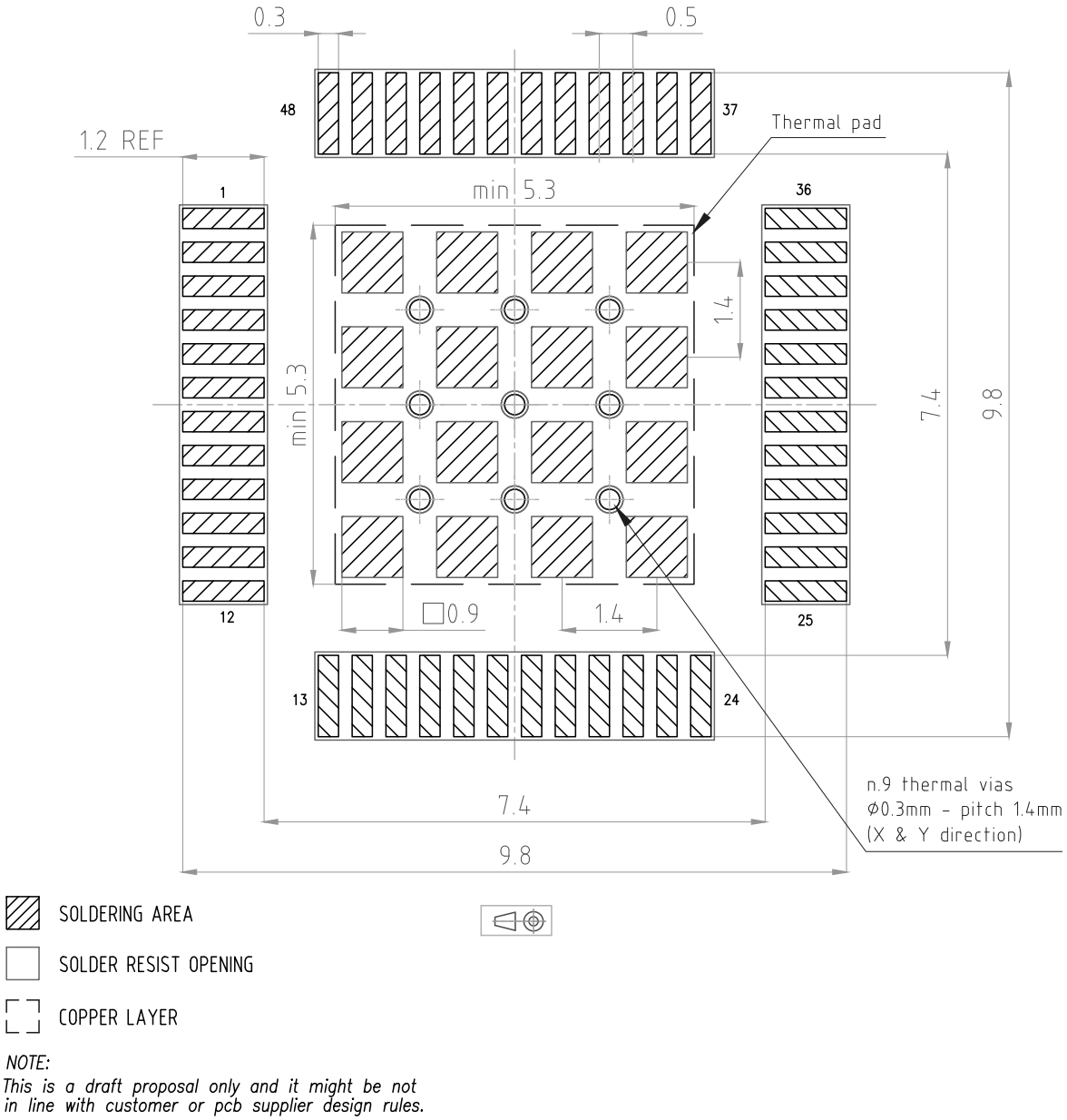


Table 152. **TQFP48 (7x7x1 mm exp. pad down) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
e	0°	3.5°	7°
e1	0°	-	-
e2	10°	12°	12°
e3	10°	12°	12°
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	-	0.20
D		9.00	
D1		7.00	
D2	-	-	5.51
D3	3.70	-	-
e	-	0.50	-
E		9.00	
E1		7.00	
E2	-	-	5.51
E3	3.70	-	-
L	0.45	0.60	0.75
L1		1.00	
N		48	
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
Tolerance of form and position			
aaa	-	0.20	-
bbb	-	0.20	-
ccc	-	0.08	-
ddd	-	0.08	-

7.2 TQFP48 (7x7x1 mm exp. pad down) PCB landpattern

Figure 93. Suggested PCB landpattern



NOTE:
This is a draft proposal only and it might be not in line with customer or pcb supplier design rules.

Revision history

Table 153. **Document revision history**

Date	Version	Changes
16-Nov-2020	1	Initial release.
03-Mar-2021	2	Updated: • Section 5.9 Internal clock; • Section 5.13.1 A/D conversion; • Section 5.13.2.3 Digital format current information • Section 5.13.3.1 Analog format current information; • Section 5.13.4 Current monitor A/D - D/A chain; • Table 12. VDD monitor electrical characteristics; • Table 36. Clock spread spectrum electrical characteristics; • Table 42. Motor battery monitor electrical characteristics; • Table 44. Pre-regulation stage electrical characteristics; • Table 48. VBP monitor electrical characteristics; • Table 51. Charge pump 2 electrical characteristics; • Table 53. Bootstrap Limiter 1 electrical characteristics; • Table 54. VCP Monitor electrical characteristics; • Table 70. Current Monitor Input characteristics; • Table 79. Current monitor`s analog output characteristics • Table 87. OFD electrical characteristics; • Table 91. OND electrical characteristics; • Table 93. PVF electrical characteristics. Removed "Restricted" watermark.
28-Mar-2022	3	Added Section 7.2 TQFP48 (7x7x1 mm exp. pad down) PCB landpattern. Updated: • Section 5.11.4 Supply distribution stage; • Section 5.12 Half bridges gate drivers; • Section 5.12.3 Shoot-Through Protection (STP); • Section 5.13.1 A/D conversion; • Section 6.3 Bill of materials; • Table 9. Quiescent current consumption in reset mode; • Table 10. Mean current consumptions in normal mode; • Table 44. Pre-regulation stage electrical characteristics; • Table 53. Bootstrap Limiter 1 electrical characteristics; • Table 54. VCP Monitor electrical characteristics; • Table 58. Pre-driver timings; • Table 60. VGS monitor electrical characteristics; • Table 76. Current monitors A/D auto-triggering latency; • Table 80. Current monitors A/D - D/A auto-triggering latency; • Table 93. PVF electrical characteristics; • Table 127. CH1_SAFETY_RELEVANT; • Table 152. TQFP48 (7x7x1 mm exp. pad down) package mechanical data; • Figure 7. Damage protected activation simplified structure; • Figure 10. Internal reset logic simplified block diagram; • Figure 23. Power-Up diagram; • Figure 26. Ext. FET gate supply simplified block diagram; • Figure 39. VGS Monitor operative ranges; • Figure 65. OFF State Diagnosis simplified block diagram; • Figure 66. OFD currents in motor phases;

Date	Version	Changes
		• Figure 68. OFD Masking and deglitch filtering - LSn_OFD Example; • Figure 69. OFD Masking and deglitch filtering - LSn_OFD Example with multiple glitches; • Figure 77. Ground pins inter-connection; • Figure 79. Junction temperature ranges; • Figure 90. Application circuit, 12 V/24 V systems; • Figure 91. Application circuit, 48 V systems. Minor text changes in: • Section 5.4 Configuration mode; • Section 5.6.4 Gate driver supply enable logic.

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