L99LD02

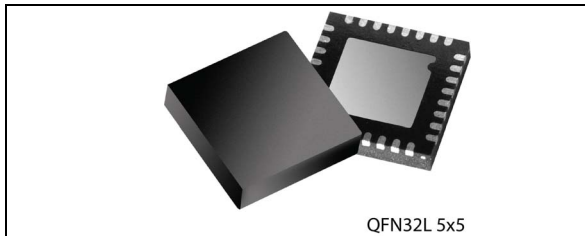## Automotive dual-phase boost DC/DC controller

QFN32L 5x5

Features

- AEC-Q100 qualified
- General
  - 32-bit ST SPI communication v 4.1
  - Stand-alone operation supported
  - QFN32L 5x5 with exposed pad
  - Timeout watchdog and Limp Home function
- Boost section
  - Wide input range: 3V to 28V operation
  - Device supply option from boost output
  - Adjustable boost output voltage - up to 80V
  - 10V Gate Driver supply for Standard-Level MOSFETs
  - Internal 10V LDO regulator
  - Fixed frequency architecture - programmable by SPI
  - Dither oscillator parameters as frequency modulation and deviation percentage - programmable by SPI
  - Peak current mode control with programmable Input Current Limitation
  - Constant voltage regulation
  - Adjustable Slope Compensation
  - Soft start
  - Multi-phase operation - up to 4-phase supported
  - SYNC I/O pin for multi-phase operation support
  - Adjustable clock distribution and phase shift
  - Programmable error amplifier gain
  - Fully configurable in Limp Home
- Protection and diagnostic
  - Boost functionality guaranteed in Cold Cranking
  - Input overcurrent protection - programmable by SPI
  - Thermal warning
  - Thermal shutdown
  - Overvoltage protection (OVP)

Applications

LED module applications.

Description

The L99LD02 is a two-phase, constant frequency, current mode boost controller able to drive N-channel power MOSFETs.

Multi-phase operation is supported by SYNC I/O pin, providing the phase shifted clock signal. The boost controllers of more devices can be stacked, in order to operate in multi-phase for high power applications. Multi-phase operation reduces system filtering capacitance and inductance requirements.

The operating frequency is configurable via SPI between 100kHz and 470kHz. Other features include an internal 10V LDO for the gate drivers, soft-start, device supply option from boost output and pre-configurable operation in Limp Home.

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1 Introduction

The L99LD02 is a dual-phase, constant frequency, current mode boost controller that drives N-channel power MOSFETs providing a regulated voltage on BST_OUT pin.

The boost controllers of more devices can be stacked, in order to operate in multi-phase for high power applications. Multi-phase operation is supported by SYNC I/O pin, providing the phase shifted clock signal. Special care has been taken for the current balancing between the different phases and for the switching activity of the boost MOSFETs with proper phase shift.

The device offers a high level of flexibility, without any change of the external components, thanks to its programmability through the ST SPI interface. This feature supports generic platform approaches, which require a software configuration of several parameters. Moreover, this robust interface offers a detailed diagnostic of the device itself.

The L99LD02 features a timeout watchdog, a monitoring of the watchdog counter and a Limp Home function. The device is fully configurable in Limp Home through OTP bits, allowing stand-alone operation.

The L99LD02 integrates a 10 V LDO to supply the gate drivers for standard level MOSFETs and features a supply option from boost output to supply the device when battery level is not enough to guarantee fully Ron external MOSFETs and to fulfill cold cranking requirement.

The input of the boost stage must be connected to the battery voltage through a reverse polarity protection.

The output of the L99LD02 can reach up to 80 V. This allows system designers to drive LED strings up to 60 V.

1.1 Typical application

Figure 1. Functional block diagram
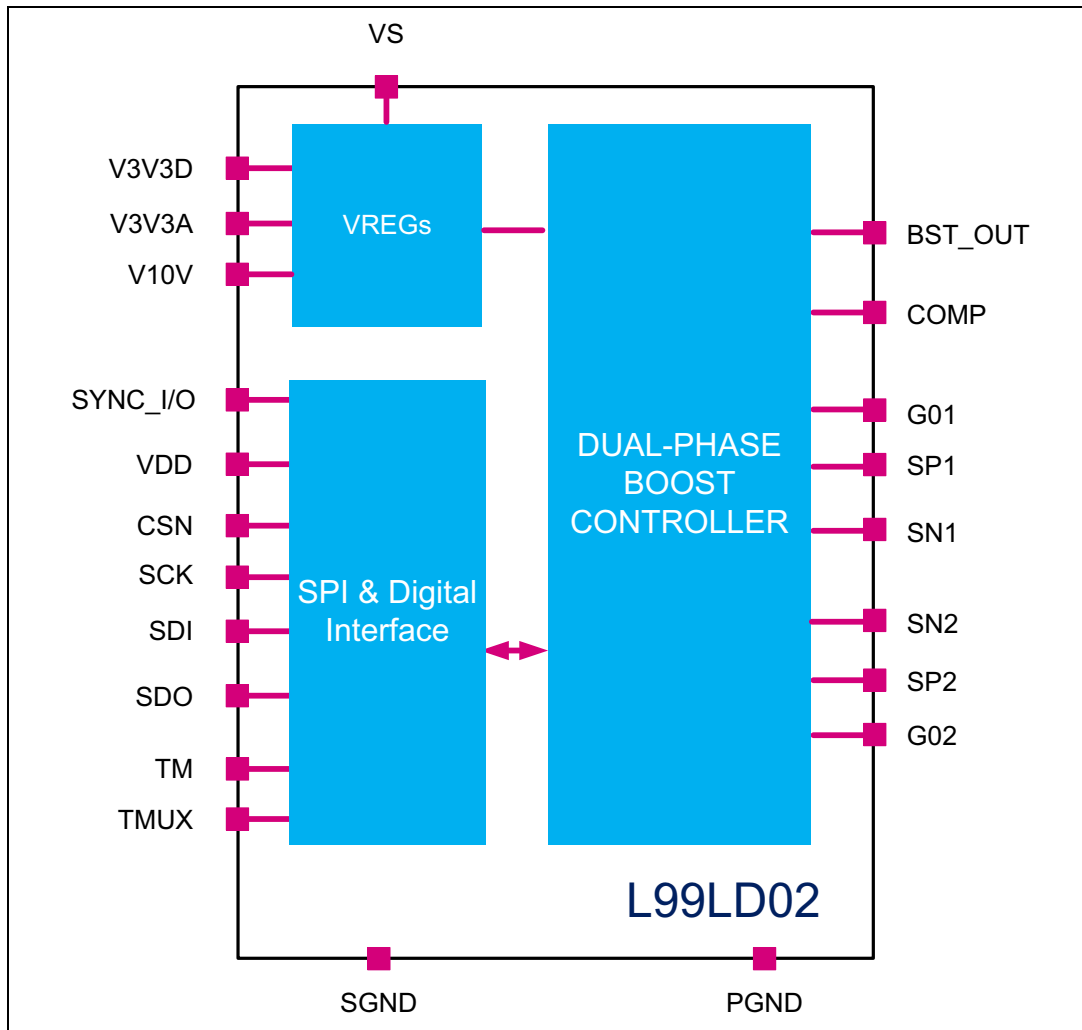
Figure 2. Typical application
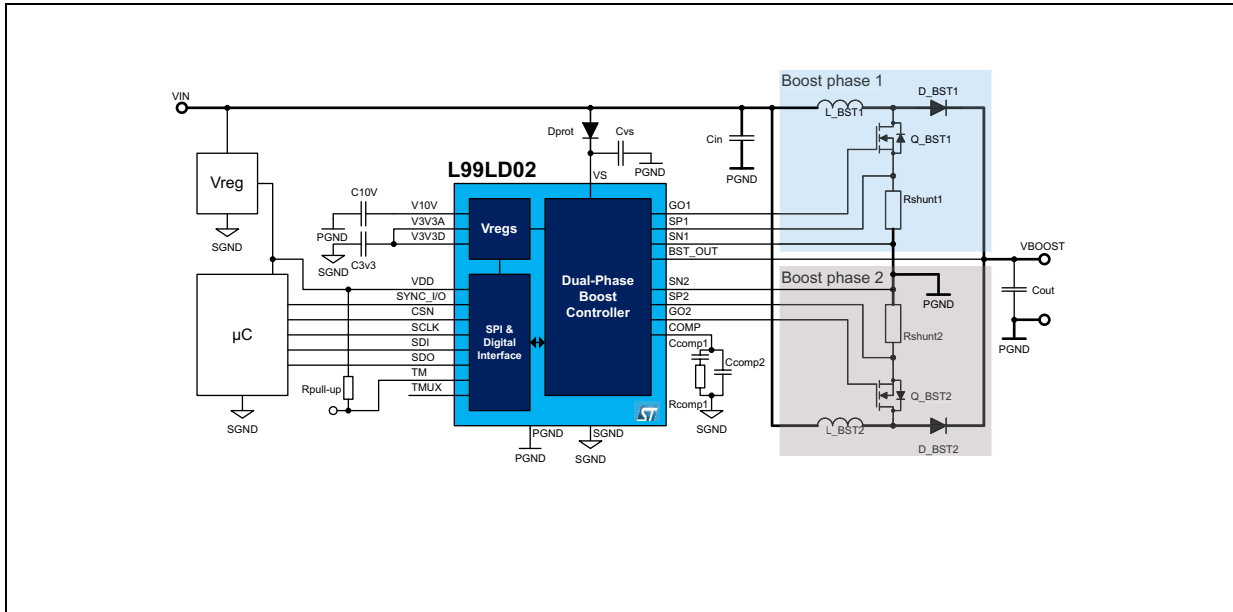
Figure 3. QFN-32L connection diagram
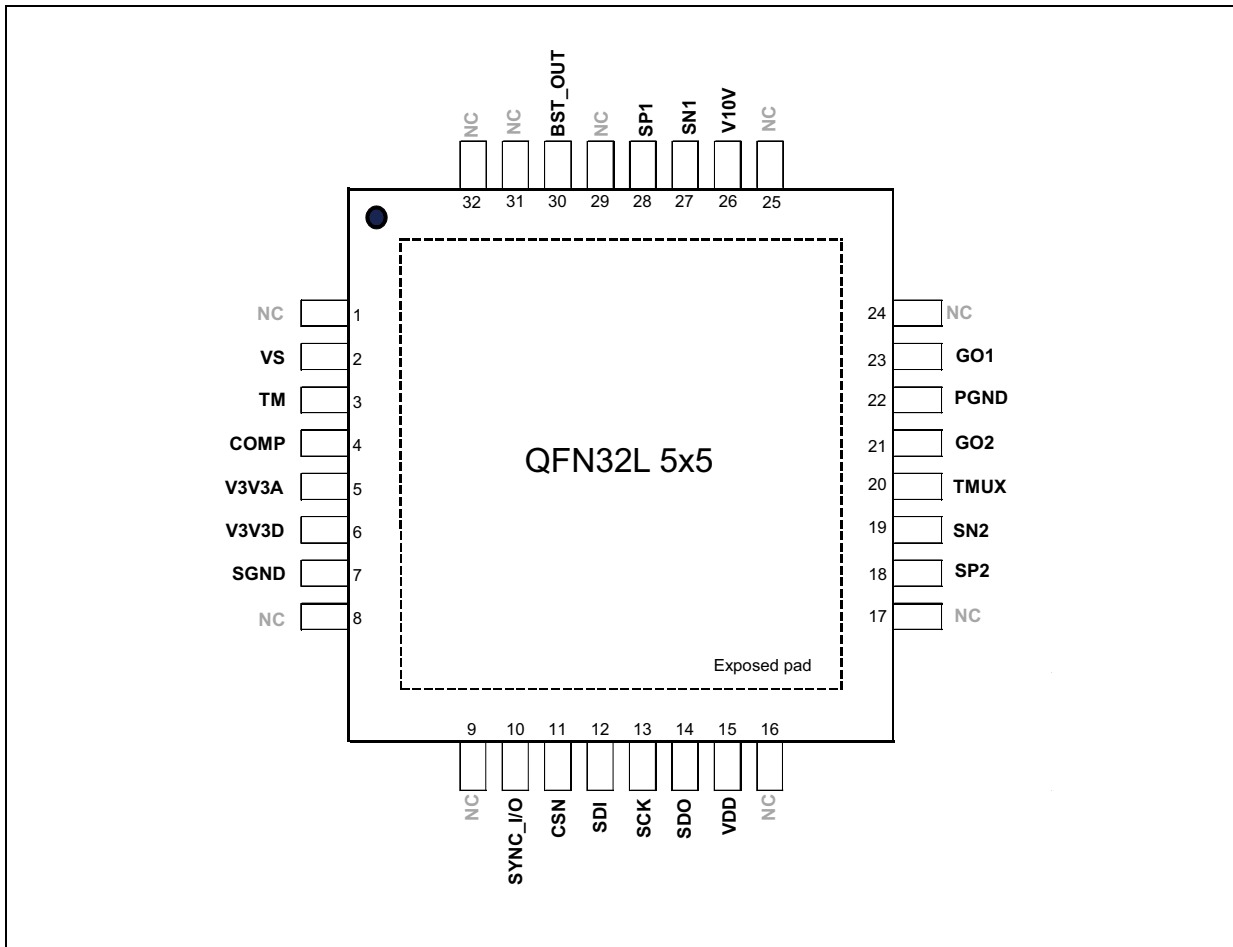
Table 1. Pin functionality

Pin Number	Name	Function
2	VS	Input supply pin of the IC. Connect to the battery voltage through a Schottky diode.
3	TM	Internal Function. Drive this line from fail safe logic or directly with microcontroller I/O pin. This pin can be used for stand-by mode activation in Limp Home.
4	COMP	Output of the error amplifier of the boost controller. Connect the compensation network between this pin and GND.
5,6	V3V3A, V3V3D (Note 1)	Output of the 3.3 V regulated internal supply (logic supply). Connect a low ESR capacitor (1uF) close to this pin.
7	SGND	Signal Ground connection.
10	SYNC_I/O	Boost synchronization Input / Output pin. This pin generates the clock signal for synchronizing another L99LD02 in multi-phase configuration.
11	CSN	Chip Select Not (active low) for SPI communication. It is the selection pin of the device. It is a CMOS compatible input.
12	SDI	Serial Data Input for SPI communication. Data is transferred serially into the device on SCLK rising edge.
13	SCK	Serial Clock for SPI communication. It is a CMOS compatible input.
14	SDO	Serial Data Output for SPI communication. Data is transferred serially out of the device on SCLK falling edge.
15	VDD	Connection to external 3.3V or 5V supplies voltage. The external supply powers SPI interface and the I/O signal pins to the microcontroller.
18	SP2	Positive connection to the boost shunt resistor 2, in series to the boost switching mosfet.
19	SN2	Negative connection (Ground) to the boost shunt resistor 2, in series to the boost switching mosfet.
20	TMUX	Internal function. Left open.
21	G02	Output of the gate driver 2 for the external the boost switching mosfet.
22	PGND	Power Ground connection.
23	G01	Output of the gate driver 1 for the external the boost switching mosfet.
26	V10V	Output of the 10V regulated internal supply (gate driver supply). Connect low ESR capacitor (1uF typical) close to this pin.
27	SN1	Negative connection (Ground) to the boost shunt resistor 1, in series to the boost switching mosfet.
28	SP1	Positive connection to the boost shunt resistor 1, in series to the boost switching mosfet.

Table 1. Pin functionality (continued)

Pin Number	Name	Function
30	BST_OUT	Boost output voltage pin. Optional supply pin of the IC.
1, 8, 9, 16, 17, 24, 25, 29, 31, 32	NC	Not Connected

Note: *At application level, V3V3A and V3V3D pins are connected together, then connected to a capacitor.*

2 Supply concept

The L99LD02 supply range is from 3V up to 28V, which guarantees compatibility with 12V systems. The device is normally supplied from VS pin; when battery level is not enough to guarantee well driven external MOSFETs, the device supply is switched to BST_OUT pin. The device supply is from:

- VS, in the range of Vs_sw up to Vsmax;
- BST_OUT when Vs < Vs_sw and Bst_out > Bst_Out_min (15V typical).

Vs_sw is determined from minimum gate driver voltage (7V typical) and voltage drop between Vs and gate driver output. Vsmax is 40V to be compatible with 12V system load dump.

This supply concept guarantees boost functionality during cranking, according to ISO16750-2 and LV124. The L99LD02 output voltage regulation in cranking is ensured according to the following formula:

Bst_Out = Vin * η * 1 / (Toff_min * Fsw)

where Vin is the minimum boost input voltage during cold cranking condition (3.2V), η is L99LD02 typical efficiency, Toff_min is the minimum off time value specified for the full spec range, Fsw is the operative switching frequency of the device.

In cold cranking, boost operation and protection functions are kept. The output power is limited only by adjusted input current limit and converter Toff_min, whilst, full functionality - without any limitation - is ensured from VS ≥ Vs_min (minimum operating supply voltage, 5.5V typical).
VS under-voltage shutdown function is implemented to avoid an operation of the external mosfet of the boost controller in linear mode, due to a too low gate driver supply. In case the VS falls below VS under-voltage threshold (Vs_uv), while device is not supplied from BST_OUT (BST_OUT < BST_OUT_MIN), the device disables the boost operation. Configuration, operating mode and diagnostic data are kept down to POR.

3   Boost controller

3.1   General description

The L99LD02 device is able to work both with a microcontroller and without it (stand-alone operation).

The device integrates two boost controllers, based on a fixed frequency, peak current mode architecture. It can drive the gates of up to two external n-channel MOSFETs in order to step up the VS input voltage to a higher stabilized output voltage.

The L99LD02 integrates a 10V LDO to supply the gate drivers for standard level MOSFETs and features a device supply option from boost output.

This features is implemented in order to avoid any operation of the external MOSFETs of the boost controller in linear mode, due to a too low gate driver supply. On top of that, with supply option from boost output, the device fulfills cold cranking requirements.

3.2   Switching frequency

The L99LD02 operates at a fixed frequency which can range from 100 kHz to 470 kHz. The switching frequency is configurable via SPI (see CR#3 Bit[7:5], BST_FREQ in *Table 24: CR#3: Control Register 3*) or through dedicated OTPs (for stand-alone configuration).

Boost operative switching frequency value can be set according to *Table 2*:

Table 2. Switching frequency configuration

BITs [3÷0]	BST_FREQ [kHz]
000	101.01
001	151.52
010	196.08
011	256.41
100	303.03
101	333.33
110	416.67
111	476.19

The L99LD02 features an internal dither oscillator. Frequency modulation as well as deviation percentage can be programmed through SPI (see CR#3 Bit[11:10] BST_FDEV, Bit[9:8] BST_FMOD in *Table 24: CR#3: Control Register 3*).

3.3   Output voltage

The boost output voltage (BST_OUT) can vary in the range [14.7÷80] V with a granularity of 7 bits.

The voltage range and the granularity are defined to give flexibility because of internal output divider: the control loop regulates the output voltage on BST_OUT pin looking to the internal feedback voltage.

Device output voltage is configurable via SPI (see CR#2 Bit[11:5], BST_OUT in *Table 23: CR#2: Control Register 2*) or through dedicated OTPs (for stand-alone configuration).

3.4 Overvoltage protection

The peak current mode requires a minimum on-time, because of the noise generated right after the turn-on of the switching MOSFET. At light load (very low output current), this minimum on-time, in combination with the selected switching frequency is no longer able to regulate the output voltage to the requested voltage. The device enters in overvoltage protection (OVP), in order to prevent an excessive rise of the boost output voltage above the target voltage.

This mode is activated when the voltage on BST_OUT pin is higher than the selected of a specified threshold value ($V_{BST\_OUT\_OV\_ON}$).

The switching activity is resumed as soon as the voltage on BST_OUT pin decreases to the selected one. In case of BST_OUT voltage increases above VBST_OUT_OV_ON, an output digital flag, called BST_OVP, is set. As soon as the output voltage decreases down to programmed target value (BST_OUT [xxxxxx]), the bit is reset after $t_{BST\_OVP\_RST}$ delay time (10ms typical). This delay time is implemented in order to eliminate the diagnostic ambiguity (toggling of the OVP flag) during permanent no load or light load operation.

BST_OVP bit is not set in case of boost disabled.

3.5 Output failure protection

The L99LD02 is protected in case of boost controller output voltage pin failure. More in detail, a specific bit, called BST_OUT_FAIL (see SR#1 Bit[6], BST_OUT_FAIL in *Table 26: SR#1: Status Register 1*), is set in case of output voltage pin (BST_OUT) pin is left floating or shorted to ground.

This bit is set:

- If device is OFF, boost controllers do not start;
- If device is ON in
- single/dual phase configuration, boost controllers are immediately switched OFF;
- If device is ON in three/four phases configuration and it is in Active mode: both Master/Salve devices are switched off when the failure is recognized on Master side; only Slave device is switched off when the failure is recognized on Slave side while the Master is managed by the microcontroller;
- If device is ON in three/four phases configuration and it is in Limp Home: both Master/Salve devices are switched off when the failure is recognized on Master side; only Slave device is switched off when the failure is recognized on Slave side, while the Master is forced to work at minimum duty cycle.

The reset of BST_OUT failure bit is demanded to the microcontroller (in Active mode) or to an auto-restart function (in Limp Home) that cyclically clears this bit with a period equal to $t_{AUTORESTART}$.

This bit is not set if BST_DIS bit is set.

3.6 Soft start

The L99LD02 features an internal soft start function, which gradually increases the boost current in 9 steps, in order to avoid a voltage overshoot of the boost output. The threshold of the current limitation reaches its nominal value after a specified soft start time (t_{SS}).

A soft-start phase is initiated at the activation of the boost controller:

- after leaving standby mode;
- after deactivation of the boost controller due to a VS under voltage;
- after a previous deactivation of the boost by SPI (see CR#3 Bit[2:1], BST_DIS in *Table 24: CR#3: Control Register 3*);
- after deactivation of the boost controllers due to a BST_OUT_FAIL;
- after deactivation of the boost controllers due to OVT.

3.7 Stability – Error Amplifier characteristics

Slope compensation is needed to ensure loop stability with all possible values of duty cycle: $D = T_{ON} / T$ ($0 < D < 1$) especially when duty cycle is greater than 0.5. The slope of the additional ramp is proportional to converter inductor current slope during the turn off phase. The L99LD02 generates an internal peak current value, I_{SLOPE}, which is added to the positive sensing signal at the output of the OTA (see the following figure).

Figure 4. Resistor ladder for slope compensation and input current limitation
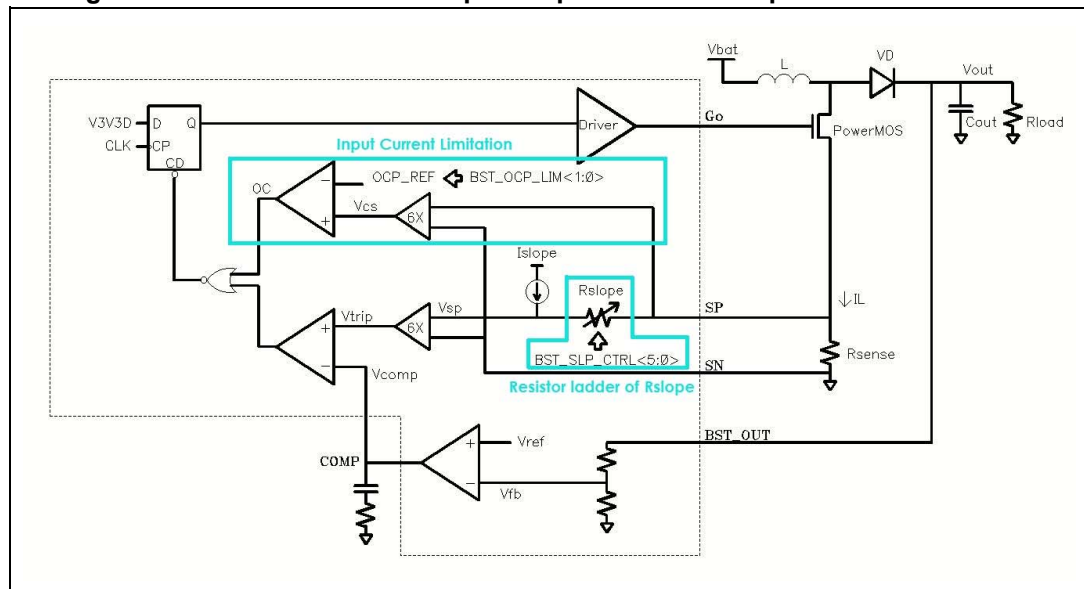
To avoid the use of external slope compensation resistor, thus limiting the coupling noise on the sense positive path, the compensation ramp slope of each boost controller can be configured by 6 bits (see Bit [23÷18], BST_SLP_CTRL, in *Table 23: CR#2: Control Register 2*) in the range [from 0.45 to 13.05] kΩ with a granularity step of 0.2 kΩ.

To keep the same compensation loop in multi-phase operation (same gain / phase-margin / band-width), without any hardware change, the OTA gain value can be configurable in 4 steps according to *Table 3*.

Table 3. OTA gain configuration

BITs [1÷0]	BST_GM_OTA [µS]
00	200
01	400
10	600
11	800

Both slope compensation and OTA gain are configurable via SPI (see CR#2 Bit[15:14], BST_GM_OTA in *Table 23: CR#2: Control Register 2*) or through dedicated OTPs (for stand-alone operation). Moreover, the OTA can be disabled through dedicated bit / OTP (see CR#2 Bit[17], BST_DIS_OTA in *Table 23: CR#2: Control Register 2*).

Homogeneous power losses distribution in multi-phases is guaranteed thanks to design specific measures ensuring the lowest spread for key-parameters like linear amplifier gain and offset (G_{LA} and G_{LA_OFFSET}), slope compensation current (I_{SLOPE}) and voltage on COMP pin (V_{COMP}).

3.8 Operation in multiphase interleaved mode

The multiphase operation mode is needed in case of high output power requirement. The maximum output power per phase in front of LED applications is typically 35W considering a cost effective design. This limitation is mainly given by power losses and thermal constraints. By sharing the current between several phases, the conduction losses (which are proportional to the square of the conducted current) are reduced and the efficiency of the boost stage increases, in comparison to a single-phase. Another advantage of multiphase topology is higher effective switching frequency and lower ripple currents which significantly reduces the filtering effort on input and output side. In ideal case of 50% duty cycle in 2-phase mode (respectively 33.3% in 3-phase or 25% in 4-phase), the input ripple current is reduced down to zero.

The L99LD02 can be configured in 1, 2, 3 or 4 phase mode. The 1 or 2 phase mode can be realized with one device as shown in *Figure 5: 1 or 2 phase configuration with single L99LD02 device*.

Figure 5. 1 or 2 phase configuration with single L99LD02 device
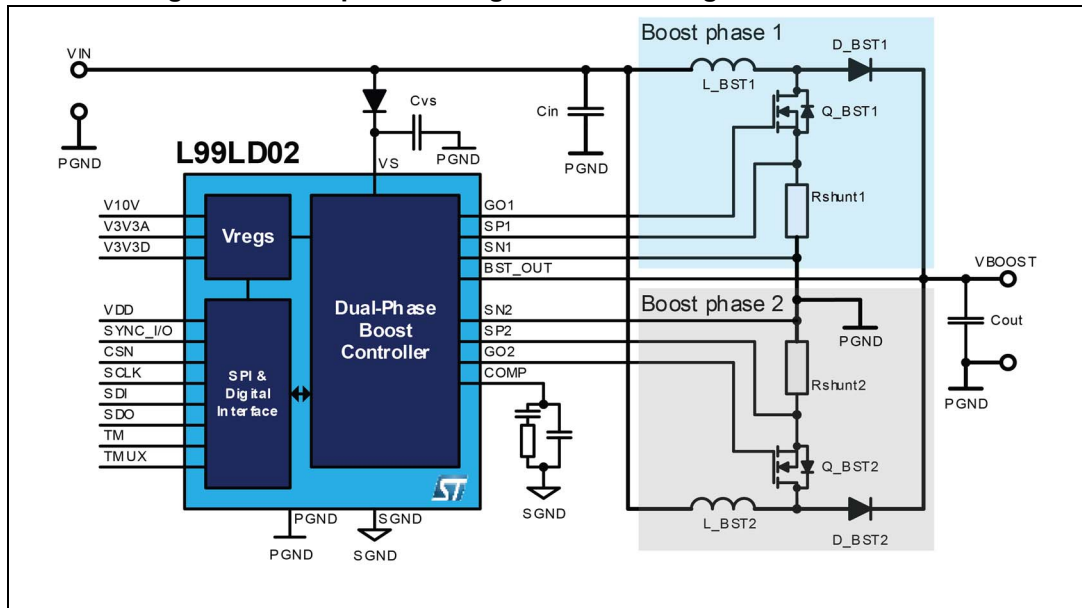
In case of 3 or 4 phase mode, two devices are needed with SYNC_I/O, BST_COMP and BST_OUT pins connected together as shown in *Figure 8: 3 or 4 phase configuration with two L99LD02 devices*. One of the devices must be configured as a master and other device as a slave by a dedicated configuration bit.

Figure 6. Clock distribution and phase shift
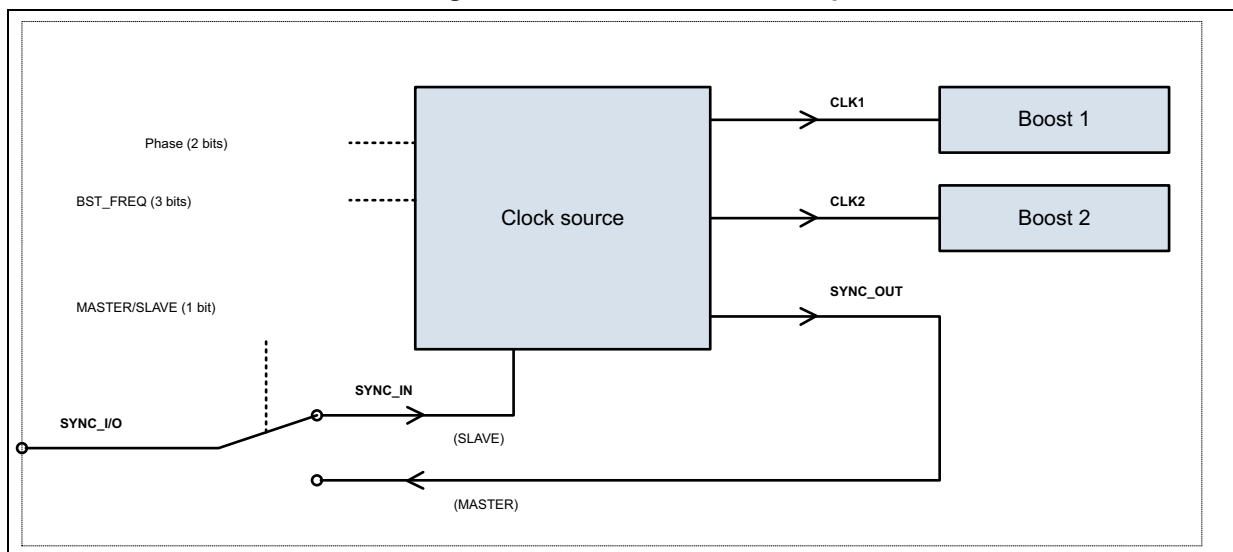
In master mode, an internal oscillator is used. The switching frequency is configurable via SPI by 3 bits. The clock signal is distributed in both boost channels and SYNC_I/O pin (output) with configurable phase shift according to the desired number of phases – see *Table 4: Clock distribution – MASTER (internal clock source)*.

In slave mode, the device uses an external clock signal from SYNC_I/O pin (input mode). This signal is used for boost channel 1 (no phase shift) and channel 2 (180˚ phase shift) – see *Table 5*.

Table 4. Clock distribution – MASTER (internal clock source)

MASTER	Phase config (2 bits)		
Signal	2 phase	3 phase	4 phase
CLK1	0°	0°	0°
CLK2	180°	120°	180°
SYNC_OUT	0°	240°	90°

Table 5. Clock distribution – SLAVE (external clock source)

SLAVE	Phase config (2 bits)		
Signal	2 phase	3 phase	4 phase
SYNC_IN	0°	0°	0°
CLK1	0°	0°	0°
CLK2	180°	180° (unused)	180°

Figure 7. Clock distribution scheme for 3 and 4 phase boost
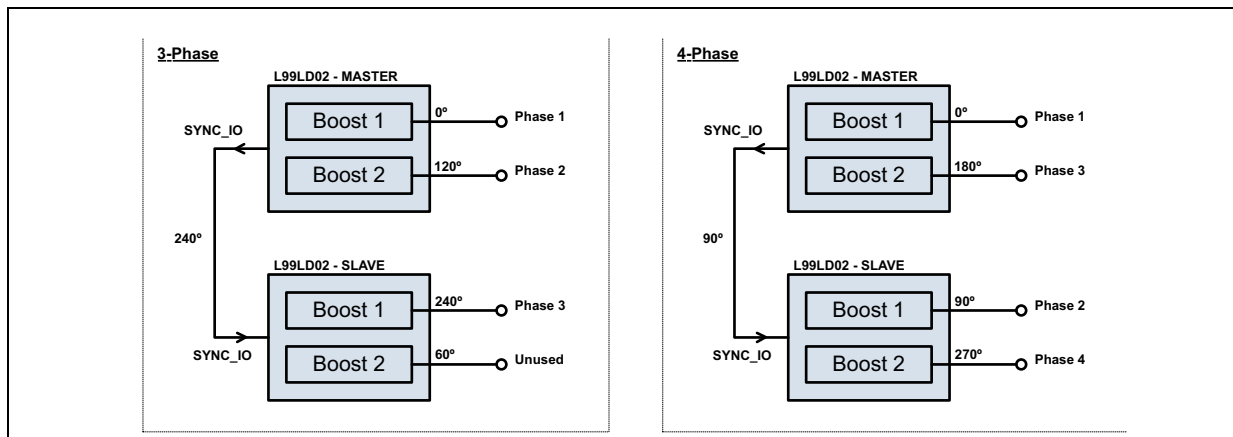
Figure 8. 3 or 4 phase configuration with two L99LD02 devices
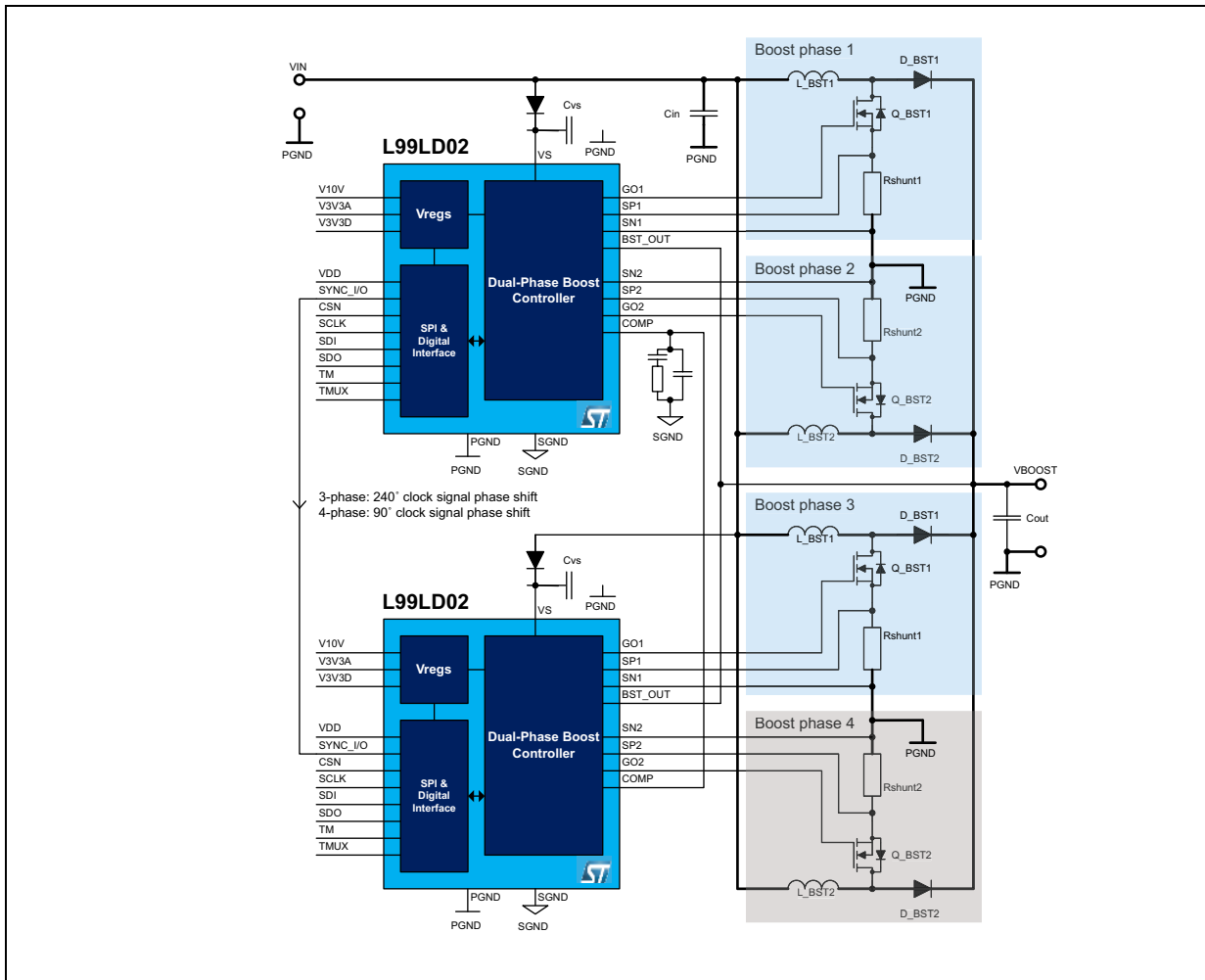
For a proper current balancing between boost phases, identical external components (especially shunt resistors and inductors) must be used. In case of interconnection of two devices (3 or 4 phase systems), the following configuration must be applied:

Table 6. Clock distribution - MASTER (internal clock source)

SPI configuration	Master device	Slave device
MS (1 bit)	0	1
BST_N_PHASE (2 bits)	3 or 4 phase	Any value (this setting has no effect in slave mode)
BST_GM_OTA (2 bits)	According to application conditions (see *Section 3.7: Stability – Error Amplifier characteristics*)	Disabled Enable is also allowed – then the resulting Gm value is a sum of Gm values of both devices. However, in case the slave device is disabled (e.g. due to lower output power demand) the Gm of only master device becomes too low with given compensation network. This would results in much lower regulation loop bandwidth than it could be. Then, another SPI command for increasing master's Gm value might be needed.
BST_SLP_CTRL (6 bits)	According to application conditions (see *Section 3.7: Stability – Error Amplifier characteristics*)	Identical as master (is a must for equal current balancing)
BST_OCP_LIM (2 bits)	According to application conditions (see CR#2 Bit[13:12], BST_OCP_LIM in *Table 23: CR#2: Control Register 2*)	Identical as master (for consistent overcurrent protection level)
BST_OUT (7 bits)	According to requested output voltage	Identical as master (for consistent overvoltage diagnostic feedback, power good flag and correct output voltage in case of slave's OTA kept enabled)
BST_DIS (2 bit)	Phase 1, Phase 2 enabled (see CR#3 Bit[2:1], BST_DIS in *Table 24: CR#3: Control Register 3*)	3-phase configuration: Phase 1 enabled, Phase 2 disabled 4-phase configuration: Phase 1, Phase 2 enabled

4   Functional description

4.1   Operating modes

Figure 9. Device state diagram
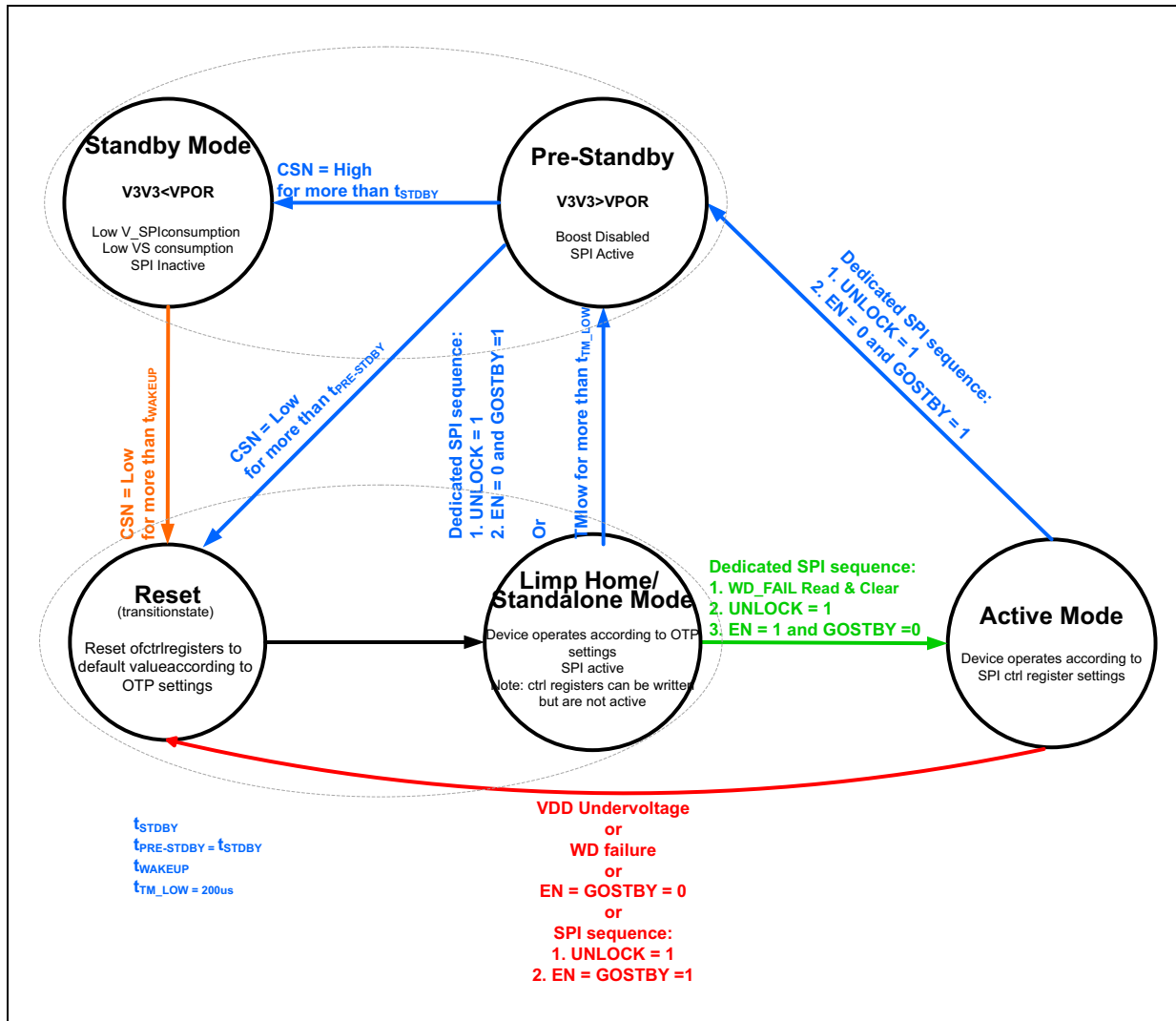
Table 7. Operating modes

Operating mode	Entering conditions	Leaving condition	Characteristics
Standby mode	– By default, once the device is powered (VS present); – CSN High for more than t_{STDBY} when the device is in Pre-standby mode	CSN pin Low for t > t_{WAKEUP}	– V3V3 < VPOR; – VS and VDD low consumption; – SPI inactive
Pre-standby mode	– Under following condition, when device is in Active mode: Two consecutive SPI frames setting: UNLOCK = 1 (EN,GOSTBY) = (0,1) – Under following condition, when device is in Limp Home: Two consecutive SPI frames setting: UNLOCK = 1 (EN,GOSTBY) = (0,1) Or – TM = Low for t_{TM_LOW}	Automatic transition to: – Standby mode if CSN pin High for t > t_{STDBY} – Reset mode if CSN pin Low for t > t_{PRE_STDBY}	– V3V3>VPOR – Boost disabled – SPI active
Reset mode	– By default, when device leaves Standby mode – Under following condition, when device is in Active mode: VDD Under voltage WD failure; One SPI frame setting (EN,GOSTBY) = (0,0) Two consecutive SPI frames setting: UNLOCK = 1 (EN,GOSTBY) = (1,1) – Under following condition, when device is in Pre-standby mode: CSN pin low for t >t_{PRE_STDBY}	Automatic transition to Limp Home after 400 ns	– All registers reset to default values according to OTP settings – V3V3>VPOR – SPI inactive

Table 7. Operating modes (continued)

Operating mode	Entering conditions	Leaving condition	Characteristics
Limp Home	– 400 ns after Reset mode	– SPI sequence to enter Active mode: – UNLOCK = 1 – (EN,GOSTBY) = (1,0) – SPI sequence to enter Pre-Standby mode: UNLOCK = 1 (EN,GOSTBY) = (1,0) OR – TM = Low for t_{TM_LOW}	– Boost enabled – Device operation according to OTP settings – SPI active
Active mode	SPI sequence: UNLOCK = 1 (EN,GOSTBY) = (1,0)	– VDD under voltage – WD failure – SPI sequence (EN,GOSTBY) = (0,0) – SPI sequence UNLOCK = 1 (EN,GOSTBY) = (1,1) – SPI sequence to enter Pre-Standby mode: UNLOCK = 1 (EN,GOSTBY) = (0,1)	– Boost enabled – SPI is active – Device operating according to SPI control register settings

4.1.1 Standby mode

The pre-requisites for this mode are:
- Device in power down
- Device in Pre-Standby mode

The device enters Standby mode under the following conditions:
- By default, once the device is powered (VS present);
- CSN High for more than t_{STDBY}

The Standby mode characteristics are:
- V3V3 < VPOR
- VDD and VS low consumption
- SPI inactive

The device leaves this mode if:
- CSN Low for a time $t > t_{WAKEUP}$

4.1.2 Pre-standby mode

The device enters Pre-standby mode under the following conditions:

- upon the two following consecutive SPI frames setting:

UNLOCK = 1

(see bit <1> on *Table 22: CR#1: Control Register 1*)

(EN,GOSTBY) = (0,1)

(see bit <3> and bit <2> on *Table 23: CR#2: Control Register 2*)

Or upon the condition of TM pin is low for more than a fixed time window (t_{TM_LOW}).

The Pre-standby mode characteristics are:

- V3V3 > VPOR
- Boost disabled
- SPI active

The device leaves automatically Pre-standby mode entering:

- Standby, if CSN high for a time t > t_{STDBY};
- Reset, if CSN Low for a time t > t_{PRE_STDBY}

4.1.3 Reset mode

The device enters Reset mode under the following conditions:

- By default, once the device leaves Standby mode;
- If in Active mode, when one of the following events occur:
  - VDD under voltage;
  - Watchdog failure
  - One SPI frame setting (EN,GOSTBY) = (0,0)
  - Two consecutive SPI frames setting

UNLOCK = 1

(EN,GOSTBY) = (1,1)

The Reset mode characteristics are:

- V3V3 > VPOR
- Control and status registers set to their default values (according to OTP settings)
- SPI inactive

The device leaves automatically Reset mode entering Limp Home after 400 ns (typical).

4.1.4 Limp Home / Stand-alone mode

The device enters Limp Home automatically 400 ns after Reset mode.

Limp Home characteristics are:

- Boost active
- Operation according to OTP settings
- SPI active:
    - All SPI write operations must be allowed without any effects on the device behavior.

When the device leaves this mode, it can enter Standby or Active mode.

If the Microcontroller sends the following SPI frames sequence:

- The first SPI frame sets UNLOCK bit = 1
  (see bit <1> on *Table 22: CR#1: Control Register 1*)
- The second consecutive SPI frame sets GO_STBY bit = 1 and EN bit = 0,
  (see bit <3> and bit <2> on *Table 23: CR#2: Control Register 2*)

Or, if in stand-alone operation, upon the condition of TM pin is low for more than a fixed time window (t_{TM_LOW}), the device enters Pre-Standby mode.

Then, the device automatically enters:

- Standby, if CSN high for a time $t > t_{STDBY;}$
- Reset, if CSN Low for a time $t > t_{PRE\_STDBY;}$

If the Microcontroller sends to the device the sequence of the following SPI frames:

- The first SPI frame reads and clears the WD-Fail bit (see bit <14> on *Table 26: SR#1: Status Register 1*)
- The second SPI frame sets UNLOCK bit = 1 (see bit <1> on *Table 22: CR#1: Control Register 1*)
- The third consecutive SPI frame sets GOSTBY bit = 0 and EN bit = 1 (see bit <3> and bit <2> on *Table 23: CR#2: Control Register 2)*

The device enters Active mode.

In Limp Home, after setting bit 27 on GSB (FE1, functional error bit), an auto-restart procedure is implemented: every $t_{AUTORESTART}$, functional error bit eventually set is automatically cleared.

4.1.5 Active mode

The device enters the Active mode if the Microcontroller sends the following SPI frames sequence:

- The first SPI frame reads and clears the WD-Fail bit (see bit <14> on *Table 26: SR#1: Status Register 1*)
- The second SPI frame sets UNLOCK bit = 1 (see bit <1> on *Table 22: CR#1: Control Register 1*)
- The third consecutive SPI frame sets GOSTBY bit = 0 and EN bit = 1 (see bit <3> and bit <2> on *Table 23: CR#2: Control Register 2)*

4.2 Protections and diagnostic

4.2.1 Temperature warning

The device integrates a temperature warning TW with two thresholds TW1 and TW2.

If the T_j (junction temperature) of the boost controllers rises above TW1 or TW2, the status bit TWx (x=1 or x=2 stands for the TW1 or TW2) is set on the status registers (see bit <18> and bit <19> on *Table 26: SR#1: Status Register 1)*. Thermal warning is also reported in the Global Status Byte register, and in particular, bit 25 (GW) is set.

If the T_j drops below the temperature warning reset threshold 1 (TW1-TW1_HYS), respectively TW2 – TW2_HYS, the corresponding status bit is automatically reset. As long as the Tj does not exceed the over temperature shutdown, the device does not latch off the boost controllers, even if a temperature warning is detected.

Note that, powering the device via the BST_OUT will produce an extra power dissipation which must be taken into account during the thermal design.

In case the device is supplied from BST_OUT pin, a flag called BST_OUT_SUPPLY is provided to inform the application. If the junction temperature rises above TW (thermal warning) threshold, the application can decide to decrease power losses on gate driver V10V regulator (switching off 1 boost phase or decreasing boost switching frequency), minimizing the risk of undesired thermal shutdown.

4.2.2 Overcurrent

On top of the normal current regulation loop comparator, the L99LD02 integrates an additional comparator to clamp the maximum physical current that can flow in the booster input circuit while the MOSFET is driven. The aim is to protect all the external components involved (inductor from saturation, diode and MOSFET from overcurrent…).

The protection is active PWM cycle−by−cycle and switches off the MOSFET gate as the voltage drop across the shunt resistor reaches its maximum threshold (BST_OCP_LIM).

This threshold can be set by SPI / OTPs according to *Table 8*.

Table 8. Boost threshold for input current limitation

BITs [1÷0]	BST_OCP_LIM [mV]
00	50
01	85
10	115
11	150

4.2.3 Over-temperature shutdown

If the junction temperature rises above the shutdown temperature T_{TSD}, an over-temperature event (OVT) is detected. The boost controllers are switched off and the corresponding bit OVT is set in the status register (see bit <20> on *Table 26: SR#1: Status Register 1*). Over-temperature event is also reported in the Global Status Byte register and

in particular bit 27 FE1 is set. In normal mode the boost controllers are latched off, until the following conditions are fulfilled:

- T_{JX} drops below the thermal shutdown reset threshold T_{TSD}-T_{TSD_HYS}.
- Subsequently the microcontroller sends a read and clear command, in order to reset OVT bit.

In fail safe mode (Limp Home), the device applies an auto restart with a period equal to $t_{AUTORESTART}$, provided that the T_{JX} falls below TSD reset threshold (T_{TSD}-T_{TSD_HYS}).

4.2.4 VS under voltage lockout

Provided device is not supplied from BST_OUT if the VS supply falls below V_{S_UV} (VS under voltage threshold), the boost controllers will be deactivated, regardless of the SPI control register. This feature is implemented, in order to avoid an operation of the external mosfet of the boost controller in linear mode, due to a too low gate driver supply.

In this case, BST_OUT_SUPPLY bit is not set whilst VS_UV_FAIL bit is set (see bit <13> on *Table 26: SR#1: Status Register 1*)

5 Serial peripheral interface (ST SPI standard)

The ST-SPI is a standard used in ST Automotive ASSP devices. Therefore the here standardized SPI is described from SPI-Slave-Device point of view: a common structure of the communication frames and specific addresses for product and status information are defined.

The ST-SPI will allow usage of generic software to operate the devices while maintaining the required flexibility to adapt it to the individual functionality of a particular product. In addition to that, failsafe mechanisms are implemented to protect the communication from external influences and wrong or unwanted usage.

5.1 Physical layer - Functional description

Figure 10. Physical layer
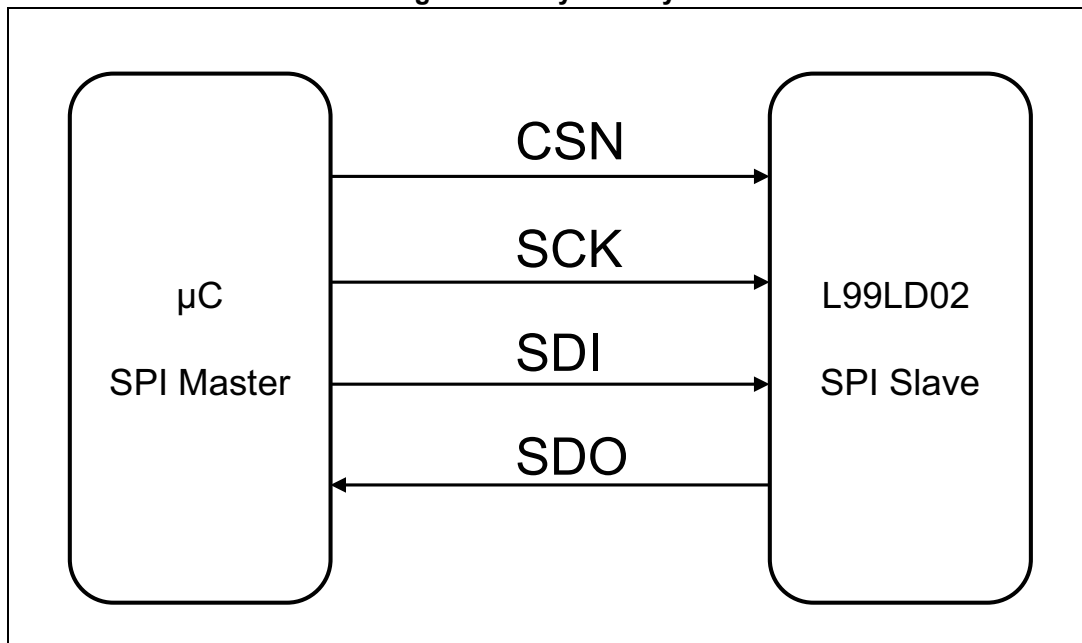
This device features a 32-bit ST SPI in slave configuration for bi-directional communication with an external microcontroller. This device supports burst read access and shall be operated in the following mode: CPOL = 0 and CPHA = 0.

For this mode, input data is sampled on the rising edge of the clock signal SCK and output data is changed on the falling edge of SCK.

During standby mode, the SPI interface is deactivated.

Signal Description:

- Chip Select Not (CSN)
  The input pin is used to select the serial interface of this device. When CSN is high, the output pin (SDO) will be in high-impedance state. In case CSN is stuck at GND, a timeout is implemented which sets the SDO line back to high-impedance to release the

SPI network. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame.

- Serial Data In (SDI)
  The input pin is used to transfer data serially into the device. The data applied to SDI will be sampled on the rising edge of the SCK signal and shifted into an internal 32-bit shift register. On the rising edge of the CSN signal, the contents of the shift register will be transferred to the Data Input Register.
  Only communication frames with 0 (read GSBN bit), 24 (standard communication frame), or 24 + (n * 16) (burst read/write) clock pulses are accepted. All others will be ignored and a communication error will be reported with the next SPI command.

- Serial Data Out (SDO)
  The data output driver is activated by a logic low level at the CSN input. After a falling edge of the CSN pin, the SDO pin will leave the tri-state condition and present the GSBN bit. At all following falling edges of the SCK signal, the following bits of the SPI frame are shifted out to the SDO pin.

- Serial Clock (SCK)
  The SCK input is used to synchronize the input and output serial bit streams. The data input (SDI) is sampled on the rising edge of the SCK and the data output (SDO) will change with the falling edge of the SCK signal. The SPI can be driven with a SCK frequency up to 4 MHz.

5.2 Physical layer – protocol

5.2.1 SDI frame

The data-in frame consists of 32 bits (OpCode + Address + Data).

The first two transmitted bits contain the Operation Code which represents the instruction to be performed. The following 6 bits represent the address on which the operation will be performed.

The subsequent 24 bits contain the payload data.

Table 9. Command byte (8 bit)

	Operating code		Address					
Bit	31	30	29	28	27	26	25	24
Name	OC1	OC0	A5	A4	A3	A2	A1	A0

Table 10. Data byte 2

	Data byte 2							
Bit	23	22	21	20	19	18	17	16
Name	D23	D22	D21	D20	D19	D18	D17	D16

Table 11. Data byte 1

	Data byte 1							
Bit	15	14	13	12	11	10	9	8
Name	D15	D14	D13	D12	D11	D10	D9	D8

Table 12. Data byte 0

	Data byte 0							
Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Table 13. Operation code definition

OC1	OC0	Meaning
0	0	<Write Mode>
0	1	<Read Mode>
1	0	<Read and Clear Mode>
1	1	<Read Device Information>

The operation code is used to distinguish between different access modes to the registers of the slave device.

The Write and Read Mode operations allow access to the RAM of the device.

The Read and Clear operation is used to read a status register and subsequently clears its content.

The Read Device Information allows access to the ROM area which contains device specific read-only data (like Device ID and SPI settings device related information) predefined by the ST SPI standard.

5.2.2 SDO Frame

The Data-Out Frame consists of 32 bits (GSB + Data).

The first eight transmitted bits contain device-related status information and are latched into the shift register at the time of the Communication Start. These 8 bits are transmitted at every SPI transaction.

The subsequent bytes contain the payload data and are latched into the shift register with the eighth positive SCK edge. This could lead to an inconsistency of data between the GSB and Payload due to different shift register load times. Anyhow, no unwanted Status Register clear should appear, as status information should just be cleared with a dedicated bit clear after read.

Table 14. Global Status Byte

	Global Status Byte							
Bit	31	30	29	28	27	26	25	24
Name	GSBN	RSTB	SPIE	FE2	FE1	DE	GW	FS

Table 15. Data byte2

	Data byte2							
Bit	13	22	21	20	19	18	17	16
Name	D23	D22	D21	D20	D19	D18	D17	D16

Table 16. Data byte1

	Data byte1							
Bit	15	14	13	12	11	10	9	8
Name	D15	D14	D13	D12	D11	D10	D9	D8

Table 17. Data byte0

	Data byte0							
Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

The Global Status Byte is described here below.

The Payload (DATA Byte 0,1 & 2) is the data transferred from the slave device with every SPI communication to the microcontroller. The Payload always follows the OpCode and the Address bit of the actual shifted in data (In-Frame-Response).

Table 18. Global Status Byte

Bit	Name	Description
31	GSBN	Global Status Bit Not This bit is a NOR combination of the remaining bits of this register: RSTB nor SPIE nor FE2 nor FE1 nor DE nor GW nor FS
30	RSTB	Reset Bit The RSTB indicates a device reset. In case this bit is set, all internal *Control Registers* are set to default and kept in that state until the bit is cleared.
29	SPIE	SPI Error The SPIE is a logical OR combination of errors related to a wrong SPI communication (SDI stuck, wrong number of clock, parity check error)
28	FE2	Functional Error 2 VS_UV_FAIL
27	FE1	Functional Error 1 OVT or BST_OUT_FAIL

Table 18. Global Status Byte (continued)

Bit	Name	Description
26	DE	Device error N_PWR_GOOD or BST_OVP
25	GW	Global warning: TW1 or TW2
24	FS	Fail safe: If this bit is set, device is in Limp Home

5.3   Address and data definition

5.3.1   Device Information Register

The Device Information Register can be read by using OpCode '11'. After shifting out the GSB, the 8-bit wide payload will be transmitted. After shifting out the GSB followed by the 8-bit wide payload, a series of '0' is shifted out at the SDO pin.

Table 19. Device information read access operating code

Operating code	
OC1	**OC0**
1	1

Table 20. RAM Memory Map

Address	Name	Access	Content
01h	Control Register 1	R/W	CR#1: 1st Control Register
02h	Control Register 2	R/W	CR#2: 2nd Control Register
03h	Control Register 3	R/W	CR#3: 3rd Control Register
04h	Control Register 4	R/W	CR#4: 4th Control Register
06h	Status Register 1	R/C	SR#1: 1st Status Register
3Eh	Ctm Trimming Register1	R/W (W only when EOT bit = 0)	CT: Customer Trimming Register1
3Fh	Ctm Trimming Register2	R/W (W only when EOT bit = 0)	CT: Customer Trimming Register2
3Fh	Advanced Operation Code	Clear	A R&C operation to this address causes all status registers to be cleared

Table 21. ROM Memory Map

Address	Name	Access	Content (hex)	Content (bin)	Comments
00h	Company Code	R	00h	00000000b	STMicroelectronics
01h	Device family	R	02h	00000010b	LED product family
02h	Device N. 1	R	55h	01010101b	'U' in ASCII
03h	Device N. 2	R	42h	01000010b	'B' in ASCII
04h	Device N. 3	R	42h	01000010b	'B' in ASCII
05h	Device N. 4	R	44h	01000100b	'D' in hex
0Ah	Silicon version	R	01h	00000001b	Second version
10h	SPI Mode	R	31h	00110001b	Bit7 = 0, burst read is disabled SPI data length = 32 bits Bit6, DL2 = 0 Bit5, DL1 = 1 Bit4, DL0 = 1 Bit3, SPI8 =0 : 8 bit frame option not available Bit2 =0 Parity check is used Bit1, S1=0 Bit0, S0=1
11h	WD Type 1	R	4Ah	01001010b	A WD is implemented Bit7, WD1 =0 Bit6, WD0 =1 WD period 50ms = 10*5ms -> WT[5:0] = 0xA Bit5, WT5 = 0 Bit4, WT4 = 0 Bit3, WT3 = 1 Bit2, WT2 = 0 Bit1, WT1 = 1 Bit0, WT0 = 0
13h	WD bit pos. 1	R	44h	01000100b	Bit7,WB1 = 0 Bit6,WB2 = 1 WBA[5-0], Bit[5-0] = address of the config. register, where the WD bit is located = 04d = 000100b

Table 21. ROM Memory Map (continued)

Address	Name	Access	Content (hex)	Content (bin)	Comments
14h	WD bit pos. 2	R	D7h	11010111b	Bit7,WB1 = 1 Bit6,WB0 = 1 Bit position of the WD bit within the corresponding configuration register = 23d = 010111b
20h	SPI CPHA Test	R	55h	01010101b	Predefined by ST SPI V4.1, it is used to verify that the SCK Phase of the SPI master is set correctly
3Eh	GSB Options	R	00h	00000000b	All bits of GSB are used
3Fh	Advanced Operation Code	R	00h	00000000b	Access to this address provokes a SW reset (all control registers are set to their default values; in addition, all status registers are cleared too). NOTE: Data field should not be "all ones", otherwise an "SDI stuck at" error occurs.

The Device Identification Registers represent a unique number identifying device part-number.

By reading out the <SPI Mode> register, general information of SPI usage of the Device Application Registers can be read.

The SPI Burst Read bit indicates if a burst read operation is implemented.

The L99LD02 does not feature SPI Burst Read.

The SPI Data Length value indicates the length of the SCK count monitor which is running for all accesses to the Device Application Register. In case of a communication frame with an SCK count not equal to the reported one, this will lead to a SPI Error and the data will be rejected.

The default frame size of the L99LD02 is 32 bits, so the SPI Data Length bits are read as '011'.

For the L99LD02, a Data Consistency Check by parity check is implemented, therefore these bits are read as '01'. An odd parity bit is used and it is calculated over the complete communication frame.

The GSB Options byte indicates that device-specific status information is used instead of the predefined one. In case a bit of the GSB is not used, it has to be fixed to '0' value and is indicated by a logical '1' in the GSB Options byte.

5.3.2 Device application registers

The Device Application Registers are all registers accessible using OpCode '00', '01' and '10'.

An access to an unused address will not lead to any error. Any data read from an unused address is not defined.

5.4 Protocol failure detection

To realize a protocol which fulfills certain failsafe requirements, a basic set of failure detection mechanisms is implemented.

5.4.1 Clock monitor

During communication (CSN low to high phase) a clock monitor counts the valid SCK clock edges. If the SCK edges do not correlate with the SPI Data Length, an SPIE is reported with the next command and the current communication is rejected.

By accessing the Device Information Registers (OpCode = '11'), the Clock Monitor is set to a minimum of 16 SCK edges plus a multiple of 8 (e.g. 16, 24, 32).

Providing no SCK edge during a CSN low to high phase is not recognized as an SPIE.

5.4.2 SCK polarity (CPOL) check

To detect wrong polarity access on SCK, the internal clock monitor is used. Providing first a negative edge on SCK during communication (CSN low to high phase) or a positive edge at last will lead to an SPI Error being reported in the next communication and the current data is rejected.

5.4.3 SCK phase (CPHA) check

To verify that the SCK phase of the SPI master is set correctly a special Device Information Register is implemented. By reading this register the data must be 55H. In case AAH is read, the CPHA setting of the SPI master is wrong and a proper communication cannot be guaranteed.

5.4.4 CSN timeout

By pulling CSN low, the SDO is set active and leaves the tri-state condition. To ensure communication between other SPI devices within the same bus even in case of CSN stuck at low, a CSN timeout is implemented. By pulling CSN low, an internal timer is started. After the timer end is reached, the current communication is rejected and the SDO is set to tri-state condition. This error is not reported in any specific status register.

5.4.5 Data stuck

- SDI stuck at GND
  As a command with all data bits set to '0' and OpCode '00' on address b'000000 cannot be distinguished from an SDI stuck-at-GND error, this command is not allowed. In case

a stuck-at-GND error is detected, the communication will be rejected and the SPIE will be set in the next communication cycle.

- SDI stuck at HIGH
As a command with all data bits set to '1' and OpCode '11' on address b'111111 cannot be distinguished from an SDI stuck-at-HIGH error, this command is not allowed. In case a stuck-at-HIGH error is detected, the communication will be rejected and the SPIE will be set in the next communication cycle.

- SDO stuck
SDO stuck-at-GND and stuck-at-HIGH errors have to be detected by the SPI master. As the definition of the GSB guarantees at least one bit toggle, a GSB with all bits set to '0' or with all bits set to '1' can be considered as an SDO stuck-at error.

5.5 Implementation remarks

5.5.1 Register change during communication

From an implementation point of view, it is guaranteed that no register change gets lost during communication. In case a register value was changed during a communication, it will be reported with the next communication frame.

5.5.2 GSB and payload inconsistency

Due to the internal implementation strategy, it may occur that data reported in the GSB does not match data reported in the payload in case the data was changed during GSB shift out. In this case, the payload data is the status quo, as it was loaded later into the SPI shift register.

5.6 Timings

All SPI related timings are defined in *Section 6.4.4: SPI bus (CSN, SCK, SDI, SDO)*.

5.7 Register description

5.7.1 Control Register

CR#1: Control Register 1

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTM_CLK_EN										Unused												UNLOCK	Parity bit
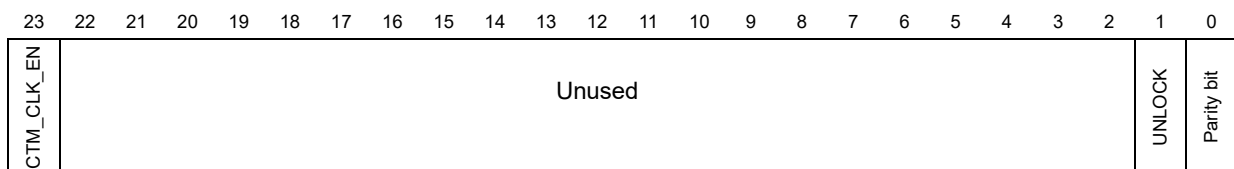
Address: 0x01h

Type: R/W

Table 22. CR#1: Control Register 1

Bit	Default	Name	Description
23	0	CTM_CLK_EN	CTM_CLK_EN can be set to 1 only if UNLOCK = 1; trying to set this bit to 1 when UNLOCK = 0 will have no effects and it will maintain its previous value. CTM_CLK_EN can be reset to 0 also when UNLOCK = 0. To set CTM_CLK_EN to 1, it is necessary to send two consecutive SPI frames, as follows: 1st SPI write operation to set UNLOCK bit to 1 (CR#1, bit1) 2nd SPI write operation to set CTM_CLK_EN bit to 1
22÷2		Unused	
1	0	UNLOCK	[0]: bits GOSTBY, EN and BST_DIS cannot be set to 1 but can be reset; [1]: bits GOSTBY, EN and BST_DIS can be set to 1, but only with the next valid SPI frame. When UNLOCK = 1, it will be automatically reset with the next valid SPI frame.
0		Parity Bit	Odd Parity Bit Check

CR#2: Control Register 2

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BST_SLP_CTRL						BST_DIS_OTA	Unused	BST_GM_OTA		BST_OCP_LIM		BST_OUT							Unused	GOSTBY	EN	MS	Parity bit
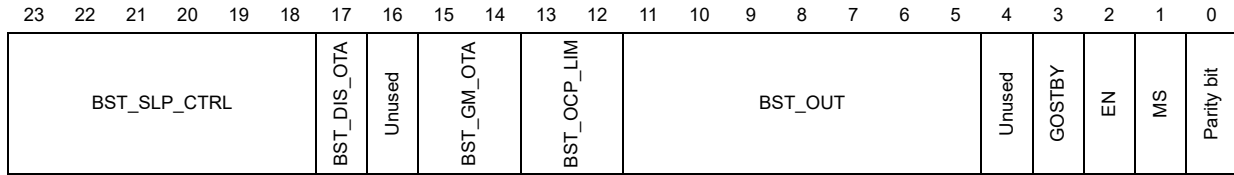
Address: 0x02h

Type: R/W

Table 23. CR#2: Control Register 2

Bit	Default	Name	Description
23÷18	Set by OTP DEF_BST_SLP_CTRL	BST_SLP_CTRL	Boost stability – Slope Compensation Control
17	Set by OTP DEF_BST_DIS_OTA	BST_DIS_OTA	BST_DIS_OTA can be set to 1 only if UNLOCK = 1; trying to set this bit to 1 when UNLOCK = 0 will have no effects and it will maintain its previous value. BST_DIS_OTA can be reset to 0 also when UNLOCK = 0. To disable Boost it is necessary to send two consecutive SPI frames as follows: 1st SPI Register write: set UNLOCK bit to 1 2nd SPI Register write: set BST_DIS_OTA to dedicate value;
16		Unused	
15÷14	Set by OTP DEF_BST_GM_OTA	BST_GM_OTA	Boost OTA gain shall be configurable in four steps: 11 --> typ. 800µS 10 --> typ. 600µS 01 --> typ. 400µS 00 --> typ. 200µS
13÷12	Set by OTP DEF_BST_OCP_LIM	BST_OCP_LIM	Boost OCP limiter The maximum drop voltage across boost shunt resistor shall be configurable in four steps 11 --> 150mV 10 --> 115mV 01 --> 85mV 00 --> 50mV
11 ÷ 5	Set by OTP DEF_BST_OUT	BST_OUT	Boost Output Voltage 0000000 --> 14.7V … 1111111 --> 80V Each step voltage is 0.51V
4		Unused	

Table 23. CR#2: Control Register 2 (continued)

Bit	Default	Name	Description
3	0	GOSTBY	Standby Mode Bit: [0]: Device waked up [1]: Standby (if EN = 0) GOSTBY can be set to 1 only if UNLOCK = 1; trying to set this bit to 1 when UNLOCK = 0 will have no effects and it will maintain its previous value. GOSTBY can be reset to 0 also when UNLOCK = 0. To set Standby mode it is necessary to send two consecutive SPI frames, as follows: 1st SPI write operation to set UNLOCK bit to 1 (CR#1, bit1) 2nd SPI write operation to set GOSTBY bit to 1 and EN bit to 0
2	0	EN	Active Mode Enable Bit: [0]: Device stays in Limp Mode (if GOSTBY = 0). This status is assumed immediately after a wake up (CSN low for a time > t_{WAKE_UP}) [1]: Device Enabled for Active Mode operation (if GOSTBY = 0). EN can be set to 1 only if UNLOCK = 1; trying to set this bit to 1 when UNLOCK = 0 will have no effects and it will maintain its previous value. EN can be reset to 0 also when UNLOCK = 0. To set Active Mode it is necessary to send two consecutive SPI frames as follows: 1st SPI write operation to set UNLOCK bit to 1 (CR#1, bit1) 2nd SPI write operation to set GOSTBY bit to 0 and EN bit to 1
1	Set by OTP DEF_MS	MS	Master/Slave bit [0]: Device is Master (pin SYNC_IO is an output, providing a 180° phase shifted replica of internal Boost clock) [1]: Device is Slave (pin SYNC_IO is an input and it is used as a clock for the Boost)
0		Parity Bit	ODD Parity Bit Check

CR#3: Control Register 3

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				Unused					BST_OUT_FAIL_FilterTime		DITH_EN	BST_FDEV		BST_FMOD		BST_FREQ			BST_N_PHASE		BST_DIS		Parity Bit

Address: 0x03h

Type: R/W

Table 24. CR#3: Control Register 3

Bit	Default	Name	Description
23÷16		Unused	
15÷13	DEF_BOF_FT(000)	BST_OUT_FAIL_FilterTime	Filtering time before setting the boost output failure bit. It takes effect after boost_power_good signal is "1" for the first time The boost out fail filtering time shall be configurable in 8 steps: 000 --> 500µs 001 --> 10µs 010 --> 50µs 011 --> 100µs 100 --> 300µs 101 --> 800µs 110 --> 1000µs 111 --> 2000µs
12	DEF_DITH_EN(0)	DITH_EN	Dithering enable: enable or disable random dither effect. If this bit is set Dithering is enabled; If the bit is reset, the dithering is disabled
11÷10	DEF_BST_FDEV(00)	BST_FDEV	Boost clock frequency deviation The clock frequency deviation shall be configurable in 4 steps: 00 --> 5% 01 --> 10% 10 --> 15% 11 --> 20%
9÷8	DEF_BST_FMOD(11)	BST_FMOD	Boost clock frequency modulation The clock frequency modulation shall be configurable in 4 steps: 00 --> 1.95 kHz 01 --> 3.90 kHz 10 --> 7.80 kHz 11 --> 15.6 kHz

Table 24. CR#3: Control Register 3 (continued)

Bit	Default	Name	Description
7÷5	DEF_BST_FREQ(011)	BST_FREQ	Boost clock frequency The switching frequency is configurable in 8 steps: 000 --> 101.01 kHz 001 --> 151.52 kHz 010 --> 196.08 kHz 011 --> 256.41 kHz 100 --> 303.03 kHz 101 --> 333.33 kHz 110 --> 416.67 kHz 111 --> 476.19 kHz

4÷3	Set by OTP
	DEF_BST_N_PHASE
		BST_N_PHASE	Boost phase selection during Master mode
			[00] : two phase mode (0/180);
			      Boost1=0;
			      Boost2=180;
			      sync_out=0;
			[01] : three phase mode(0,120,240)
			      Boost1=0;
			      Boost2=120;
			      sync_out=240;
			[10] : four phase mode(0,90,180,270)
			      Boost1=0;
			      Boost2=180;
			      sync_out=90;
			
			Boost phase selection during Slave mode
			[00] : two phase mode (0/180);
			      sync_in=0;
			      Boost1= sync_in=0;
			      Boost2=not sync_in=180;
			[01] : three phase mode(0,120,240)
			      sync_in=240;
			      Boost1= sync_in=240;
			      Boost2 is disabled;
			[10] : four phase mode(0,90,180,270)
			      sync_in=90;
			      Boost1= sync_in=90;
			      Boost2=not sync_in=270;

Table 24. CR#3: Control Register 3 (continued)

Bit	Default	Name	Description
2÷1	Set by OTP DEF_BST_DIS	BST_DIS	BST_DIS[0] -> disable Boost1 when set to 1; BST_DIS[1] -> disable Boost2 when set to 1; BST_DIS can be set to 1 only if UNLOCK = 1; trying to set this bit to 1 when UNLOCK = 0 will have no effects and it will maintain its previous value. BST_DIS can be reset to 0 also when UNLOCK = 0. To disable Boost it is necessary to send two consecutive SPI frames as follows: 1st SPI Register write: set UNLOCK bit to 1 2nd SPI Register write: set BST_DIS to 1
0		Parity Bit	ODD Parity Bit Check

CR#4: Control Register 4

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD_TRIG											Unused												Parity Bit

Address: 0x04h

Type: R/W

Table 25. CR#4: Control Register 4

Bit	Default	Name	Description
23	0	WD_TRIG	In order to keep device in Active Mode, this bit must be cyclically toggled within a period equal to t_{WD} to refresh the watchdog.
22÷1		Unused	
0		Parity Bit	ODD Parity Bit Check

5.7.2 Status Register description

SR#1: Status Register 1

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Unused			OVT	TW2	TW1	VSPI_FAIL	WD_STATUS		WD_FAIL	VS_UV_FAIL	Unused	BST_OUT_SUPPLY	Unused		N_PWR_GOOD	BST_OVP	BST_OUT_FAIL	Unused	BST2_OCP_LIM	BST1_OCP_LIM	N_COMP2_LEVEL_REACH	N_COMP1_LEVEL_REACH	Parity Bit
			R/C	R					R/C	R		R			R		R/C		R/C		R		

Address: 0x06h

Type: R, R/C

Table 26. SR#1: Status Register 1

Bit	Default	Name	Description	Access
23÷21		Unused		
20	0	OVT	Over temperature for Boost 1/2 (set when $T_J \geq T_{TSD}$ for more than t_{OVT}); if this bit is set: – (a) in Active Mode: Both Boost 1/2 are latched OFF; reset is performed by a R&C command, which will be successful only if $T_J < TW_2$. Then Boost is allowed to turn on again. – (b) in Limp Home, after setting an OVT, an auto restart procedure is implemented: every $t_{AUTORESTART}$ OVT bit is automatically cleared and, if $T_J < TW_2$, then Boost 1/2 is allowed to turn on again, otherwise OVT bit is set again.	R/C
19	0	TW2	Thermal warning 2 for Boost 1/2. This bit is set if $T_J \geq TW_2$. This is a read only and real time bit. When Boost 1 temperature decreases under a second threshold ($T_J < TW_1$), this bit is cleared.	R
18	0	TW1	Thermal warning 1 for Boost 1/2. This bit is set if $T_J \geq TW_1$. This is a read only and real time bit. When Boost 1 temperature decreases under a second threshold ($T_J < TW_1 - TW_{1\_HYS}$) this bit is cleared	R
17	0	VSPI_FAIL	External SPI supply [0]: external SPI supply present [1]: external SPI supply not present (V_{DD} voltage lower than $V_{DD, UV}$). When this bit is set, device goes to Limp Home	R

Table 26. SR#1: Status Register 1 (continued)

Bit	Default	Name	Description	Access
16÷15	00	WD_STATUS	Watchdog status bit WD timer status: 00 --> [0…25%] 01 --> [25% … 50%] 10 --> [50% … 75%] 11 --> [75% … 100%]	R
14	0	WD_FAIL	Watchdog failure bit: [0]: Watchdog OK; [1]: Watchdog failure in Active Mode When this bit is set, device goes to Limp Home	R/C
13	0	VS_UV_FAIL	VS undervoltage bit [0]: VS > $V_{S,UV}$ + V_{S,UV_HYS} OR BST_OUT_SUPPLY = 1 [1]: VS ≤ VS,UV AND BST_OUT_SUPPLY = 0	R
12		Unused		
11	0	BST_OUT_SUPPLY	The supply voltage of 10V regulator has changed from VS to BST_OUT [0]: VS > $V_{S,LV}$+ V_{S,LV_HYS} ($V_{S,LV}$=0) OR BST_OUT<15V [1]: VS ≤ $V_{S,LV}$ ($V_{S,LV}$=1) AND BST_OUT ≥ 15V	R
10÷9	00	Unused		
8	0	N_PWR_GOOD	This bit reflects the status of signal boost power good (negative) [0]: Output Boost voltage higher than or equal to 92.5% of its target value [1]: Output Boost voltage lower than 92.5% of its target value N_PWR_GOOD is not set when BST_DIS = 1	R
7	0	BST_OVP	Boost Over Voltage Protection. This bit is set when V_{FB} > $V_{FB\_OV\_ON}$ for more than t_{BST_OVP}, while is reset when V_{FB} < $V_{FB\_OV\_OFF}$ for more than $t_{BST\_OVP\_RST}$ IF BST_DIS = 1 then BST_OVP is not set. IF BST_OUT_FAIL = 1 then BST_OVP is not set.	R

Table 26. SR#1: Status Register 1 (continued)

Bit	Default	Name	Description	Access
6	0	BST_OUT_FAIL	BST_OUT pin failure. This bit is set when BST_OUT pin is floating or shorted to ground. When this bit is set: - if Boost is in off-state, then it will not be allowed to start up; - if Boost is in on-state, then it will immediately switched OFF; - in both cases, no clock is delivered through SYNC_IO pin; - in Limp Home, COMP pin will be pulled down. IF BST_DIS =1, BST_OUT_FAIL bit will not be set. When BST_OUT_FAIL = 1, Boost is disabled until a read and clear command of this bit has been acknowledged. In Limp Home, an auto restart procedure cyclically clears BST_OUT_FAIL bit with a period equal to $t_{AUTORESTART}$.	R/C
5	0	Unused		
4	0	BST2_OCP_LIM	Overcurrent limit status bit [0]: BST2_OCP_LIM limit is not reached or continuous time is less than 2ms. [1]: If BST2_OCP_LIM limit is reached during a filtering time of typically 2ms. – Once BST2_OCP_LIM is reached for the first time an internal flag is set. – This internal flag is re-evaluated cycle by cycle and is going to be reset upon the condition that three consecutive switching cycles have not reached BST2_OCP_LIM threshold. – If the internal flag is still set after elapse of typically 2ms filtering time, the BST2_OCP_LIM status bit accessible in the diagnostic status registers is set and latched.	R/C
3	0	BST1_OCP_LIM	Overcurrent limit status bit [0]: BST1_OCP_LIM limit is not reached or continuous time is less than 2ms. [1]: If BST1_OCP_LIM limit is reached during a filtering time of typically 2ms. – Once BST1_OCP_LIM is reached for the first time an internal flag is set. – This internal flag is re-evaluated cycle by cycle and is going to be reset upon the condition that three consecutive switching cycles have not reached BST1_OCP_LIM threshold. – If the internal flag is still set after elapse of typically 2ms filtering time, the BST1_OCP_LIM status bit accessible in the diagnostic status registers is set and latched.	R/C

Table 26. SR#1: Status Register 1 (continued)

Bit	Default	Name	Description	Access
2	0	N_COMP2_LEVEL_REACH	Timeout of internal peak current comparator of Boost2, COMP2 LEVEL not reached Status bit [0]: Cleared when COMP2 level reached for 10 consecutive switching cycles [1]: When COMP2 level not reached for 10 consecutive switching cycles	R
1	0	N_COMP1_LEVEL_REACH	Timeout of internal peak current comparator of Boost1, COMP1 LEVEL not reached Status bit [0]: Cleared when COMP1 level reached for 10 consecutive switching cycles [1]: When COMP1 level not reached for 10 consecutive switching cycles	R
0		Parity Bit	ODD Parity Bit Check	

5.7.3 Customer trimming registers

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTM_TRIM_COD			DEF_BST_OUT							DEF_BST_OCP_LIM		DEF_BST_FREQ			DEF_BST_FMOD		DEF_BST_FDEV		Reserved				Parity Bit

Address: 0x03Eh

Type: Read / Write allowed in NM only when CTM_TRIM_COD = 100 and EOT = 0

Table 27. CT: Ctm Trimming Register 1

Bit	Default	Name	Comment
23÷21	000	CTM_TRIM_COD	Operation Code for Trimming Operation: 001 --> Standard Read 010 --> Margin Mode Read 011 --> Blank Check 100 --> Burn 111 --> End of Trimming
20÷14	0000000	DEF_BST_OUT	
13÷12	00	DEF_BST_OCP_LIM	
11÷9	000	DEF_BST_FREQ	
8÷7	00	DEF_BST_FMOD	
6÷5	00	DEF_BST_FDEV	
4÷1	0000	-	Reserved: empty
0		Parity Bit	ODD Parity Bit Check

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTM_TRIM_COD			DEF_BST_N_PHASE		DEF_MS	DEF_BST_DIS		DEF_BST_SLP_CTRL						DEF_BST_GM_OTA		DEF_BST_DIS_OTA	DEF_DITH_EN	EOT	Reserved				Parity Bit
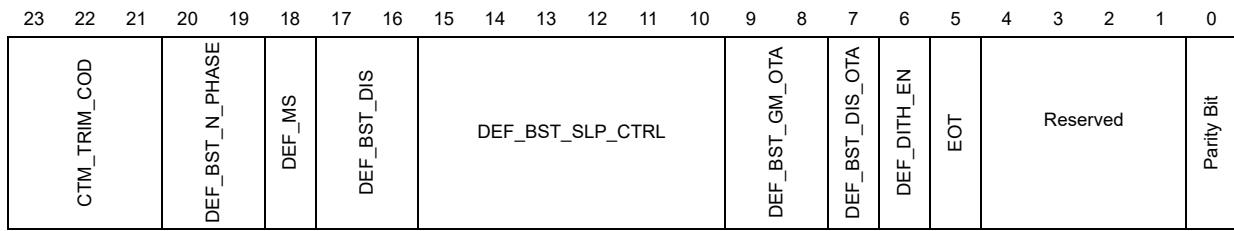
Address: 0x03Fh

Type: Read / Write allowed in NM only when CTM_TRIM_COD = 100 and EOT = 0

Table 28. CT: Ctm Trimming Register 2

Bit	Default	Name	Comment
23÷21	000	CTM_TRIM_COD	Operation Code for Trimming Operation: 001 --> Standard Read 010 --> Margin Mode Read 011 --> Blank Check 100 --> Burn 111 --> End of Trimming
20÷19	00	DEF_BST_N_PHASE	
18	0	DEF_MS	
17÷16	00	DEF_BST_DIS	
15÷10	000000	DEF_BST_SLP_CTRL	
9÷8	00	DEF_BST_GM_OTA	
7	0	DEF_BST_DIS_OTA	
6	0	DEF_DITH_EN	
5	0	EOT	End of Ctm Trimming
4÷1	0000	-	Reserved: empty
0		Parity Bit	ODD Parity Bit Check

5.7.4   Customer test and trimming procedure description

General description

The writing procedure is performed connecting the two terminals of the anti-fuse capacitor at 15 V and ground respectively. This is achieved by providing 15V on VS battery pin.

After this phase, the capacitor is burnt and behaves like a resistance; its value (the residual resistance) strictly depends on the effectiveness of the burning procedure. During physical reading operation, the residual resistance is compared with a fixed threshold. If the residual resistance is greater than threshold a bit 0 is given, and the OTP cell is considered unwritten, otherwise a bit 1 is given and the OTP cell is considered written. Blank check reading is executed to verify that all anti-fuses are unwritten after fabrication, while margin mode, usually performed immediately after the burning process, is used to verify if burned cells are properly written.

Executing a blank-check reading after all writing operations have been completed allows verifying that unwritten cells haven't been degraded by burning processes.

Recommended test flow

Testing procedure starts with a blank check read.

After this operation, it is possible to select the bits to be written and to start programming. Writing operation should be performed up to 3 times. At the end of programming, a reading procedure should be performed in Margin Mode.

At the end of the test, it is strongly recommended executing a blank-check read in order to verify that unwritten cells haven't been degraded.

Table 29 summarizes the writing test conditions.

Table 29. Writing test conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VS	15 V supply			15		V
I_{HV}	HV current during programming				28	mA
—	Temperature		-40	27	150	°C
—	Environment	Dark				
—	External capacitance		2	5	10	nF

Note: *An external capacitance must be applied between VS and GROUND pins.*

6 Electrical specifications

6.1 Absolute maximum ratings

Stressing the device above the rating listed in the *Table 30* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 30. Absolute maximum ratings

Symbol	Parameter		Value	Unit
VS	Battery supply voltage		-0.3 to 40	V
V10V	10 V Voltage regulator capacitor output	VS<20V	-0.3 to VS+0.3	V
		VS ≥ 20V	-0.3 to 20	
V3V3A, V3V3D	3V3 voltage regulator capacitor output		-0.3 to 4.6	V
SYNC_I/O	Boost synchronization I/O pin		-0.3 to V3V3 +0.3	V
VDD	Supply voltage of the SPI interface		-0.3 to 6.5	V
CSN, SDI, SCK	SPI pins voltage		-0.3 to 6.5 + 0.3	V
SDO	SPI pins voltage		-0.3 to VDD + 0.3	V
G01, G02	Boost gate drivers pin voltage		-0.3 to V10V + 0.3	V
SP1, SP2	Boost sense positive and negative pins voltage		-0.3 ÷ 1	V
COMP	Boost compensation network pin voltage		-0.3 ÷ V3V3 + 0.3	V
BST_OUT	Boost output voltage pin		-0.3 to 85	V
SGND, SN1, SN2	Signal Ground pin			
PGND	Power Ground pin			
TM	Test mode high voltage input		-0.3 to 20	V
TMUX	Test mode output		-0.3 ÷ V3V3 + 0.3	
T_j	Junction operating temperature range		-40 to 150	°C
T_{STG}	Storage temperature range		-55 to 150	°C

6.2   ESD protection

Table 31. ESD protection

Parameter	Value	Unit
Electrostatic Discharge Test (AECQ100-002-E) all pins	+/-2	kV
Electrostatic Discharge Test (AECQ100-002-E) all output pins	+/-4	kV
Charge Device Model (CDM-AEC-Q100-011) all pins	+/-500	V
Charge Device Model (CDM-AEC-Q100-011) corner pins	+/-750	V

6.3   Thermal data

Table 32. QFN 32L (5x5) thermal resistance

Symbol	Parameter	Min	Typ	Max	Unit
$R_{thj-amb}$ [1]	Thermal resistance junction to ambient (JEDEC JESD 51-2)	—	34	—	°C/W
$R_{thj-board}$	Thermal resistance junction to board (JEDEC JESD 51-8)	—	12.6	—	°C/W
$R_{thj-case}$	Junction-to-case thermal resistance	—	7.6	—	°C/W

1.   Device mounted on 2s2p four layers PCB (thermally enhanced, slug included).

Table 33. Thermal characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{J_OP}	Operating junction temperature	-40		150	°C
TW_1	Junction temperature warning 1	116	130	142	°C
TW_{1_HYS}	Temperature warning 1 hysteresis		30		°C
TW_2	Junction temperature warning 2	126	140	153	°C
TW_{2_HYS}	Temperature warning 2 hysteresis		10		°C
T_{TSD}	Junction thermal shutdown	157	168	181	°C
T_{TSD_HYS}	Junction thermal shutdown hysteresis		28		°C

6.4 Electrical characteristics

5.5 V < V_S < 28 V, -40 °C < T_j < 150 °C, unless otherwise specified.

The device is still operative and functional at higher temperatures (up to 175°C).

Note: *Parameter limits at temperatures higher than 150°C may change respect to what is specified as per the standard temperature range.*
Device functionality at high temperature is guaranteed by characterization.

6.4.1 Supply

Table 34. Supply

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Digital I/O supply voltage		3.0		5.5	V
$V_{DD,UV}$	V_{DD} under voltage	V_S = 13.5 V, V_{DD} = 5 V Ramp on V_{DD} from 3.2 V to 1.8 V	2.0	2.5	3.0	V
$V_{DD,UV,HYST}$	V_{DD} under voltage - hysteresis			0.08		V
$I_{VDD,STBY}$	V_{DD} standby current	Device in standby mode V_{DD} = 5 V		1	2	µA
$I_{VDD,Q}$	V_{DD} quiescent current	Device in active mode Boost active in open loop V_{DD} = 5 V V_{BST_OUT} = 25 V BST_FREQ= 100 kHz			1.5	mA
V_S	Operating VS supply voltage		5.5		28	V
V_{S_SW1}	Minimum VS voltage for IC supply from VS		10.7	11.1	11.6	V
V_{S_SW2}	Min VS voltage for IC supply from BST_OUT	V_{BST_OUT} > 15V	7.2	7.5	7.9	V
$V_{S,UV,L}$	VS under voltage shutdown - low limit	V_{DD} = 5 V Ramp on V_S from 5.5 V to 4 V Device not supplied by BST_OUT pin	4.5		5	V
$V_{S,UV,HYST}$	VS under voltage hysteresis			0.35		V
$I_{S,Q}$	VS quiescent current	V_S = 13.5 V Boost disabled		6	7	mA
$I_{S,STBY}$	VS standby current	Device in standby mode V_S = 13.5 V		6	10	µA

Table 34. Supply (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_S	VS operating current	Device in active mode Boost active in open loop V_{DD} = 5 V V_S = 13.5 V V_{BST_OUT} = 25 V BST_FREQ= 100 kHz			22	mA
V_{3V3}	Output Voltage of 3V3 LDO	Vs > 4V Iload= 1mA; C_{3V3} = 1µF	3.2	3.3	3.4	V
I_{3V3_LIM}	Current capability of 3V3 LDO	Vs = 13.5V V3V3 pin forced to 2.5V			40	mA
$V_{POR,H}$	Power-on reset high state	Ramp on V3V3 from 2.8 V to 2 V		2.35	2.7	V
$V_{POR,HYST}$	Power-on reset hysteresis			0.035		V

6.4.2 Boost controller

Table 35. Boost gate driver

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{G0x}	Gate driver output rise and fall time	V_S = 13.5 V CG0x = 4.7 nF V_{GS_G0x} rising from 10% ÷ 90%			100	ns
		V_S = 13.5 V; CG0x = 4.7 nF V_{GS_G0x} falling from 90% ÷ 10%			100	ns
V_{G0x_H}	Gate driver High output voltage		0.9 * V10V		V10V	V
V_{G0x_L}	Gate driver Low output voltage				0.3	V
RON_{HS}	High−side switch impedance	V_S = 13.5 V V_{DD} = 5 V V_{SN} = 0 V I_{load} = 100 mA (current sunk from GOx pin)		2.5	5.2	Ω
RON_{LS}	Low−side switch impedance	V_S = 13.5 V V_{DD} = 5 V V_{SN} = 0 V I_{load} = 100 mA (current sourced from GOx pin)		0.7	1.6	Ω

Table 35. Boost gate driver (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{BST\_OUT\_min}$	Minimum boost output voltage	$V_S = 13.5$ V $V_{DD} = 5$ V	14	14.7	15.2	V
$V_{BST\_OUT\_max}$	Maximum boost output voltage	Boost active in open loop $V_{BST\_OUT} = 80$ V	77.4	80	82.3	V
$V_{BST\_OUT\_step}$	Boost output voltage step	SP1, SP2 pins floating V_{SN1}, $V_{SN2} = 0$ V	0.35	0.51	0.7	V
$V_{10V,VS}$	Output voltage of 10V LDO from Vs	$V_S = 13.5$ V $C_{V10V} = 1$ µF $I_{load} = 1$ mA	9.7	10	10.3	V
V_{10V,BST_OUT}	Output voltage of 10V LDO from Bst_Out	$V_{BST\_OUT} = 25$ V $C_{V10V} = 1$ µF $I_{load} = 1$ mA	9.7	10	10.3	V
V_{10V_DROP}	Min voltage drop of 10V LDO respect to V_S: $V_{10V\_DROP} = (V_S - V_{10V})$	$V_S = 10$ V $I_{(V10V)} = -1$ mA		40	200	mV
$I_{10V,LIM}$ [1]	Current capability of 10V LDO from Vs input	$V_S = 13.5$ V V_{10V} forced to GND T_{ROOM}		0.09		A

1. $I_{10V,LIM} = Q_{tgate}$ x F_{boost_sw} (external MOSFET total gate charge multiplied by boost switching frequency).

Table 36. Boost controller

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$F_{BOOST\_SW\_MAX}$	Boost maximum operative switching frequency	$V_S = 13.5$ V $V_{DD} = 5$ V V_{SP1}, $V_{SP2} = 0.3$ V V_{SN1}, $V_{SN2} = 0$ V $V_{COMP} = 0$ V		470		kHz
$F_{BOOST\_SW\_MIN}$	Boost minimum operative switching frequency	$V_S = 13.5$ V $V_{DD} = 5$ V V_{SP1}, $V_{SP2} = 0.3$ V V_{SN1}, $V_{SN2} = 0$ V $V_{COMP} = 0$ V		100		kHz
F_{BOOST_ACC}	Boost Switching Frequency accuracy		-8		8	%

Table 36. Boost controller (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{BST\_OCP\_LIM\ [00]}$	Boost shunt threshold voltage for current limitation.	[0,0] Ramp on SP from 25 mV to 75 mV in 5ms		50		mV
		Accuracy	-28		28	%
$V_{BST\_OCP\_LIM\ [01]}$		[0,1] Ramp on SP from 55 mV to 105 mV in 5ms		85		mV
		Accuracy	-15		15	%
$V_{BST\_OCP\_LIM\ [10]}$		V_{BST_OUT} = 25 V V_{SN} = 0 V [1,0] Ramp on SP from 95 mV to 145 mV in 5ms		115		mV
		Accuracy	-12		12	%
$V_{BST\_OCP\_LIM\ [11]}$		[1,1] Ramp on SP from 125 mV to 175 mV in 5ms		150		mV
		Accuracy	-10		10	%
$t_{ON\_BOOST\_MIN}$	Minimum boost on-time	Vs = 13.5 V V_{DD} = 5 V Boost active in open loop BST_FREQ set to [111] V_{SP1}, V_{SP2} = 0.3 V V_{SN1}, V_{SN2} = 0 V V_{COMP} = 0 V		250	340	ns
$t_{OFF\_BOOST\_MIN}$	Minimum boost off-time	Vs = 13.5 V V_{DD} = 5 V Boost active in open loop BST_FREQ set to [111] V_{SP1}, V_{SP2} = 0 V V_{SN1}, V_{SN2} = 0 V V_{COMP} = 3 V			200	ns
D_{BOOST_MAX}	Boost maximum duty cycle			95		%
t_{SS}	Soft start duration	Guaranteed by scan and frequency oscillator (20 MHz, typical)		8		ms

Table 36. Boost controller (continued)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
G_{M_OTA}	Error amplifier trans-conductance gain	Vs = 13.5 V V_{DD} = 5 V Ramp on BST_OUT pin V_{COMP} = 1.65 V	[0,0]		200		µS
			[0,1]		400		
			[1,0]		600		
			[1,1]		800		
I_{COMP}	Error Amplifier trans conductance output current	Sourcing current into COMP pin; BST_OUT pin foating V_S = 13.5 V V_{COMP} = 1.5 V	[0,0]		60		µA
			[0,1]		120		
			[1,0]		180		
			[1,1]		240		
		Sinking current from COMP pin; BST_OUT pin foating V_S = 13.5 V V_{COMP} = 1.5 V	[0,0]		-60		
			[0,1]		-120		
			[1,0]		-180		
			[1,1]		-240		
G_{LA}	Gain of linear amplifier	V_S = 13.5 V V_{SP1}, V_{SP2} = 200 mV V_{SN1}, V_{SN2} = 0 V			6		V/V
I_{SLOPEx}	Slope compensation current value injected to SPx pin	Vs = 13.5 V V_{DD} = 5 V V_{BST_OUT} = 25 V BST_FREQ = 100 KHz V_{SP1}, V_{SP2} = 0 V R_{SLOPE} = 4.4 kΩ			5.7		A/s
R_{SLOPE}	Integrated configurable slope compensation resistance	BST_SLP_CTRL [000000]		0.36	0.47	0.8	kΩ
		BST_SLP_CTRL [111111]		11.35	13.4	18.5	
		BST_SLP_CTRL step			0.2		
Vcomp_min[1]	Minimum value for boost output regulation	Vs = 13.5 V V_{DD} = 5 V Boost active in closed loop Ramp on BST_OUT from 80 V to 14.7 V Load on BST_OUT = 136 Ω BST_FREQ = 303 KHz R_{SLOPE} = 3 kΩ GM_OTA = 200 µS			2.6		mV

Table 36. Boost controller (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Vcomp_max[1]	Maximum value for boost output regulation	Vs = 13.5 V V_{DD} = 5 V Boost active in closed loop Ramp on BST_OUT from 14.7 V to 80 V Load on BST_OUT = 136 Ω BST_FREQ = 303 KHz R_{SLOPE} = 3 kΩ GM_OTA = 200 µS		3[2]		V
Icomp_leak	Comp output leakage if boost is deactivated	Error Amplifier disabled, high-impedance tri-state			1	µA

1. Parameter guaranteed by design and characterization - not subject to production test.

2. Vcomp_max value is also achieved performing the test in open load.

Table 37. Boost controller reference voltage

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{BST\_OUT\_OV\_ON}$	Boost output overvoltage activation threshold	Vs = 13.5 V V_{DD} = 5 V Ramp on BST_OUT pin from 77 V up to 85 V	80.5	1.03 * $V_{BST\_OUT[1111111]}$	85.8	V
$V_{BST\_OUT\_OV\_OFF}$	Boost output overvoltage de-activation threshold	Vs = 13.5 V V_{DD} = 5 V Ramp on BST_OUT pin from 85 V down to 77 V	76.9	$V_{BST\_OUT\ [1111111]}$	82	V

6.4.3 System Oscillator and Digital Timings

Digital timings guaranteed by scan. WD and auto-restart timings limits added to give indication on application cases.

Table 38. Digital timings description

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{WD}	Watchdog timeout period		45	50	55	ms
$t_{CSN\_TIMEOUT}$	CSN timeout		90	115	140	ms
$t_{AUTORESTART}$	Autorestart time in Limp Home mode		45	50	55	ms
$t_{VS,UV}$	VS undervoltage filter time			32		µs
t_{VDD_FT}	VDD Filtering Time			32		µs
t_{WAKEUP}	Time for a complete wake up ($V3V3 > V_{POR\_L}$)	CSN low for $t > t_{WAKEUP}$ Cap on V3V3 = 1µF V3V3 > 3V		129		µs
t_{STDBY}	Time needed for a transition to standby mode ($V3V3 < V_{POR\_L}$)	CSN high for $t > t_{STDBY}$ Cap on V3V3 = 1µF V3V3 < 2.5V		1		ms
t_{OVT}	Filtering time for overtemperature (OVT bit will be set if $T_j > T_{TSD}$ for more than t_{OVT})			1.2		µs
t_{BST_OVP}	BST_OVP flag set filtering time			32		µs
$t_{BST\_OVP\_RST}$	BST_OVP flag reset filtering time			10		ms
$t_{BOOST\_OUT\_FAIL}$	BST_OUT_FAIL flag set filtering time			1.6		µs
t_{TM_LOW}	Time needed for a transition to pre-standby mode ($V3V3 > V_{POR\_L}$)			200		µs

6.4.4 SPI bus (CSN, SCK, SDI, SDO)

Table 39. CSN, SCK, SDI input

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IN_L}	Input voltage low threshold				$0.3 * V_{3V3}$	V
V_{IN_H}	Input voltage high threshold		$0.7 * V_{3V3}$		V_{3V3}	V
$I_{IN\_L,\ SDI,SCK}$	Low level input current	$V_{IN} = 0.3 * V_{3V3}$	1			µA
$I_{IN\_L,\ CSN}$			-10			µA
$I_{IN\_H,\ SDI,SCK}$	High level input current	$V_{IN} = 0.7 * V_{3V3}$			10	µA
$I_{IN\_H,\ CSN}$					-1	µA

Table 40. SDO output

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{OUT_L}	Output voltage low threshold	Iout = 4 mA			$0.2 * V_{DD}$	V
V_{OUT_H}	Output voltage high threshold	Iout = −4 mA	$0.8 * V_{DD}$			V
I_{OUT_LEAK}	Output leakage current	V_{OUT} = 0 V	-5		5	µA

Table 41. SPI timing

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{sck}	Serial clock (SCK) period		250			ns
t_{Hsck}	SCK high time		100			ns
t_{Lsck}	SCK low time		100			ns
t_{rise_in}	CSN, SCK, SDI rise time	Fsck = 4MHz			25	ns
t_{fall_in}	CSN, SCK, SDI fall time	Fsck = 4MHz			25	ns
t_{Hcsn}	CSN high time		6			µs
t_{Scsn}	CSN setup time, CSN low before SCK rising		100			ns
t_{Ssck}	SCK setup time, SCK low before CSN rising		100			ns
t_{Ssdi}	SDI setup time before SCK rising		25			ns
t_{hold_sdi}	SDI hold time		25			ns
t_{csn_v}	CSN falling until SDO valid	Cout = 50pF; Iout = ±1mA			100	ns
t_{csn_t}	CSN rising until SDO tristate	Cout = 50pF; Iout = ±4mA			100	ns
t_{sck_v}	SCK falling until SDO valid	Cout = 50pF			60	ns
t_{Rsdo}	SDO rise time	Guaranteed by scan and frequency oscillator (20 MHz, typical)			100	ns
t_{Fsdo}	SDO fall time	Guaranteed by scan and frequency oscillator (20 MHz, typical)			100	ns
$t_{csn\_low\_t}$	CSN low timeout		20	35	50	ms

7   Package and PCB thermal data

7.1   QFN-32L 5x5 thermal data
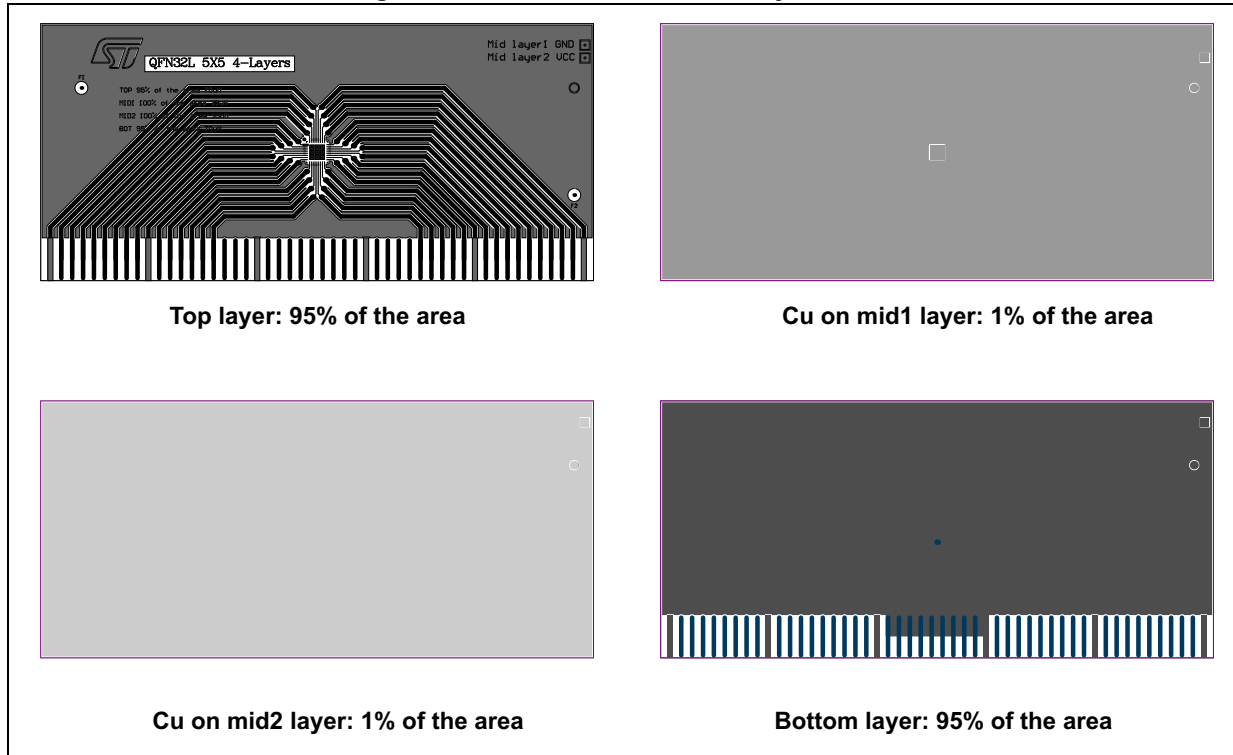
Figure 11. QFN-32L 5x5 on four-layers PCB

Top layer: 95% of the area

Cu on mid1 layer: 1% of the area

Cu on mid2 layer: 1% of the area

Bottom layer: 95% of the area

Table 42. PCB proprieties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	129 mm x 60 mm
Board material	FR4
Copper thickness (outer layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of *ECOPACK* packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

8.1 QFN-32L 5x5 package information
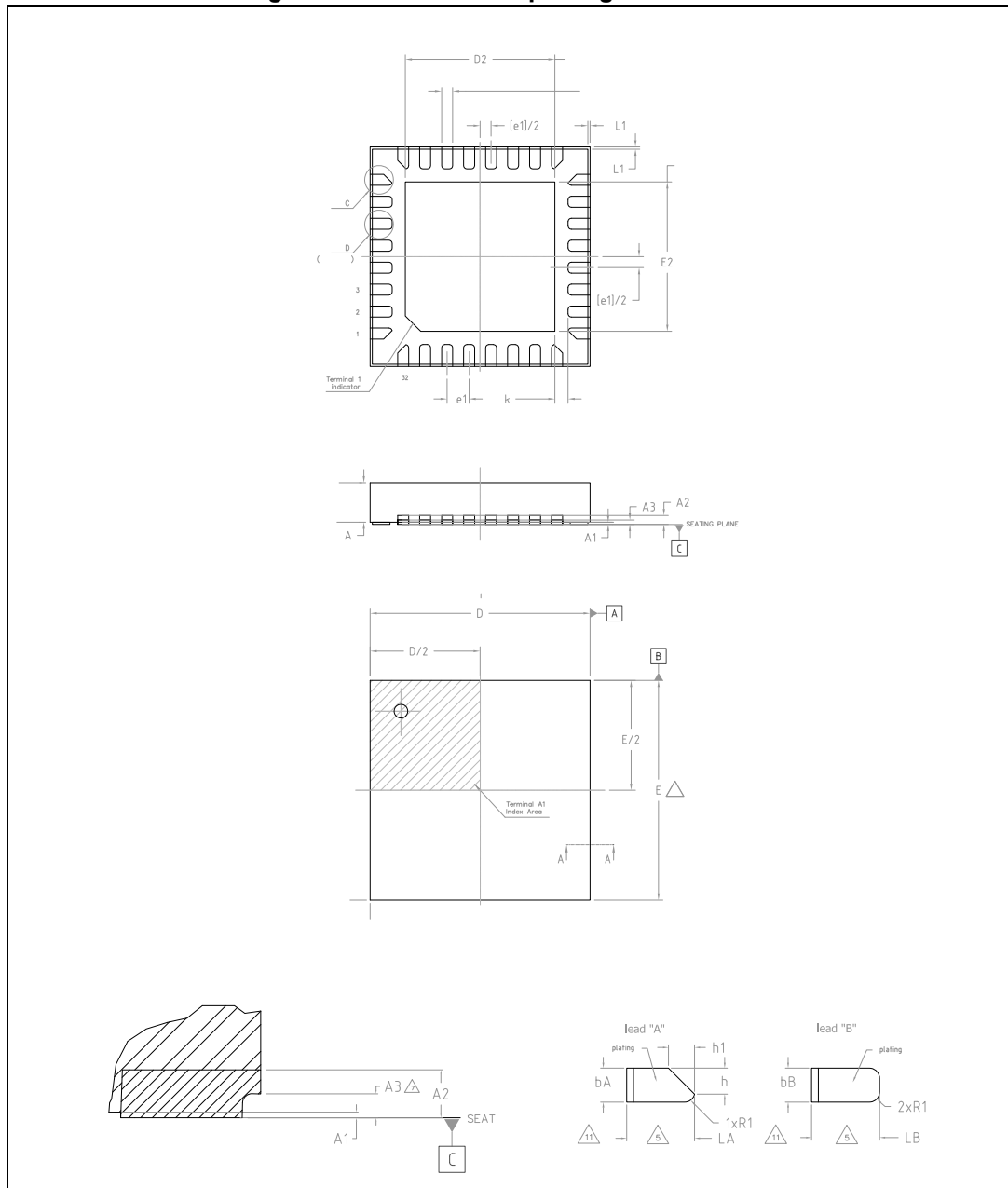
Figure 12. QFN-32L 5x5 package dimensions

Table 43. QFN-32L 5x5 package information

Symbol	Min.	Typ.	Max.
Dimensions			
	(mm)		
A	0.85	0.90	0.95
A1	0		0.05
A2		0.2 REF	
A3	0.07		0.17
D	5.00 BSC		
D2	3.45	3.50	3.55
E	5.00 BSC		
E2	3.45	3.50	3.55
e1	0.5 BSC		
k	0.20		
L1			0.05
La	0.47	0.50	0.53
bA	0.22	0.25	0.28
h		0.19 REF	
h1		0.19 REF	
LB	0.47	0.50	0.53
bB	0.22	0.25	0.28
N	32		
R1			0.1

9 Order codes

Table 44. Device summary

Package	Order codes	
	Tray	**Tape and Reel**
QFN32L	L99LD02Q505	L99LD02Q505TR

Appendix A   Glossary

Table 45. Glossary

Acronym	Description
µC	Microcontroller
ADC	Analog / Digital converter
ASSP	Application Specific Standard Product
CPHA	Clock Phase
CPOL	Clock Polarity
CSN	Chip select not (normal low) (SPI)
CTRL	Control register
FE	Functional Error
FS	Fail Safe
DE	Device Error
GSB	Global Status Byte
GSBN	Global Status Bit Not
GW	Global Warning
I/O	Input /Output pins
DIN	Direct input
LH	Limp Home
LSB	Least Significant Bit
MCU	Microcontroller
SDI	SPI Data Input (slave)
SDO	SPI Data Output (slave)
MSB	Most Significant Bit

Revision history

Table 46. Document revision history

Date	Revision	Changes
02-Feb-2018	1	Initial release.
01-Mar-2019	2	Document status changed from target specification to preliminary data. Updated features in cover page. Updated: – *Table 1: Functional block diagram* – *Figure 9: Device state diagram* – *Table 7: Operating modes* – *Section 4.1.1: Standby mode* – *Table 21: ROM Memory Map* – *Table 24: CR#3: Control Register 3* – *Table 26: SR#1: Status Register 1* – *Table 32: QFN 32L (5x5) thermal resistance* – *Table 34: Supply* – *Table 35: Boost gate driver* – *Table 36: Boost controller* – *Table 38: Digital timings description* – *Table 39: CSN, SCK, SDI input* – *Table 41: SPI timing* – *Section 4.1.4: Limp Home / Stand-alone mode* – *Section 8: Package information* Added: – *Figure 4: Resistor ladder for slope compensation and input current limitation* – *Table 40: SDO output* – *Section 7: Package and PCB thermal data* Minor text changes.
15-Jan-2020	3	Document status changed from preliminary data to production data. Updated: – *CR#3: Control Register 3* – *SR#1: Status Register 1* – *Table 33: Thermal characteristics* – *Table 34: Supply* – *Table 35: Boost gate driver* – *Table 36: Boost controller* – *Table 39: CSN, SCK, SDI input* – *Table 40: SDO output* Added: – IS parameter in *Table 34: Supply* Minor text changes.

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