L99MOD50XP

Multi-output driver for automotive applications

Datasheet - production data

PowerSSO-36

Features

- AEC-Q100 qualified
- Two half bridges for 6 A load (R_{DSon} = 150 mΩ)
- Two half bridges for 3 A load (R_{DSon} = 300 mΩ)
- Two half bridges for 0.75 A load (R_{DSon} = 1600 mΩ)
- One high-side driver for 6 A load (R_{DSon} = 90 mΩ)
- Two configurable high-side drivers for up to 1.5A load (R_{DSon} = 500 mΩ) or 0.4 A load (R_{DSon} = 1800 mΩ)
- Two high-side drivers for 0.5 A load (R_{DSon} = 1600 mΩ)
- Programmable soft start function to drive loads with higher inrush currents as current limitation value
- Very low current consumption in standby mode (I_S < 6 µA typ; $T_j \leq$ 85 °C; I_{CC}<5 µA typ; $T_j \leq$ 85 °C)
- Current monitor output for all high-side drivers
- Device contains temperature warning and protection
- Open-load detection for all outputs
- Over-current protection for all outputs
- PWM control of all outputs
- Charge pump output for reverse polarity protection
- ST standard serial peripheral interface (ST-SPI 3.0)

Applications

L99MOD devices are recommended for those applications that need multiple motors control with additional loads in high-side configuration, such as bulbs/LEDs or requiring protected supply, like sensors or cameras.

Description

The L99MOD50XP is a microcontroller-driven multifunctional actuator driver for automotive applications.

Up to five DC motors and five grounded resistive loads can be driven with six half bridges and five high-side drivers.

The integrated SPI controls all operating modes (forward, reverse, brake and high impedance).

Also all diagnostic information is available via SPI read.

Table 1. Device summary

Package	Order codes	Packing
PowerSSO-36	L99MOD50XPTR	Tape and reel

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1 Block diagram and pin description

Figure 1. Block diagram

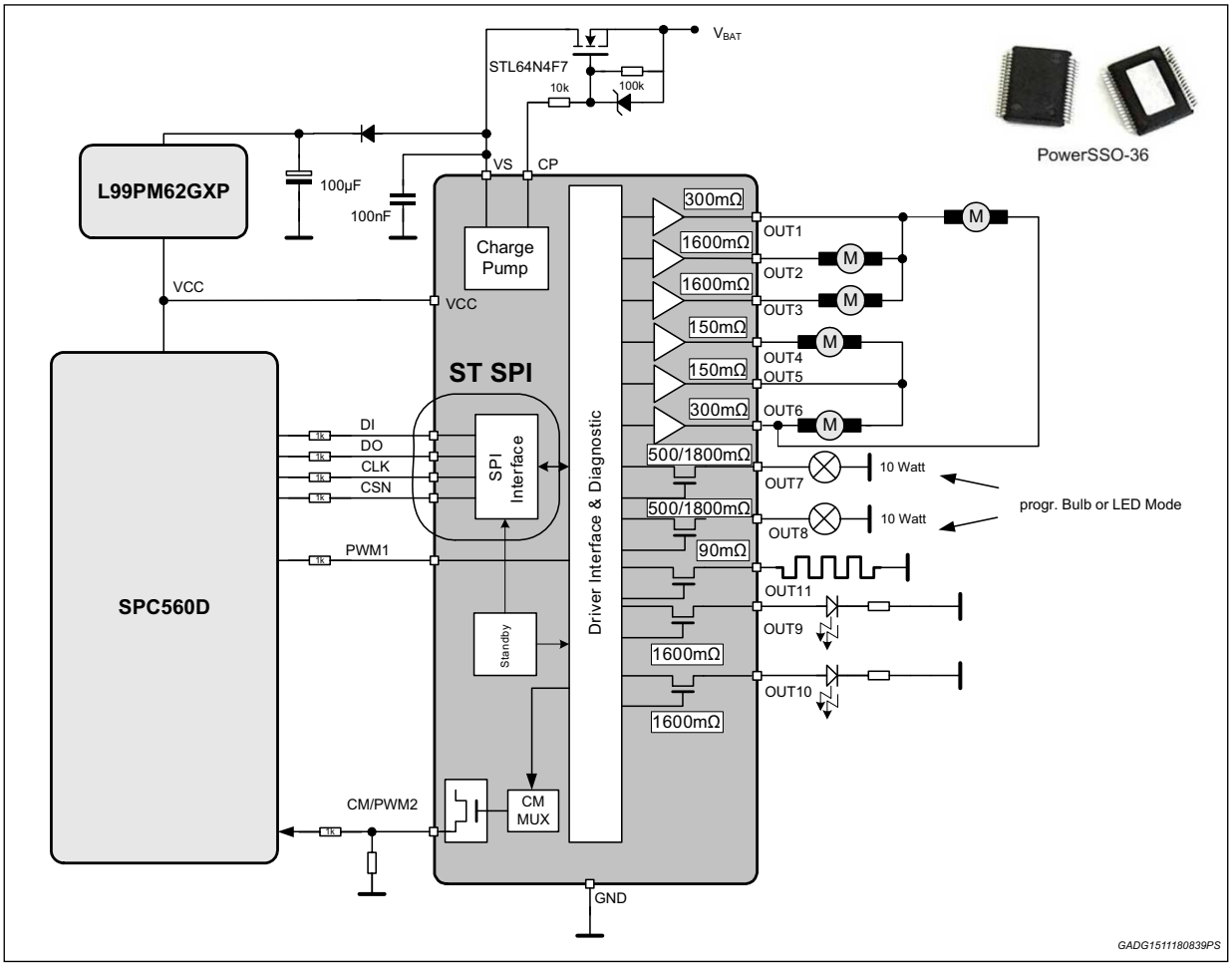
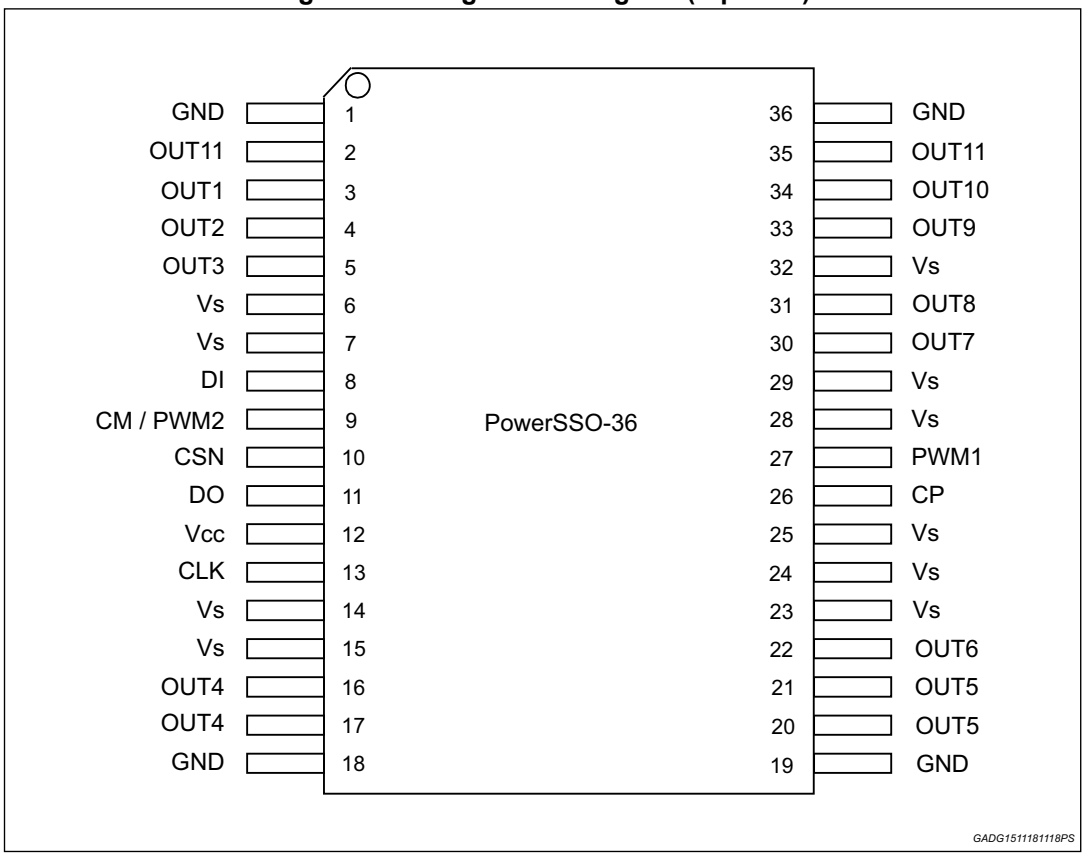


Figure 2. Configuration diagram (top view)



Note: All pins with the same name must be externally connected.

Table 2. Pin definition and functions

Pin	Symbol	Function
1, 18, 19, 36	GND	Ground: reference potential. *Important:* For the capability of driving the full current at the outputs all pins of GND must be externally connected!
2, 35	OUT11	High-side driver output 11. The output is built by a high-side switch and is intended for resistive loads, therefore the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present, but the energy which can be dissipated is limited. The high-side driver is a power DMOS transistor with an internal parasitic reverse diode from the output to VS (bulk-drain-diode). The output is over-current protected. *Important:* for the capability of driving the full current at the outputs both pins of OUT11 must be externally connected!
3 4 5	OUT1, OUT2, OUT3	Halfbridge outputs 1,2,3. The output is built by a high-side and a low-side switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output). This output is over-current protected.
6, 7, 14, 15, 23, 24, 25, 28, 29, 32	V_S	Power supply voltage (external reverse protection required). For this input a ceramic capacitor as close as possible to GND is recommended. *Important:* For the capability of driving the full current at the outputs all pins of VS must be externally connected! Pins 25 and 32 can be connected to VS to maintain compatibility with other L99MOD products; otherwise they should be left Not Connected
8	DI	Serial data input. The input requires CMOS logic levels and receives serial data from the microcontroller. The data is a 24 bit control word and the most significant bit (MSB, bit 23) is transferred first.
9	CM/ PWM2	Current monitor output/PWM2 input. Depending on the selected multiplexer bits of the control register this output sources an image of the instant current through the corresponding high-side driver with a ratio of 1/10.000 or 1/2000. This pin is bidirectional. The microcontroller can overdrive the current monitor signal to provide a second PWM input for the outputs OUT5, OUT8 and OUT10.
10	CSN	Chip Select Not input This input is low active and requires CMOS logic levels. The serial data transfer between L99MOD50XP and the microcontroller is enabled by pulling the input CSN to low level.
11	DO	Serial data output. The diagnosis data is available via the SPI and this tristate-output. The output will remain in tristate, if the chip is not selected by the input CSN (CSN = high)
12	VCC	Supply voltage. For this input a ceramic capacitor as close as possible to GND is recommended.
13	CLK	Serial clock input. This input controls the internal shift register of the SPI and requires CMOS logic levels.
16,17 20,21 22	OUT4, OUT5, OUT6	Half-bridge outputs 4,5,6: see OUT1 (pin 3). *Important:* For the capability of driving the full current at the outputs both pins of OUT4 (OUT5, respectively) must be externally connected!

Table 2. Pin definition and functions (continued)

Pin	Symbol	Function
26	CP	Charge pump output. This output is provided to drive the gate of an external n-channel power MOS used for reverse polarity protection (see *Figure 1.*).
27	PWM1	PWM1 input. This input signal can be used to control the drivers OUT1-4, OUT6-7, OUT9 and OUT11 by an external PWM signal.
30 31	OUT7, OUT8,	High-side driver outputs 7,8: see OUT9. By selection of one of the 2 power DMOS at same output is it possible to supply a bulb with low on-resistance or a LED with higher on-resistance in a different application.
33	OUT9	High-side driver output 9. The output is built by a high-side switch and is intended for resistive loads, hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. The high-side driver is a power DMOS transistor with an internal parasitic reverse diode from the output to VS (bulk-drain-diode). The output is over-current and open load protected.
34	OUT10	High-side driver output 10: see OUT9. *Important:* beside the bit10 in control register 1 this output can be switched on setting bit1 for electrocromic control mode with higher priority.

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
Vs	DC supply voltage	-0.3...28	V
	Single pulse t_{max} < 400 ms	40	V
Vcc	Stabilized supply voltage, logic supply	-0.3 to 5.5	V
V_{DI}, V_{DO}, V_{CLK}, V_{CSN}, V_{PWM}	Digital input / output voltage	-0.3 to V_{CC} + 0.3	V
V_{CM}	Current monitor output	-0.3 to V_{CC} + 0.3	V
V_{CP}	Charge pump output	-25 to V_S + 11	V
V_{OUTn}	Static output voltage (n= 1 to 11)	-0.3 to V_S + 0.3	V
$I_{OUT,2,3,9,10}$	Output current	±1.25	A
$I_{OUT1,6,7,8}$	Output current	±5	A
$I_{OUT4,5,11}$	Output current	±10	A

2.2 ESD protection

Table 4. ESD protection

Parameter	Value	Unit
All pins	± 2 (1)	kV
Output pins: OUT1 - OUT6	± 4 (2)	kV

1. HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A.
2. HBM with all unzapped pins grounded.

2.3 Thermal data

Table 5. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 150	°C

Table 6. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{jTW\ ON}$	Temperature warning threshold junction temperature	T_j	130		150	°C
$T_{jSD\ ON}$	Thermal shutdown threshold junction temperature	T_j increasing			170	°C
$T_{jSD\ OFF}$	Thermal shutdown threshold junction temperature	T_j decreasing	150			°C
$T_{jSD\ HYS}$	Thermal shutdown hysteresis			5		°K

2.4 Electrical characteristics

V_S = 8 to 16 V, V_{CC} = 4.5 to 5.3 V, T_j = - 40 to 150 °C, unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 7. Supply

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
7.1	VS	Operating voltage range		7		28	V
7.2	I_S	V_S DC supply current	V_S = 16 V, V_{CC} = 5.3 V active mode OUT1 - OUT11		7	20	mA
7.3		V_S quiescent supply current	V_S = 16 V, V_{CC} = 0 V standby mode OUT1 - OUT11 T_{test} = -40°C, 25°C		4	12	µA
7.4(1)			T_{test} = 85°C		6	25	
7.5	I_{CC}	V_{CC} DC supply current	V_S = 16 V, V_{CC} = 5.3 V CSN = V_{CC}, active mode OUT1 - OUT11		1	3	mA
7.6(2)		V_{CC} quiescent supply current	V_S = 16 V, V_{CC} = 5.3 V_{CSN} = V_{CC} standby mode OUT1 - OUT11 T_{test} = -40°C, 25°C		3	6	µA
7.7(1)			T_{test} = 85°C		5	10	

1. This parameter is guaranteed by design.
2. CM/ PWM 2 = V_{CC} or 0 V.

Table 8. Overvoltage and under voltage detection

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
8.1	$V_{SUV\ on}$	V_S UV-threshold voltage	V_S increasing	5.6		7.2	V
8.2	$V_{SUV\ off}$	V_S UV-threshold voltage	V_S decreasing	5.2		6.1	V
8.3	$V_{SUV\ hyst}$	V_S UV-hysteresis	$V_{SUV\ ON}$ - $V_{SUV\ OFF}$		0.5		V
8.4	$V_{SOV\ off}$	V_S OV-threshold voltage	V_S increasing	18		24.5	V
8.5	$V_{SOV\ on}$	V_S OV-threshold voltage	V_S decreasing	17.5		23.5	V
8.6	$V_{SOV\ hyst}$	V_S OV-hysteresis	$V_{SOV\ OFF}$ - $V_{SOV\ ON}$		1		V
8.7	$V_{POR\ off}$	Power-on-reset threshold	V_{CC} increasing			2.9	V
8.8	$V_{POR\ on}$	Power-on-reset threshold	V_{CC} decreasing	2.0			V
8.9	$V_{POR\ hyst}$	Power-on-reset hysteresis	$V_{POR\ OFF}$ - $V_{POR\ ON}$		0.11		V

Table 9. Current monitor output CM / PWM 2

Item	Symbol	Parameter	Test condition		Min.	Typ.	Max	Unit
9.1	V_{CM}	Functional voltage range			0		V_{CC}-1V	V
9.2	$I_{CM,r}$	Current monitor output ratio: I_{CM} / $I_{OUT1,4,5,6,11\ and\ 7,8}$ (low on-resistance)	0 V <= V_{CM} <= 4 V, V_{CC}=5 V			$\frac{1}{10.000}$		
9.3		I_{CM} / $I_{OUT2,3,9,10\ and\ 7,8}$ (high on-resistance)				$\frac{1}{2000}$		
9.4	$I_{CM\ acc}$	Current monitor accuracy $acclI_{CMOUT1,4,5,6,11}$ and 7, 8 (low on-res.)	V_{CM} <= 3.8 V, V_{CC} = 5 V	$I_{Out,min}$= 500 mA $I_{Out4,5,11max}$= 5.9 A $I_{Out1,6\ max}$= 2.9 A $I_{Out7,8\ max}$= 1.3 A	-8% - 2%FS (1)	0	8% + 2%FS (1)	A
9.5		$acclI_{CMOUT2,3,9,10,}$ and 7, 8 (high on-res.)		$I_{Out,min}$= 100 mA $I_{Out2,3\ max}$= 0.6 A $I_{Out9,10max}$= 0.4 A $I_{Out8\ max}$= 0.3 A				

1. FS (full scale)= I_{OUTmax} * I_{CMr_typ} .

Table 10. Charge pump output CP

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max	Unit
10.1	V_{CP}	Charge pump output voltage	V_S = 8 V, I_{CP} = -60 µA	V_S+6		V_S+13	V
10.2			V_S = 10 V, I_{CP} = -80 µA	V_S+8		V_S+13	V
10.3			V_S >=12 V, I_{CP} = -100 µA	V_S+10		V_S+13	V
10.4	I_{CP}	Charge pump output current	V_{CP} = V_S+10 V, V_S =13.5 V	95	150	300	µA

2.4.1 Outputs OUT1 - OUT11

Table 11. On-resistance and switching times

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
11.1	$r_{ON\ OUT1,}$ $r_{ON\ OUT6}$	On-resistance to supply or GND	V_S = 13.5 V, T_j = 25 °C, $I_{OUT1,6}$ = ± 1.5 A		300	400	mΩ
11.2			V_S = 13.5 V, T_j = 125 °C, $I_{OUT1,6}$ = ± 1.5 A		450	600	mΩ
11.3	$r_{ON\ OUT2,}$ $r_{ON\ OUT3}$	On-resistance to supply or GND	V_S = 13.5 V, T_j = 25 °C, $I_{OUT2,3}$ = ± 0.4 A		1600	2200	mΩ
11.4			V_S = 13.5 V, T_j = 125 °C, $I_{OUT2,3}$ = ± 0.4 A		2500	3400	mΩ
11.5	$r_{ON\ OUT4,}$ $r_{ON\ OUT5}$	On-resistance to supply or GND	V_S = 13.5 V, T_j = 25 °C, $I_{OUT4,5}$ = ± 3.0 A		150	200	mΩ
11.6			V_S = 13.5 V, T_j = 125 °C, $I_{OUT4,5}$ = ± 3.0 A		225	300	mΩ
11.7	$r_{ON\ OUT9,}$ $r_{ON\ OUT10}$	On-resistance to supply	V_S = 13.5 V, T_j = 25 °C, $I_{OUT9,10}$ = -0.4 A		1600	2200	mΩ
11.8			V_S = 13.5 V, T_j = 125 °C, $I_{OUT9,10}$ = -0.4 A		2500	3400	mΩ
11.9	$r_{ON\ \ OUT11}$	On-resistance to supply	V_S = 13.5 V, T_j = 25 °C, I_{OUT11} = -3.0 A		90	130	mΩ
11.10			V_S = 13.5 V, T_j = 125 °C, I_{OUT11} = -3.0 A		130	180	mΩ

Table 11. On-resistance and switching times (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
11.11	$r_{ON\,OUT7}$ $r_{ON\,OUT8}$	On-resistance to supply in low mode (control register 1 bits 12 to15: 0101)	V_S = 13.5 V, T_j = 25 °C, $I_{OUT7,8}$ = - 0.8 A		500	700	mΩ
11.12			V_S = 13.5 V, T_j = 125 °C, $I_{OUT7,8}$ = - 0.8 A		700	950	mΩ
11.13		On-resistance to supply in high mode (control register 1 bits 12 to15: 1010)	V_S = 13.5 V, T_j = 25 °C, $I_{OUT7,8}$ = - 0.2 A		1800	2400	mΩ
11.14			V_S = 13.5 V, T_j = 125 °C, $I_{OUT7,8}$ = - 0.2 A		2500	3400	mΩ
11.15	I_{QLH}	Switched-off output current high-side drivers of OUT1-6, 8-11	V_{OUT}= 0 V, standby mode	-5	-2		µA
11.16			V_{OUT}= 0 V, active mode	-10	-7		µA
11.17	$I_{QLH7,8}$	Switched-off output current high-side drivers of OUT7-8	V_{OUT}= 0 V, standby mode	-5	-2		µA
11.18			V_{OUT}= 0 V, active mode	-15	-10		µA
11.19	I_{QLL}	Switched-off output current low-side drivers of OUT1-6	V_{OUT}= V_S, standby mode		80	120	µA
11.20			V_{OUT}= 0 V, active mode	-10	-7		µA
11.21	$t_{d\,ON\,H}$	Output delay time, high-side driver on (OUT_X except $OUT_{7,8}$)	V_S = 13.5 V, V_{CC} = 5 V (1)(2)(3)	20	40	80	µs
11.22		Output delay time, high-side driver on ($OUT_{7,8}$ in high R_{DSon} mode)		15	35	60	µs
11.23		Output delay time, high-side driver on ($OUT_{7,8}$ in low R_{DSon} mode)		10	35	80	µs
11.24	$t_{d\,OFF\,H}$	Output delay time, high-side driver off ($OUT_{1,4,5,6,11}$)	V_S = 13.5 V, V_{CC} = 5 V(1)(2)(3)	60	150	200	µs
11.25		Output delay time, high-side driver off ($OUT_{2,3,7}$, high/low $R_{DSon\,,\,8}$ high/low $R_{DSon\,,\,9,\,10}$)		40	70	100	µs

Table 11. On-resistance and switching times (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
11.26	$t_{d\ ON\ L}$	Output delay time, low-side driver On	V_S = 13.5 V, V_{CC} = 5 V, corresponding high-side driver is not active(1)(2)(3)	15	30	70	µs
11.27	$t_{d\ OFF\ L\ 1\text{-}6}$	Output delay time, low-side driver OUT 1-6 off	V_S=13.5 V, V_{CC}=5 V(1)(2)(3)	40	150	300	µs
11.28	$t_{D\ HL}$	Cross current protection time	$t_{cc\ ONLS\_OFFHS}$ - $t_{d\ OFFH}$(4)	50	200	400	µs
11.29	$t_{D\ LH}$		$t_{cc\ ONHS\_OFFLS}$ -$t_{d\ OFFL}$(4)				
11.30	$dV_{OUT}/dt_{on/off}$	Slew rate of OUTx	V_S = 13.5 V, V_{CC} = 5 V(1)(2)(3)	0.1	0.2	0.6	V/µs

1. Rload = 16 Ω at OUT1, 6 and 7,8 in low on-resistance mode.
2. Rload = 4 Ω at OUT4, 5 and 11.
3. Rload = 64 Ω at OUT2, 3, 9, 10 and 7, 8 in high On-resistance mode.
4. t_{cc} is the switch-on delay time if complement in half bridge has to switch-off.

Table 12. Current monitoring

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
12.1	$\|I_{OC1}\|$, $\|I_{OC6}\|$	Over-current threshold to supply or GND	V_S = 13.5 V, V_{CC} = 5 V, sink and source	3		5	A
12.2	$\|I_{OC2}\|$, $\|I_{OC3}\|$			0.75		1.25	A
12.3	$\|I_{OC4}\|$, $\|I_{OC5}\|$			6		10	A
12.4	$\|I_{OC9}\|$, $\|I_{OC10}\|$	Over-current threshold to supply	V_S = 13.5 V, V_{CC} = 5 V, source	0.5		1.0	A
12.5	$\|I_{OC11}\|$			6		10	A
12.6	$\|I_{OC7}\|$, $\|I_{OC8}\|$	Over-current threshold to supply in low on-resistance mode	V_S = 13.5 V, V_{CC} = 5 V, source, control register 1 bits 12 to 15: 0101	1.5		2.5	A
12.7		Over-current threshold to supply in high on-resistance mode	V_S = 13.5 V, V_{CC} = 5 V, source, control register 1 bits 12 to 15: 1010	0.35		0.65	A
12.8	t_{FOC}	Filter time of over-current signal	Duration of over-current condition to set the status bit	10	55	100	µs
12.9	f_{rec0}	Recovery frequency for OC recovery duty cycle bit= 0		1		4	kHz
12.10	f_{rec1}	Recovery frequency for OC recovery duty cycle bit= 1		2		6	kHz

Table 12. Current monitoring (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
12.11	$\|I_{OLD1}\|$, $\|I_{OLD6}\|$	Under-current threshold to supply or GND	V_S = 13.5 V, V_{CC} = 5 V, sink and source	10	30	80	mA
12.12	$\|I_{OLD2}\|$, $\|I_{OLD3}\|$			10	20	30	mA
12.13	$\|I_{OLD4}\|$, $\|I_{OLD5}\|$			60	150	300	mA
12.14	$\|I_{OLD9}\|$, $\|I_{OLD10}\|$	Under-current threshold to supply	V_S = 13.5 V, V_{CC} = 5 V, source	5	10	15	mA
12.15	$\|I_{OLD11}\|$			30	150	300	mA
12.16	$\|I_{OLD7}\|$, $\|I_{OLD8}\|$	Under-current threshold to supply in low on-resistance mode		15	40	60	mA
12.17		Under-current threshold to supply in high on-resistance mode		5	10	15	mA
12.18	t_{FOL}	Filter time of under-current	Duration of under-current condition to set the status bit	0.5		3	ms

2.5 SPI - Electrical characteristics

V_S = 8 to 16 V, V_{CC} = 4.5 to 5.5 V, T_j = - 40 to 150°C, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 13. Delay time from standby to active mode

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
14.1	t_{set}	Delay time	Switching from standby to active mode. Time until output drivers are enabled after CSN going to high and set bit 0=1 of control register 0.		256	300	µs

Table 14. Inputs: CSN, CLK, PWM1/2 and DI

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
15.1	V_{inL}	Input low level	V_{CC} = 5 V			0.3* Vcc	V
15.2	V_{inH}	Input high level	V_{CC} = 5 V	0.7* Vcc			V
15.3	$V_{in\ Hyst}$	Input hysteresis	V_{CC} = 5 V	500			mV
15.4	$R_{CSN\ in}$	CSN pull up resistor	V_{CC} = 5 V 0 V<V_{CSN}<0.7 V_{CC}	30	120	250	kΩ

Table 14. Inputs: CSN, CLK, PWM1/2 and DI (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
15.5	$R_{CLK\ in}$	CLK pull down resistor	V_{CC} = 5 V V_{CLK} = 1.5 V	30	60	150	kΩ
15.6	$R_{DI\ in}$	DI pull down resistor	V_{CC} = 5 V V_{DI} = 1.5 V	30	60	150	kΩ
15.7	$R_{PWM1\ in}$	PWM1 pull down resistor	V_{CC} = 5 V V_{PWM1}= 1.5 V	30	60	150	kΩ
15.8	C_{in} (1)	Input capacitance at input CSN, CLK, DI and PWM1/2	0 V < V_{CC} < 5.3 V			10	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 15. SDI timing

Item	Symbol	Parameter(1)	Test condition	Min.	Typ.	Max.	Unit
16.1	t_{CLK}	Clock period	V_{CC} = 5 V		1000		ns
16.2	t_{CLKH}	Clock high time	V_{CC} = 5 V	115			ns
16.3	t_{CLKL}	Clock low time	V_{CC} = 5 V	115			ns
16.4	$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	V_{CC} = 5 V	400			ns
16.5	$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	V_{CC} = 5 V	400			ns
16.6	$t_{set\ DI}$	DI setup time	V_{CC} = 5 V	200			ns
16.7	$t_{hold\ DI}$	DI hold time	V_{CC} = 5 V	200			ns
16.8	$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	V_{CC} = 5 V			100	ns
16.9	$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	V_{CC} = 5 V			100	ns

1. DI timing parameters tested in production by a passed / failed test:
   Tj = -40°C / +25°C: SPI communication @ 2 MHz.
   Tj = +125°C: SPI communication @ 1.25 MHz.

Table 16. DO

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
17.1	V_{DOL}	Output low level	I_{DO} = -5 mA			0.2V_{CC}	V
17.2	V_{DOH}	Output high level	I_{DO} = 5 mA	0.8 V_{CC}			V
17.3	I_{DOLK}	Tristate leakage current	V_{CSN} = V_{CC}, 0 V < V_{DO} < V_{CC}	-10		10	µA
17.4	C_{DO} (1)	Tristate input capacitance	V_{CSN} = V_{CC}, 0 V < V_{CC} < 5.3 V			10	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 17. DO timing

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
18.1	$t_{r\ DO}$	DO rise time	C_{DO} = 100 pF		80	140	ns
18.2	$t_{f\ DO}$	DO fall time	C_{DO} = 100 pF		50	100	ns
18.3	$t_{en\ DO\ tri\ L}$	DO enable time from tristate to low level	C_{DO} = 100 pF, I_{load} = 1 mA pull-up load to V_{CC}		100	250	ns
18.4	$t_{dis\ DO\ L\ tri}$	DO disable time from low level to tristate	C_{DO} = 100 pF, I_{load} = 4 mA pull-up load to V_{CC}		380	450	ns
18.5	$t_{en\ DO\ tri\ H}$	DO enable time from tristate to high level	C_{DO} =100 pF, I_{load} = -1 mA pull-down load to GND		100	250	ns
18.6	$t_{dis\ DO\ H\ tri}$	DO disable time from high level to tristate	C_{DO} = 100 pF, I_{load} = -4 mA pull-down load to GND		380	450	ns
18.7	$t_{d\ DO}$	DO delay time	V_{DO} < 0.3 V_{CC}, V_{DO} > 0.7 V_{CC}, C_{DO} = 100 pF		50	250	ns

Table 18. CSN timing

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
19.1	$t_{CSN\_HI,stb}$	Minimum CSN HI time, switching from standby mode	Transfer of SPI-command to input register		20	50	µs
19.2	$t_{CSN\_HI,min}$	Minimum CSN HI time, active mode	Transfer of SPI-command to input register		2	4	µs

Figure 3. SPI - Transfer timing diagram

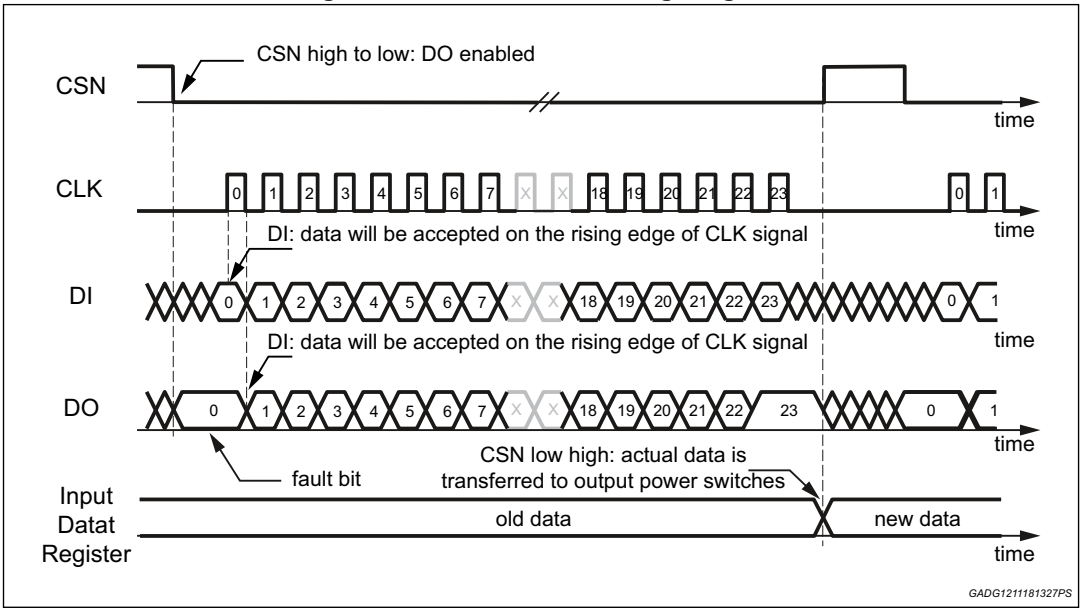


Figure 4. SPI - Input timing

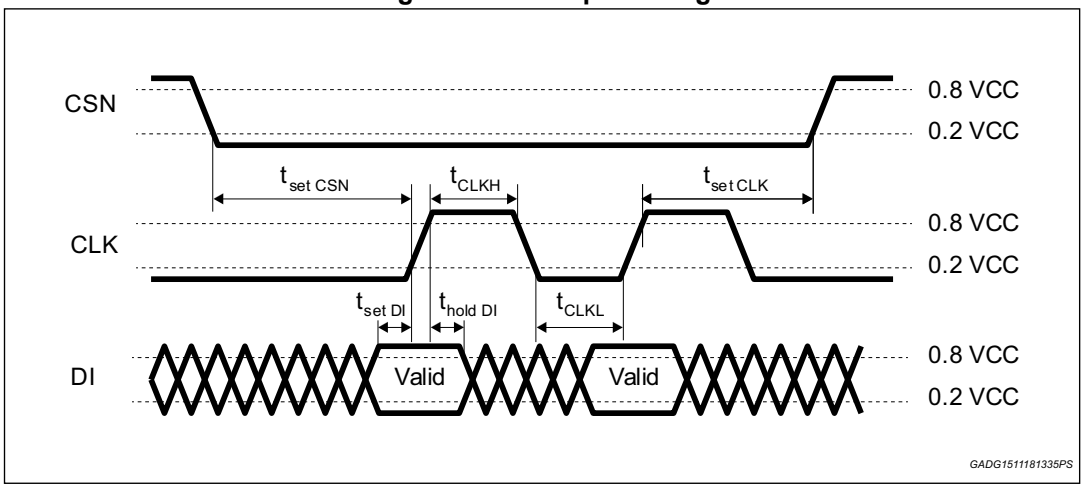


Figure 5. SPI - DO valid data delay time and valid time

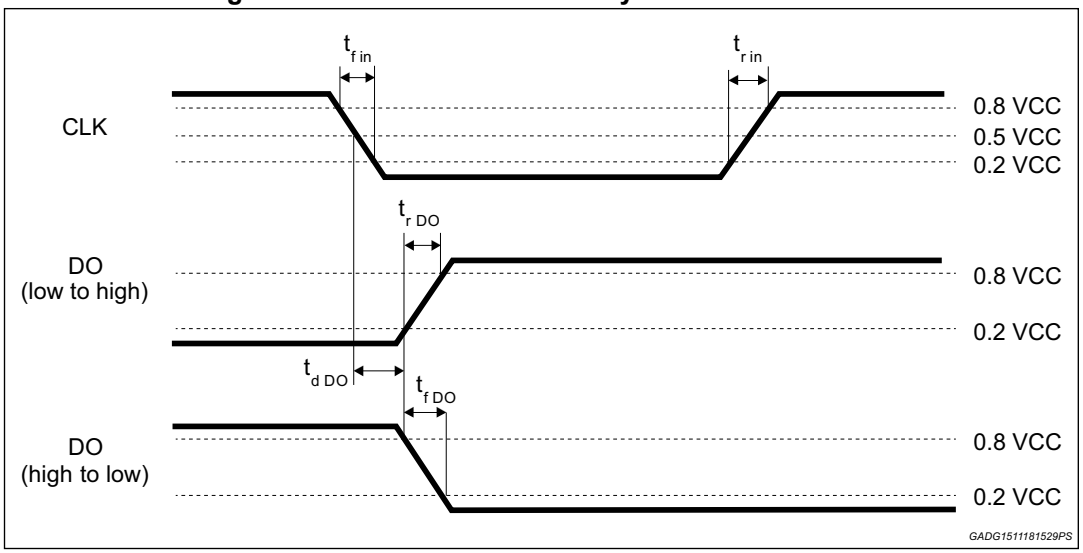


Figure 6. SPI - DO enable and disable time

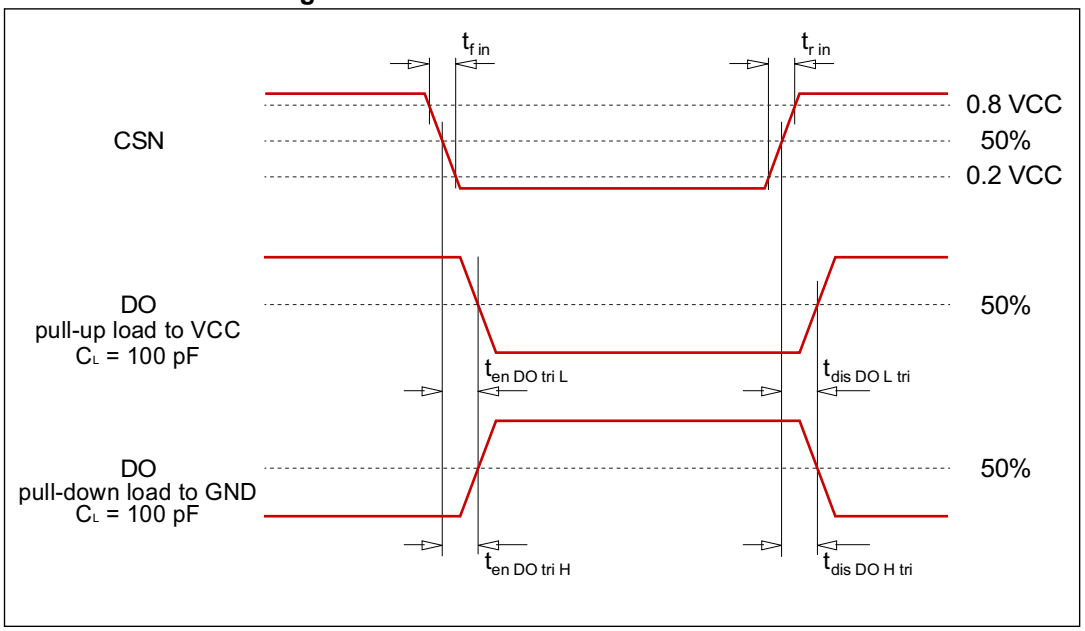
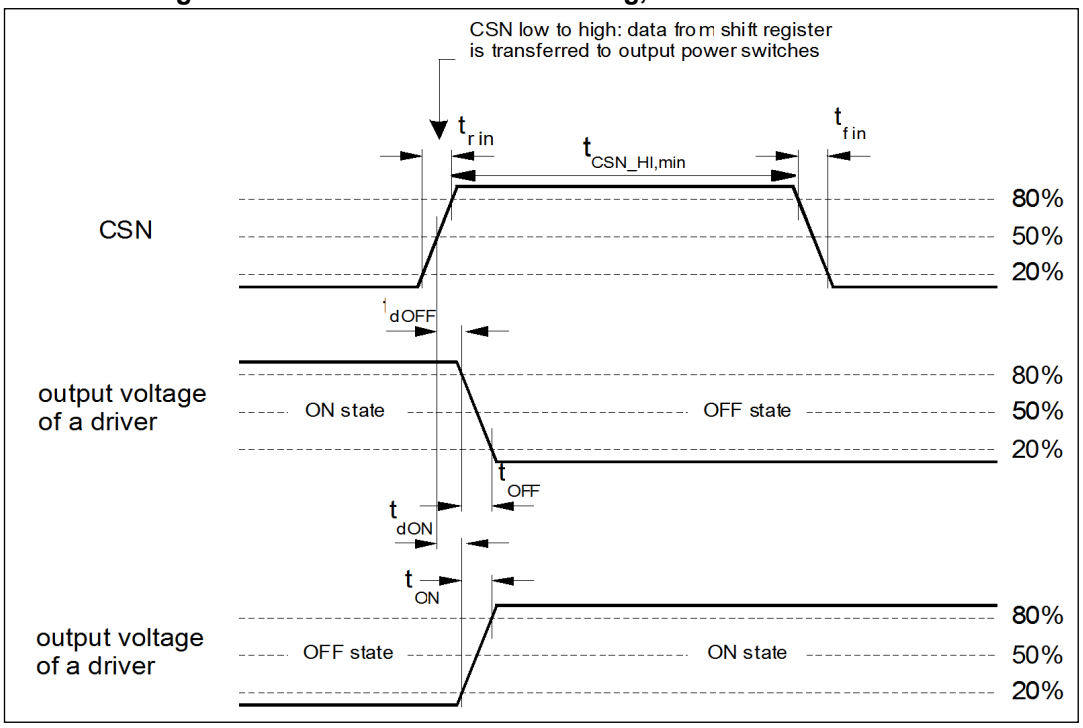


Figure 7. SPI - driver turn on/off timing, minimum CSN HI time



3 Application information

3.1 Dual power supply: V_S and V_{CC}

The power supply voltage V_S supplies the half bridges and the high-side drivers. An internal charge-pump is used to drive the high-side switches. The logic supply voltage V_{CC} is used for the logic part and the SPI of the device.

Due to the independent logic supply voltage the control and status information is not lost, if there are temporary spikes or glitches on the power supply voltage.

3.2 Wake up and active mode / standby mode

After power up of VS and Vcc the device operates in standby-mode. Pulling the signal CSN to low level wakes the device up and the analog part is activated (active mode).

After at least 10µs, the first SPI communication is valid and bit 0 of the Control Register 0 can be used to set the EN-mode. If bit 0 is not set to 1, the device doesn't remain in the active mode. After at least 256 µs all latched data are cleared and the inputs and outputs are switched to high impedance. In standby mode the current at V_S (V_{CC}) is less than 6 µA (5 µA) for CSN = high (DO in tristate).

3.3 Charge pump

In standby mode the charge-pump is turned off. After enabling the device by SPI command (bit0=1 Control Register 0) the oscillator starts and the voltage begins to increase. The output drivers are enabled after at least 256 µs after CSN went to high.

3.4 Diagnostic functions

All diagnostic functions (over/under-current, power supply over-/undervoltage, temperature warning and thermal shutdown) are internally filtered. The condition has to be valid for at least 32 µs (open load: 1 ms) before the corresponding status bit in the status registers is set.

The filters are used to improve the noise immunity of the device. The under-current and temperature warning functions are intended for information purpose and don’t change the state of the output drivers. On the contrary, the over-current condition disables the corresponding driver and thermal shutdown disables all drivers. Without setting the over-current recovery bits in the input data register, the microcontroller has to clear the over-current status bits to reactivate the corresponding drivers.

3.5 Overvoltage and undervoltage detection at V_S

If the power supply voltage VS rises above the overvoltage threshold $V_{SOV\ OFF}$ (typical 21 V), the outputs OUT1 to OUT11 are switched to high impedance state to protect the load. When the voltage VS drops below the undervoltage threshold $V_{SUV\ OFF}$ (UV-switch-OFF voltage), the output stages are switched to high impedance to avoid the operation of the power devices without sufficient gate driving voltage (increased power dissipation). If the

supply voltage V_S recovers (control register 3: bit 4=0) to normal operating voltage then the outputs stages return to the programmed state. If the undervoltage/overvoltage recovery disable bit is set (control register 3: bit 4=1), the automatic turn-on of the drivers is deactivated.

The microcontroller needs to clear the status bits to reactivate the drivers. It is recommended to set bit1 control register 3 to avoid a possible high current oscillation in case of a shorted output to GND and low battery voltage.

3.6 Overvoltage and undervoltage detection at V_{CC}

In case of power-on (VCC increases from undervoltage to $V_{POR\ OFF}$ = 2.9 V) the circuit is initialized by an internally generated power-on-reset (POR). If the voltage VCC decreases below the minimum threshold ($V_{POR\ ON}$ = 2.0 V), the outputs are switched to tristate (high impedance) and the status registers are cleared.

3.7 Temperature warning and thermal shutdown

If the junction temperature rises above $T_{j\ TW}$, a temperature warning flag is set after at least 32 µs and it can be read via the SPI. If the junction temperature increases above the second threshold $T_{j\ SD}$, the thermal shutdown bit is set and the power DMOS transistors of all output stages are switched off to protect the device after at least 32 µs.

The temperature warning and thermal shutdown flags are latched and the bits must be cleared by the microcontroller. This is possible only if the temperature has decreased below trigger temperature. If the thermal shutdown bit has been cleared the output stages are reactivated.

3.8 Inductive loads

Each half bridge is built by internally connected high-side and low-side power DMOS transistors. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs OUT1 to OUT6 without external free-wheeling diodes. The high-side drivers OUT7 to OUT11 are intended to drive resistive loads. Therefore only a limited energy (E<1 mJ) can be dissipated by the internal ESD-diodes in freewheeling condition. For inductive loads (L>100 µH) an external free-wheeling diode connected between GND and the corresponding output is required.

3.9 Open load detection

The open load detection monitors the load current in each activated output stage. If the load current is below the open load detection threshold for at least 1 ms (t_{dOL}) the corresponding open load bit is set in the status register. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3 ms) can be used to test the open load status without changing the mechanical/electrical state of the loads.

3.10 Over-load detection

In case of an over-current condition a flag is set in the status register in the same way as during open load detection. If the over-current signal is valid for at least t_{ISC}(typ) = 55 µs, the over-current flag is set and the corresponding driver is switched off to reduce the power dissipation and to protect the integrated circuit. If the over-current recovery bit of the output is zero, the microcontroller has to clear the status bits to reactivate the corresponding driver.

3.11 Current monitor

The current monitor output sources a current image at the current monitor output which has two fixed ratios of the instantaneous current of the selected high-side driver. Outputs with a resistance of 500 mΩ and higher have a ratio of 1/2000 and those with a lower resistance of 1/10000. The signal at output CM is blanked after switching on the driver until correct settlement of the circuitry (at least for 64 µs). The bits 0 to 3 of the control register 3 define which of the outputs are multiplexed to the current monitor output CM/PWM2. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open- or overload condition. For example it can be used to detect the motor state (starting, free-running, stalled). Moreover, it is possible to control the power of the defroster more precisely by measuring the load current. The current monitor output is bidirectional (PWM inputs).

3.12 PWM inputs

Each driver has a corresponding PWM enable bit, which can be programmed by the SPI interface. If the PWM enable bit is set in control registers 2 or 3, the output is controlled by the logically AND-combination of the PWM signal and the output control bit in Control Registers 0 and 1. The outputs OUT1-4, 6, 7, 9, OUT11 are controlled by the PWM1 input and the outputs OUT5, 8 and OUT10 are controlled by the bidirectional input CM/PMW2. For example, the two PWM inputs can be used to dim two lamps independently by external PWM signals. In case of switching off a high/low side switch in PWM mode a minimum off time of appr. (256 µs – td_{on}+td_{off}) is predefined by the state machine, to avoid switching on the high/low side again during the negative slope. For a PWM frequency of 100Hz this means the maximum duty cycle is about 98%. Larger duty cycles can be realized by applying pulse skipping.

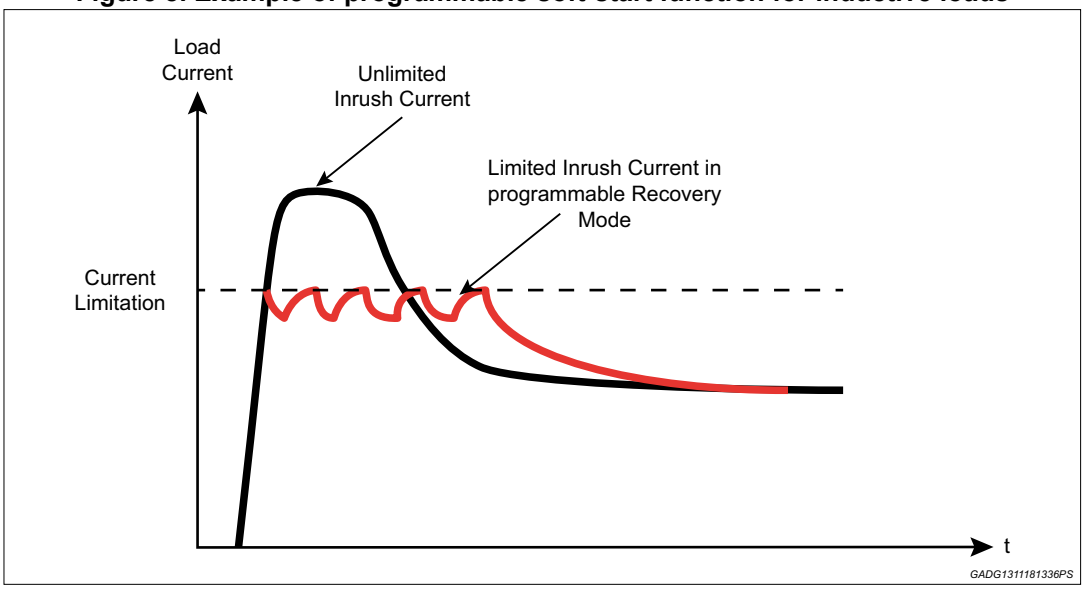
3.13 Cross-current protection

The six half bridges of the device are cross-current protected by an internal delay time. If one driver (LS or HS) is turned off, the activation of the other driver of the same half bridge is automatically delayed by the cross-current protection time. After the cross-current protection time is expired the slew-rate limited switch-off phase of the driver is changed to a fast turn-off phase and the opposite driver is turned-on with slew-rate limitation. Due to this behavior it is always guaranteed that the previously activated driver is completely turned off before the opposite driver starts to conduct.

3.14 Programmable soft-start function to drive loads with higher inrush current

Loads with start-up currents higher than the over-current limits (e.g. inrush current of lamps, start current of motors and cold resistance of heaters) can be driven by using the programmable softstart function (i.e. overcurrent recovery mode). Each driver has a corresponding over-current recovery bit. If this bit is set, the device automatically switches the outputs on again after a programmable recovery time. The duty cycle in over-current condition can be programmed by the SPI interface to about 12% or 25%. The PWM modulated current provides sufficient average current to power up the load (e.g. heat up the bulb) until the load reaches operating condition. The PWM frequency settles at 1.7 kHz and 3 kHz. The device itself cannot distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. For over-load detection the microcontroller can switch on the light bulbs by setting the over-current recovery bit for the first e.g. 50 ms. After clearing the recovery bit the output is automatically switched off, if the overload condition remains. This over-load detection procedure has to be followed in order make it possible to switch on the low-side driver of a bridge output, if the associated high-side driver has been used in recovery mode before.

Figure 8. Example of programmable soft-start function for inductive loads



4 Functional description of the SPI

4.1 General description

Standard ST-SPI Interface Version 3.0.

The SPI communication is based on a Serial Peripheral Interface structure using CSN (Chip Select Not), DI (Serial Data In), DO (Serial Data Out/Error) and CLK (Serial Clock) signal lines.

4.1.1 Chip Select Not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) is in high impedance state. A low signal wakes up the device and a serial communication can be started. The state when CSN is going low until the rising edge of CSN is called a communication frame.

Note: The device includes a test mode. This mode is activated by a dedicated sequence which includes a high voltage at the CSN pin. The CSN pin must be kept at nominal voltage levels in order to avoid accidental activation of the test mode.

4.1.2 Serial Data In (DI)

The input pin is used to transfer data serially into the device. The data applied to the DI is sampled at the rising edge of the CLK signal.

4.1.3 Serial Clock (CLK)

This input signal provides the timing of the serial interface. The Data Input (DI) is latched at the rising edge of Serial Clock CLK. The SPI can be driven by a micro controller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0. Data on Serial Data Out (DO) is shifted out at the falling edge of the serial clock (CLK). The serial clock CLK must be active only during a frame (CSN low). Any other switching of CLK close to any CSN edge could generate set up/hold violations in the SPI logic of the device.

The clock monitor counts the number of clock pulses during a communication frame (while CSN is low). If the number of CLK pulses does not correspond to the frame width indicated in the <SPI-frame-ID> (ROM address 03H) the frame is ignored and the *<frame error>* bit in the *<Global Status Byte>* is set.

Note: Due to this safety functionality, daisy chaining the SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

4.1.4 Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and goes from high impedance to a low or high level depending on the global status bit 7 (Global Error Flag). The first rising edge of the CLK input after a high to low transition of the CSN pin transfers the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK shifts the next bit out.

4.1.5 SPI communication flow

At the beginning of each communication the master can read the contents of the *<SPI-frame-ID>* register (ROM address 03H) of the slave device. This 8-bit register indicates the SPI frame length (24 bit) and the availability of additional features.

Each communication frame consists of a command byte which is followed by 2 data bytes.

The data returned on DO within the same frame always starts with the *<Global Status>* Byte. It provides general status information about the device. It is followed by 2 data bytes (i. e. '*In-frame-response*').

For Write cycles the *<Global Status>* Byte is followed by the previous content of the addressed register.

Figure 9. Write and read SPI

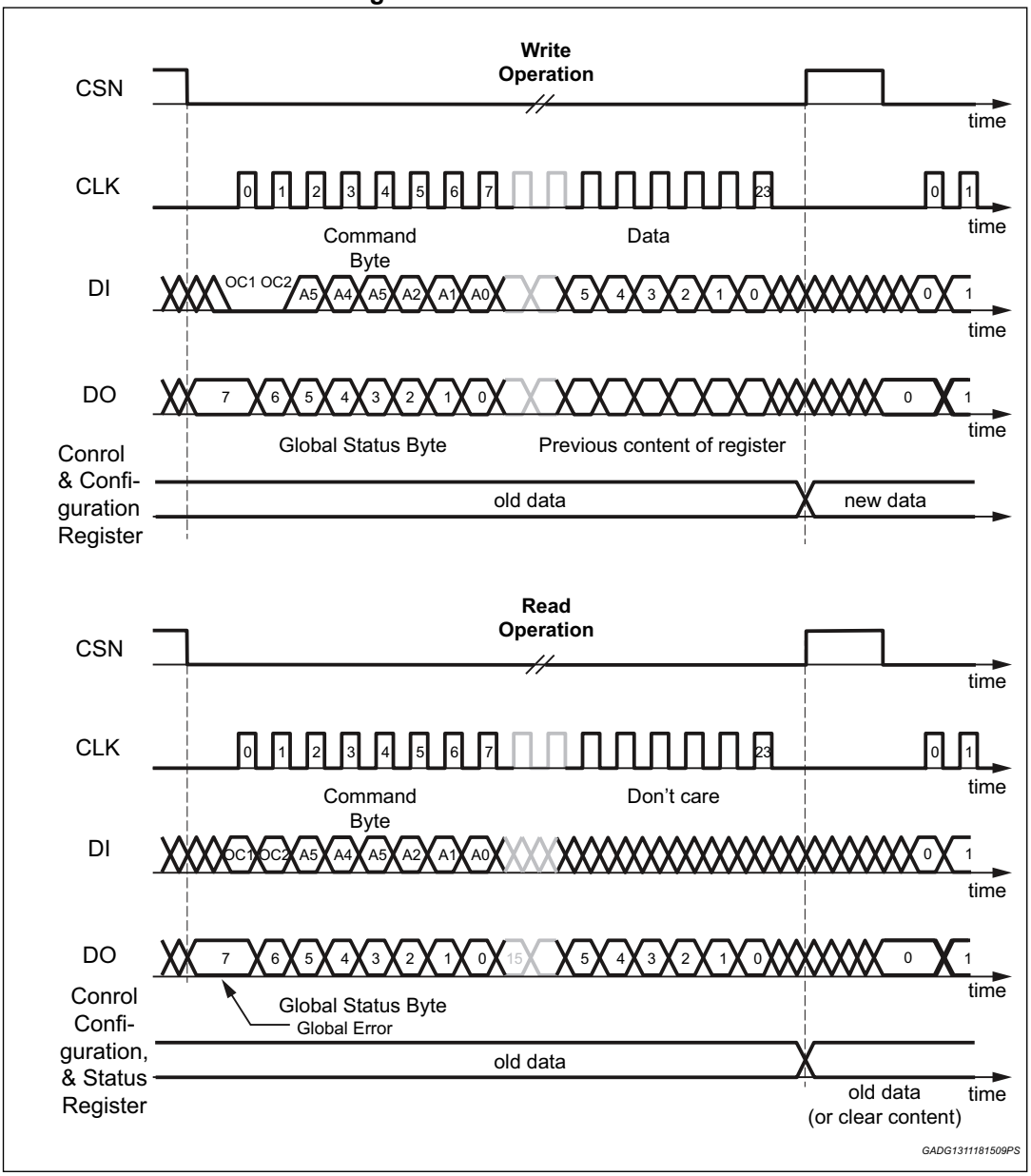


Table 19. SPI frame

	Command byte								Data byte															
Bit	23	22	21	29	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OC 1	OC0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

Ocx: Operation code

Ax: Address

Dx: Data Bit

4.2 Command byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (*<Read>, <Write>, <Read and Clear>, <Read Device Information>*) and a 6 bit address. If less than 6 address bits are required, the remaining bits are unused but are reserved.

4.2.1 Operation code definition

Table 20. Operation code definition

OC1	OC0	Meaning
0	0	<Write Mode>
0	1	<Read Mode>
1	0	<Read and Clear Mode>
1	1	<Read Device Information>

The <Write Mode> and <Read Mode> operations allow access to the RAM of the device.

A <Read and Clear Mode> operation is used to read a status register and subsequently clear its content.

The <Read Device Information> allows access to the ROM area which contains device related information such as <ID-Header>, <Product Code>, <Silicon Version and Category> and *<SPI-frame-ID>.*

4.3 Global status byte

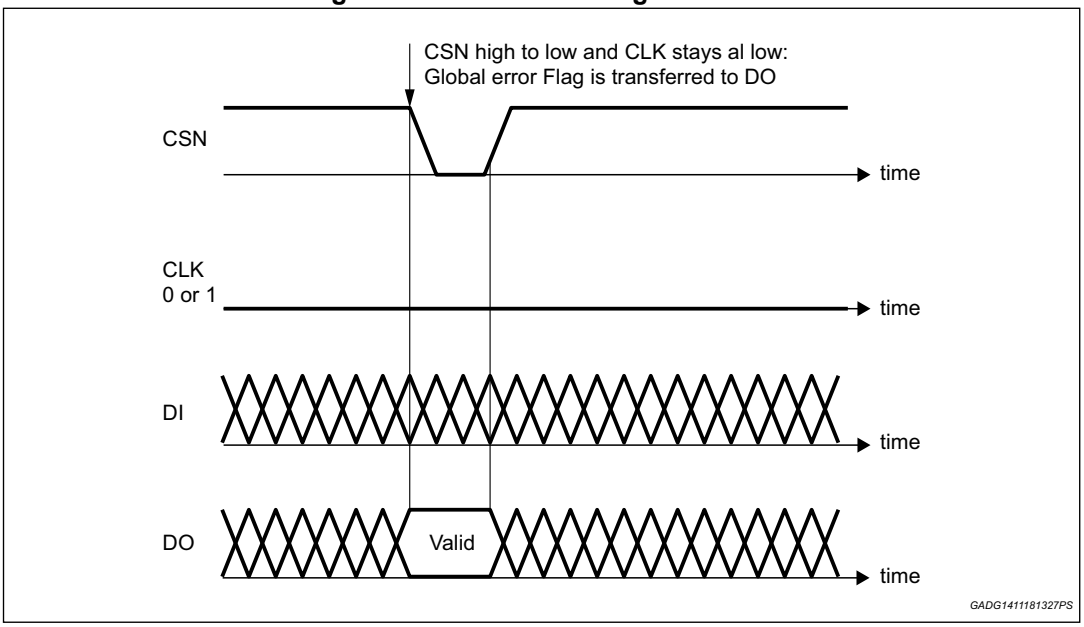
Table 21. Global status byte

Bit	7	6	5	4	3	2	1	0
Name	GL_ER	CO_ER	C_RESET	TSD	TW	UOV_OC	OL	NR
Reset	0	0	1	0	0	0	0	0

Description:

- GL_ER: Global Error Flag. Failures of Bits 0-6 are always linked to the Global Error Flag. This flag is generated by an OR combination of all failure events of the device. It is reflected via the DO pin while CSN is held low and no clock signal is available. The flag remains as long as CSN is low. This operation does not cause the Communication Error bit in the <Global Status> to be set. The signal TW bit3 and OL bit1can be masked.
- CO_ER: Communication Error. If the number of clock pulses within the previous frame is not 24 the frame is ignored and this bit is set.
- C_RESET: Chip RESET. If a stuck at '1' on input DI during any SPI frame occurs, or if a Power On Reset (VCC monitor) occurs. C_RESET resets ('1') with any SPI command. When C_RESET is active ('0'), the Gate drivers are switched off (resistive path to source).
  After a startup of the circuit the C_RESET is active because of the POR pulse and the Gate drivers are switched off. The Gate drivers can only be activated after the C_RESET has been reset with a SPI command.
- TSD: Thermal shutdown due to an internal sensor. All the gate drivers and the charge pump are switched off (resistive path to source). The TSD bit has to be cleared through a software reset to reactivate the gate drivers and the charge pump.
- TW: Thermal Warning. This bit is maskable by configuration register.
- UOV_OC: Logical OR among the filtered under-/over-voltage signals and over-current signals.
- OL: Open Load. Logical OR among the filtered under-current signals. This bit is maskable by configuration register.
- NR: Not Ready. After switching the device from standby mode to active mode an internal timer is started to allow charge-pump to settle before the outputs can be activated. This bit is cleared automatically after start up time has finished.

Figure 10. Global error flag definition



4.4 Address mapping

Table 22. RAM memory map

Address	Name	Access	Content
00h	Control register 0	Read/write	Enable of device and bridge control
01h	Control register 1	Read/write	High/low-side control and Electrocrome block set up
02h	Control register 2	Read/write	Bridge recovery mode and PWM set up and Electrocrome block set up
03h	Control register 3	Read/write	High-side recovery mode and PWM set up and current monitor selection
10h	Status register 0	Read only	Bridge over-current diagnosis
11h	Status register 1	Read only	Bridge open load (under-current) diagnosis
12h	Status register 2	Read only	Open load (under-current) diagnosis, VS and electrocrome diagnosis
3Fh	Configuration register	Read/write	Mask of bits in global status register and for global error bit

Table 23. ROM memory map

Address	Name	Access	Content
00h	ID header	Read only	4300h (ASSP ST_SPI)
01h	Version	Read only	0300h
02h	Product code 1	Read only	4300h (67 ST_SPI)
03h	Product code 2	Read only	4800h (H ST_SPI)
3Eh	SPI-frame ID	Read only	0200h SPI-Frame-ID register (ST_SPI)

5 SPI - control and status registers

5.1 Control register 0

Table 24. Control register 0 (read/write)

Bit	Name	Comment
15	OUT1 – HS on/off	If a bit is set the selected output driver is switched on. If the corresponding PWM enable bit is set the driver is only activated if PWM1 (PWM2) input signal is high. The outputs of OUT1-OUT6 are half bridges. If the bits of HS- and LS-driver of the same half bridge are set, the internal logic prevents that both drivers of this output stage can be switched on simultaneously in order to avoid a high internal current from Vs to GND.
14	OUT1 – LS on/off	
13	OUT2 – HS on/off	
12	OUT2 – LS on/off	
11	OUT3 – HS on/off	
10	OUT3 – LS on/off	
9	OUT4 – HS on/off	
8	OUT4 – LS on/off	
7	OUT5 – HS on/off	
6	OUT5 – LS on/off	
5	OUT6 – HS on/off	
4	OUT6 – LS on/off	
3	0	Reserved (has to be set to '0')
2	0	
1	0	
0	Enable bit	If enable bit is set the device will be switched in active mode. If enable bit is cleared, the device enters standby mode and all bits are cleared.

5.2 Control register 1

Table 25. Control register 1 (read/write)

Bit	Name	Comment				
15	OUT7 – HS1 on/off	OUT7/8				
14	OUT7 – HS2 on/off		HS1	HS2	Mode	
			1	1	Off	
13	OUT8 – HS1 on/off		1	0	Low on-resistance	
			0	1	High on-resistance	
12	OUT8 – HS2 on/off		0	0	Off	

Table 25. Control register 1 (read/write) (continued)

Bit	Name	Comment
11	OUT9 – HS on/off	If a bit is set, the selected output driver is switched on. If the corresponding PWM enable bit is set the driver is only activated if PWM1 (PWM2) input signal is high. The outputs of OUT1-OUT6 are half bridges. If the bits of HS- and LS-driver of the same half bridge are set, the internal logic prevents that both drivers of this output stage can be switched on simultaneously in order to avoid a high internal current from VS to GND.
10	OUT10 – HS on/off	
9	OUT11 – HS on/off	
8-1	Reserved	Reserved (has to be set to '0')
0	0	Reserved (has to be set to '0')

5.3 Control register 2

Table 26. Control register 2 (read/write)

Bit	Name	Comment
15	OUT1 – OCR enable	In case of an over-current event the over-current status bit (Status Register 0) is set and the output is switched off. If the Over-current Recovery Enable bit (OCR) is set, the output will be automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle (bit 5 of control register 3). Depending on occurrence of over-current event and internal clock phase it is possible that one recovery cycle is executed even if this bit is set to zero.
14	OUT2 – OCR enable	
13	OUT3 – OCR enable	
12	OUT4 – OCR enable	
11	OUT5 – OCR enable	
10	OUT6 – OCR enable	
9	0	Reserved (has to be set to '0')
8	0	Reserved (has to be set to '0')
7	OUT1 PWM1 enable	If the PWM1/2 Enable bit is set and the output is enabled (control register 0 or 1) the output is switched on if PWM1/2 input is high and switched off if PWM1/2 input is low. OUT5, 8 and OUT10 are controlled by PWM2 input, all other outputs are controlled by PWM1 input.
6	OUT2 PWM1 enable	
5	OUT3 PWM1 enable	
4	OUT4 PWM1 enable	
3	OUT5 PWM2 enable	
2	OUT6 PWM1 enable	
1	Reserved	
0	Reserved	Reserved

5.4 Control register 3

Table 27. Control register 3 (read/write)

<table>
<tr><th>Bit</th><th>Name</th><th>Comment</th></tr>
<tr><td>15</td><td>OUT7-OCR enable</td><td rowspan="5">In case of an over-current event the over-current status bit (Status register 1) is set and the output is switched off. If the Over-current Recovery Enable bit (OCR) is set the output will be automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle (bit 5). Depending on the occurrence of the over-current event and the internal clock phase it is possible that one recovery cycle is executed even if this bit is set to zero.</td></tr>
<tr><td>14</td><td>OUT8-OCR enable</td></tr>
<tr><td>13</td><td>OUT9-OCR enable</td></tr>
<tr><td>12</td><td>OUT10-OCR enable</td></tr>
<tr><td>11</td><td>OUT11-OCR enable</td></tr>
<tr><td>10</td><td>OUT7 PWM1 enable</td><td rowspan="5">If the PWM1/2 Enable bit is set and the output is enabled (control register 0 or 1) the output is switched on if PWM1/2 input is high and switched off if PWM1/2 input is low. OUT5, 8 and OUT10 are controlled by PWM2 input all other outputs are controlled by PWM1 input.</td></tr>
<tr><td>9</td><td>OUT8 PWM2 enable</td></tr>
<tr><td>8</td><td>OUT9 PWM1 enable</td></tr>
<tr><td>7</td><td>OUT10 PWM2 enable</td></tr>
<tr><td>6</td><td>OUT11 PWM1 enable</td></tr>
<tr><td>5</td><td>OCR frequency
0: 1.7 kHz
1: 3 kHz</td><td>This bit defines in combination with the over-current recovery bit (Input Register 1) the over-current recovery frequency of an activated driver.</td></tr>
<tr><td>4</td><td>OV/UVR disable</td><td>If this bit is set the microcontroller has to clear the status register after undervoltage/overvoltage event to enable the outputs.</td></tr>
<tr><td>3</td><td>CM select bit 3</td><td rowspan="4">Depending on combination of bit 3 to 0 the current image of the selected high-side output OUTn will be multiplexed to the CM/PWM2 output (see table below).
Other combinations deactivate the current monitor.

<table><tr><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Current image of</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>OUT1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>OUT2</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>OUT3</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>OUT4</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>OUT5</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>OUT6</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>OUT7</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>OUT8</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>OUT9</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>OUT10</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>OUT11</td></tr></table></td></tr>
<tr><td>2</td><td>CM select bit 2</td></tr>
<tr><td>1</td><td>CM select bit 1</td></tr>
<tr><td>0</td><td>CM select bit 0</td></tr>
</table>

5.5 Status register 0

Table 28. Status register 0 (read)

Bit	Name	Comment
15	OUT1 – HS OC	In case of an over-current event the corresponding status bit is set and the output driver is disabled. If the over-current Recovery Enable bit is set the output will be automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle. If the over-current recovery bit is not set, the micro controller has to clear the over-current bit to reactivate the output driver.
14	OUT1 – LS OC	
13	OUT2 – HS OC	
12	OUT2 – LS OC	
11	OUT3 – HS OC	
10	OUT3 – LS OC	
9	OUT4 – HS OC	
8	OUT4 – LS OC	
7	OUT5 – HS OC	
6	OUT5 – LS OC	
5	OUT6 – HS OC	
4	OUT6 – LS OC	
3	0	Reserved
2	0	
1	0	
0	0	

5.6 Status register 1

Table 29. Status register 1 (read)

Bit	Name	Comment
15	OUT1 – HS UC	Maskable by the configuration register
14	OUT1 – LS UC	
13	OUT2 – HS UC	The open load detection monitors the load current in each activated output stage. If the load current is below the under-current detection threshold for at least 1 ms (t_{dOL}), the corresponding under-current bit UC is set. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3ms) can be used to test the open load status without changing the mechanical/electrical state of the loads.
12	OUT2 – LS UC	
11	OUT3 – HS UC	
10	OUT3 – LS UC	
9	OUT4 – HS UC	
8	OUT4 – LS UC	
7	OUT5 – HS UC	
6	OUT5 – LS UC	
5	OUT6 – HS UC	
4	OUT6 – LS UC	

Table 29. Status register 1 (read) (continued)

Bit	Name	Comment
3	0	Reserved
2	0	
1	0	
0	0	

5.7 Status register 2

Table 30. Status register 2 (read)

Bit	Name	Comment
15	OUT7 – OC	In case of an over-current event the corresponding status bit OC is set and the output driver is disabled. If the over-current recovery enable bit is set the output will be automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle. If the over-current recovery bit is not set the micro controller has to clear the over-current bit to reactivate the output driver. The open load detection monitors the load current in each activated output stage. If the load current is below the under-current detection threshold for at least 1 ms (t_{dOL}) the corresponding under-current bit UC is set. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3 ms) can be used to test the open load status without changing the mechanical/electrical state of the loads.
14	OUT7 – UC	
13	OUT8 – OC	
12	OUT8 – UC	
11	OUT9 – OC	
10	OUT9 – UC	
9	OUT10 – OC	
8	OUT10 – UC	
7	OUT11 – OC	
6	OUT11 – UC	
5	Reserved	
4	Reserved	
3	VS under-voltage	In case of an over-voltage or under-voltage event the corresponding bit is set and the outputs are deactivated. If VS voltage recovers to normal operating conditions outputs are reactivated automatically (if bit 4 of control register 3 is not set).
2	VS over-voltage	
1	0	Reserved
0	0	

5.8 Configuration register

Table 31. Configuration register (read/write)

Bit	Name	Comment
15	0	Reserved (has to be set to '0')
14	0	
13	0	
12	0	
11	0	
10	0	
9	0	
8	0	
7	0	
6	0	
5	Mask for bit 15 of status reg. 1	Open-load event (under-current status bit of OUT1 HS) is not considered in open-load bit 1 of global status register.
4	Mask for bit 14 of status reg. 1	Open-load event (under-current status bit of OUT1 LS) is not considered in open-load bit 1 of global status register.
3	Mask for bit 3 of global status reg.	Temperature warning event is not considered in the 'Global Error Flag'.
2	0	Reserved (has to be set to '0')
1	Mask for bit 1 of global status reg.	Open-load event (under-current status bit of OUTn) is not considered in the 'Global Error Flag'.
0	0	Reserved (has to be set to '0')

6 Package and PCB thermal data

6.1 PowerSSO-36 thermal data

Figure 11. PowerSSO-36 2 layer PCB

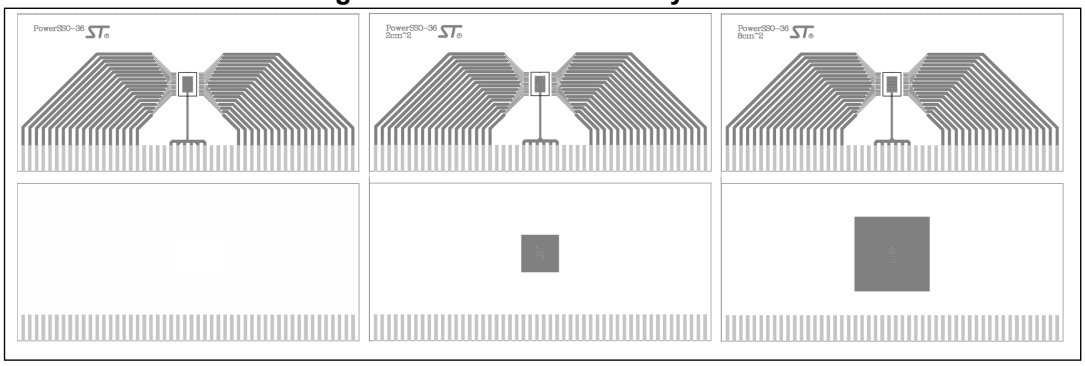
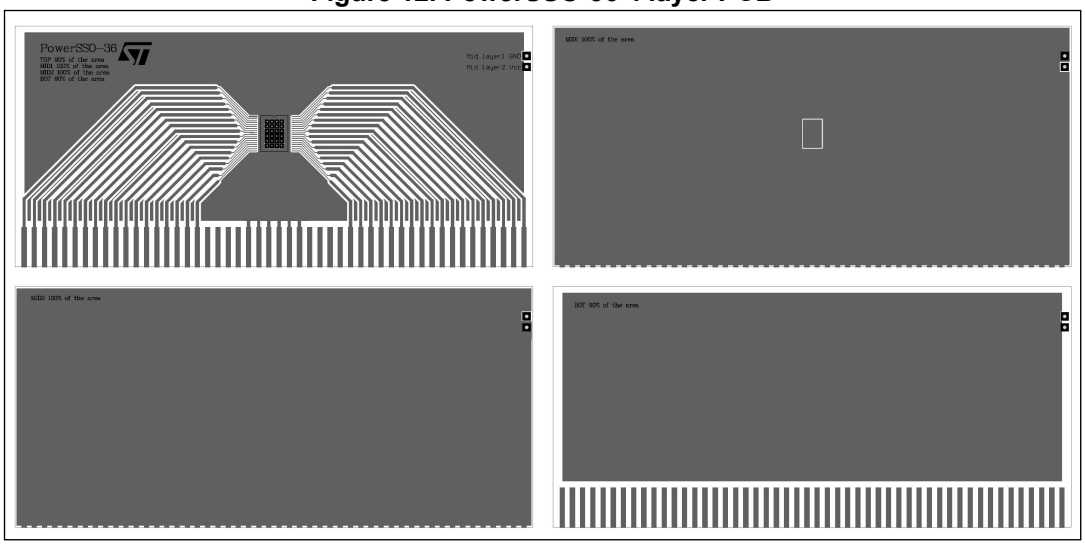
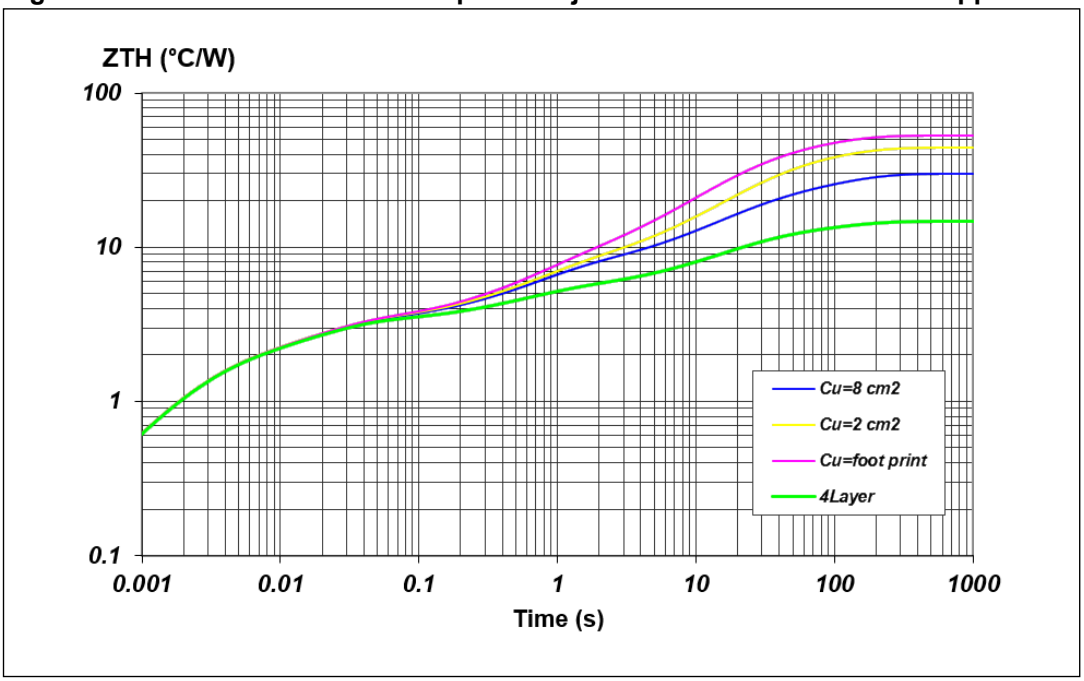


Figure 12. PowerSSO-36 4 layer PCB



Note: Layout condition of R_{th} and Z_{th} measurements (board finish thickness 1.6 mm ±10%, board double layer and four layers, board dimension 129 mm x 60 mm, board material FR4, Cu thickness 0.070 mm (outer layers), Cu thickness 0.035 mm (inner layers), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm ±0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 4.1 mm x 6.5 mm). 4-layer PCB: Cu on mid1 and mid2 layer: 76.45 cm^2. Cu on bottom layer: 68.8 cm^2. Z_{th} measured on the major power dissipator contributor.

Figure 13. PowerSSO-36 thermal impedance junction to ambient vs PCB copper area



7 Package and packing information

7.1 ECOPACK

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK is an ST trademark.

7.2 PowerSSO-36 package information

Figure 14. PowerSSO-36 package dimensions

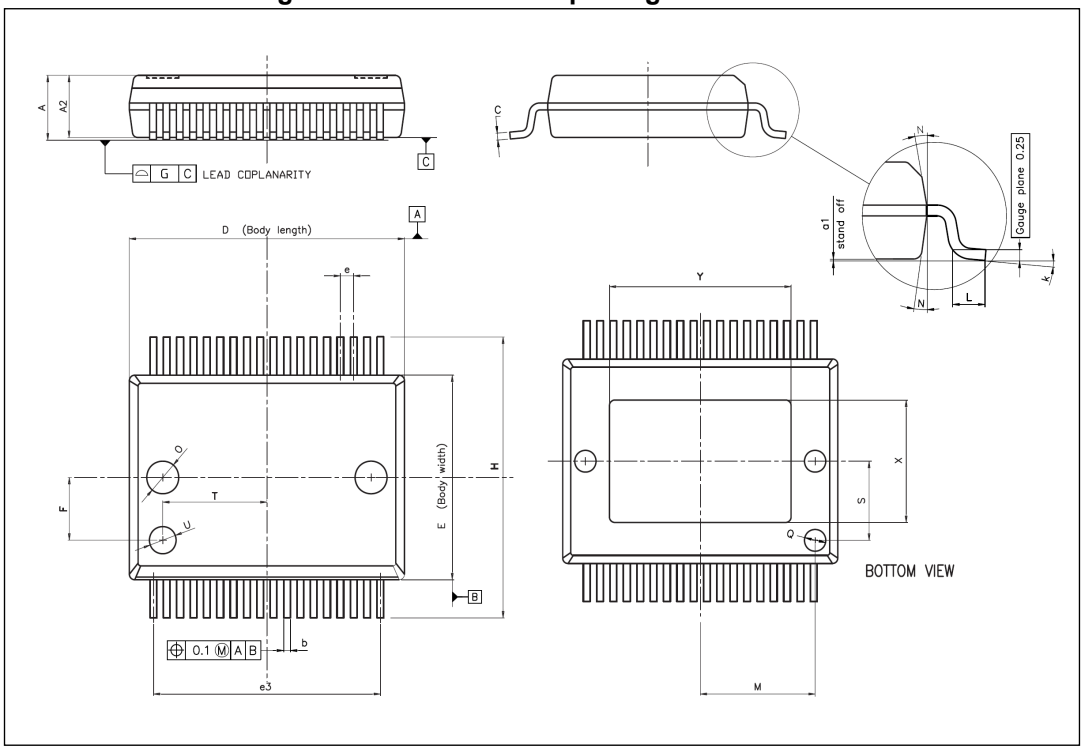


Table 32. PowerSSO-36 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	-	-	2.45
A2	2.15	-	2.35
a1	0	-	0.1
b	0.18	-	0.36
c	0.23	-	0.32
D(1)	10.10	-	10.50

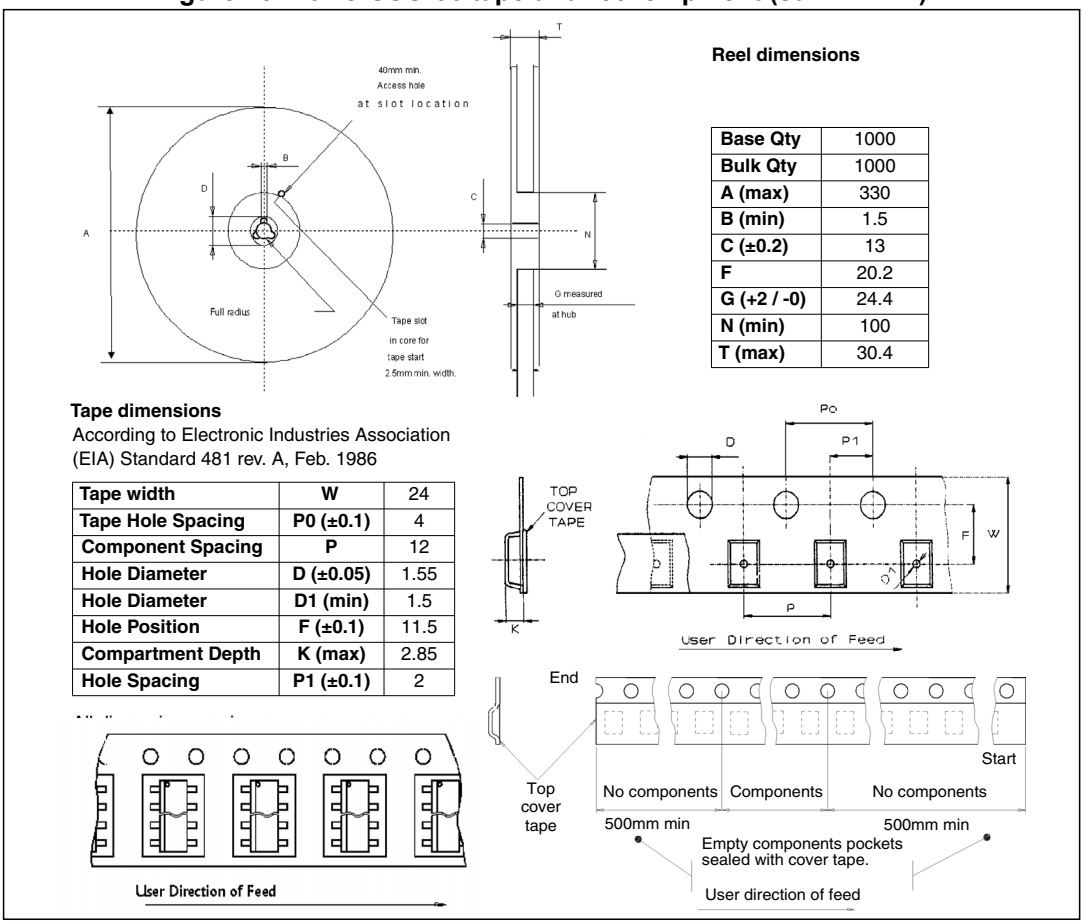
Table 32. PowerSSO-36 mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
E	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
F	-	2.3	-
G	-	-	0.1
G1	-	-	0.06
H	10.1	-	10.5
h	-	-	0.4
k	0°	-	8°
L	0.55	-	0.85
M	-	4.3	-
N	-	-	10°
O	-	1.2	-
Q	-	0.8	-
S	-	2.9	-
T	-	3.65	-
U	-	1	-
X	4.3	-	5.2
Y	6.9	-	7.5

1. “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side (0.006”).

7.3 PowerSSO-36 packing information

Figure 15. PowerSSO-36 tape and reel shipment (suffix “TR”)



Reel dimensions

Base Qty	1000
Bulk Qty	1000
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (±0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (±0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (±0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (±0.1)**	2

8 Revision history

Table 33. Document revision history

Date	Revision	Description of changes
18-Sep-2018	1	Initial release.
07-Nov-2018	2	Added *Section 6: Package and PCB thermal data*.
17-Jun-2019	3	Updated the maturity from target specification to production data.
08-Oct-2019	4	Updated *Applications* on cover page. Updated *Table 2: Pin definition and functions*. Updated *Section 4.1.1: Chip Select Not (CSN)* and *Section 4.3: Global status byte*. Minor text changes

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