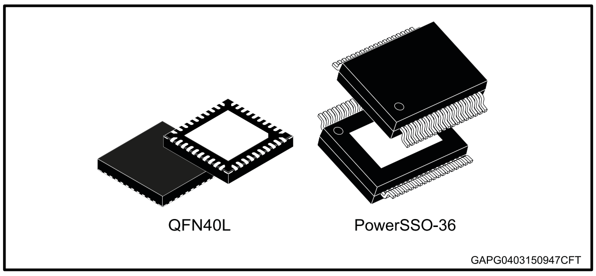
L99SM81V

Programmable stepper motor driver for automotive applications with micro-stepping and stall detection

Datasheet - Production data



Features

- AEC-Q100 qualified
- Stepper motor driver with up to 1.35 A current capability
- Programmable Step mode:
  - Full step, Half step, Mini step, 1/8 Micro step, 1/16 Micro step
- Current regulation by integrated PWM control with fully integrated current sensing
- Equivalent 10 bit resolution on current regulation loop:
  - Two 4-bit programmable full scale current amplitudes: one for RUN and one for HOLD mode
  - 6-bit DAC for reference current generation (whatever programmed full scale amplitude)
- 4 programmable decay modes:
  - Slow-mode, mixed-mode and 2x automatically selected decay-modes
- 3x programmable inputs for direct control of step clock, direction, hold and step modes
- 1x programmable analog output for T_j measurement or band-gap reference
- 2x programmable digital outputs for internally generated PWM ON duty cycles, error signals, coils voltage measurement synchronization signals
- Programmable MOSFETs switching speed: four options for EMC and power dissipation trade-off optimization
- PWM frequency wobbling for reduction of conducted EM energy
- Outputs protection and diagnosis (open load, short to battery, short to GND)
- Integrated ADC for coil voltage measurement and stall detection
- 5 V low drop voltage regulator short-circuit protected
- Very low current consumption in standby mode (typ. 10 µA)
- Thermal warning and shutdown
- ST SPI 4.1 interface for control and diagnostics

Applications

Bipolar 2 phase stepper motor driver for automotive applications like adaptive front light systems or projectors for head-up displaying

Description

The L99SM81V is an automotive grade integrated driver for bipolar two-phase stepper motors capable of current controlled micro-stepping with programmable amplitude. The device features a 5 V voltage regulator to supply external sensors.

The integrated Serial Peripheral Interface (SPI) makes it possible to adjust device parameters, control all operating modes and read out diagnostic information. Digital I/Os are also optionally usable for more flexible and reliable application control.

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1 Block diagram and pin description

Figure 1: Block diagram (QFN40L)

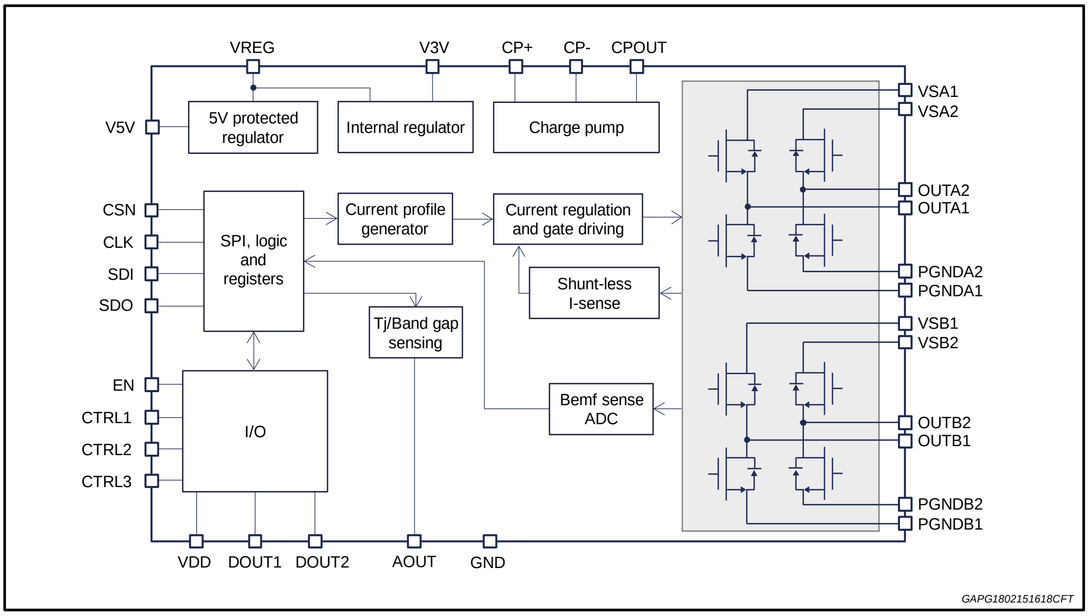


Figure 2: Block diagram (PowerSSO-36)

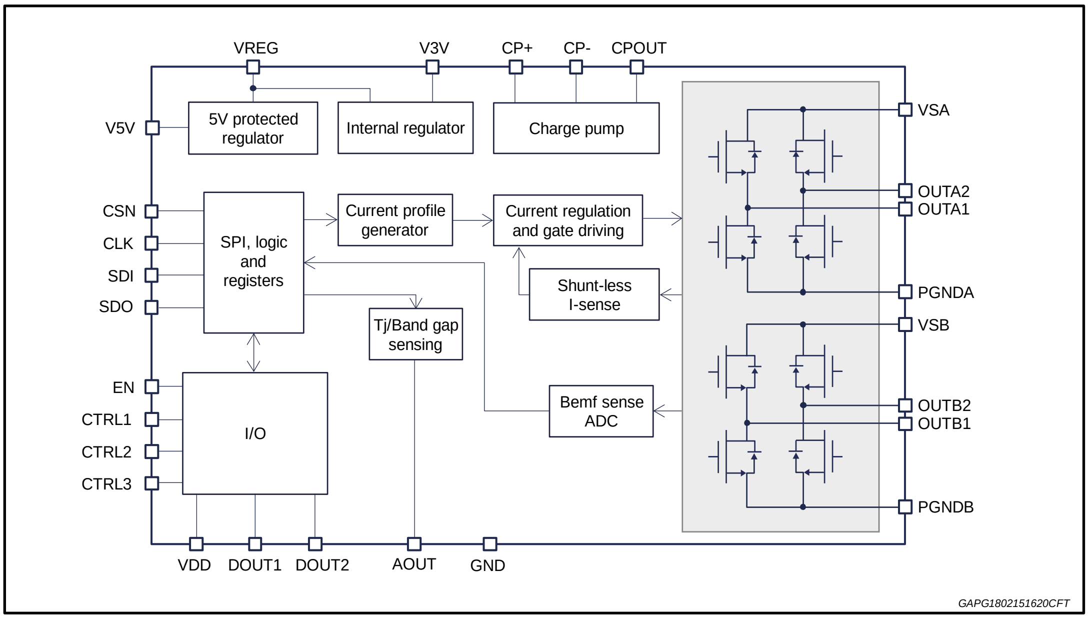


Figure 3: QFN40 pin connections (top view)

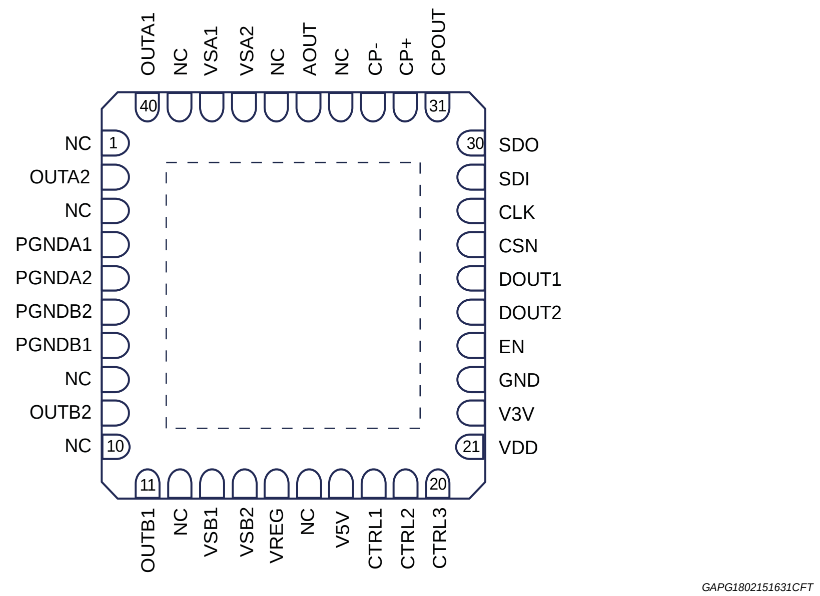
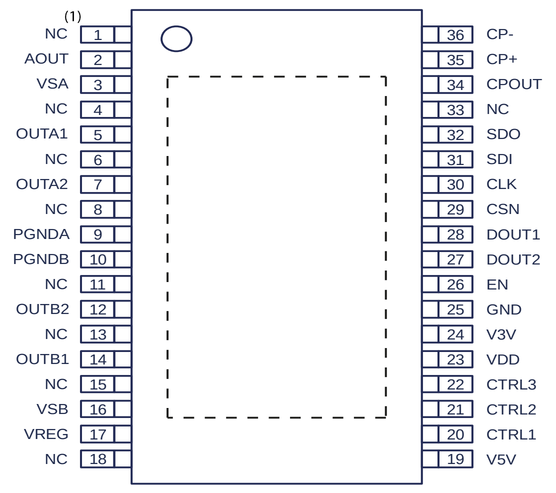


Figure 4: PSSO36 pin connections (top view)



(1) Pin 1 is connected to the slug. Slug connection to GND is recommended.

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Table 1: Pin definition and function

Symbol	Function	I/O Type
NC	Not connected	—
OUTA1	Output of leg 1 of H-Bridge A	O
OUTA2	Output of leg 2 of H-Bridge A	O
PGNDAn	Power ground for leg n of H-Bridge A (QFN40 option only; n = 1,2)	PGND
PGNDA	Power ground for H-Bridge A (PSSO36 only)	PGND

Symbol	Function	I/O Type
PGNDBn	Power ground for leg n of H-Bridge B (QFN40 option only; n = 1,2)	PGND
PGNDB	Power ground for H-Bridge B (PSSO36 option only)	PGND
OUTB2	Output of leg 2 of H-Bridge B	O
OUTB1	Output of leg 1 of H-Bridge B	O
VSBn	Supply voltage for leg n of H-Bridge B (QFN40 option only; n = 1,2)	Supply
VSB	Supply voltage for H-Bridge B (PSSO36 option only)	Supply
VSAn	Supply voltage for leg n of H-Bridge A (QFN40 option only; n = 1,2)	Supply
VSA	Supply voltage for H-Bridge A (PSSO36 option only)	Supply
CTRL3	Configurable control pin 3	I
CTRL2	Configurable control pin 2	I
CTRL1	Configurable control pin 1	I
VREG	Supply voltage for 5 V regulator	Supply
V5V	5 V regulator output	O
VDD	Digital I/Os supply	Supply
V3V	Internal 3V regulator decoupling output	O
GND	GND connection	GND
EN	Enable input	I
DOUT2	Configurable digital output 2	O
DOUT1	Configurable digital output 1	O
CSN	SPI chip select NOT input	I
CLK	SPI serial clock input	I
SDI	SPI serial data input	I
SDO	SPI serial data output	O
CPOUT	Charge pump output	O
CP+	Charge pump pin for capacitor, positive side	O
CP-	Charge pump pin for capacitor, negative side	O
AOUT	Analog Output	O

2 Device description

2.1 Supply pins (VS, VREG, VDD)

The device has three different supply input pins:

- VSx pins are used to supply the four H-bridges, VSA pin(s) is (are) also used to supply the charge pump. All of VS pins must be protected against negative voltages.
- VREG pin supplies the embedded 5 V LDO regulator and the 3.3 V regulator supplying internal logic. It must be protected against negative voltages
- VDD supplies all of the digital I/Os, it is intended to be equal to the voltage used to supply the application micro-controller; both 3.3 V and 5 V are supported.

2.2 Voltage regulator (V5V)

The device integrates a low-drop voltage regulator capable of supplying external devices (e.g. external sensors) with a continuous load current up to 50 mA. The output voltage is stable with ceramic output capacitors equal to 220 nF or bigger, placed close to the device. The voltage regulator is protected against short circuit to both GND and battery (for the latter, VREG must be present).

2.3 Charge Pump (CP)

L99SM81V embeds a single stage charge pump which requires a ‘flying’ external ceramic capacitor placed in between pins CP+ and CP- and an additional ceramic capacitor on pin CP. The charge pump operation is internally monitored and a condition that avoids proper operation of the charge pump will be indicated by the respective SPI diagnosis flag. The charge pump frequency can be modulated with a wobble frequency generator to optimize EMC performance.

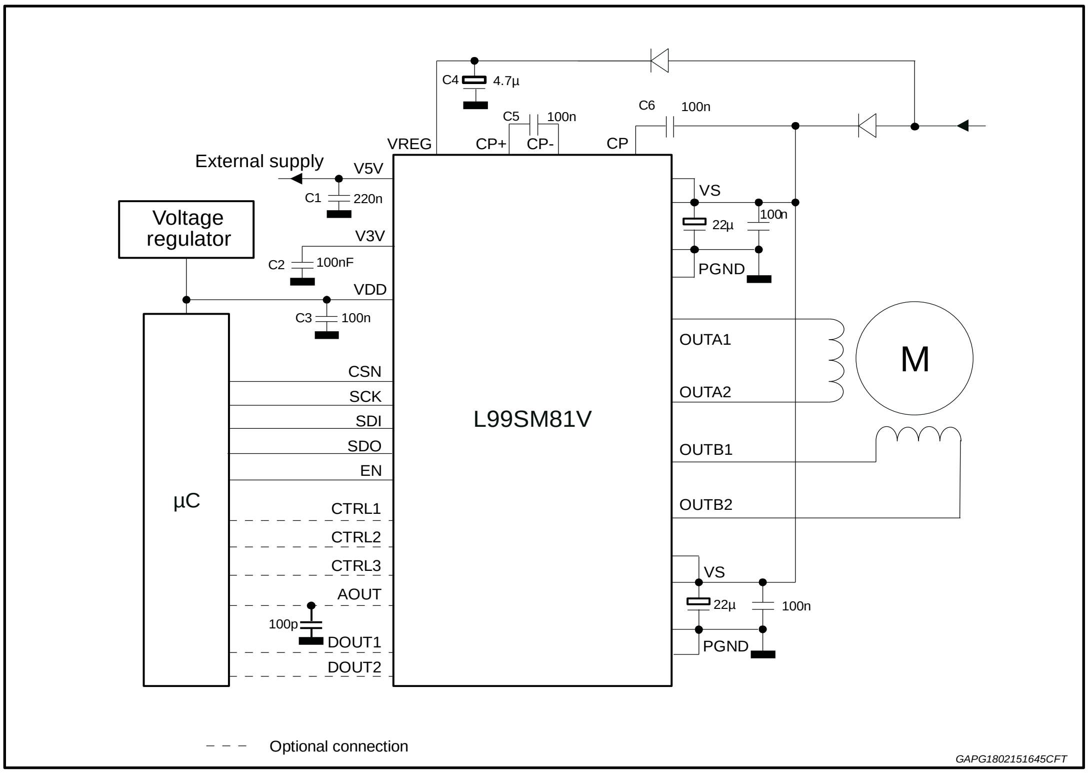
2.4 Standby mode (EN)

The EN input has an internal pull-down resistor. The device is in standby mode if EN input is set to logic low level. In this case the voltage regulator, the charge pump and all of the outputs are turned off, registers content is also set to default value.

If EN is set to logic high level then the device enters the active mode after a start-up time equal to t_{START}. In active mode all functions are available and the device is controlled by the ST SPI interface and the digital control pins.

2.5 Application block diagram

Figure 5: Stepper motor driver application block diagram



As it can be seen from the application block diagram, the device may be driven either by Serial Peripheral Intreface (SPI) or by digital inputs/outputs.

2.6 Stepping modes and step update

Depending on desired step resolution - as shown in *Figure 6: "Electrical revolution in 1/16th micro step (current profile and phase counter values)"* to *Figure 10: "Electrical revolution in full step mode (current profiles and phase counter values)"* - one stepper motor electrical cycle can consist of 64 micro steps (1/16th micro step mode), 32 micro steps (1/8th micro step mode), 16 mini steps (mini step mode), 8 half steps (half step mode) or 4 full steps (full step mode).

Figure 6: Electrical revolution in 1/16th micro step (current profile and phase counter values)

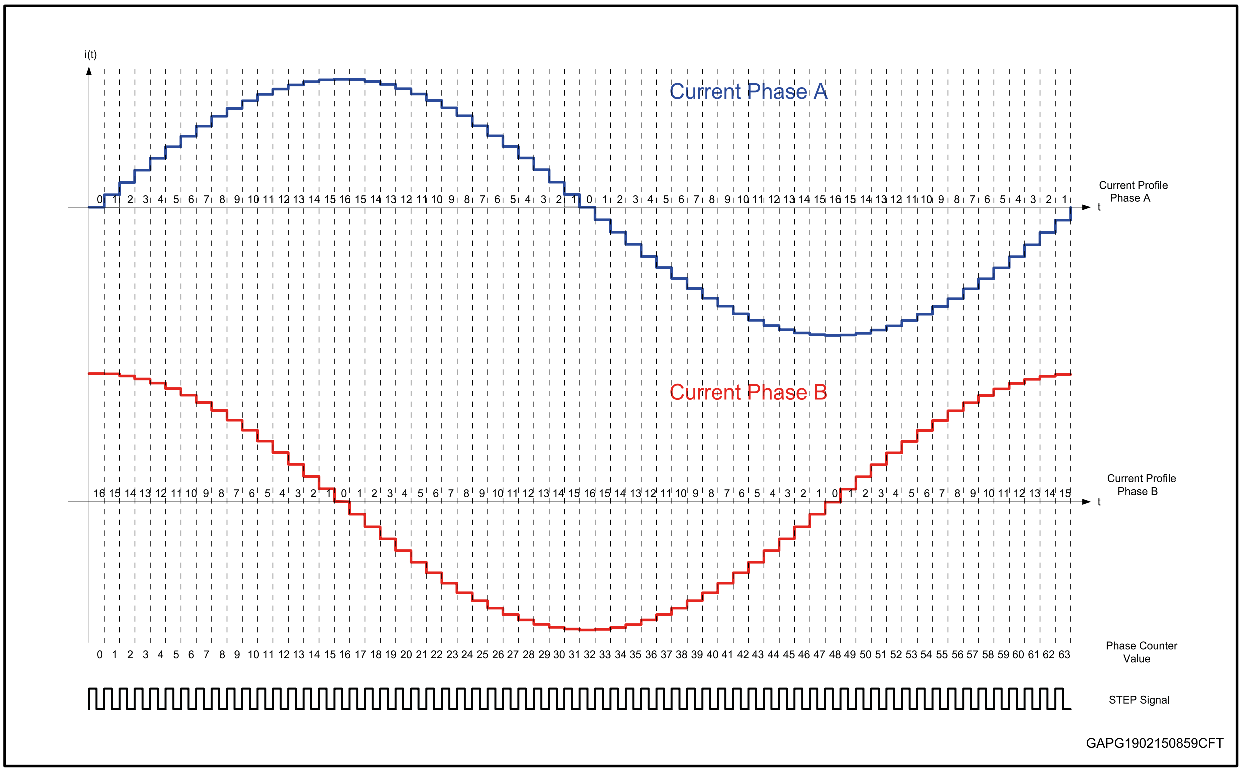


Figure 7: Electrical revolution in 1/8th micro step (current profile and phase counter values)

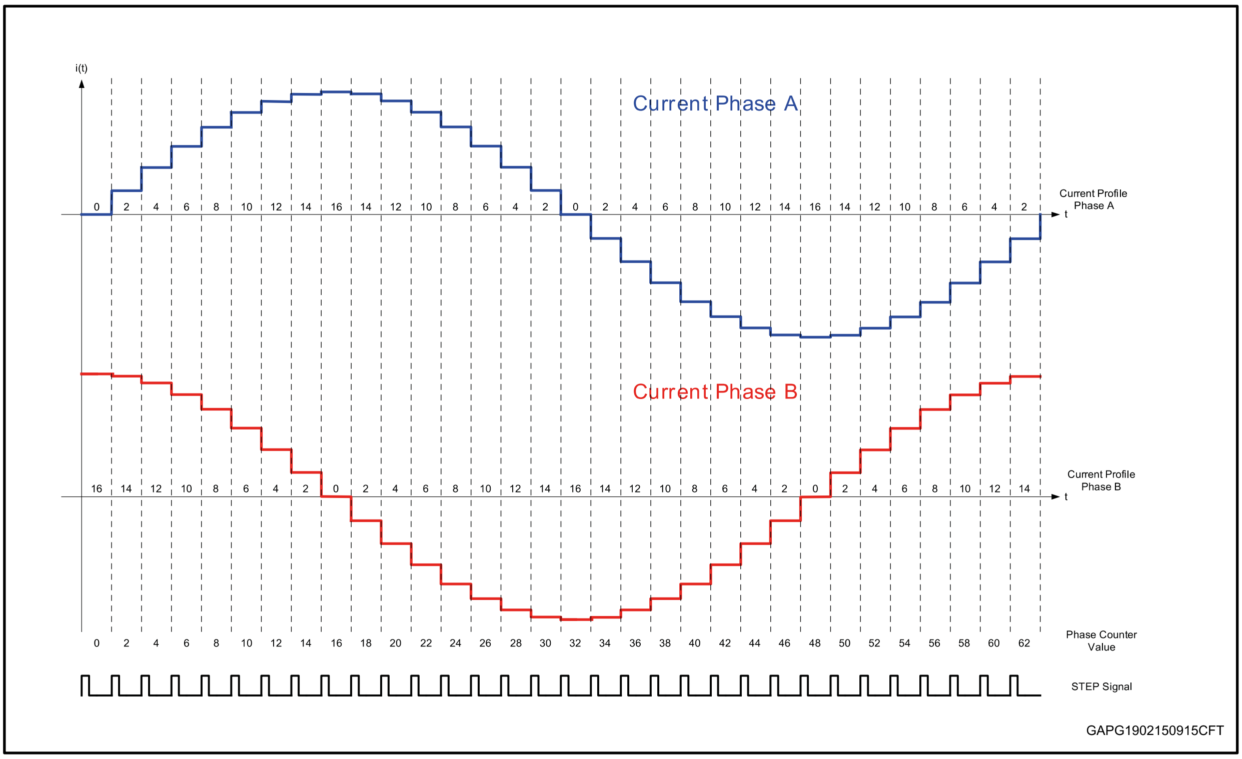


Figure 8: Electrical revolution in mini step (current profiles and phase counter values)

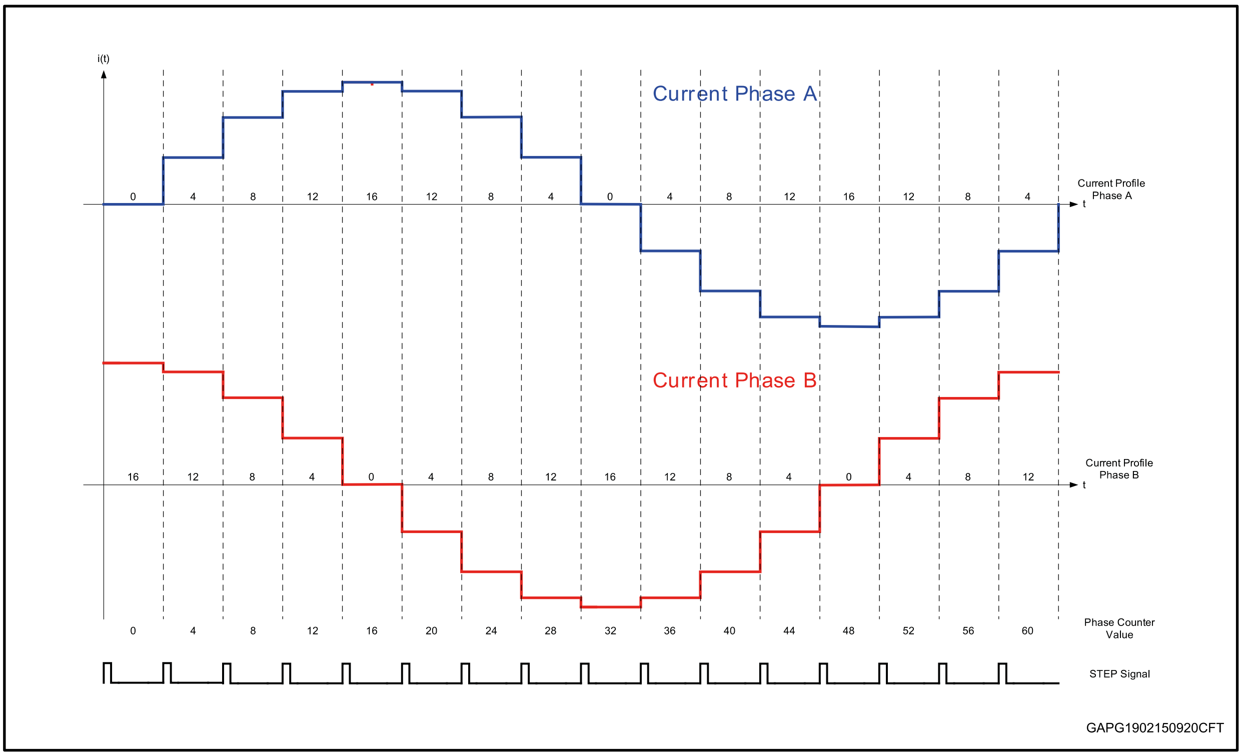


Figure 9: Electrical revolution in half step (current profiles and phase counter values)

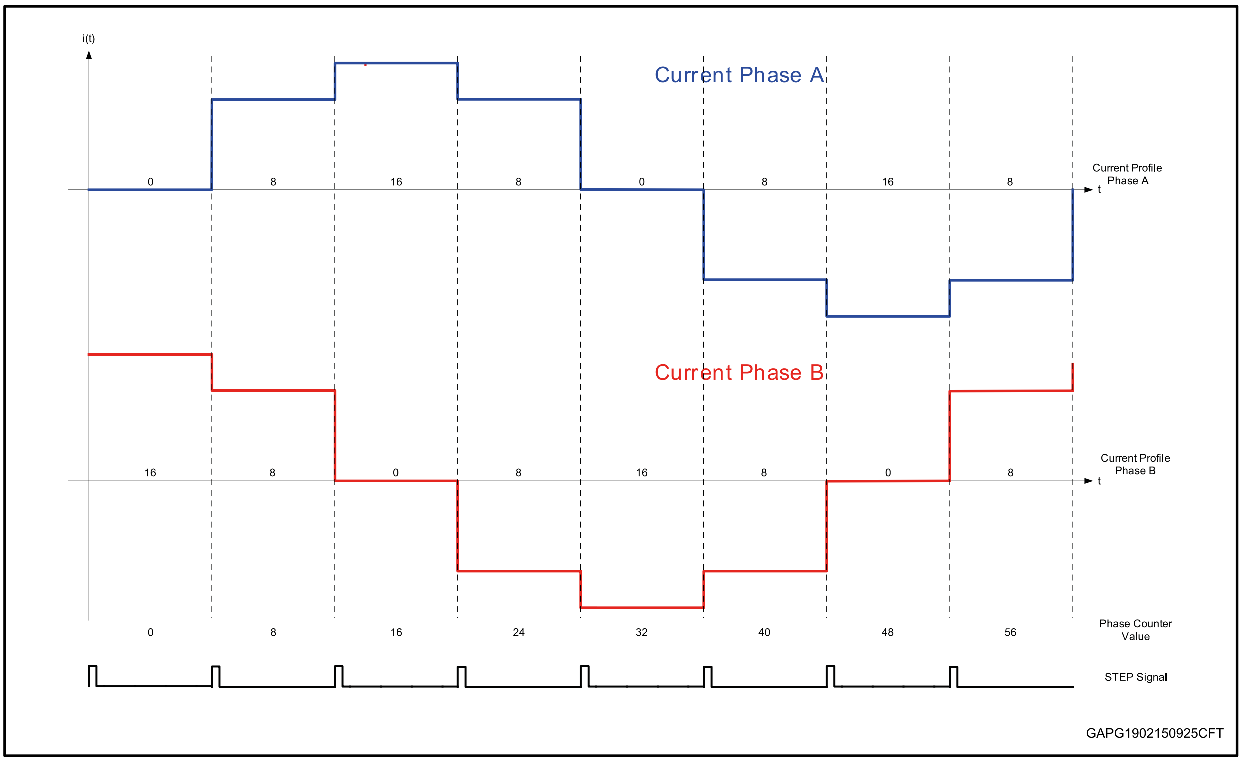
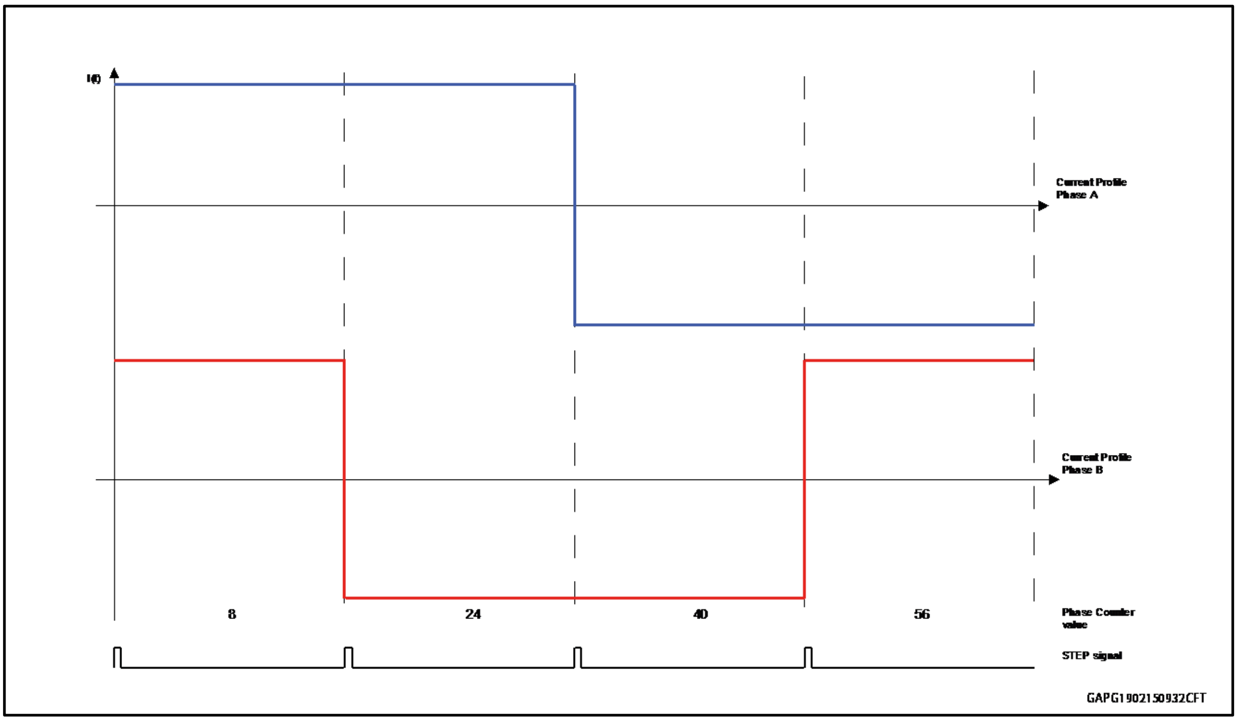


Figure 10: Electrical revolution in full step mode (current profiles and phase counter values)



The current profile generated by the device depends on the phase counter value (stored in PH[5:0] bits in MCR1 register) and it can be altered in an exclusive way either via the SPI interface (MX1 bit = 0) by directly writing PH[5:0] bits or through the CTRL1 pin (MX1 bit = 1) on each rising edge.

Phase counter update becomes effective on next PWM period.

In case MX1 bit is set, user has read-only rights to PH[5:0] bits and the phase counter can only be updated through rising edges on CTRL1 pin. In particular, PH[5:0] is incremented or decremented (depending on running motor direction) by a quantity automatically computed and dependent on the applied Step mode (normally SM[2:0]). Additionally, in case MX3[1:0] (in GCR1 register) is equal to 0x01, the CTRL3 pin can also be used to simultaneously select whether the current Step mode is the one specified by SM[2:0] bits or ASM[2:0] bits (MCR1 register). The automatic increment/decrement of the phase counter amounts to 1 LSB in case of 1/16th microstep mode (SM[2:0] or ASM[2:0] equal to 0x00), 2LSBs in case of 1/8 th microstep mode (SM[2:0] or ASM[2:0] equal to 0x01), 4 LSBs in case of mini-step mode (SM[2:0] or ASM[2:0] equal to 0x02), 8 LSBs in case of half-step mode (SM[2:0] or ASM[2:0] equal to 0x03), 16 LSBs in case of full-step mode (SM[2:0] or ASM[2:0] equal to 0x04).

Whenever changing the step mode from a higher resolution to a lower one, the phase counter is adjusted to the next closer phase counter value coherently with the new Step mode. This adjustment is actually applied on the first PWM period after a phase counter change command.

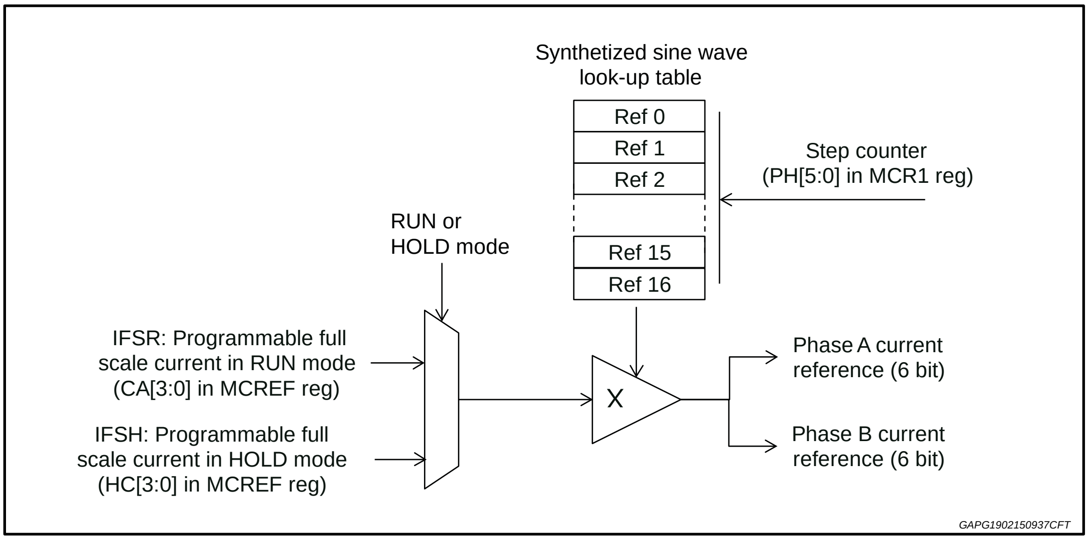
On the contrary, in case MX1 bit is reset, phase counter can only be accessed via SPI and logic level on CTRL1 input is discarded. In order to ensure the maximum flexibility for the application, the computation of the next phase counter value to be written in PH[5:0] is totally left to the application microcontroller. The step mode control bits, which will usually have no impact on the current profile generation when the PHase counter is updated via SPI, will impact the current profile generation only in full step mode.

Any modification of the step mode (either through CTRL3 pin in case MX3[1:0]=0x01 or through SPI writing of bit SM[2:0] and ASM[2:0] in MCR1 register) becomes effective at the beginning of the first PWM cycle following a phase counter update command (either received via CTRL1 pin with MX1=1 or through a SPI writing of PH[5:0] bits with MX1=0).

2.7 Current references generation and PWM regulation

L99SM81V embeds a look-up table composed by 17 entries synthetizing a quarter of a sinusoidal cycle; table elements have 6 bit accuracy. In 1/16th microstep mode each of these table entries represent the value that, once multiplied by the full scale factor stored into CA[3:0] bit of MCREF register, constitute in RUN mode the digital current references for a whole micro step. In HOLD mode, bits HC[3:0] are automatically used instead as full scale factor (see *Figure 11: "Current reference generation block diagram"*).

Figure 11: Current reference generation block diagram



Due to the symmetry of the sinusoidal waveform, all the 64 target motor current pairs of an electrical revolution (in 1/16th micro step) can be referenced by both the 17 table entries and the phase counter register. The 6 bit step (phase) counter - in fact - defines both the sign of the current flowing through phases A and B and which of the 17 current entries is to be used for current reference computation

In full step mode - the full scale current defined by either CA[3:0] or HC[3:0] bits in MCREF is entirely applied to the two motor phases (sine-wave look-up table not used), being current direction dependent on step counter value (see *Figure 10: "Electrical revolution in full step mode (current profiles and phase counter values)"*).

In order to achieve the motor current regulation, the current references generated in this way are then compared with the internal motor current mirror (no external shunt resistor).

At the beginning of each PWM period, H-bridges A and B are actively driven (PWM ON phase) until the related current reference is reached.

Once a H-bridge reaches its current reference, it is switched to one of the two possible PWM OFF configurations depending on the selected decay mode (see *Figure 12: "PWM ON and PWM OFF switching states"* for an overview of the switching states).

The PWM frequency for the current regulation is configurable (MCR2 FREQ[1:0]) and can be modulated with a wobble frequency generator by activating this option via SPI (GCR1 MWBE).

In order to avoid spurious misleading triggering of the comparator used for the current regulation loop, a minimum PWM on-time, equal to the sum of the programmable comparator blanking time (t_B) plus the glitch filter delay time (t_{TF}), is always applied.

2.8 HOLD mode

The L99SM81V features a HOLD mode intended to be used when it's required to hold the motor in a given position; HOLD mode is entered either by setting via SPI the HOLDM bit in register MCR1 (if MX3[1:0] ≠ 10b) or by setting a logic high value on pin CTRL3 (if MX3[1:0] = 10b).

In case bit AHMSD in MCR3 register is set, then HOLDM bit is set automatically (regardless of MX3 bits value and CTRL3 input level) after a stall condition is detected for a number of consecutive times equal to SD[2:0] (in this case it's necessary either to clear the SDF bit in the Status Register or to reset the AHMSD in the MCR3 Register before HOLDM bit can be cleared).

When In HOLD mode:

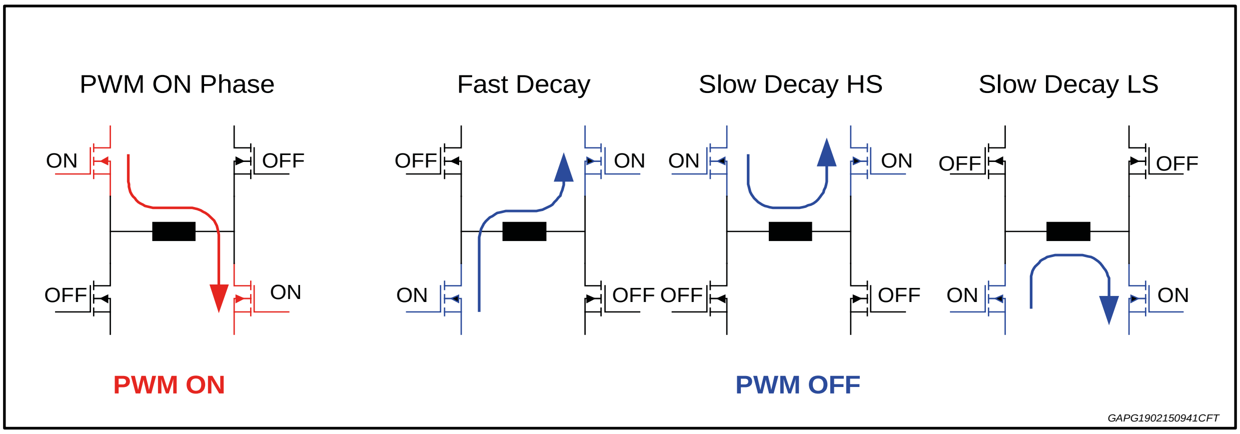
- The motor current reference is computed automatically for both motor phases starting from the full scale factor stored in bits HC[3:0] of MCREF register.
- The applied decay mode is set accordingly to DMH bit in MCR2
- The PH[5:0] bits can be still updated unless the HOLDM bit is set because of the AHMSD control bit set to one on a stall event detection pointed out by the SDF flag; only in this latter case the phase counter will be frozen as long as both bits (SDF and AHMSD) are set.

2.9 Decay modes

This device features different types of current decay modes. They are implemented to allow a flexible adaptation of the current regulation loop properties to the application requirements. The decay mode can be selected via SPI register MCR2 (DMR[1:0] bits for RUN mode, DMH bit for HOLD mode).

Figure 12: "PWM ON and PWM OFF switching states" shows an overview of the basic switching states during the PWM ON phase and the PWM OFF phase. Each decay mode is a combination of these basic switching states with different trigger events.

Figure 12: PWM ON and PWM OFF switching states



For the slow decay state it is configurable which freewheeling current path will be used (either high-side or low-side) see SPI Register MCR2 SDAFW&SDBFW.

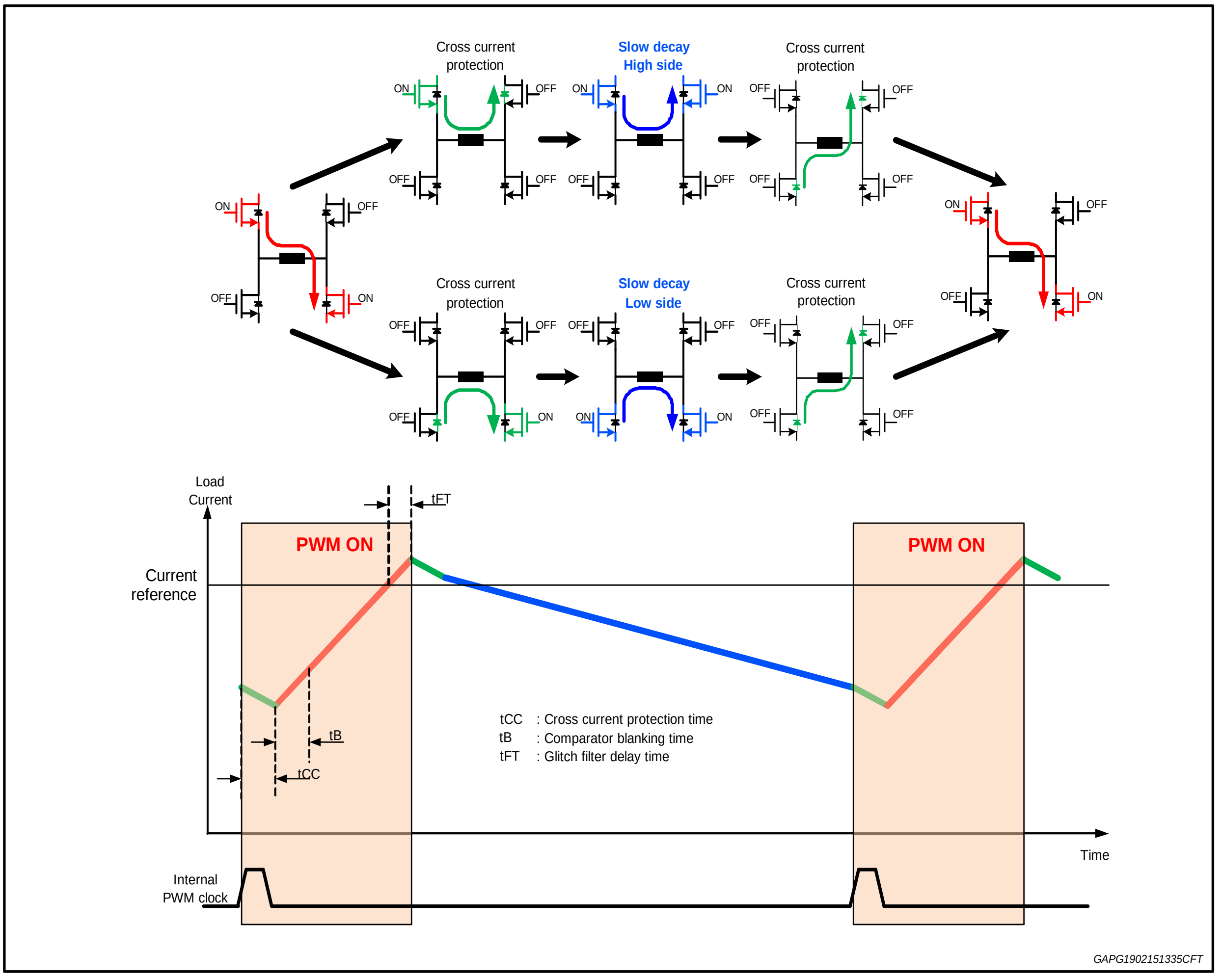
In Fast Decay state the opposite switches in each half - bridge are active – like when driving the current in the opposite direction in PWM ON phase. This allows decreasing the motor phase current faster if compared to Slow Decay but results in a higher current ripple.

In order to combine the advantages of a low current ripple with those of a fast and responsive current regulation, L99SM81V features a dedicated configuration (auto decay mode 2) in which the decay mode is dynamically and automatically adjusted by the device as described in *Section 2.9.4: "DMR[1:0] bits = 11b - Auto decay mode 2"*.

2.9.1 DMR[1:0] bits = 01b, DMH = 0 - Slow decay mode always applied

If DMR[1:0] bits are equal to 01b, Slow Decay Mode is always applied in RUN mode after the PWM ON phase. Likewise, slow decay mode is also always applied in HOLD mode if DMH = 0.

Figure 13: PWM switching sequence (slow decay)



2.9.2 DMR[1:0] bits = 10b, DMH = 1 - Mixed decay mode always applied

If DMR[1:0] bits are equal to 10b, Mixed Decay Mode is always applied in RUN mode. Likewise, mixed decay mode is also always applied in HOLD mode if DMH = 1. In Mixed Decay Mode the PWM ON phase is followed by a fast decay state, which is followed in turn by a slow decay. The start of the slow decay is triggered as soon as the actual current crosses the reference current and the filter time t_{FT} has elapsed.

Figure 14: Mixed decay

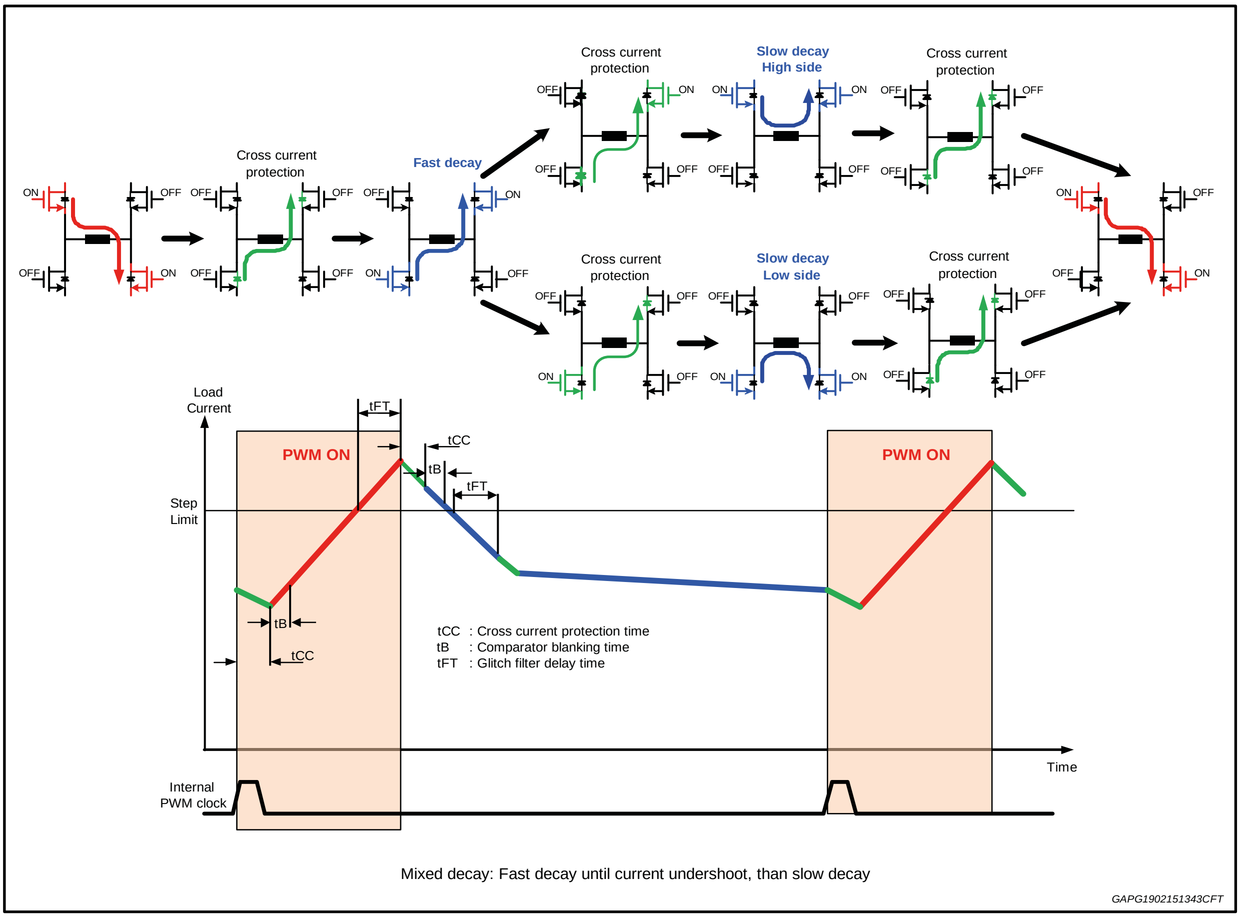
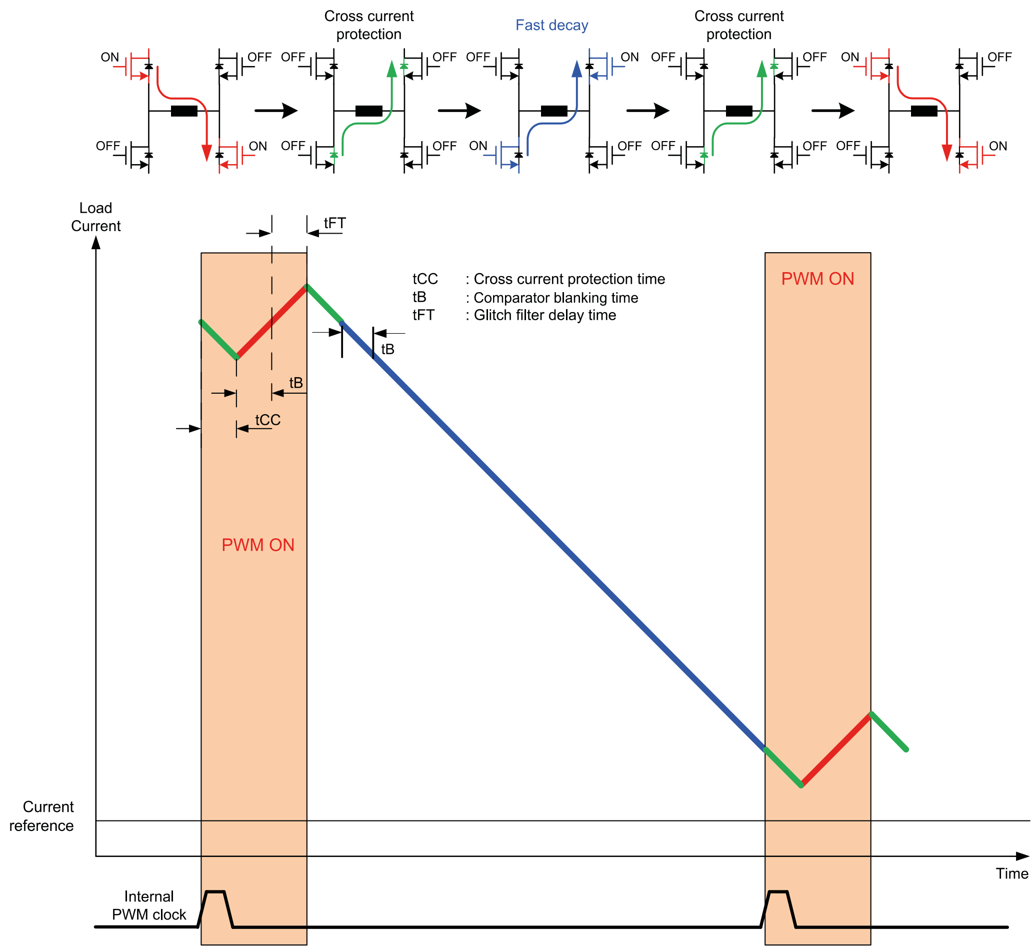


Figure 15: Mixed decay (current undershoot / limit not reached)



Mixed decay: Fast decay, current undershoot not reached

GAPG1902151346CFT

2.9.3 DMR[1:0] bits = 00b - Auto decay mode 1

In Auto Decay Mode1 the phase counter value and the motor spinning direction (DIR bit) are taken into account to select the appropriate switching state specifically, either a slow decay or a mixed decay are applied.

The next two figures show the dependency of the applied decay mode from the phase counter and the direction bit. See also paragraph *Section 2.9.2: "DMR[1:0] bits = 10b, DMH = 1 - Mixed decay mode always applied"* for mixed decay mode description.

Figure 16: Electrical revolution in auto decay mode 1 (DIR = 1)

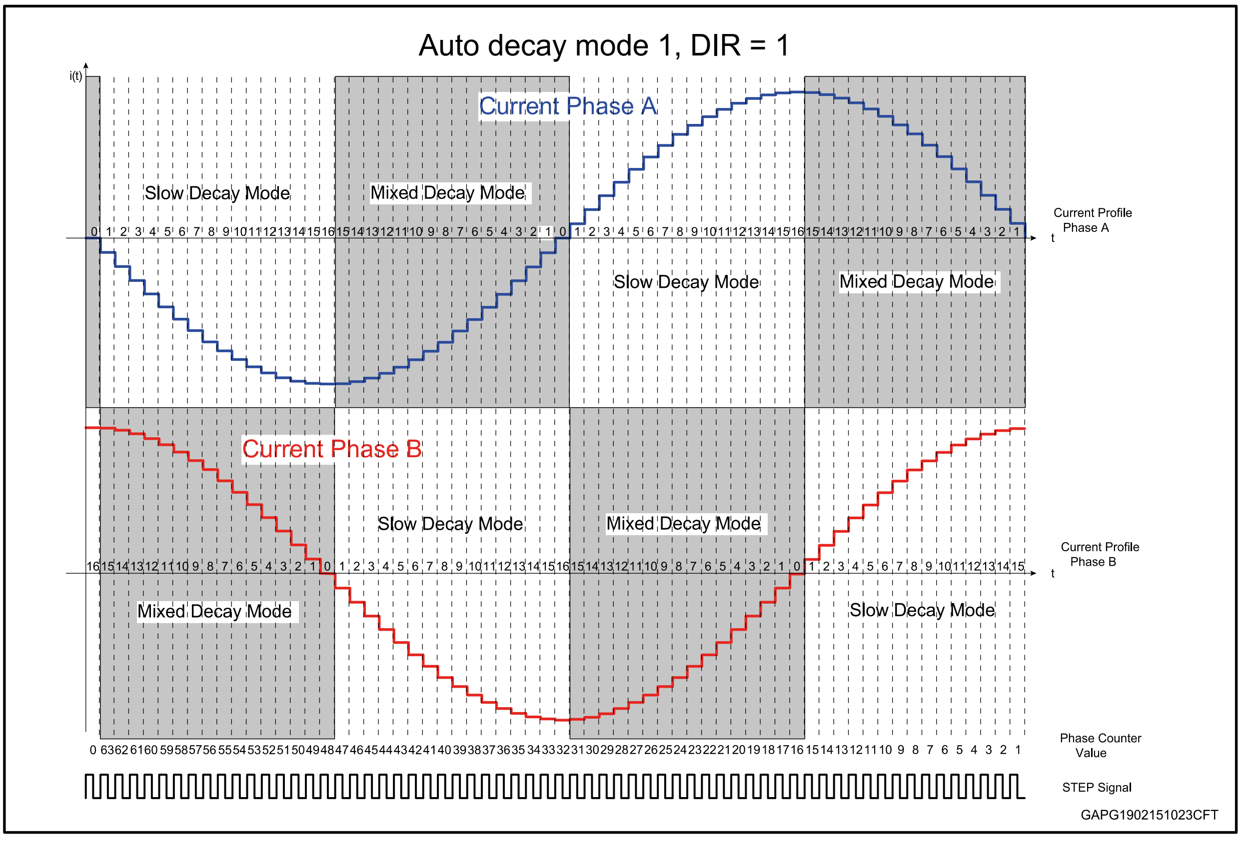


Figure 17: Electrical revolution in auto decay mode 1 (DIR = 0)

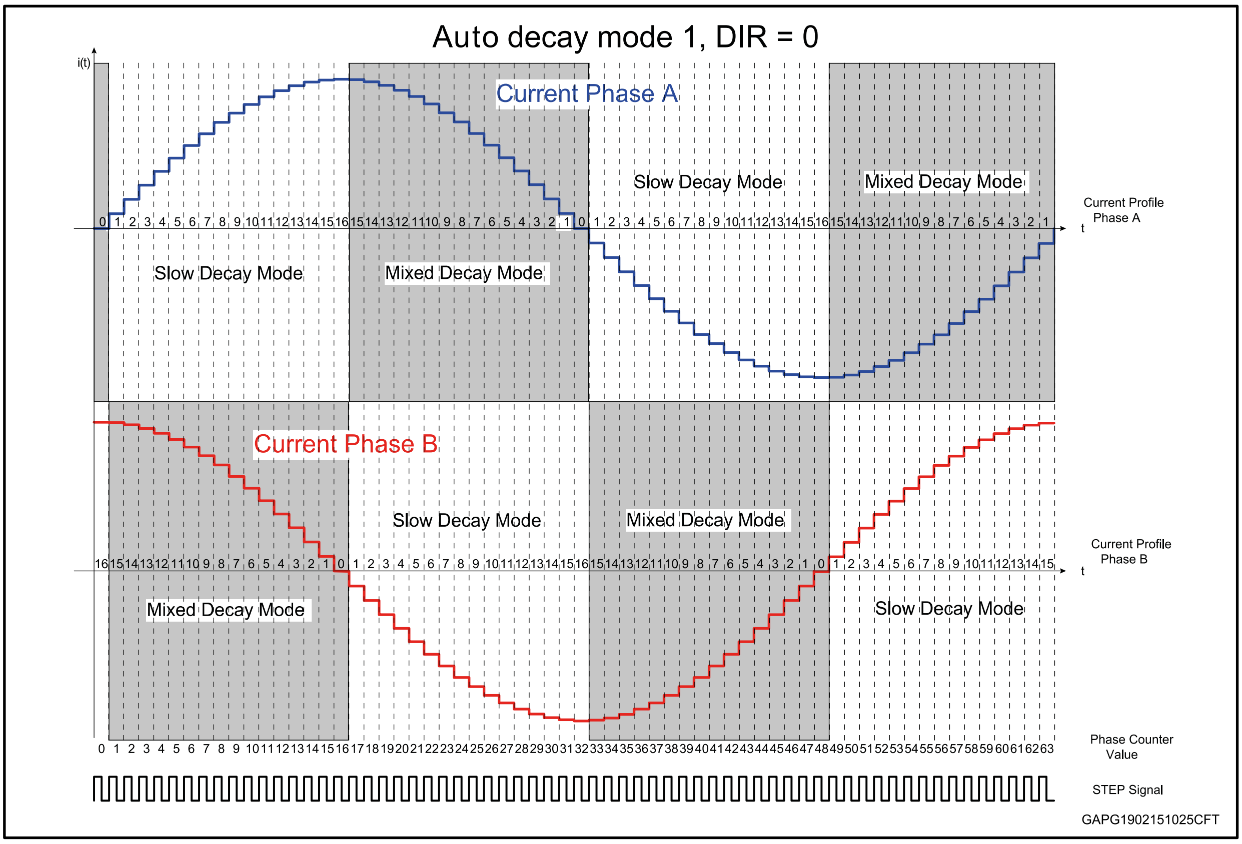
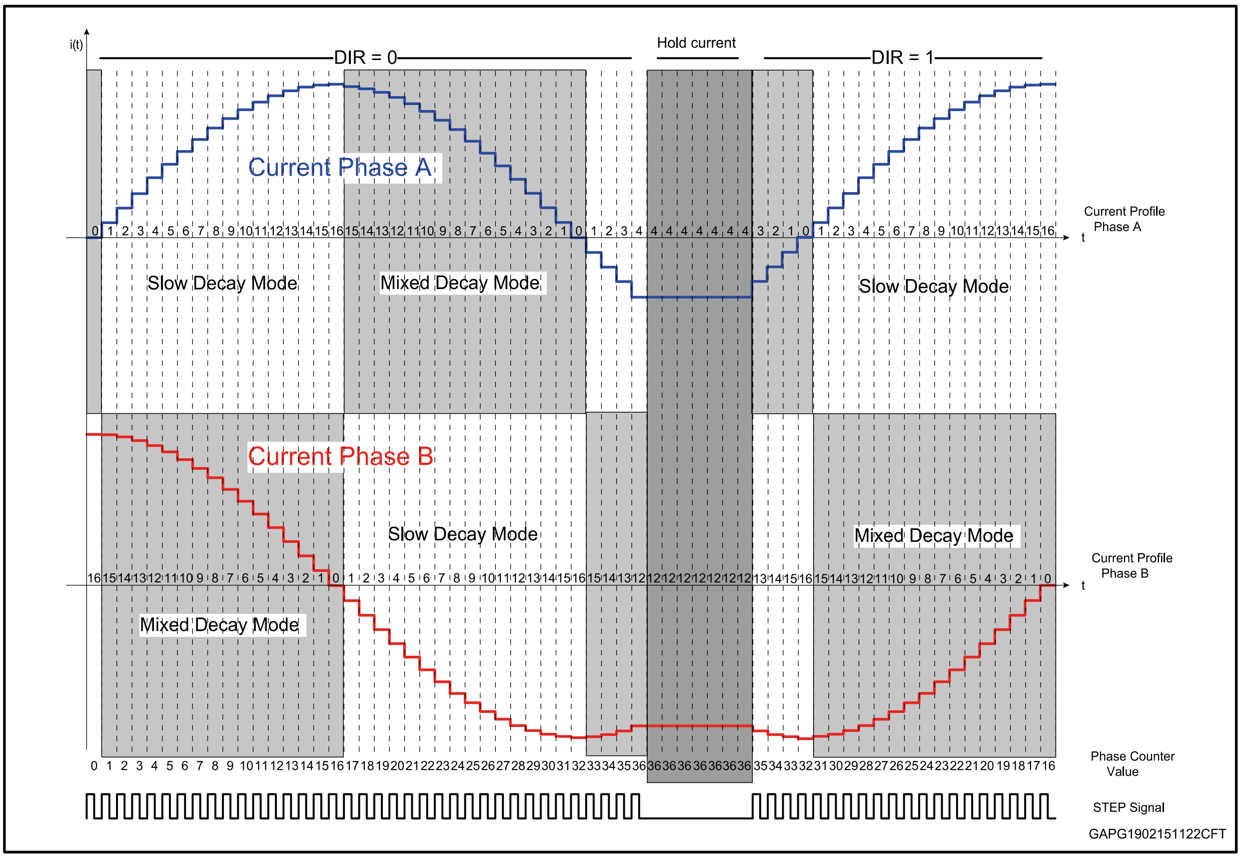


Figure 18: Auto decay mode 1 with direction change



2.9.4 DMR[1:0] bits = 11b - Auto decay mode 2

Auto decay mode 2 allows combining at the best the advantages of a low current ripple together with those of a fast and responsive current regulation. In Auto Decay Mode2, the phase counter value, the motor spinning direction (DIR bit) and the status of the real current vs. the current reference are taken into account to select the appropriate switching state. *Figure 19: "Auto decay mode 2, DIR = 0"* shows the dependence of the decay mode from the phase counter in case DIR=0 (applied decay mode are opposite in case of DIR =1)

In particular, with reference to the areas where a combination of slow and mixed decay modes is applied, mixed decay is used - in order to achieve the fastest current responsiveness - as soon as a new step begins and till the moment the motor phase current crosses the new (lower in absolute value) current reference, slow decay is then applied in order to reduce the switching losses and the current ripple vs. the mixed decay mode. See also paragraph *Section 2.9.2: "DMR[1:0] bits = 10b, DMH = 1 - Mixed decay mode always applied"* for mixed decay mode description.

Figure 19: Auto decay mode 2, DIR = 0

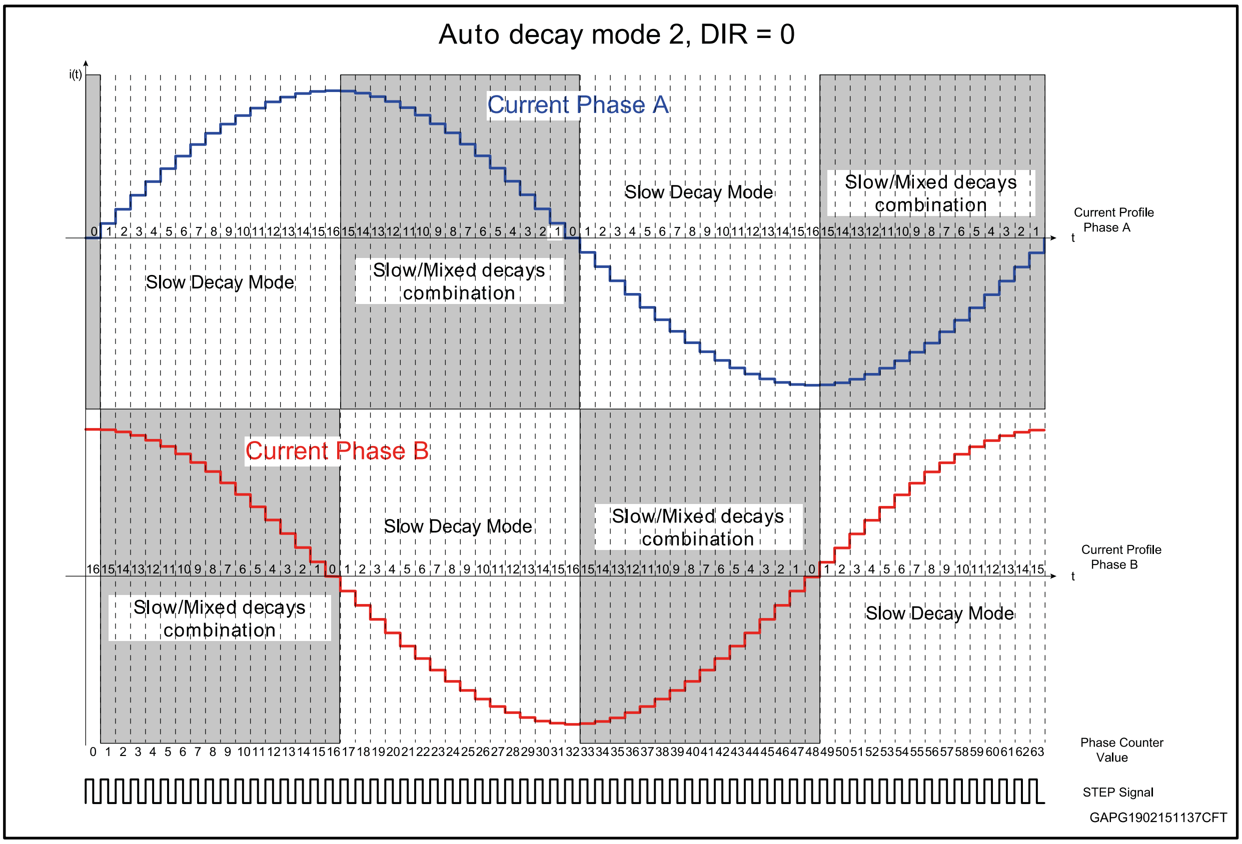


Figure 20: Auto decay mode 2, behavior at micro-step change (dead-time omitted)

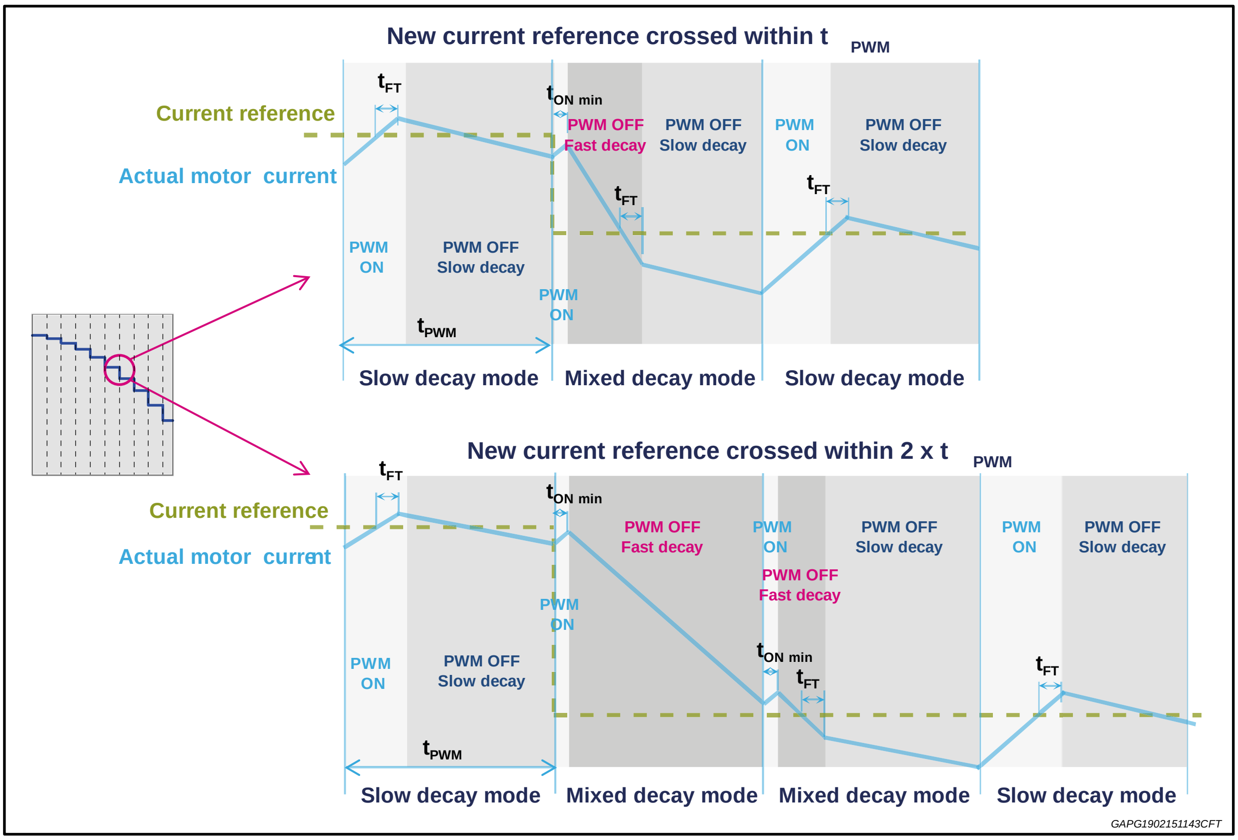
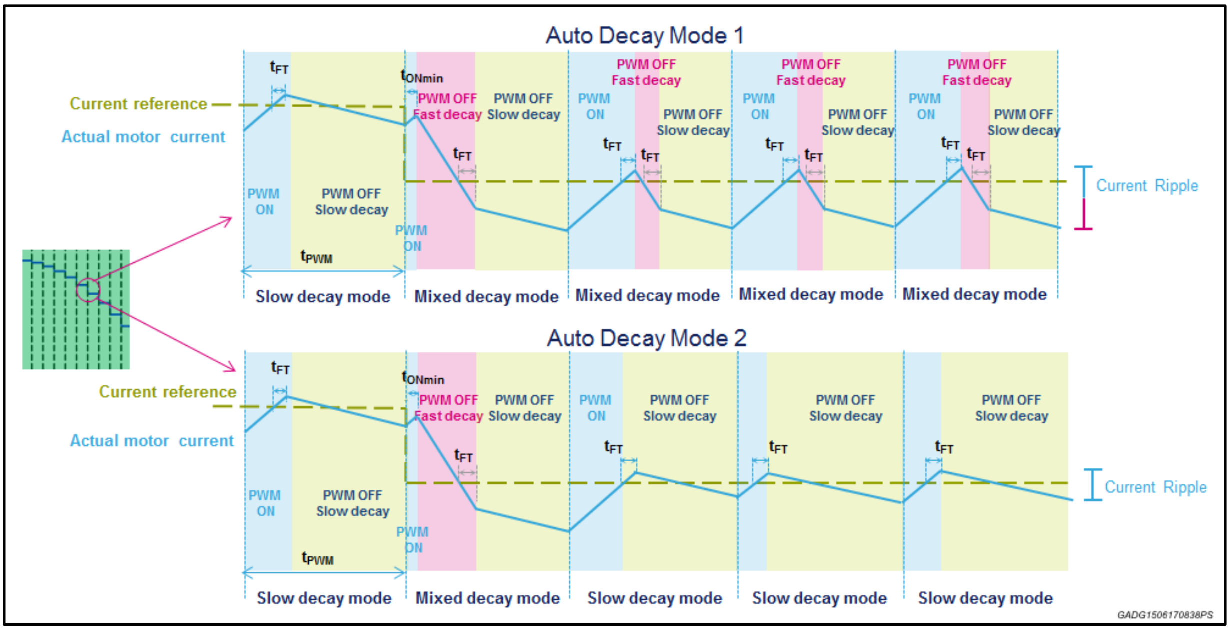


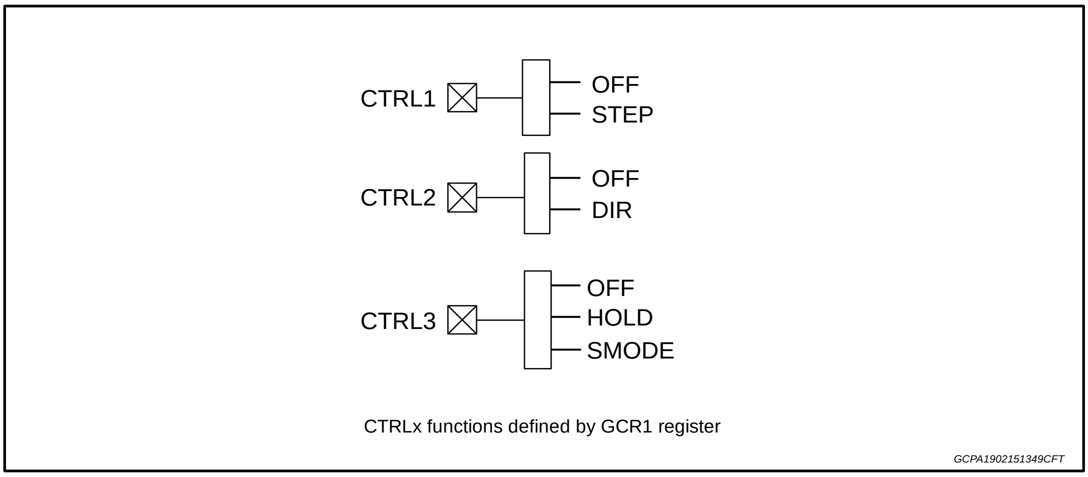
Figure 21: Comparative Auto decay mode 1 vs. Auto decay mode 2



2.10 Control pins (CTRLx)

Some of the functions in the L99SM81V can be controlled directly by application microcontroller I/Os (without using SPI communications) through the CTRLx digital input pins. The action to be executed by these pins is defined by MX bits in GCR1 registers.

Figure 22: CTRL pin multiplex options



2.10.1 Step Control (STEP)

If MX1 bit in GCR1 register is reset, no function is associated to the CTRL1 pin. Any step change can only be achieved by writing to the SPI PH[5:0] bits via SPI. If MX1 bit is set, a rising edge on this digital input causes the phase counter to be immediately updated (according to DIR bit) whereas the reference current is updated with the new value at the beginning of next PWM cycle (PH[5:0] can only be read through SPI in this case). If the DIR bit in the motor control register is reset then the phase counter will be incremented; if the DIR bit is set, then the phase counter will be decremented.

The decrement or increment value depends on the currently applied Step mode.

2.10.2 Direction Control (DIR)

If MX1 bit is reset in GCR1 register, the update of the phase counter (via SPI) is totally left to the application microcontroller. As a consequence, whatever is the value of MX2 bit, the direction is thus as well managed by the external microcontroller.

If MX1 is set, CTRL1 input holds the STEP functionality; the motor spinning direction is set in this case either via SPI or through direct input (CTRL2) depending on the value of MX2 bit.

If MX2 bit in GCR1 register is reset, no function is associated to the CTRL2 pin; DIR bit in MCR1 can only be written through SPI in this case.

If MX2 bit is set, the DIR bit can only be altered by CTRL2 pin: a high (low) logic level on this digital input will cause the direction bit DIR to be synchronously set (reset).

2.10.3 Step mode Control (SMODE) and HOLD mode

If MX3[1:0] bits in GCR1 register are equal to 0x00 or 0x03, no function is associated to the CTRL3 pin. The Step mode utilized in this case is either defined by SM[2:0] bits (MX1 bit = 1) or left to application microcontroller (MX1 bit = 0, full step mode apart). HOLD mode is entered by setting HOLDM bit in MCR1 through SPI.

If MX3[1:0] bits in GCR1 register are equal to 0x01, CTRL3 input selects the Step mode to be used: if CTRL3 = 0, the active step mode is the one defined by SM[2:0], otherwise the active step mode is the one defined by ASM[2:0]. To be noticed that if MX1 is reset, Step mode is intrinsically managed by the application microcontroller as it defines by itself the amount of increment or decrement to be applied on the phase counter. HOLD mode is entered by setting HOLDM bit in MCR1 through SPI.

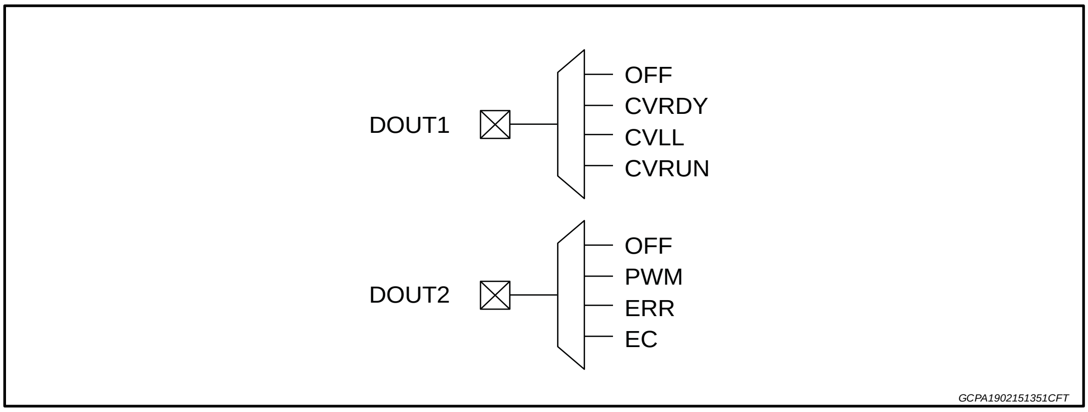
If MX3[1:0] bits in GCR1 register are equal to 0x02, CTRL3 pin is used as HOLD input, HOLDM bit reflects the logic state on CTRL3 and can't be altered through SPI. In case AHMSD is set, HOLDM bit is set in case of stall detection (SDF flag set) independently from CTRL3 pin logic level.

2.11 Digital outputs

The device features several diagnostic functions that can be reported to the microcontroller without starting an SPI communication. These signals can be assigned to device outputs by programming SPI configuration bits [11:7] in register GCR2.

If bits DOUT1[1:0] or DOUT2[1:0] in GCR2 register are set to 00b, the device will not drive the corresponding DOUTn pin.

Figure 23: Configurable I/O multiplex options



2.11.1 Error/ warning indicator (ERR)

This signal is a logical OR combination of all diagnostic and warning flags contained in Global Status Register (GSR).

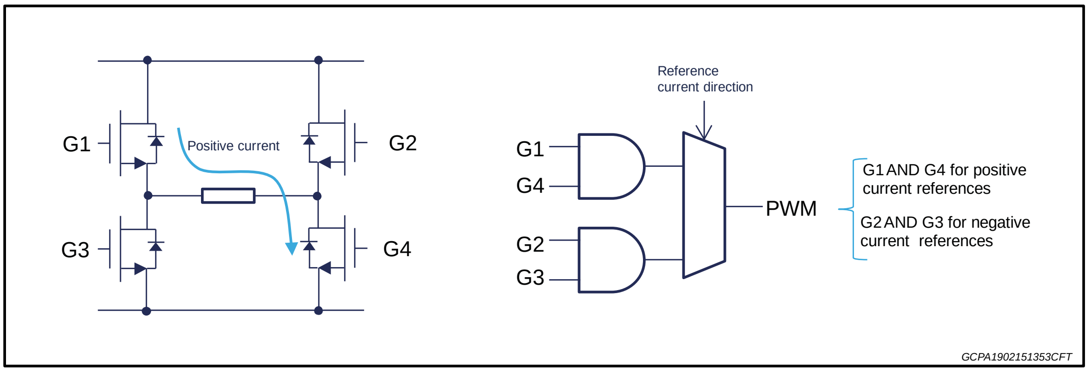
2.11.2 Error/ warning change indicator (EC)

This signal is set every time any of the diagnostic and warning flags contained in GSR is set. Any read access to the GSR register will reset this signal to low level.

2.11.3 PWM

As shown in *Figure 24: "PWM signal generation"* this signal reflects the PWM control signal applied to the H-bridge A outputs.

Figure 24: PWM signal generation



2.11.4 Coil Voltage Conversion Ready (CVRDY)

A rising edge on this signal indicates that averaged coil voltage measurement is available in the respective MCV register.

A falling edge on this signal occurs when a new zero-current micro-step begins.

2.11.5 Coil Voltage Runaway (CVRUN)

CVRUN signal is updated every time a new coil voltage measurement is available. If the latest stored coil voltage value is higher than CVUL threshold or lower than CVLLA threshold, the signal is set, otherwise is reset.

2.11.6 Coil Voltage Lower Limit Underrun (CVLL)

CVLL signal is updated every time a new coil voltage measurement is available (rising edge of signal CVRDY). If the latest stored coil voltage value is lower than CVLLB, the signal is set, otherwise it is reset.

2.12 Analog output

The device features an analog output which - depending on AOUT[1:0] bits in GCR1 register - can be used either to feed back the device embedded thermal sensor output (AOUT[1:0]=01b) or a precise band-gap voltage reference (AOUT[1:0]=10b).

2.13 Motor coil voltage measurement for stall detection

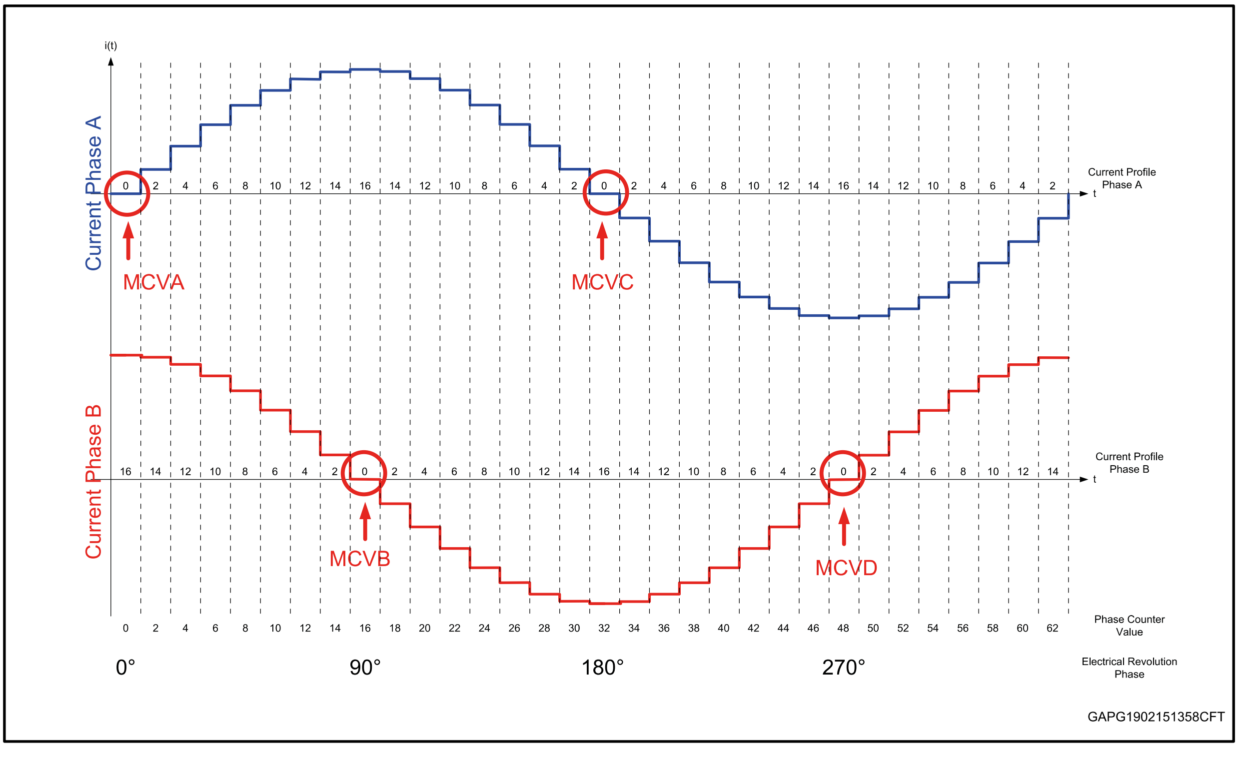
Setting CVE bit in MCR3 enables the automatic measurement of the voltage across the motor terminals during each zero-current step; this makes it possible to measure the voltage induced by the rotor movement (BEMF) and thus have information about motor speed.

In order for the motor coil voltage measurement to be correctly performed, it's required that bit MWBE in GCR1 is reset.

Four BEMF values are converted within a complete electrical cycle (*Figure 25: "Coil voltage registers content (DIR = 0, positive current flowing from OUTx1 to OUTx2; x = A, B)"*), related digital values are stored into registers MCVA, MCVB, MCVC, MCVD and bits CVLUR[1:0] in MCR3 indicate which of MCVx registers was lastly updated.

The motor terminal to be sampled is automatically selected depending on the rotation direction and on phase counter value so that only positive BEMF is always measured (see also *Table 2: "Coil voltage synopsis table"*).

Figure 25: Coil voltage registers content (DIR = 0, positive current flowing from OUTx1 to OUTx2; x = A, B)



In order for the sampled coil voltage to be really equal to the BEMF induced by the rotor, the PWM signals applied to the H-bridge driving the coil under examination are switched off as soon as the zero-current step begins. In addition - after a dead-time and according to *Table 2: "Coil voltage synopsis table"* - the low side power switch opposite to the output to be converted is switched on (see *Figure 26: "Coil voltage measurement sequence example"*) in order to have coil voltage measurement referred to GND.

Figure 26: Coil voltage measurement sequence example

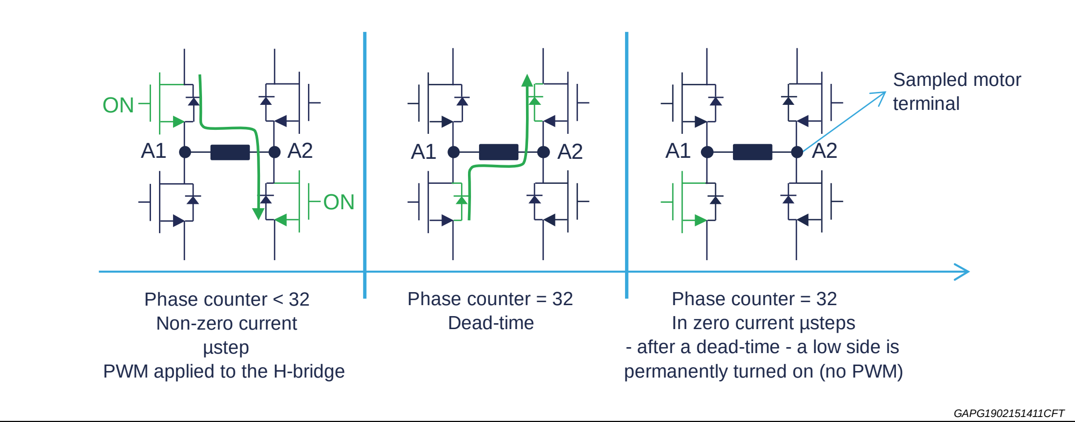


Table 2: Coil voltage synopsis table

	DIR bit = 0 (phase counter increasing)		DIR bit = 1 (phase counter decreasing)		
Phase counter	Output to GND	Motor terminal sampled	Output to GND	Motor terminal sampled	Updated register
0	A2	A1	A1	A2	MCVA
16	B1	B2	B2	B1	MCVB
32	A1	A2	A2	A1	MCVC
48	B2	B1	B1	B2	MCVD

2.13.1 Coil voltage measurement triggering

In order to filter out any PWM commutation noise, several A/D conversions are carried out and averaged over each PWM period (the number of averaged samples ranges from 8 to 16, depending on programmed PWM frequency). The digital averaged value is then transferred into proper MCVx register on a triggering event which depends on bits D[4:0] in register MCR3:

1. D[4:0] = 00000b; trigger at the end of the zero-current step.
   Digital averaged coil voltage is transferred into MCVx register at the end of a zero current step (that is as soon as a step counter change becomes effective, default option).
2. D[4:0] > 00001b; trigger delayed from the start of the zero-current step.
   During a zero-current step, the digital averaged coil voltage is transferred into MCVx register after a given number of PWM cycles – defined by bits D[4:0] in register MCR3 – have elapsed. In case the step counter update command is given before the programmed PWM cycles have elapsed, the zero-current step duration is extended till that time, thus delaying the actual phase counter update.

2.13.2 Coil voltage measurement processing

As soon as the triggering event occurs, both proper MCVx register and bits CVLUR[1:0] in MCR3 (indicating which of MCVx registers lastly changed) are updated. Also, CVRDY signal goes from low to high (falling edge of CVRDY signal indicates that zero-current step has started).

As soon as a new value is stored into MCVx register, the same value is automatically compared with user-configurable thresholds:

- CVUL, stored in MCVUL register
- CVLLA, stored in MCVLLA register
- CVLLB, stored in MCVLLB register

Depending on the comparison result, flags CVULF, CVLLAF and CVLLBF are also updated in MSR:

- CVULF is set if sampled coil voltage exceeds CVUL threshold, it is reset otherwise
- CVLLAF is set if sampled coil voltage falls below CVLLA threshold, it is reset otherwise
- CVLLBF is set if sampled coil voltage falls below CVLLB threshold, it is reset otherwise

Additionally

- CVRUN signal is set if latest stored coil voltage value is higher than CVUL or lower than CVLLA, it is reset otherwise
- CVLL signal is set if the latest sampled coil voltage value is lower than CVLLB, it is reset otherwise

If the sampled coil voltage value is out of the range [CVLLA; CVUL] for a number of consecutive acquisitions (zero-current steps) equal to SD[2:0], then the bit SDF of the GSR is set. If the bit AHMSD in MCR3 register is set, then the HOLDM bit (in MCR1) is also automatically set and the driver enters HOLD mode. See also *Section 2.8: "HOLD mode"* for more information about HOLD mode.

The SDF status flag is also reported in the Global Status Byte as FE.

2.14 Serial peripheral interface (ST SPI standard)

This device features a 24-bit ST SPI in slave configuration for bi-directional communication with an external microcontroller. This device supports burst read access and shall be operated in the following mode: CPOL = 0 and CPHA = 0.

For this mode, input data is sampled on the rising edge of the clock signal SCK and output data is changed on the falling edge of SCK.

During standby mode, the SPI interface is deactivated.

Signal Description:

- Chip Select Not (CSN)
  The input pin is used to select the serial interface of this device. When CSN is high, the output pin (SDO) will be in high-impedance state. In case CSN is stuck at GND, a timeout is implemented which sets the SDO line back to high-impedance to release the SPI network. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame.
- Serial Data In (SDI)
  The input pin is used to transfer data serially into the device. The data applied to SDI will be sampled on the rising edge of the SCK signal and shifted into an internal 24-bit shift register. On the rising edge of the CSN signal, the contents of the shift register will be transferred to the Data Input Register. Only communication frames with 0 (read GSBN bit), 24 (standard communication frame), or 24 + (n * 16) (burst read/write) clock pulses are accepted. All others will be ignored and a communication error will be reported with the next SPI command.
- Serial Data Out (SDO)
  The data output driver is activated by a logic low level at the CSN input. After a falling edge of the CSN pin, the SDO pin will leave the tri-state condition and present the GSBN bit. At all following falling edges of the SCK signal, the following bits of the SPI frame are shifted out to the SDO pin.

- Serial Clock (SCK)
  The SCK input is used to synchronize the input and output serial bit streams. The data input (SDI) is sampled on the rising edge of the SCK and the data output (SDO) will change with the falling edge of the SCK signal. The SPI can be driven with a SCK frequency up to 4 MHz.

3 Protections and diagnostics

3.1 Supply diagnostics

3.1.1 VS overvoltage and undervoltage

If the voltage on the supply pins VS rises above the overvoltage threshold, VSOV flag in GSR register is set and latched, the charge pump is switched off and ME bit (MCR1 register) is cleared, thus putting the device outputs in high impedance. VS has to drop below the overvoltage threshold minus the over-voltage hysteresis to allow the clearing of VSOV bit.

Likewise, if the voltage on the supply pins VS falls below its undervoltage threshold, the corresponding undervoltage diagnosis flag (VSUV bit in GSR register) is set, ME bit is cleared and charge pump is switched off. VSUV bit can be cleared (and consequently, ME bit can be set) by the microcontroller when VS voltage has risen above the undervoltage threshold plus the undervoltage hysteresis.

3.1.2 VREG overvoltage and undervoltage

If the voltage on the supply pin VREG rises above its overvoltage threshold, the corresponding overvoltage diagnosis flag (VREGOV bit in GSR register) is set and the V5V regulator is switched off. VREGOV bit can be cleared by the microcontroller when VREG voltage has dropped below the overvoltage threshold minus the overvoltage hysteresis.

If the voltage on the supply pin VREG falls below its undervoltage threshold warning, the corresponding undervoltage diagnosis flag (VREGUV bit in GSR register) is set. VREGUV flag can be cleared by the microcontroller when VREG voltage has risen above the undervoltage threshold plus the undervoltage hysteresis. If VREG voltage decreases further below the VREG POR threshold, the device is reset and the registers are reset to their default value.

3.1.3 CP failure

The charge pump operation is internally monitored. If the charge pump voltage falls below the VCPLOW threshold, the CP failure flag CPFAIL in GSR is set and the charge pump is switched off. This clear also the ME bit, thus disabling the output drivers. The CP failure flag can be cleared through a dedicated Read & Clear SPI command. Once the flag is cleared, the ME bit can be set.

3.1.4 V5V undervoltage warning

If the output voltage on pin V5V drops below the undervoltage warning threshold V5UVW, the V5V undervoltage warning flag V5UVW in GSR is set.

This flag can be cleared by a Read & Clear SPI command.

3.1.5 V5V failure

If the output voltage on pin V5V rises above the V5V overvoltage threshold (V5VOV), then the V5V failure flag is set and the voltage regulator is disabled.

In case the 5V regulator output drops below the V5VFAIL threshold, the L99SM81V detects a short circuit to ground, the V5V failure flag (V5VUV) is latched and the voltage regulator is disabled. If the output of the regulator doesn’t exceed the V5VFAIL threshold after a time equal to t_{FTO}, the device detects a short-circuit condition, the regulator is switched off and the corresponding failure flag is set. To re-enable the voltage regulator, the failure flag has to be cleared.

3.1.6 VDD failure

In case VDD voltage falls below the threshold VDDPORF, the internal registers are reset to their default values. The power-on reset is released once VDD rises above VDDPORR.

3.2 Thermal warning and thermal shutdown

If the junction temperature reaches the TW threshold, the TW flag in GSR is set and latched. In case the junction temperature increases and reaches the TSD threshold, the two full-bridges, the charge pump and the voltage regulator V5V are disabled to protect the device and the TSD flag in GSR is set and latched. In order to re-enable the driver, the junction temperature must decrease below the thermal shutdown threshold, the thermal shutdown error flag must be cleared by the microcontroller and the ME bit must be set again.

3.3 Cross current protection (dead-time)

The device features an internal dead-time generator for cross current protection. The duration of the dead-time is automatically adjusted according to the SR[1:0] bits in MCR2 register which set the turn-on and turn-off speed of the integrated power MOSFETs.

3.4 Driver diagnostic

3.4.1 Overcurrent detection

If the current through any of the switches in the output driver exceeds the output overcurrent limit IOCxn for longer than tOC, then the corresponding overcurrent error flag in the motor status register MSR is set and the outputs are set in high impedance state (ME bit reset in MCR1).

To re-enable the output drivers, the error flag OC has to be cleared in GSR by the application microcontroller and the ME bit must be set again.

3.4.2 Open load detection

Starting from the beginning of any PWM cycle, if the motor current doesn’t reach the current reference for a period of time longer then a programmable delay (OLDLY bit in MCR2), then the corresponding open load flag (OLA or OLB bits, depending on which of the motor phase is failing) is set in MSR register.

These flags don't affect the output drivers and can be cleared by clearing the OL flag in GSR.

4 Electrical characteristics

4.1 Absolute maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
VS	Power supply voltage	-0.3 to 40	V
VREG	Voltage regulator power supply	-0.3 to 40	V
VDD	Digital I/Os supply	-0.3 to 6	V
V5V	Voltage regulator output	-0.3 to 40	V
VCP, CP+	Charge pump output voltage, positive connection for charge pump capacitor	VSA - 0.3 to 45 V (in case VSA >28V) or VSA +17 V (in case VSA<28)	V
CP-	Charge pump pin for negative capacitor connection	-0.3 to VSA+0.3 V	V
VOUTxn	Output voltage (x = A,B; n = 1,2)	-0.3 to VS + 0.3	V
VEN, VCTRLn, VDOUTn, VSDO, VSDI, VCLK, VCSN	Logic I/O voltage range (x = 1,2; n = 1,2,3)	-0.3 to 6	V
AOUT	Analog output	-0.3 to 40	V

All maximum ratings are absolute ratings. Exceeding any of these values may cause an irreversible damage of the integrated circuit!

4.2 Operating range

Table 4: Operating range

Symbol	Parameter	Value	Unit
VS	Power supply voltage	6 to 28	V
VREG	Voltage regulator power supply	6 to 28	V
VDD	Digital I/Os supply	3 to 5.5	V
VEN, VCTRLn, VDOUTn, VSDO, VSDI, VCLK, VCSN	Logic I/O voltage range (x = 1,2; n = 1,2,3)	0 to VDD	V

4.3 ESD protection

Table 5: ESD protection

Parameter	Value	Unit
Electrostatic Discharge Test (AECQ100-002-E) all pins	±2	kV
Electrostatic Discharge Test (AECQ100-002-E) output pins VOUTKXN (X = A,B; N, K = 1,2)	±4	kV
Charge device model (CDM-AEC-Q100-011) all pins	±500	V
Charge device model (CDM-AEC-Q100-011) corner pins	±750	V

4.4 Thermal data

Table 6: Thermal data

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{stg}	Storage temperature		-55		150	°C
T_j	Operating junction temperature		-40		150	°C
$T_{j\text{-}peak}$	Peak junction temperature (1)			160		°C
$R_{th\ j\text{-}amb}$	Junction-to-ambient thermal resistance (2)	PowerSSO-36 package		17		°C/W
		QFN40L package		23		
$R_{th\ j\text{-}case}$	Junction-to-case thermal resistance	PowerSSO-36 package		5		°C/W
		QFN40L package		6.5		°C/W

Notes:

(1)No more than 100 cumulative hours over lifetime.

(2)Device soldered on 2s2p PCB thermally enhanced (slug included).

Table 7: Thermal warning and thermal shutdown

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
TW	Thermal warning threshold (1)		140	150	160	°C
TSD	Thermal shutdown threshold		160	170	180	°C
TSDH	Thermal shutdown hysteresis			5		°C
t_{TFT}	Thermal filter time	Tested by scan chain		64		µs

Notes:

(1)Thermal warning and shutdown thresholds not overlapping.

4.5 Main electrical characteristics

Voltages are referred to ground and currents are assumed positive when the current flows into the pin.

The device is operated in the specified operating range, unless otherwise specified.

Table 8: Supply and supply monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VSOV	Overvoltage threshold on VS supply		28.1	30	32	V
VSOVH	Overvoltage hysteresis on VS supply		0.5			V
VSUV	Undervoltage threshold on VS supply		5.2	5.5	5.9	V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VSUVH	Undervoltage hysteresis on VS supply		0.3			V
VREGOV	Overvoltage threshold on VREG supply		28.1	30	32	V
VREGOVH	Overvoltage hysteresis on VREG supply		0.5			V
VREGUV	Undervoltage warning threshold on VREG supply		5.2	5.5	5.9	V
VREGUVH	Undervoltage warning hysteresis on VREG supply		0.3			V
t_{VFT}	Overvoltage and undervoltage filter time	Tested by scan chain		64		µs
I_S	VS supply current in active mode	VS = 13.5 V; EN = VDD = 5 V; open outputs; SR = 70 V/µs; FREQ[1:0] = 01b (30 kHz PWM)		4	6	mA
I_{DD}	VDD supply current in active mode	VS = 13.5 V; EN = CSN = VDD = 5 V; SCK = SDI = STEP = 0 V; open outputs		1.2	1.8	mA
I_{REG}	VREG supply current in active mode	VS = VREG = 13.5 V; EN = VDD = 5 V; open outputs; SR = 70 V/µs; FREQ[1:0] = 01b (30 kHz PWM)		7.5	12.3	mA
I_{SQ}	VS quiescent supply current in standby mode	VS = 13.5 V; VDD = 5 V; EN = 0V; open outputs; T_{TEST} = -40 °C to 25 °C;		3	10	µA
		VS = 13.5 V; VDD = 5 V EN = 0V; open outputs; T_{TEST} = 125 °C;		6	20	µA
I_{DDQ}	VDD quiescent supply current in standby mode	VS = 13.5 V; VDD = 5 V EN = 0V; open outputs; T_{TEST} = -40 °C to 25 °C;		3	10	µA
		VS = 13.5 V; VDD = 5 V EN = 0V; open outputs; T_{TEST} = 125 °C;		6	20	µA
I_{REGQ}	VREG quiescent supply current in standby mode	VS = VREG = 13.5 V; VDD = 5 V; EN = 0 V; open outputs			5	µA

Table 9: Power on reset

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDDPORR	Power-on-reset rising	VDD rising	2.2		2.8	V
VDDPORF	Power-on-reset falling	VDD falling	2	2.3	2.5	V
VDDPORH	Power-on-reset hysteresis	VDD POR hysteresis	0.2			V
VREGPORR	Power-on-reset rising	VREG rising	3.1	3.5	3.9	V
VREGPORF	Power-on-reset falling	VREG falling	2.9	3.3	3.8	V
VREGPORH	Power-on-reset hysteresis	VREG POR hysteresis	25			mV

Table 10: Voltage regulator V5V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V5V	Output voltage			5.0		V
V5V	Output voltage tolerance including line and load regulation	Active mode; 0 mA < I_{V5V} <= 40 mA; 8 V <= VREG < 28 V	-5		5	%
		Active mode; 0 mA < I_{V5V} <= 25 mA; 6 V <= VREG < 8 V	-5		5	%
		Active mode; 25 mA < I_{V5V} <= 40 mA; 6 V <= VREG < 8 V	-5		5	%
I_{V5VP}	Output peak current	Max. continuous load current			50	mA
I_{V5VLIM}	Short-circuit output current	Current limitation	50		150	mA
CV5V	Load capacitor	Ceramic (+/- 20%)		0.22		µF
V5UVW	Undervoltage warning threshold		4	4.2	4.4	V
V5VOV	Overvoltage threshold		5.42	5.9	6.38	V
V5VFAIL	Fail threshold		1.8	2	2.2	V
t_{UVFT}	Undervoltage warning filter time	Tested by scan chain		16		µs
t_{OVFT}	Overvoltage filter time	Tested by scan chain		16		µs
t_{FFT}	Fail filter time	Tested by scan chain		16		µs
t_{FTO}	Fail time-out filter (start-up condition)	Tested by scan chain		4		ms

Table 11: AOUT electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VBG	Output voltage bandgap	T_j = 25 °C		1.206		V
	Whole range accuracy	-40 °C < T_j < 150 °C; 6 V < VREG < 28 V	-2.5		2.5	%
T_{SENSE}	Thermal sensor output	T_j = 25 °C		1.32		V
	Thermal coefficient			-4.24		mV/K

Table 12: OUTxn outputs (x = A,B; n = 1,2)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Rxn_HS	ON-resistance OUTxn to VS	VS = 13.5 V; T_J = 25°C; Ixn = -1.25 A		0.7	-	Ω
		VS = 13.5 V; T_J = 150 °C; Ixn = -1.25 A		1.14	1.3	Ω
Rxn_LS	ON-resistance OUTxn to PGND	VS = 13.5 V; T_J = 25 °C; Ixn = 1.25 A		0.7	-	Ω
		VS = 13.5 V; T_J = 150 °C; Ixn = 1.25 A		1.14	1.3	Ω
|IOCxn|	Output overcurrent protection threshold	Static test	1.9	2.2	2.75	A
|IFSR|	Full scale current threshold in RUN mode	CA[3:0] = 0x0F	1204	1353	1502	mA
		CA[3:0] = 0x0E		1160		
		CA[3:0] = 0x0D		1051		
		CA[3:0] = 0x0C		920		
		CA[3:0] = 0x0B		812		
		CA[3:0] = 0x0A		679		
		CA[3:0] = 0x09		571		
		CA[3:0] = 0x08		465		
		CA[3:0] = 0x07		396		
		CA[3:0] = 0x06		375		
		CA[3:0] = 0x05		329		
		CA[3:0] = 0x04		323		
		CA[3:0] = 0x03		302		
		CA[3:0] = 0x02		220		
		CA[3:0] = 0x01		198		
		CA[3:0] = 0x00	141	176	211	mA
|IFSH|	Full scale output current in HOLD mode	HC[3:0] = 0x0F	290	326	362	mA
		HC[3:0] = 0x0E		292		

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
		HC[3:0] = 0x0D		264		
		HC[3:0] = 0x0C		230		
		HC[3:0] = 0x0B		202		
		HC[3:0] = 0x0A		168		
		HC[3:0] = 0x09		140		
		HC[3:0] = 0x08		118		
		HC[3:0] = 0x07		101		
		HC[3:0] = 0x06		95		
		HC[3:0] = 0x05		84		
		HC[3:0] = 0x04		79		
		HC[3:0] = 0x03		73		
		HC[3:0] = 0x02		62		
		HC[3:0] = 0x01		50		
		HC[3:0] = 0x00	7	28	49	mA
IRELERR	Relative error on current reference between Motor X Phase A and Phase B	CA[3:0] = 0x0F	-7.5		7.5	%
t_{CC}	Cross current protection time (dead-time)	See *Table 14: "PWM control"*				

Table 13: Charge pump

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CP}	Charge pump output voltage	VS = 6 V, I_{CP} = -6 mA	VS + 4.6	VS + 4.9		V
		VS ≥ 10 V, I_{CP} = -6 mA	VS+8	VS + 8.5		V
		VS ≥ 13.5 V; I_{CP} = -6 mA	VS+10			V
I_{CPLIM}	Charge pump output current limitation	VCP = VS; VS = 13.5 V; C1 = CCP = 100 nF			70	mA
V_{CPLOW}	Charge pump low threshold voltage		VS + 3.7	VS + 4.2	VS + 4.5	V
f_{CP}	Charge pump frequency	CPWBE=0		500		kHz
		CPWBE=1		500 ±62.5		kHz
C_{FLY}	Fly capacitor		50	100	150	nF

Table 14: PWM control

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{PWM}	Frequency of PWM cycles	FREQ[1:0] = 00b; MWBE=0		20		kHz
		FREQ[1:0] = 00b; MWBE=1		19.5 ±0.5		kHz
		FREQ[1:0] = 01b; MWBE=0		30		kHz
		FREQ[1:0] = 01b; MWBE=1		29.2 ±0.8		kHz
		FREQ[1:0] = 1xb; MWBE=0		40		kHz
		FREQ[1:0] = 1xb; MWBE=1		39 ±1		kHz
t_{CC}	Cross current protection time	VS = 13.5 V, SR[1:0] = 11		0.9		µs
		VS = 13.5 V, SR[1:0] = 10		1.2		µs
		VS = 13.5 V, SR[1:0] = 01		1.8		µs
		VS = 13.5 V, SR[1:0] = 00		4.8		µs
t_B	Current comparators blanking time	Tested by scan chain SR[1:0]=11, TBE=0		1		µs
		Tested by scan chain SR[1:0]=11, TBE=1		4		µs
		Tested by scan chain SR[1:0]=10, TBE=0		1.2		µs
		Tested by scan chain SR[1:0]=10, TBE=1		4		µs
		Tested by scan chain SR[1:0]=01, TBE=0		1.8		µs
		Tested by scan chain SR[1:0]=01, TBE=1		4		µs
		Tested by scan chain SR[1:0] = 00		4.0		µs
t_{FT}	Current comparators filter time for current regulation loop	Tested by scan chain FT[1:0]=00, FTOCE=0		0.5		µs
		Tested by scan chain FT[1:0]=00, FTOCE=1		0.7		µs
		Tested by scan chain FT[1:0]=01, FTOCE=0		1		µs
		Tested by scan chain FT[1:0]=01, FTOCE=1		1.2		µs
		Tested by scan chain FT[1:0]=10, FTOCE=0		2		µs
		Tested by scan chain FT[1:0]=10, FTOCE=1		2.2		µs

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
		Tested by scan chain FT[1:0]=11, FTOCE=0		3		µs
		Tested by scan chain FT[1:0]=11, FTOCE=1		3.2		µs
tOC	Overcurrent filter delay time	Tested by scan chain FTOCE=0		0.2	0.2+ 1xtclock	µs
		Tested by scan chain FTOCE=1		0.4	0.4+ 1xtclock	µs
VSR	Slew rate (dV/dt 30% - 70%) at HS and LS switches with resistive load of 18Ω;	VS = 13.5 V, SR[1:0] = 11		100		V/µs
		VS = 13.5 V, SR[1:0] = 10		70		V/µs
		VS = 13.5 V, SR[1:0] = 01		40		V/µs
		VS = 13.5 V, SR[1:0] = 00		10		V/µs

Table 15: Clock characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{SYS}	System clock frequency		—	10	—	MHz

Table 16: Digital inputs CTRL1, CTRL2, CTRL3, EN

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{INL}	Input voltage low threshold				0.8	V
V_{INH}	Input voltage high threshold		2.0			V
V_{INHY}	Input hysteresis		0.2	0.4		V
I_{IN}	Input pull down current	V_{IN} = 2.0 V	5	30	60	µA
R_{INEN}	Input pull down resistance at input EN		50	100	200	kΩ
t_{START}	Device starting time after EN is set (charge pump powered-up and SPI registers accessible)				1.5	ms

Table 17: Coil voltage acquisition

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VCVIN	Coil voltage measurement range				28	V
VCVRES	ADC LSB resolution	6 V ≤ V_S ≤ 27 V		27		mV
CVA	Coil voltage measurement total unadjusted error	6 V ≤ V_S ≤ 27 V		±3		LSB

The coil voltage is sampled with 10 bit resolution in the range from 0 V to 24 V.

Table 18: Digital outputs DOUT1, DOUT2

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VOUTL	Output low level	I_{OUT} = 4mA		0.2	0.5	V
VOUTH	Output high level	I_{OUT} = -4mA	VDD-0.5	VDD-0.2		V
I_{LK}	Output leakage current		-1		1	µA

4.6 SPI bus (CSN, SCK, SDI, SDO)

Figure 27: SPI transfer timing diagram

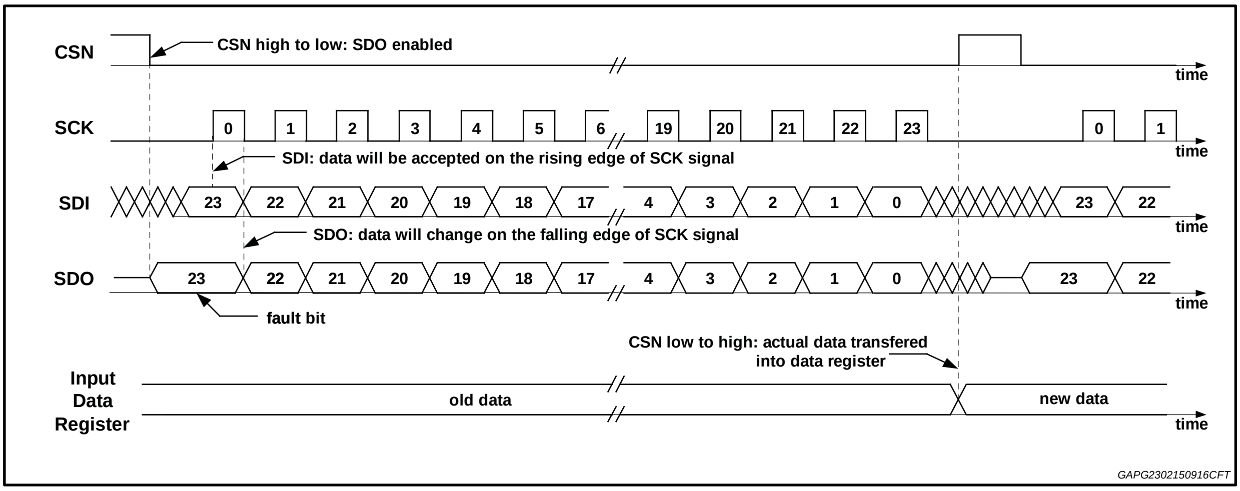


Table 19: CSN, SCK, SDI input

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VINL	Input voltage low threshold				0.8	V
VINH	Input voltage high threshold		2.0			V
VINHY	Input hysteresis		0.2	0.4		V
RINCSN	CSN pull up resistor	V_{IN} = 0.8 V	50	100	200	kΩ
IINSCK	SCK pull down current	V_{IN} = 2.0 V	5	30	60	µA
IINSDI	SDI pull down current	V_{IN} = 2.0 V	5	30	60	µA

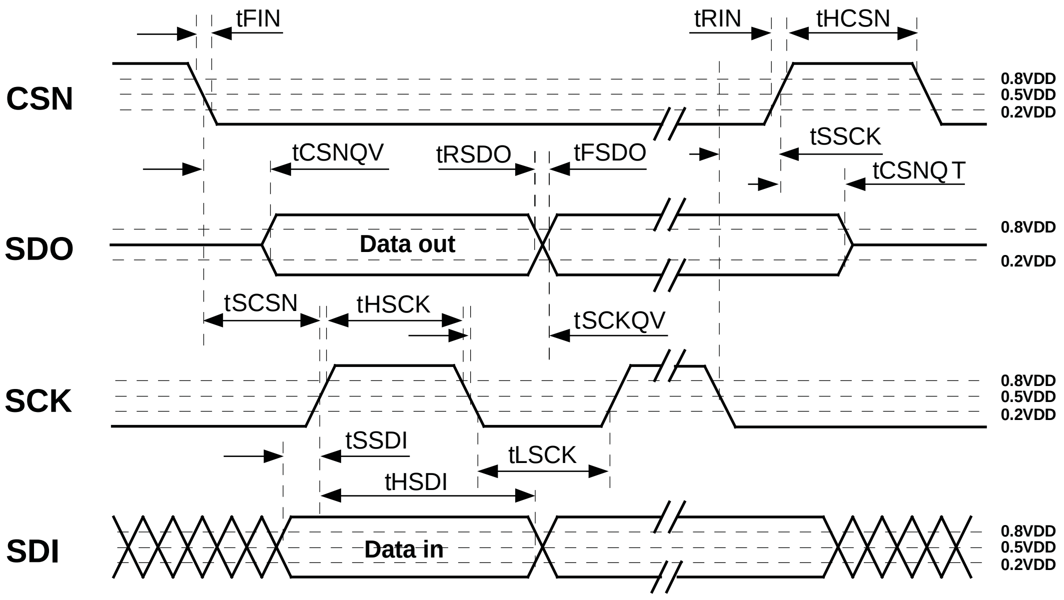
Table 20: SDO output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VOUTL	Output low level	I_{OUT} = 4 mA		0.2	0.5	V
VOUTH	Output high level	I_{OUT} = -4 mA	VDD-0.5	VDD-0.2		V
ILK	Output leakage current		-1		1	µA

Table 21: SPI timing

Symbol	Parameter	Test condition	Min.	Typ.	Max	Unit
t_{SCK}	Serial clock period		250			ns
t_{HSCK}	SCK high time		100			ns
t_{LSCK}	SCK low time		100			ns
t_{RIN}	CSN, SCK, SDI rise time	f_{SCK} = 4 MHz			25	ns
t_{FIN}	CSN, SCK, SDI fall time	f_{SCK} = 4 MHz			25	ns
t_{HCSN}	CSN high time		6			µs
t_{SCSN}	CSN setup time, CSN low before SCK rising		100			ns
t_{SSCK}	SCK setup time, SCK low before CSN rising		100			ns
t_{SSDI}	SDI setup time before SCK rising		25			ns
t_{HSDI}	SDI hold time		25			ns
t_{CSNQV}	CSN falling until SDO valid	C_{OUT} = 50 pF; I_{OUT} = ±1 mA			100	ns
t_{SCNQT}	CSN rising until SDO tristate	C_{OUT} = 50 pF; I_{OUT} = ±4 mA			100	ns
t_{SCKQV}	SCK falling until SDO valid	C_{OUT} = 50 pF			60	ns
t_{RSDO}	SDO rise time	C_{OUT} = 50 pF; I_{OUT} = -1 mA		50	100	ns
t_{FSDO}	SDO fall time	C_{OUT} = 50 pF; I_{OUT} = 1 mA		50	100	ns
t_{CSNLTO}	CSN low timeout		20	35	50	ms

Figure 28: SPI timing diagram



tFIN : CSN, SCK, SDI fall time
tRIN : CSN, SCK, SDI rise time
tHCSN : CSN high time
tCSNQV : CSN falling until SDO valid
tRSDO : SDO rise time
tFSDO : SDO fall time
tSSCK : SCK setup time before CSN rising
tCSNQT : CSN rising until SDO tristate
tSCSN : CSN setup time before SCK rising
tHSCK : SCK high time
tSCKQV : SCK falling until SDO valid
tSSDI : SDI setup time before SCK rising
tHSDI : SDI hold time
tLSCK : SCK low time

GAPG2302150929CFT

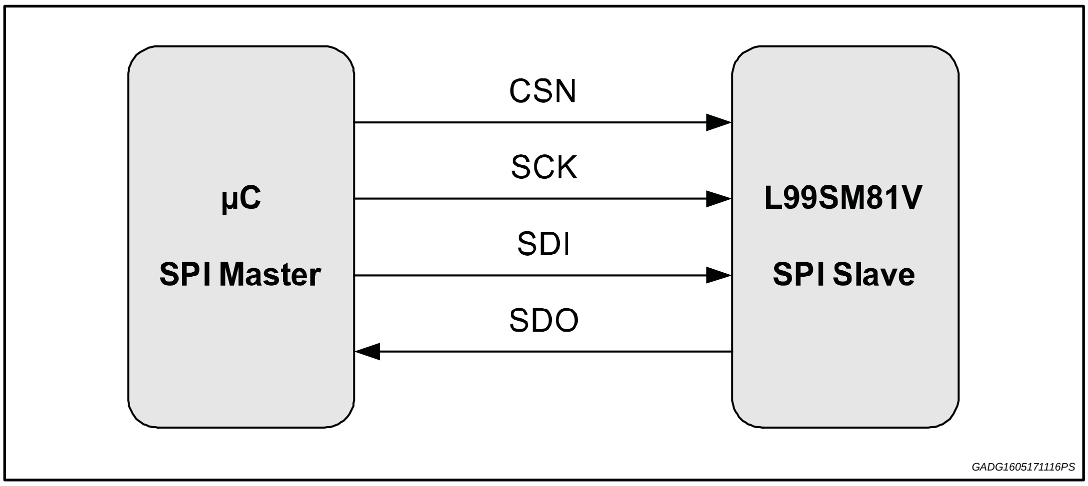
5 ST SPI protocol

The ST-SPI is a standard used in ST Automotive ASSP devices. Therefore the here standardized SPI is described from SPI-Slave-Device point of view.

The ST-SPI will allow usage of generic software to operate the devices while maintaining the required flexibility to adapt it to the individual functionality of a particular product. In addition to that, failsafe mechanisms are implemented to protect the communication from external influences and wrong or unwanted usage.

5.1 Physical layer

Figure 29: SPI pin description



The physical layer description can be found in the functional description *Section 2.14: "Serial peripheral interface (ST SPI standard)"* and in the electrical characteristics *Section 4.6: "SPI bus (CSN, SCK, SDI, SDO)"*

5.2 Protocol

5.2.1 SDI frame

The data-in frame consists of 24 bits (OpCode + Address + Data).

The first two transmitted bits (MSB, MSB-1) contain the Operation Code which represents the instruction to be performed. The following 6 bits (MSB-2 to MSB-7) represent the address on which the operation will be performed.

The subsequent 16 bits contain the payload data.

Figure 30: SDI frame

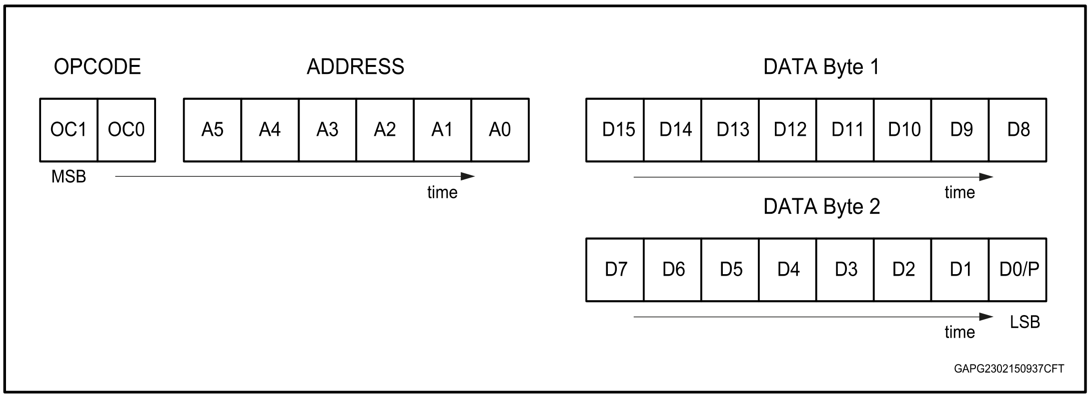


Table 22: Operation codes

OC1	OC0	Description
0	0	Write Operation
0	1	Read Operation
1	0	Read & Clear Operation
1	1	Read Device Information

The operation code is used to distinguish between different access modes to the registers of the slave device.

A Write Operation will lead to a modification of the addressed data by the payload if a write access is allowed (e.g. Control Register, valid data). Besides this a shift out of the content (data present at Communication Start) of the registers is performed.

A Read Operation shifts out the data present in the addressed register at Communication Start. The payload data will be ignored and internal data will not be modified. In this device a Burst Read can be performed.

A Read & Clear operation will lead to a clear of the addressed status bits. The bits to be cleared are defined first by address and secondly by the payload bits set to ‘1’. Besides this a shift out of the content (data present at Communication Start) of the registers is performed.

Status registers which change status during communication could be cleared by the current Read & Clear Operation and are neither reported in the current communication nor in the following communications. To avoid a loss of any reported status it is recommended to clear selectively the bits of the status registers, coherently with what reported in previous communications.

Followed by the two OpCode bits, the six address bits are a fixed part of the communication frame. The six address bits, in combination with the OpCode, give access to a 2x64 word wide address range.

Table 23: Device application access

Operating code	
OC1	**OC0**
0	0
0	1
1	0

Table 24: Device information read access

Operating code	
OC1	**OC0**
1	1

Table 25: Address range

Address	Data	Type		Address	Data	Type
3FH	Advanced operation code			3FH	Advanced operation code	
3EH		R/W or C		3EH	<GSB options>	R
					...	
				11H	<WD type>	R
				10H		R
				03H	<Device number 2>	R
				02H	<Device number 1>	R
				01H	<Device family>	R
00H		R/W or C		00H	<Company code>	R

The data contained in the Device Information address range is predefined by the ST SPI standard. The data is read-only and represents device-specific data like Device ID and SPI settings.

Besides the separate writing of all control registers and the bitwise clearing of all status registers, there are two Advanced Operation Codes that can be used to set all control registers to their default value and to clear all status registers.

A 'set all control registers to default' command is performed when an OpCode '11' at address b'111111 is performed.

Please consider that potential device-specific write-protected registers cannot be cleared with this command and therefore a device Power-On-Reset is needed.

A 'clear all status registers' command is performed when an OpCode '10' at address b'111111 is performed.

The Payload (data byte 1 to data byte 2) is the data transferred to the slave device with every SPI communication. The Payload always follows the OpCode and the Address bits.

For write access the Payload represents the new data written to the address registers. For Read & Clear operations the Payload indicates the clearing of specific bit in a Status Register in case of a '1' at the corresponding bit position.

For a Read Operation the Payload is not used. For functional safety reasons it is recommended to set unused Payload to '0'.

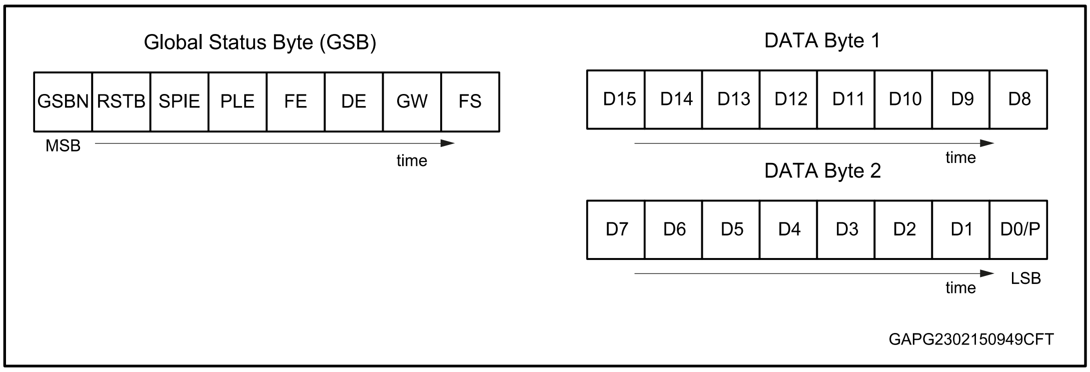
5.2.2 SDO Frame

The Data-Out Frame consists of 24 bits (GSB+Data).

The first eight transmitted bits contain device-related status information and are latched into the shift register at the time of the Communication Start. These 8 bits are transmitted at every SPI transaction.

The subsequent bytes contain the payload data and are latched into the shift register with the eighth positive SCK edge. This could lead to an inconsistency of data between the GSB and Payload due to different shift register load times. Anyhow, no unwanted Status Register clear should appear, as status information should just be cleared with a dedicated bit clear after read.

Figure 31: SDO frame



The Global Status Byte is described here below.

The Payload (DATA Byte 1 & 2) is the data transferred from the slave device with every SPI communication to the microcontroller. The Payload always follows the OpCode and the Address bit of the actual shifted in data (In-Frame-Response).

5.2.2.1 Global Status Byte GSB

Table 26: Global Status Byte GSB

SDO frame: Global Status Byte								
	Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
Bit name	GSBN	RSTB	SPIE	-	FE	DE	GW	-
Default	1	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 27: Global Status Byte GSB (bit description)

SDO frame	Name	Description
Bit 23	GSBN	Global Status Bit Not The GSBN is a logically NOR combination of Bit 0 to Bit 6. This bit can also be used as Global Status Flag without starting a complete communication frame as it is present directly after pulling CSN low. GSBN = 1 (No Error) GSBN = 0 (Error)
Bit 22	RSTB	Reset Bit RSTB is set to one after any POR (either VDD POR or Vreg POR), it is reset after first valid SPI transfer
Bit 21	SPIE	SPI Error The SPIE is a logical OR combination of errors related to a wrong SPI communication. Beside the SCK count and SDI stuck at errors, also the parity error is reported here. The SPIE is automatically cleared by a valid SPI communication.
Bit 20	-	Reserved
Bit 19	FE	Functional Error The FE is a logical OR combination of errors coming from application specific functional items: • Overcurrent outputs status bits (OC) • Voltage regulator V5V Overvoltage (V5VOV) • Voltage regulator V5V Short (V5VUV) • Stall Detection (SDF)
Bit 18	DE	Device Error The DE is a logical OR combination of errors related to device specific blocks. For the L99SM81V this includes • Overvoltage status bits (VSOV, VREGOV) • Undervoltage status bit (VSUV) • Charge Pump Fail status bit (CPFAIL) • Thermal shutdown status bit (TSD)
Bit 17	GW	Global Warning The GW is a logical OR combination of all warning flags: • VREG Undervoltage warning (VREGUV) • Voltage Regulator V5V undervoltage warning (V5UVW) • Thermal warning (TW) • Open Load (OL)
Bit 16	-	Reserved

5.3 Address and data definition

5.3.1 Device Information Register

The Device Information Register can be read by using OpCode ‘11’. After shifting out the GSB, the 8-bit wide payload will be transmitted. After shifting out the GSB followed by the 8-bit wide payload, a series of ‘0’ are shifted out at the SDO pin.

Table 28: Device information read access operation code

Operating code	
OC1	OC0
1	1

Table 29: Device information registers

Address	Data	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FH	<Advanced option>									
3EH	<GSB options>	R	0	0	0	Masking bits for GSB				
...	...		...							
20H	<SPI CPHA test>	R	0	1	0	1	0	1	0	1
1FH	<WD bit pos. 14>opt.	R	Not used							
...	...	R								
14H	<WD bit pos. 2>opt.	R								
13H	<WD bit pos. 1>opt.	R								
12H	<WD type 2>	R								
11H	<WD type 1>	R								
10H	<SPI mode>	R	Please refer to section “SPI mode”							
...	...	R	...							
0AH	<Silicon version>	R	Major silicon change revision no.				Minor silicon change revision no.			
09H	<Device number 8>	R	00H							
08H	<Device number 7>	R	00H							
07H	<Device number 6>	R	00H							
06H	<Device number 5>	R	00H							
05H	<Device number 4>	R	04H							
04H	<Device number 3>	R	4AH							
03H	<Device number 2>	R	41H							
02H	<Device number 1>	R	55H							
01H	<Device family>	R	01H							
00H	<Company code>	R	00H							

The Device Identification Registers (00H → 0AH) represent a unique number identifying device part-number.

By reading out the <SPI Mode> register, general information of SPI usage of the Device Application Registers can be read.

Table 30: SPI mode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BR	DL2	DL1	DL0	0	0	S1	S0

Table 31: SPI Burst Read

Bit 7	Description
0	BR disabled
1	BR enabled

The SPI Burst Read bit indicates if a burst read operation is implemented. The intention of a Burst Read is e.g. used to perform a device internal memory dump to the SPI Master.

The start of the Burst Read is like a normal Read Operation. The difference is that after the SPI Data Length the CSN is not pulled high and the SCK will be continuously clocked. When the normal SCK max count is reached (SPI Data Length), the consecutive addressed data will be latched into the shift register. This procedure is performed every time when the SCK payload length is reached.

In case the automatic increment address is not used by the device, undefined data is shifted out. An automatic address overflow is implemented when address 3FH is reached.

The SPI Burst Read is limited by the CSN low timeout.

The L99SM81V features SPI Burst Read.

The SPI Data Length value indicates the length of the SCK count monitor which is running for all accesses to the Device Application Register. In case of a communication frame with an SCK count not equal to the reported one, this will lead to a SPI Error and the data will be rejected.

Table 32: SPI data length

Bit 6	Bit 5	Bit 4	Description
DL2	DL1	DL0	
0	0	0	Invalid
0	0	1	16-bit SPI
0	1	0	24-bit SPI
...	...	...	…
1	1	1	64-bit SPI

The default frame size of the L99SM81V is 24 bits, so the SPI Data Length bits are read as ‘010’.

Table 33: SPI data consistency check

Bit 1	Bit 0	Description
S1	S0	
0	0	Not used
0	1	Parity used
1	0	CRC used

Bit 1	Bit 0	Description
1	1	Invalid

For the L99SM81V, a Data Consistency Check by parity check is implemented, therefore these bits are read as ‘01’. An odd parity bit is used and it is calculated over the complete communication frame.

The GSB Options byte indicates that device-specific status information is used instead of the predefined one. In case a bit of the GSB is not used, it has to be fixed to ‘0’ value and is indicated by a logical ‘1’ in the GSB Options byte.

5.3.2 Device Application Registers

The Device Application Registers are all registers accessible using OpCode ‘00’, ‘01’ and ‘10’.

An access to an unused address will not lead to any error, but should be prevented. Any data read from an unused address is not defined.

5.4 Protocol failure detection

To realize a protocol which fulfills certain failsafe requirements, a basic set of failure detection mechanisms is implemented.

5.4.1 Clock monitor

During communication (CSN low to high phase) a clock monitor counts the valid SCK clock edges. If the SCK edges do not correlate with the SPI Data Length, an SPIE is reported with the next command and the current communication is rejected.

By accessing the Device Information Registers (OpCode = ‘11’), the Clock Monitor is set to a minimum of 16 SCK edges plus a multiple of 8 (e.g. 16, 24, 32).

Providing no SCK edge during a CSN low to high phase is not recognized as an SPIE. For a SPI Burst Read also the SPI Data Length plus multiple number of Payload SCK edges are assumed as a valid communication.

5.4.2 SCK Polarity (CPOL) check

To detect wrong polarity access on SCK, the internal clock monitor is used. Providing first a negative edge on SCK during communication (CSN low to high phase) or a positive edge at last will lead to an SPI Error being reported in the next communication and the current data is rejected.

5.4.3 SCK Phase (CPHA) check

To verify that the SCK phase of the SPI master is set correctly a special Device Information Register is implemented. By reading this register the data must be 55H. In case AAH is read, the CPHA setting of the SPI master is wrong and a proper communication cannot be guaranteed.

5.4.4 CSN timeout

By pulling CSN low, the SDO is set active and leaves the tri-state condition. To ensure communication between other SPI devices within the same bus even in case of CSN stuck at low, a CSN timeout is implemented. By pulling CSN low, an internal timer is started. After the timer end is reached, the current communication is rejected and the SDO is set to tri-state condition. This error is not reported in any specific status register.

5.4.5 Data Stuck

- SDI stuck at GND
  As a command with all data bits set to ‘0’ and OpCode ‘00’ on address b’000000 cannot be distinguished from an SDI stuck-at-GND error, this command is not allowed. In case a stuck-at-GND error is detected, the communication will be rejected and the SPIE will be set in the next communication cycle.
- SDI stuck at HIGH
  As a command with all data bits set to ‘1’ and OpCode ‘11’ on address b’111111 cannot be distinguished from an SDI stuck-at-HIGH error, this command is not allowed. In case a stuck-at-HIGH error is detected, the communication will be rejected and the SPIE will be set in the next communication cycle.
- SDO stuck
  SDO stuck-at-GND and stuck-at-HIGH errors have to be detected by the SPI master. As the definition of the GSB guarantees at least one bit toggle, a GSB with all bits set to ‘0’ or with all bits set to ‘1’ can be considered as an SDO stuck-at error.

5.5 Implementation remarks

5.5.1 Register change during communication

From an implementation point of view, it is guaranteed that no register change gets lost during communication. In case a register value was changed during a communication, it will be reported with the next communication frame.

5.5.2 GSB and Payload inconsistency

Due to the internal implementation strategy, it may occur that data reported in the GSB does not match data reported in the payload in case the data was changed during GSB shift out. In this case, the payload data is the status quo, as it was loaded later into the SPI shift register.

5.6 Timings

All SPI related timings are defined in *Section 4.6: "SPI bus (CSN, SCK, SDI, SDO)"*.

6 SPI registers

6.1 Register map overview

Table 34: Complete device SPI register table

Address	Name	Bit											
Hex		15	14	13	12	11	10	9	8	7	6	5	4
0x01	*GSR*	VSOV	VSUV	VREGOV	VREGUV	—	CPFAIL	V5UVW	V5VOV	V5VUV	TW	TSD	OL
0x02	*MSR*	OCA1HS	OCA1LS	OCA2HS	OCA2LS	OCB1HS	OCB1LS	OCB2HS	OCB2LS	OLA	OLB	—	—
0x03	*GCR1*	CPWBE	MWBE	—	AOUT1	AOUT0	V5VE	—	—	—	—	MX1	—
0x04	*GCR2*	—	—	—	—	DOUT11	DOUT10	—	DOUT21	DOUT20	—	—	—
0x05	*MCR1*	ME	HOLDM	ASM2	ASM1	ASM0	SM2	SM1	SM0	DIR	PH5	PH4	PH3
0x06	*MCR2*	FREQ1	FREQ0	FTOCE	TBE	FT1	FT0	SR1	SR0	DMR1	DMR0	SDAFW	SDBF
0x07	*MCR3*	CVE	—	D4	D3	D2	D1	D0	SD2	SD1	SD0	CVLUR1	CVLUR
0x08	*MCREF*	HC3	HC2	HC1	HC0	—	—	—	—	—	—	—	CA3
0x09	*MCVA*	—	—	—	—	—	CV9	CV8	CV7	CV6	CV5	CV4	CV3
0x0A	*MCVB*	—	—	—	—	—	CV9	CV8	CV7	CV6	CV5	CV4	CV3
0x0B	*MCVC*	—	—	—	—	—	CV9	CV8	CV7	CV6	CV5	CV4	CV3
0x0C	*MCVD*	—	—	—	—	—	CV9	CV8	CV7	CV6	CV5	CV4	CV3
0x0D	*MCVLLB*	—	—	—	—	—	CVLLB9	CVLLB8	CVLLB7	CVLLB6	CVLLB5	CVLLB4	CVLLB
0x0E	*MCVLLA*	—	—	—	—	—	CVLLA9	CVLLA8	CVLLA7	CVLLA6	CVLLA5	CVLLA4	CVLLA
0x0F	*MCVUL*	—	—	—	—	—	CVUL9	CVUL8	CVUL7	CVUL6	CVUL5	CVUL4	CVUL

6.2 Global Status Register GSR (0x01)

Table 35: Global Status Register GSR

Global Status Register (0x01)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	VSOV	VSUV	VREGOV	VREGUV	—	CPFAIL	V5UVW	V5VOV
Default	0	0	0	0	0	0	0	0
Access	R/C	R/C	R/C	R/C	R	R/C	R/C	R/C
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	V5VUV	TW	TSD	OL	OC	SDF	—	P
Default	0	0	0	0	0	0	0	—
Access	R/C	R/C	R/C	R/C	R/C	R/C	R	—

Table 36: Global Status Register GSR (bit description)

	Name	Description
Bit 15	VSOV	VS Overvoltage error flag When set, it indicates an over-voltage error on VS supply.
Bit 14	VSUV	VS Undervoltage error flag When set, it indicates an under-voltage error on VS supply.
Bit 13	VREGOV	VREG Overvoltage error flag When set, it indicates an over-voltage error on V_{REG} supply.
Bit 12	VREGUV	VREG Undervoltage warning flag When set, it indicates an under-voltage warning on V_{REG} supply.
Bit 11	—	Reserved
Bit 10	CPFAIL	Charge pump error Flag Indicates that safe operation of charge pump cannot be guaranteed
Bit 9	V5UVW	V5V Regulator Undervoltage Warning Flag Indicates that V5V output voltage is below V5V under-voltage warning threshold
Bit 8	V5VOV	V5V Regulator Overvoltage Error Flag Indicates that V5V output voltage exceeds V5V overvoltage error threshold
Bit 7	V5VUV	V5V Regulator Undervoltage Error Flag Indicates that V5V output voltage droped below V5V undervoltage error threshold
Bit 6	TW	Thermal Warning Flag Indicates that device temperature exceeds thermal warning threshold
Bit 5	TSD	Thermal Shutdown Error Flag Indicates that device temperature exceeds thermal shutdown threshold
Bit 4	OL	Open Load Warning Flag This bit is set as soon as either OLA or OLB bit in MSR is set. Clearing this bit automatically results in the clearing of OLA and OLB in MSR
Bit 3	OC	Overcurrent Error Flag This bit is set as soon as any of the bits [15:8] of MSR is set. Clearing this bit automatically results in the clearing of bits [15:8] in MSR.

	Name	Description
Bit 2	SDF	Stall detection Flag This bit is set if CVE is set and sampled coil voltage is out of the range [CVLLAx; CVULx] for a number of consecutive acquisitions (zero current steps) equal to SD[2:0]
Bit 1	—	Reserved
Bit 0	P	Parity bit

6.3 Motor and driver Status Register MSR (0x02)

Table 37: Motor and driver Status Register MSR

Motor and driver Status Register (0x02)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	OCA1HS	OCA1LS	OCA2HS	OCA2LS	OCB1HS	OCB1LS	OCB2HS	OCB2LS
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	OLA	OLB	—	—	CVULF	CVLLAF	CVLLBF	P
Default	0	0	0	0	0	0	0	—
Access	R	R	R	R	R	R	R	—

Table 38: Motor and driver Status Register MSR (bit description)

	Name	Description
Bit 15	OCA1HS	Overcurrent Output A1 High Side Switch Error Flag Indicates overcurrent situation in high side switch of output A1 This bit is automatically cleared by clearing OC bit in GSR
Bit 14	OCA1LS	Overcurrent Output A1 Low Side Switch Error Flag Indicates overcurrent situation in low side switch of output A1 This bit is automatically cleared by clearing OC bit in GSR
Bit 13	OCA2HS	Overcurrent Output A2 High Side Switch Error Flag Indicates overcurrent situation in high side switch of output A2 This bit is automatically cleared by clearing OC bit in GSR
Bit 12	OCA2LS	Overcurrent Output A2 Low Side Switch Error Flag Indicates overcurrent situation in low side switch of output A2 This bit is automatically cleared by clearing OC bit in GSR
Bit 11	OCB1HS	Overcurrent Output B1 High Side Switch Error Flag Indicates overcurrent situation in high side switch of output B1 This bit is automatically cleared by clearing OC bit in GSR
Bit 10	OCB1LS	Overcurrent Output B1 Low Side Switch Error Flag Indicates overcurrent situation in low side switch of output B1 This bit is automatically cleared by clearing OC bit in GSR
Bit 9	OCB2HS	Overcurrent Output B2 High Side Switch Error Flag Indicates overcurrent situation in high side switch of output B2 This bit is automatically cleared by clearing OC bit in GSR
Bit 8	OCB2LS	Overcurrent Output B2 Low Side Switch Error Flag Indicates overcurrent situation in low side switch of output B2 This bit is automatically cleared by clearing OC bit in GSR
Bit 7	OLA	Openload Phase A Warning Flag Indicates that current reference for phase A has not been reached within the programmed delay. This bit is automatically cleared by clearing OL bit in GSR

	Name	Description
Bit 6	OLB	Openload Phase B Warning Flag Indicates that current reference for phase B has not been reached within the programmed delay. This bit is automatically cleared by clearing OL bit in GSR
Bit 5	—	Reserved
Bit 4	—	Reserved
Bit 3	CVULF	Coil Voltage Upper Limit Flag This bit will be updated automatically if the CVE coil voltage enable bit in the motor control register 3 MCR3 is set. It will be set if sampled coil voltage exceeds the limit defined as upper limit (CVUL[9:0]) , it will be reset otherwise
Bit 2	CVLLAF	Coil Voltage Lower Limit 1 Flag This bit will be automatically updated if the CVE coil voltage enable bit in the motor control register 3 MCR3 is set. It will be set if sampled coil voltage underruns the limit defined as lower limit A (CVLLA[9:0]) , it will be reset otherwise
Bit 1	CVLLBF	Coil Voltage Lower Limit 2 Flag This bit will be automatically updated if the CVE coil voltage enable bit in the motor control register 3 MCR3 is set. It will be set if sampled coil voltage underruns the limit defined as lower limit B (CVLLB[9:0]) , it will be reset otherwise
Bit 0	P	Parity bit

6.4 Global Configuration Register 1 GCR1 (0x03)

Table 39: Global Configuration Register 1 GCR1

Global Configuration Register 1 (0x03)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	CPWBE	MWBE	—	AOUT1	AOUT0	V5VE	—	—
Default	0	0	0	0	0	1	0	0
Access	R/W	R/W	R	R/W	R/W	R/W	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	—	—	MX1	—	MX2	MX3_1	MX3_0	P
Default	0	0	1	0	1	0	0	—
Access	R	R	R/W	R	R/W	R/W	R/W	—

Table 40: Global Configuration Register 1 GCR1 (bit description)

	Name	Description
Bit 15	CPWBE	Charge Pump Wobble Frequency Enable 1 = Charge Pump with Spread Spectrum Feature 0 = Fixed Charge Pump Frequency
Bit 14	MWBE	Wobble Frequency Enable 1 = Frequency Generator with Spread Spectrum Feature 0 = Fixed PWM Frequency
Bit 13	—	Reserved
Bit 12	AOUT1	Analog Output selection 00 or 11 = Disabled 01 = Voltage proportional to junction temperature 10 = Band-gap voltage
Bit 11	AOUT0	
Bit 10	V5VE	V5V Voltage Regulator Enable 1 = V5V Voltage Regulator enabled 0 = V5V Voltage Regulator disabled
Bit 9	—	Reserved
Bit 8	—	Reserved
Bit 7	—	Reserved
Bit 6	—	Reserved
Bit 5	MX1	CTRL1 Function Select If this bit is reset the CTRL1 pin is deactivated and phase counter can only be updated through SPI, if it is set the CTRL1 pin holds the STEP function (PH[5:0] bits in read-only)
Bit 4	—	Reserved
Bit 3	MX2	CTRL2 Function Select If this bit is reset the CTRL2 pin is deactivated, DIR bit can only be changed via SPI; if it is set the CTRL2 pin holds the DIR functionality and the DIR bit reflects CTRL2 logic level.
Bit 2	MX3_1	CTRL3 Function Select

	Name	Description
Bit 1	MX3_0	00 or 11 = OFF 01 = SMODE 10 = HOLD (see also *Section 2.10: "Control pins (CTRLx)"*)
Bit 0	P	Parity bit

6.5 Global Configuration Register 2 GCR2 (0x04)

Table 41: Global Configuration Register 2 GCR2

Global Configuration Register 2 (0x04)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	—	—	—	—	DOUT11	DOUT10	—	DOUT21
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R	R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	DOUT20	—	—	—	—	—	—	P
Default	0	0	0	0	0	0	0	—
Access	R/W	R	R	R	R	R	R	—

Table 42: Global Configuration Register 2 GCR2 (bit description)

	Name	Description
Bit 15	—	Reserved
Bit 14	—	Reserved
Bit 13	—	Reserved
Bit 12	—	Reserved
Bit 11	DOUT11	DOUT1 Function Select 00 = OFF; 01 = CVRDY; 10 = CVLL; 11 = CVRUN
Bit 10	DOUT10	
Bit 9	—	Reserved
Bit 8	DOUT21	DOUT2 Function Select 00 = OFF; 01 = PWM; 10 = ERR; 11 = EC
Bit 7	DOUT20	
Bit 6	—	Reserved
Bit 5	—	Reserved
Bit 4	—	Reserved
Bit 3	—	Reserved
Bit 2	—	Reserved
Bit 1	—	Reserved
Bit 0	P	Parity bit

6.6 Motor Control Register 1 MCR1 (0x05)

Table 43: Motor Control Register 1 MCR1

Motor Control Register 1 (0x05)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	ME	HOLDM	ASM2	ASM1	ASM0	SM2	SM1	SM0
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	DIR	PH5	PH4	PH3	PH2	PH1	PH0	P
Default	0	0	0	0	0	0	0	—
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

Table 44: Motor Control Register 1 MCR1 (bit description)

	Name	Description
Bit 15	ME	Motor Enable When this bit is reset all switches are off setting the outputs in high impedance state. When this bit is set, the outputs are controlled according to the selected operating mode.
Bit 14	HOLDM	HOLD mode 0: HOLD mode disabled 1: HOLD mode enabled If MX3 = 10b the bit is read-only and reflects CTRL3 input logic state. If SDF and AHMSD bits are set, then SDF must be cleared before HOLDM can be cleared
Bit 13	ASM2	Alternative Step Mode (active step mode if MX1 is set and MX3 = 01b and CTRL3 is high) 000, 101, 110, 111: 1/16th microstep; 001: 1/8th microstep; 010: ministep; 011: halfstep; 100: fullstep
Bit 12	ASM1	
Bit 11	ASM0	
Bit 10	SM2	Step Mode (active step mode in following cases: MX1 is set and MX3 is different from 01b; MX1 is set and MX3 is equal to 01b and CRTL3 pin is low) 000, 101, 110, 111: 1/16th microstep; 001: 1/8th microstep; 010: ministep; 011: halfstep; 100: fullstep
Bit 9	SM1	
Bit 8	SM0	
Bit 7	DIR	Direction This bit defines the action to be taken when MX1 is set and a rising edge on input CTRL1 is detected: 0: increment phase counter 1: decrement phase counter If MX2 is reset, this bit can only be modified through SPI, if MX2 is set this bit can only be altered by CTRL2 pin and the status of this bit reflects the logic state of CTRL2 pin.

	Name	Description
Bit 6	PH5	Step (Phase) Counter [5..0] These bits reflect the applied angular step position ("000000" = 0°, "011111" = 180°) and determine the current profiles to be applied to the motor phases. The bits are read-only if MX1 bit is set in GCR1 (see also *Section 2.6: "Stepping modes and step update"*). In case bit MX1=0, a new Phase counter value (written by SPI) becomes effective and hence can be read via SPI only after the next PWM period begins
Bit 5	PH4	
Bit 4	PH3	
Bit 3	PH2	
Bit 2	PH1	
Bit 1	PH0	
Bit 0	P	Parity bit

6.7 Motor Control Register 2 MCR2 (0x06)

Table 45: Motor Control Register 2 MCR2

Motor Control Register 2 (0x06)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	FREQ1	FREQ0	FTOCE	TBE	FT1	FT0	SR1	SR0
Default	0	0	0	0	1	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	DMR1	DMR0	SDAFW	SDBFW	OLDLY	DMH	—	P
Default	0	0	0	0	0	0	0	—
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	—

Table 46: Motor Control Register 2 MCR2 (bit description)

	Name	Description
Bit 15	FREQ1	PWM Clock Frequency 00: 20kHz 01: 30kHz 1x: 40kHz
Bit 14	FREQ0	
Bit 13	FTOCE	If this bit is set, both tFT and tOC filtering time are extended by two system clock cycles (200ns typical)
Bit 12	TBE	If this bit is set, tB time is extended to 4us indipendently from SR[1:0] settings
Bit 11	FT1	Current comparators output filter time This filtering time t_{FT} is applied on current comparator output to avoid false triggering of current regulation loop 00: 0.5µs 01: 1.0µs 10: 2.0µs 11: 3.0µs
Bit 10	FT0	
Bit 9	SR1	Slew Rate 00: 10V/µs 01: 40V/µs 10: 70V/µs 11: 100V/µs
Bit 8	SR0	
Bit 7	DMR1	Decay Mode in RUN mode 00: Auto Decay mode 1 11: Auto Decay mode 2 01: Slow Decay Mode always applied 10: Mixed decay mode always applied
Bit 6	DMR0	
Bit 5	SDAFW	Slow Decay Freewheeling Path (Phase A) 0: High Side Freewheeling 1: Low Side Freewheeling
Bit 4	SDBFW	Slow Decay Freewheeling Path (Phase B) 0: High Side Freewheeling 1: Low Side Freewheeling

	Name	Description
Bit 3	OLDLY	Open load detection time 0: 30ms 1: 60ms
Bit 2	DMH	Decay Mode in HOLD mode 0: Slow Decay Mode always applied 1: Mixed decay mode always applied
Bit 1	—	Reserved
Bit 0	P	Parity bit

6.8 Motor Control Register 3 MCR3 (0x07)

Table 47: Motor Control Register 3 MCR3

Motor Control Register 3 (0x07)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	CVE	—	D4	D3	D2	D1	D0	SD2
Default	0	0	0	0	0	0	0	0
Access	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	SD1	SD0	CVLUR1	CVLUR0	AHMSD	—	—	P
Default	0	0	0	0	0	0	0	—
Access	R/W	R/W	R	R	R/W	R	R	—

Table 48: Motor Control Register 3 MCR3 (bit description)

	Name	Description
Bit 15	CVE	Coil Voltage Capture Enable If this bit is set coil voltage will be captured according to selected capture mode. If this bit is cleared no voltage will be captured.
Bit 14	—	Reserved
Bit 13	D4	Coil Voltage Timing This value represents the time - expressed in PWM periods - between the beginning of a zero current step and the moment where the coil voltage is sampled. This number has to be greater than 1. If D4..D0 = '00000' then the voltage is automatically sampled at the end of the zero current step.
Bit 12	D3	
Bit 11	D2	
Bit 10	D1	
Bit 9	D0	
Bit 8	SD2	Stall detection bits If CVE bit is set, SD[2:0] represent the number of consecutive times the sampled coil voltage value has to be out of the range [CVLLAx; CVULx] before SDF bit is set. Depending on AHMSD bit, HOLD mode could also be automatically entered. Setting SD[2:0] to 000b is equivalent to 001b.
Bit 7	SD1	
Bit 6	SD0	
Bit 5	CVLUR1	Coil voltage latest update register It contains the pointer to latest update coil voltage register (MCVx) 00: MCVA 01: MCVB 10: MCVC 11: MCVD
Bit 4	CVLUR0	
Bit 3	AHMSD	Automatic HOLD mode on stall detection If this bit is set - as soon as a stall is detected setting the SDF bit - HOLDM bit is then automatically set and HOLD mode entered. If this bit is reset, HOLD mode is not automatically entered (HOLDM bit not automatically set) on a stall detection event (SDF bit set).
Bit 2	—	Reserved
Bit 1	—	Reserved
Bit 0	P	Parity bit

6.9 Motor current reference register MCREF (0x08)

Table 49: Motor current reference register MCREF

Motor Current reference register (0x08)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	HC3	HC2	HC1	HC0	—	—	—	—
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	—	—	—	CA3	CA2	CA1	CA0	P
Default	0	0	0	0	0	0	0	—
Access	R	R	R	R/W	R/W	R/W	R/W	—

Table 50: Motor Current reference register MCREF (bit description)

	Name	Description
Bit 15	HC3	Full scale motor current in HOLD mode Depending on the value of bits HC[3:0], the full scale current used in HOLD mode to generate motor current references is changed according to data reported in the electrical characteristics section of this document
Bit 14	HC2	
Bit 13	HC1	
Bit 12	HC0	
Bit 11	—	Reserved
Bit 10	—	Reserved
Bit 9	—	Reserved
Bit 8	—	Reserved
Bit 7	—	Reserved
Bit 6	—	Reserved
Bit 5	—	Reserved
Bit 4	CA3	Full scale motor current in RUN mode Depending on the value of bits CA[3:0], the full scale current used in RUN mode to generate motor current references is changed according to data reported in the electrical characteristics section of this document
Bit 3	CA2	
Bit 2	CA1	
Bit 1	CA0	
Bit 0	P	Parity bit

6.10 Motor Coil Voltage 0° MCVA (0x09)

Table 51: Motor Coil Voltage 0° MCVA

Motor Coil voltage 0° (0x09)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	—	—	—	—	—	CV9	CV8	CV7
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	CV6	CV5	CV4	CV3	CV2	CV1	CV0	P
Default	0	0	0	0	0	0	0	—
Access	R	R	R	R	R	R	R	—

Table 52: Motor Coil Voltage 0° MCVA (bit description)

	Name	Description
Bit 15	—	Reserved
Bit 14	—	Reserved
Bit 13	—	Reserved
Bit 12	—	Reserved
Bit 11	—	Reserved
Bit 10	CV9	Coil voltage digital value at 0° Averaged coil voltage measurement corresponding to the micro-step with phase counter equal to 0. Full scale referred to maximum V_S operating range (28V)
Bit 9	CV8	
Bit 8	CV7	
Bit 7	CV6	
Bit 6	CV5	
Bit 5	CV4	
Bit 4	CV3	
Bit 3	CV2	
Bit 2	CV1	
Bit 1	CV0	
Bit 0	P	Parity bit

6.11 Motor Coil Voltage 90° MCVB (0x0A)

Table 53: Motor Coil Voltage 90° MCVB

Motor Coil voltage 90° (0x0A)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	—	—	—	—	—	CV9	CV8	CV7
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	CV6	CV5	CV4	CV3	CV2	CV1	CV0	P
Default	0	0	0	0	0	0	0	—
Access	R	R	R	R	R	R	R	—

Table 54: Motor Coil Voltage 90° MCVB (bit description)

	Name	Description
Bit 15	—	Reserved
Bit 14	—	Reserved
Bit 13	—	Reserved
Bit 12	—	Reserved
Bit 11	—	Reserved
Bit 10	CV9	Coil voltage digital value at 90° Averaged coil voltage measurement corresponding to the microstep with phase counter equal to 16. Full scale referred to maximum V_S operating range (28 V)
Bit 9	CV8	
Bit 8	CV7	
Bit 7	CV6	
Bit 6	CV5	
Bit 5	CV4	
Bit 4	CV3	
Bit 3	CV2	
Bit 2	CV1	
Bit 1	CV0	
Bit 0	P	Parity bit

6.12 Motor Coil Voltage 180° MCVC (0x0B)

Table 55: Motor Coil Voltage 180° MCVC

Motor Coil voltage 180° (0x0B)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	—	—	—	—	—	CV9	CV8	CV7
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	CV6	CV5	CV4	CV3	CV2	CV1	CV0	P
Default	0	0	0	0	0	0	0	—
Access	R	R	R	R	R	R	R	—

Table 56: Motor Coil Voltage 180° MCVC (bit description)

	Name	Description
Bit 15	—	Reserved
Bit 14	—	Reserved
Bit 13	—	Reserved
Bit 12	—	Reserved
Bit 11	—	Reserved
Bit 10	CV9	Coil voltage digital value at 180° Averaged coil voltage measurement corresponding to the micro-step with phase counter equal to 32. Full scale referred to maximum Vs operating range (28V)
Bit 9	CV8	
Bit 8	CV7	
Bit 7	CV6	
Bit 6	CV5	
Bit 5	CV4	
Bit 4	CV3	
Bit 3	CV2	
Bit 2	CV1	
Bit 1	CV0	
Bit 0	P	Parity bit

6.13 Motor Coil Voltage 270° MCVD (0x0C)

Table 57: Motor Coil Voltage 270° MCVD

Motor Coil voltage 270° (0x0C)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	—	—	—	—	—	CV9	CV8	CV7
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	CV6	CV5	CV4	CV3	CV2	CV1	CV0	P
Default	0	0	0	0	0	0	0	—
Access	R	R	R	R	R	R	R	—

Table 58: Motor Coil Voltage 270° MCVD (bit description)

	Name	Description
Bit 15	—	Reserved
Bit 14	—	Reserved
Bit 13	—	Reserved
Bit 12	—	Reserved
Bit 11	—	Reserved
Bit 10	CV9	Coil voltage digital value at 270° Averaged coil voltage measurement corresponding to the micro-step with phase counter equal to 48. Full scale referred to maximum Vs operating range (28V)
Bit 9	CV8	
Bit 8	CV7	
Bit 7	CV6	
Bit 6	CV5	
Bit 5	CV4	
Bit 4	CV3	
Bit 3	CV2	
Bit 2	CV1	
Bit 1	CV0	
Bit 0	P	Parity bit

6.14 Motor Coil Voltage Low Limit B MCVLLB (0x0D)

Table 59: Motor Coil Voltage Low Limit B MCVLLB

Motor Coil Voltage Low Limit B Register (0x0D)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	—	—	—	—	—	CVLLB9	CVLLB8	CVLLB7
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	CVLLB6	CVLLB5	CVLLB4	CVLLB3	CVLLB2	CVLLB1	CVLLB0	P
Default	0	0	0	0	0	0	0	—
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

Table 60: Motor Coil Voltage Low Limit B MCVLLB (bit description)

	Name	Description
Bit 15	—	Reserved
Bit 14	—	Reserved
Bit 13	—	Reserved
Bit 12	—	Reserved
Bit 11	—	Reserved
Bit 10	CVLLB9	Coil Voltage Lower Limit B Lower threshold B for coil voltage value. CVLLBF bit is set if latest coil voltage measurement falls below this threshold, reset otherwise.
Bit 9	CVLLB8	
Bit 8	CVLLB7	
Bit 7	CVLLB6	
Bit 6	CVLLB5	
Bit 5	CVLLB4	
Bit 4	CVLLB3	
Bit 3	CVLLB2	
Bit 2	CVLLB1	
Bit 1	CVLLB0	
Bit 0	P	Parity bit

6.15 Motor Coil Voltage Low Limit A MCVLLA (0x0E)

Table 61: Motor Coil Voltage Low Limit A MCVLLA

Motor Coil Voltage Low Limit A Register (0x0E)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	—	—	—	—	—	CVLLA9	CVLLA8	CVLLA7
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	CVLLA6	CVLLA5	CVLLA4	CVLLA3	CVLLA2	CVLLA1	CVLLA0	P
Default	0	0	0	0	0	0	0	—
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

Table 62: Motor Coil Voltage Low Limit A MCVLLA (bit description)

	Name	Description
Bit 15	—	Reserved
Bit 14	—	Reserved
Bit 13	—	Reserved
Bit 12	—	Reserved
Bit 11	—	Reserved
Bit 10	CVLLA9	Coil Voltage Lower Limit A Lower threshold A for coil voltage value. CVLLAF bit is set if latest coil voltage measurement falls below CVLLA[9:0] threshold, reset otherwise.
Bit 9	CVLLA8	
Bit 8	CVLLA7	
Bit 7	CVLLA6	
Bit 6	CVLLA5	
Bit 5	CVLLA4	
Bit 4	CVLLA3	
Bit 3	CVLLA2	
Bit 2	CVLLA1	
Bit 1	CVLLA0	
Bit 0	P	Parity bit

6.16 Motor Coil Voltage Upper Limit MCVUL (0x0F)

Table 63: Motor Coil Voltage Upper Limit MCVUL

Motor Coil Voltage Upper Limit Register (0x0F)								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Bit name	—	—	—	—	—	CVUL9	CVUL8	CVUL7
Default	0	0	0	0	0	1	1	1
Access	R	R	R	R	R	R/W	R/W	R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Bit name	CVUL6	CVUL5	CVUL4	CVUL3	CVUL2	CVUL1	CVUL0	P
Default	1	1	1	1	1	1	1	—
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

Table 64: Motor Coil Voltage Upper Limit MCVUL (bit description)

	Name	Description
Bit 15	—	Reserved
Bit 14	—	Reserved
Bit 13	—	Reserved
Bit 12	—	Reserved
Bit 11	—	Reserved
Bit 10	CVUL9	Coil Voltage Upper Limit Upper threshold for coil voltage value. CVULF bit is set if latest coil voltage measurement exceeds CVUL[9:0] threshold, reset otherwise.
Bit 9	CVUL8	
Bit 8	CVUL7	
Bit 7	CVUL6	
Bit 6	CVUL5	
Bit 5	CVUL4	
Bit 4	CVUL3	
Bit 3	CVUL2	
Bit 2	CVUL1	
Bit 1	CVUL0	
Bit 0	P	Parity bit

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

7.1 QFN40L package information

Figure 32: QFN40L package outline

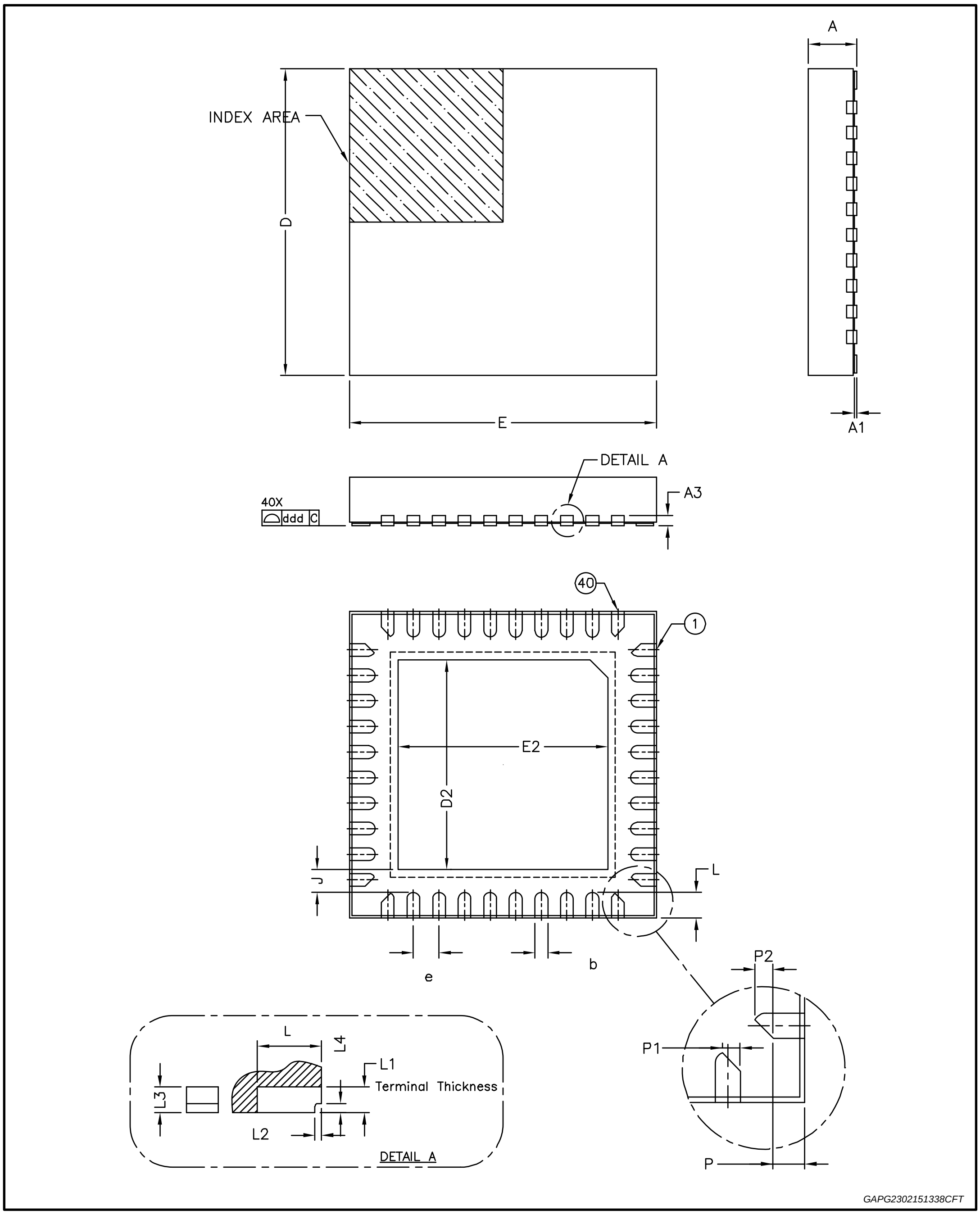


Table 65: QFN40L package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.85	0.95	1.05
A1	0		0.05
A3		0.20	
b	0.20	0.25	0.30
D	5.85	6.00	6.15
E	5.85	6.00	6.15
D2	3.95	4.10	4.25
E2	3.95	4.10	4.25
e		0.50	
J		0.45	
L	0.40	0.50	0.60
L1		0.20	
L2		0.05	
L3		0.20	
L4		0.075	
P		0.31	
P1		0.18	
P2		0.18	
ddd			0.08

7.2 PowerSSO-36 package information

Figure 33: PowerSSO-36 package outline

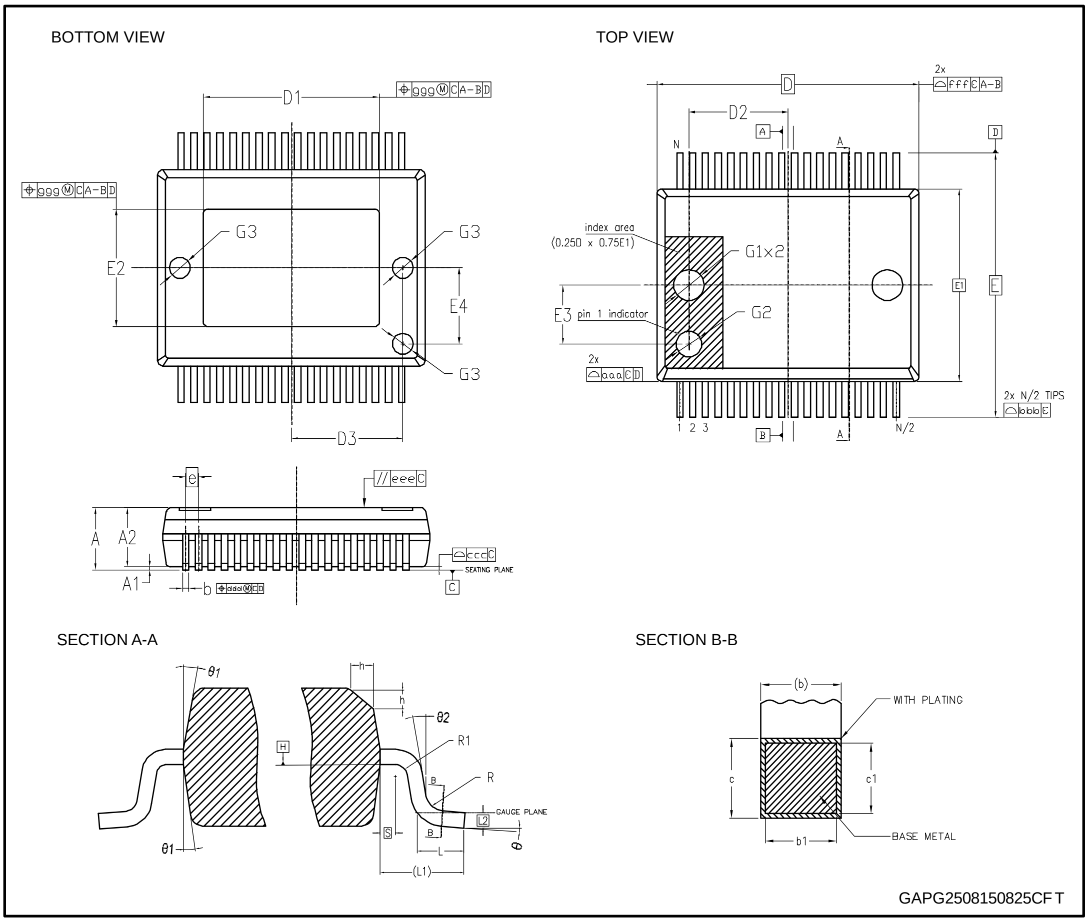


Table 66: PowerSSO-36 package mechanical data

Ref.	Dimensions		
	Millimeters		
	Typ.	Min.	Max.
Θ	0°		8°
Θ1	5°		10°
Θ2	0°		
A	2.15		2.45
A1	0.00		0.10
A2	2.15		2.35
b	0.18		0.32
b1	0.13	0.25	0.30
c	0.23		0.32
c1	0.20	0.20	0.30
D	10.30 BSC		
D1	4.9		5.5

Ref.	Dimensions		
	Millimeters		
	Typ.	Min.	Max.
D2		3.65	
D3		4.30	
e	0.50 BSC		
E	10.30 BSC		
E1	7.50 BSC		
E2	4.10		4.70
E3		2.30	
E4		2.90	
G1		1.20	
G2		1.00	
G3		0.80	
h	0.30		0.40
L	0.55	0.70	0.85
L1	1.40		
L2	0.25 BSC		
N	36		
R	0.30		
R1	0.20		
S	0.25		
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
eee	0.10		
ffff	0.20		
ggg	0.15		

7.3 Marking information

Figure 34: QFN40L marking information

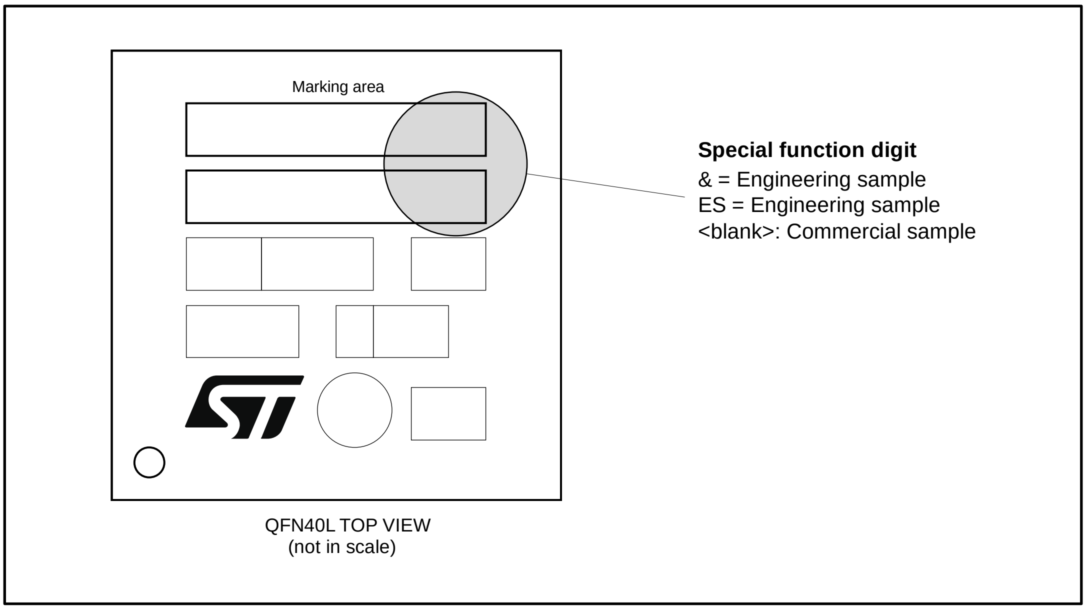
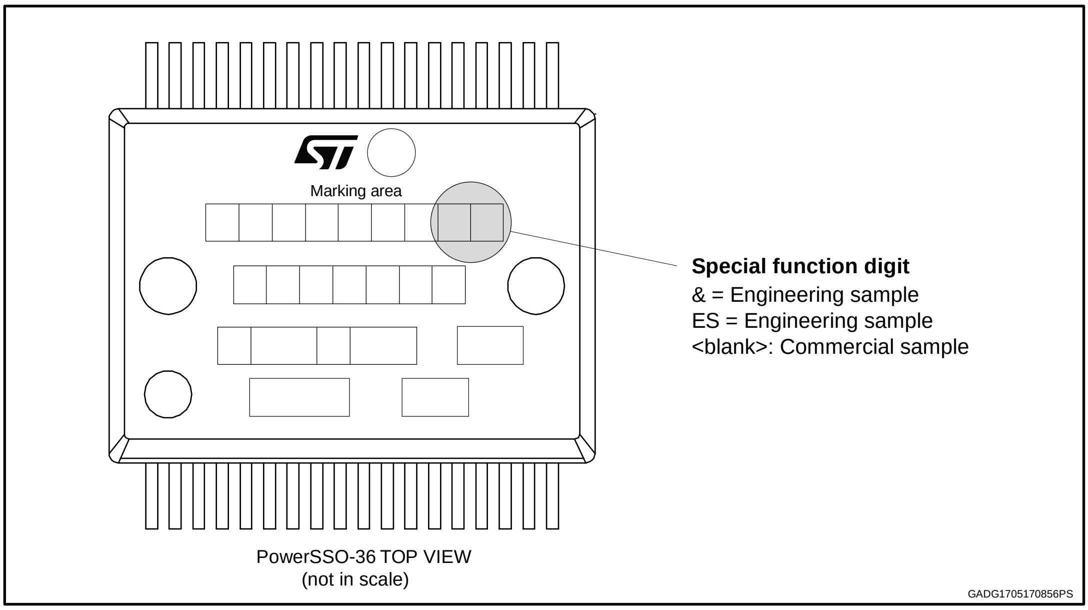


Figure 35: PowerSSO-36 marking information



Parts marked as '&' or 'ES' are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

8 Order codes

Table 67: Device summary

Order code	Package	Packing
L99SM81VQ6TR	QFN40L	Tape and reel
L99SM81VYTR	PowerSSO-36	Tape and reel

9 Revision history

Table 68: Document revision history

Date	Revision	Changes
04-Mar-2015	1	Initial release.
19-Oct-2015	2	Updated Section "Features" Updated following sections: • Section 2: "Device description" • Section 5.2.2.1: "Global Status Byte GSB" • Section 5.3.2: "Device Application Registers" • Section 5.4.5: "Data Stuck" • Section 6: "SPI registers" Removed Section "Temperature feedback" Added following sections: • Section 2.12: "Analog output" • Section 3.1.5: "V5V failure" Table 8: "Supply and supply monitoring": • VSUV, VREGUV: updated value Table 10: "Voltage regulator V5V": • CV5V, I_{V5VLIM}: updated values Table 14: "PWM control": • t_{CC}, t_B, t_{OC}: updated values Table 16: "Digital inputs CTRL1, CTRL2, CTRL3, EN": • t_{START}: added row Table 19: "CSN, SCK, SDI input": • RINCSN: updated test condition Updated Table 29: "Device information registers" Updated Table 65: "QFN40L package mechanical data" Updated Section 8: "Order codes"

Date	Revision	Changes
01-Jun-2015	3	Updated *Section "Features"* Updated following sections: • *Section 2.5: "Application block diagram"* • *Section 2.8: "HOLD mode"* • *Section 3: "Protections and diagnostics"* • *Section 4: "Electrical characteristics"* • *Section 5: "ST SPI protocol"* Updated following tables: • *Table 3: "Absolute maximum ratings"* • *Table 4: "Operating range"* • *Table 6: "Thermal data"* • *Table 7: "Thermal warning and thermal shutdown"* • *Table 9: "Power on reset"* • *Table 10: "Voltage regulator V5V"* • *Table 11: "AOUT electrical characteristics"* • *Table 14: "PWM control"* • *Table 15: "Clock characteristics"* • *Table 16: "Digital inputs CTRL1, CTRL2, CTRL3, EN"* • *Table 17: "Coil voltage acquisition"* • *Table 35: "Global Status Register GSR"* • *Table 36: "Global Status Register GSR (bit description)"* • *Table 34: "Complete device SPI register table"* • *Table 35: "Global Status Register GSR"* • *Table 36: "Global Status Register GSR (bit description)"* • *Table 37: "Motor and driver Status Register MSR"* • *Table 38: "Motor and driver Status Register MSR (bit description)"* • *Table 43: "Motor Control Register 1 MCR1"* • *Table 45: "Motor Control Register 2 MCR2"* • *Table 46: "Motor Control Register 2 MCR2 (bit description)"* • *Table 48: "Motor Control Register 3 MCR3 (bit description)"* • *Table 59: "Motor Coil Voltage Low Limit B MCVLLB"* • *Table 66: "PowerSSO-36 package mechanical data"* Updated following figures: • *Figure 4: "PSSO36 pin connections (top view)"* • *Figure 5: "Stepper motor driver application block diagram"* • *Figure 13: "PWM switching sequence (slow decay)"* • *Figure 14: "Mixed decay"* • *Figure 15: "Mixed decay (current undershoot / limit not reached)"*

Date	Revision	Changes
15-Jun-2017	4	Updated following sections: • *Section "Features"* • *Section 2.6: "Stepping modes and step update"* • *Section 2.8: "HOLD mode"* • *Section 2.9: "Decay modes"* • *Section 2.10: "Control pins (CTRLx)"* • *Section 2.11: "Digital outputs"* • *Section 2.13: "Motor coil voltage measurement for stall detection"* • *Section 3.1: "Supply diagnostics"* • *Section 3.2: "Thermal warning and thermal shutdown"* • *Section 3.3: "Cross current protection (dead-time)"* Updated following tables: • *Table 1: "Pin definition and function"* • *Table 6: "Thermal data"* • *Table 9: "Power on reset"* • *Table 10: "Voltage regulator V5V"* • *Table 11: "AOUT electrical characteristics"* • *Table 12: "OUTxn outputs (x = A,B; n = 1,2)"* • *Table 13: "Charge pump"* • *Table 14: "PWM control"* • *Table 17: "Coil voltage acquisition"* • *Table 21: "SPI timing"* • *Table 32: "SPI data length"* • *Table 34: "Complete device SPI register table"* • *Table 36: "Global Status Register GSR (bit description)"* • *Table 40: "Global Configuration Register 1 GCR1 (bit description)"* • *Table 44: "Motor Control Register 1 MCR1 (bit description)"* • *Table 45: "Motor Control Register 2 MCR2"* • *Table 46: "Motor Control Register 2 MCR2 (bit description)"* • *Table 47: "Motor Control Register 3 MCR3"* • *Table 48: "Motor Control Register 3 MCR3 (bit description)"* • *Table 60: "Motor Coil Voltage Low Limit B MCVLLB (bit description)"* • *Table 61: "Motor Coil Voltage Low Limit A MCVLLA (bit description)"* Updated following figures: • *Figure 1: "Block diagram (QFN40L)"* • *Figure 2: "Block diagram (PowerSSO-36)"* • *Figure 5: "Stepper motor driver application block diagram"* • *Figure 14: "Mixed decay"* • *Figure 29: "SPI pin description"* Added • *Figure 21: "Comparative Auto decay mode 1 vs. Auto decay mode 2"* • *Section 7.3: "Marking information"*