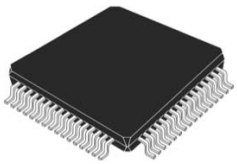
L99UDL01

L99UDL01 Automotive Universal Door Lock IC

Datasheet - production data



TQFP64L 10x10

Features

- AEC-Q100 qualified
- Six integrated fully protected 0.09 Ω half bridges
- Integrated half bridges can be fully independent or paralleled up to three in parallel
- Two levels of standby
  - Standby (SPI initiated)
  - Sleep (VDD=0 V)
- Very low current consumption in standby
  - Only wake-up circuit active
- High level of programmability
  - On-time duration
  - Direction
  - Current level
  - Off-state fault detection
- 2 external half bridge controllers (using external N-channel MOSFETs or Smart Power devices)
- External half bridges protected by drain source monitoring and off-state fault detection
- 2 stage charge pump for low voltage operation
- PWM current regulation up to 25 kHz
- 4 MHz 24 bit SPI interface for control and diagnostics
- Output enable for high security
- High level diagnostics
- 10 bit digital current feedback (via SPI) for load integrity check
- Thermal warning and shutdown protection
- Reverse battery protection using an external N-Ch MOSFET.
- TQFP64L exposed pad package

Application

The L99UDL01 is designed for use in a central door lock system driving all of the door lock actuators. This device is able to adapt to most central door lock configurations.

Description

The L99UDL01 is a multiple half-bridge IC with 6 integrated outputs that are PWM configurable and current regulated and up to two externally configured half bridges for higher current nodes. The level of diagnostics includes open load, short to battery, short to ground, and load integrity via 10 bit current feedback.

The L99UDL01 is commanded entirely by SPI using duration and current level commands.

Table 1. Device summary

Package	Order codes	
	Tray	Tape and reel
TQFP64L	L99UDL01	L99UDL01TR

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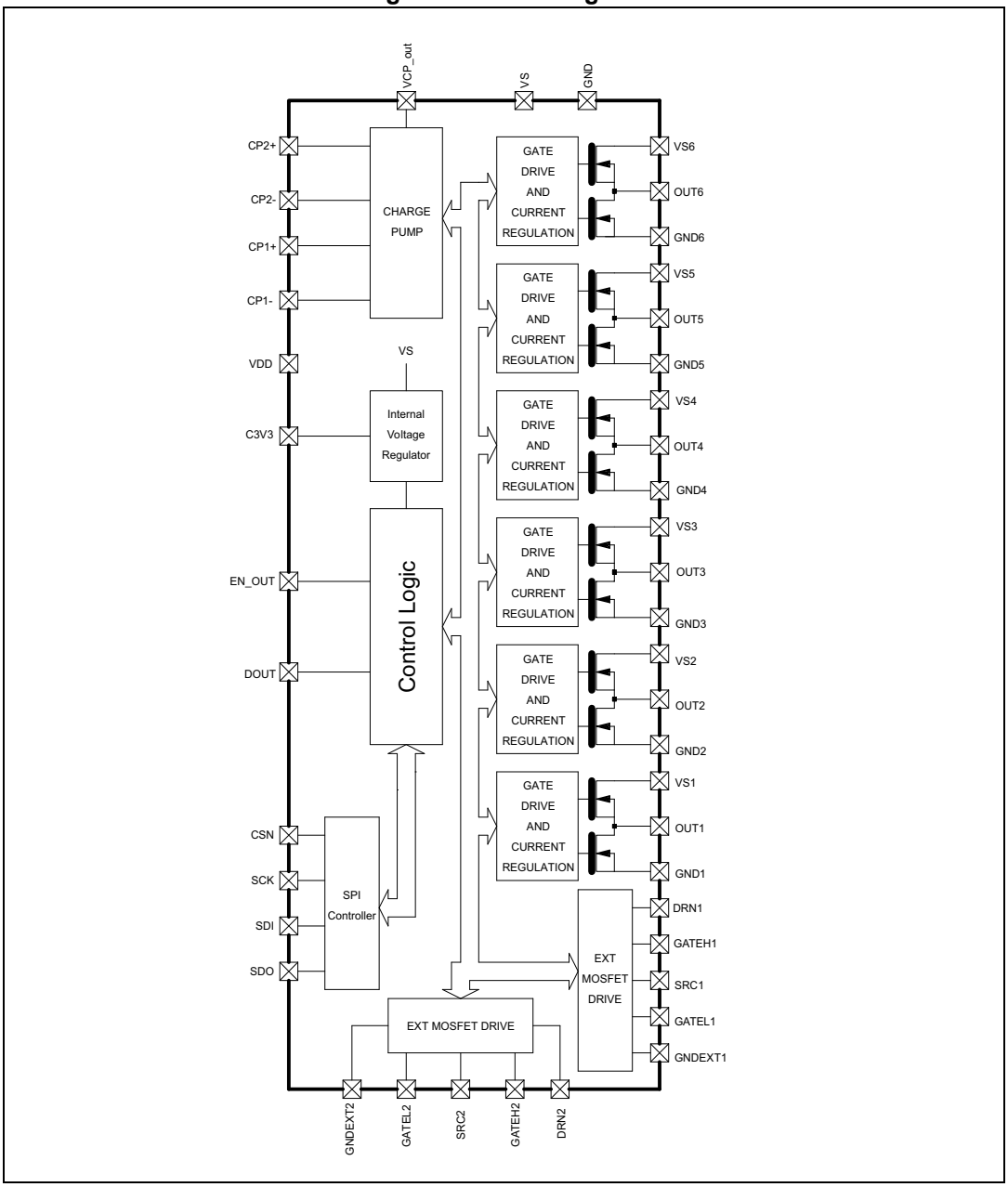
1 Block diagram and pin descriptions

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Table 2. Pin description

Pin #	Name	Description
1	VS1_2	Supply for half bridge 1
2	OUT1_1	Half bridge output 1
3	OUT1_2	Half bridge output 1
4	GND1_1	Ground for half bridge 1
5	GND1_2	Ground for half bridge 1
6	VS2_1	Supply for half bridge 2
7	VS2_2	Supply for half bridge 2
8	OUT2_1	Half bridge output 2
9	OUT2_2	Half bridge output 2
10	GND2_1	Ground for half bridge 2
11	GND2_2	Ground for half bridge 2
12	VS3_1	Supply for half bridge 3
13	VS3_2	Supply for half bridge 3
14	OUT3_1	Half bridge output 3
15	OUT3_2	Half bridge output 3
16	GND3_1	Ground for half bridge 3
17	GND3_2	Ground for half bridge 3
18	EN_OUT	Failsafe logic input. On its rising edge, EN_OUT activates outputs including External MOSFET drivers. Low disables all actuations.
19	DOUT	Programmable I/O pin / Default as Global Fault Flag
20	GNDEXT1	Ground for VDS reference for low side MOSFET
21	GATEL1	Gate drive for low side external MOSFET
22	SRC1	Source – Drain node between high and low side MOSFETS. Used for VDS detection of both high and low side MOSFETs
23	GATEH1	Gate drive for high side external MOSFET
24	DRN1	Drain connection for external H-Bridge, Sensing for VDS fault
25	GNDEXT2	Ground for VDS reference for low side MOSFET
26	GATEL2	Gate drive for low side external MOSFET
27	SRC2	Programmable I/O pin / Optional Source – Drain node between high and low side auxiliary MOSFETS. Used for VDS detection of both high and low side MOSFETs
28	GATEH2	Programmable I/O pin / optional external gate drive for auxiliary high side MOSFET
29	DRN2	Drain connection for external H-Bridge, Sensing for VDS fault
30	GND	Ground pin
31	NC	Not Connected pin; to leave floating

Table 2. Pin description (continued)

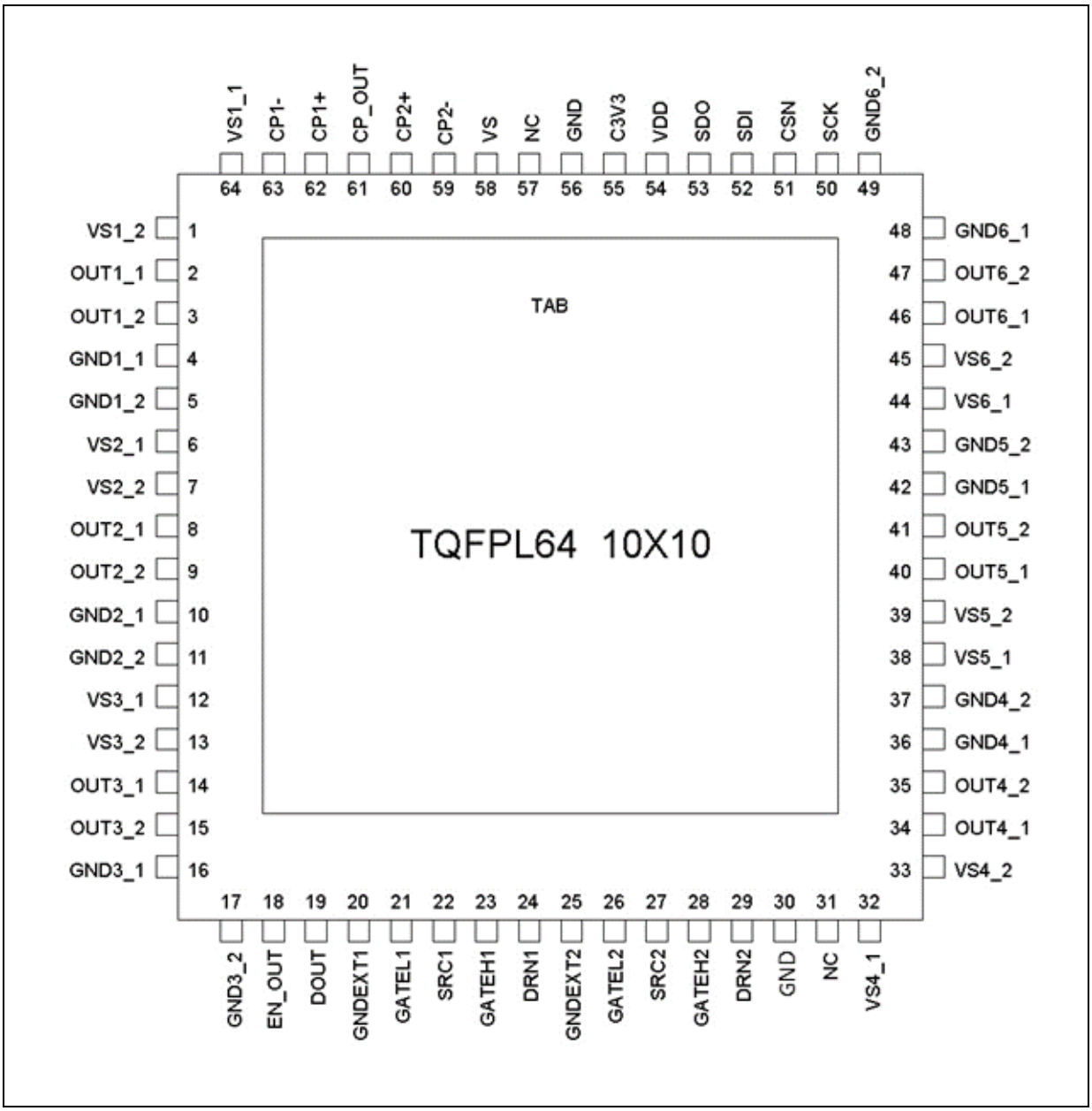
Pin #	Name	Description
32	VS4_1	Supply for half bridge 4
33	VS4_2	Supply for half bridge 4
34	OUT4_1	Half bridge output 4
35	OUT4_2	Half bridge output 4
36	GND4_1	Ground for half bridge 4
37	GND4_2	Ground for half bridge 4
38	VS5_1	Supply for half bridge 5
39	VS5_2	Supply for half bridge 5
40	OUT5_1	Half bridge output 5
41	OUT5_2	Half bridge output 5
42	GND5_1	Ground for half bridge 5
43	GND5_2	Ground for half bridge 5
44	VS6_1	Supply for half bridge 6
45	VS6_2	Supply for half bridge 6
46	OUT6_1	Half bridge output 6
47	OUT6_2	Half bridge output 6
48	GND6_1	Ground for half bridge 6
49	GND6_2	Ground for half bridge 6
50	SCK	SPI Clock - This SCK provides the clock of the SPI. Data present at Serial Data Input (SDI) is latched on the rising edge of Serial Clock (SCK) into the internal shift registers while on the falling edge data from the internal shift registers are shifted out to Serial Data Out (SDO).
51	CSN	SPI Chip Select Not -The communication interface is deselected, when this input signal is logically high. A falling edge on CSN enables and starts the communication while a rising edge finishes the communication and the sent command is executed when a valid frame was sent. During communication start and stop the Serial Clock (SCK) has to be logically low. The Serial Data Out (SDO) is in high impedance when CSN is high or a communication timeout was detected
52	SDI	Serial Data In - This input is used to transfer data serially into the device. Data is latched on the rising edge of Serial Clock (SCK).
53	SDO	Serial Data Out - This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK).
54	VDD	I/O Supply (+5 V or 3.3 V)
55	C3V3	Capacitor decoupling pin for internal 3.3 V regulator
56	GND	Ground for IC and I/O
57	NC	Not Connected pin; to leave floating
58	VS	Supply for IC
59	CP2-	Charge pump capacitor pin

Table 2. Pin description (continued)

Pin #	Name	Description
60	CP2+	Charge pump capacitor pin
61	CP_OUT	Charge pump out, also used for biasing reverse battery MOSFET
62	CP1+	Charge pump capacitor pin
63	CP1-	Charge pump capacitor pin
64	VS1_1	Supply for half bridge 1
TAB		Connect to ground

1.3 Pin connections (top view)

Figure 2. Pin connection diagram



2 Device description

2.1 Overview

The L99UDL01 is a 6+2 channel half bridge driver monolithic integrated circuit designed to power a centralized door lock system. This device is made possible by the incorporation of current regulated drivers limiting the current in the door lock motors to a preset level (for example the current levels seen at a 9 V battery).

The current is regulated by controlling the PWM duty cycle at a programmed frequency.

2.2 Supply monitoring

2.2.1 Low Voltage Inhibit (VS_{LVI})

The Vs supply has a low voltage warning function with hysteresis. When Vs drops below VS_{LVI_F} the outputs (internal half bridges and drivers for external MOSFET) are disabled and the VS_{LVI} bit is set in register 12H (the SPI diagnostic register).

Once Vs rises above the rising VS_{LVI_R} threshold the outputs are re-enabled and ready for use. Actuation can be restarted via SPI frame or EN_OUT rising edge according to configuration registers. The VS_{LVI} bit remains set in the SPI diagnostic register and is cleared only upon read & clear.

2.2.2 Overvoltage (VS_{OVSD})

When VS rises above VS_{OVSD} the outputs (internal half bridges and drivers for external MOSFETs) are disabled and the V_{OVSD} bit is set in the SPI diagnostic register.

Once VS falls below VS_{OVSD} the outputs are re-enabled and ready for use. Actuation can be restarted according to configuration registers via SPI frame or EN_OUT rising edge. The VSOVSD bit (diagnostic register 12H) remains set until read & clear SPI frame.

2.2.3 VDD monitoring

The VDD pin (5 V/3.3 V) is a supply pin for the L99UDL01 I/O. This pin is monitored by 2 under voltage conditions. In case of an undervoltage condition during Normal mode ($VDD < VDD_{UV}$) the device will enter into stand-by mode and all of the control registers will be reset to their default values after t_{VDDUV}. In case of an undervoltage condition ($VDD<VDD_{SLEEP}$), the device enters into the ultra-low quiescent sleep mode and the internal regulator is disabled. CSN must be held high while VDD falls below VDD_{SLEEP} to ensure the L99UDL01 enters into sleep mode.

Upon rising out of VDD_{SLEEP} the device will perform a power-on reset and enter into Standby mode until a CSN wake-up has occurred. The reset (RSTB) bit will remain set until the first SPI communication.

2.2.4 3V3 monitoring

The internal 3.3 V regulator, 3V3, is monitored for under voltage conditions to ensure the logic integrity.

The 3V3 supply has a low voltage warning function with hysteresis. When the 3V3 regulator drops below $3V3_{UV}$ threshold for t_{3V3UV}, timed actuation is halted, the outputs (internal half bridges and drivers for external MOSFET) are disabled, and the V3V3UV bit is set in the SPI diagnostic register 13h.

If, for any reason the 3V3 supply falls below $V3V3_{RST\_F}$ the Logic State machine and all of the registers are RESET to their default state and held there.

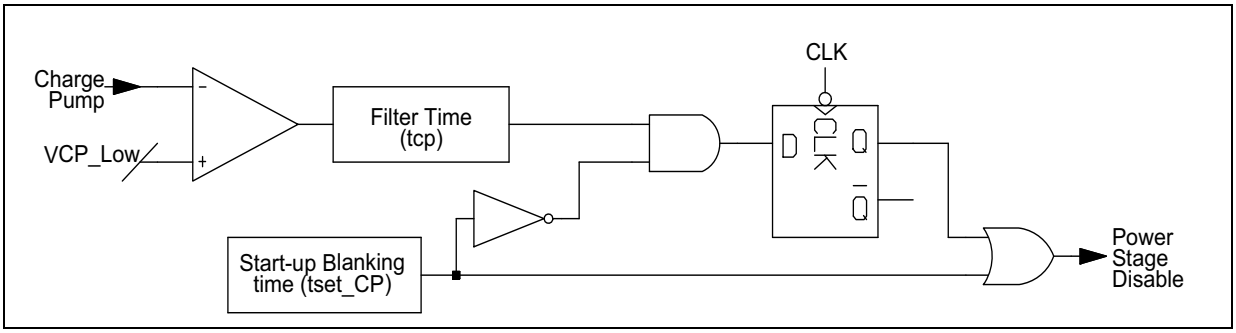
Upon rising out of $V3V3_{RST\_R}$ RESET will be disabled and the L99UDL01 will enter Standby mode.

The C3V3 pin is intended only for supply to the IC. It is not recommended that the C3V3 pin is used to power any other circuitry.

2.3 Charge pump

The charge pump uses two external flying capacitors, which are switched with f_{CP}. The output of the charge pump has a current limitation. In standby mode or after a global thermal shutdown has been triggered the charge pump is disabled.

Figure 3. Charge pump low filtering and start-up



At coming out of standby the outputs are enabled t_{SET_CP} seconds after the charge pump is re-enabled as long as the V_{CPLOW} threshold is achieved. The CPLOW bit will remain set, indicating that the charge pump was low since the last reading of the register.

At any time the charge pump output voltage drops below V_{CPLOW} the CPLOW bit is set and the internal half bridges and the external H-Bridge MOSFET gate drivers are pulled low. After a CPLOW event the outputs are re-enabled t_{CP} seconds after the charge pump voltage rises above V_{CPLOW}. Actuation can be restarted via SPI frame or EN_OUT rising edge according to configuration registers. In this case the outputs that are actuated by the output override (OUTx_on) bits will automatically turn back on when the charge pump is above CPLOW.

An over voltage or under voltage fault (VSovsd, VDDuv, V3V3uv) will disable the charge pump only while that condition exists. The charge pump will automatically restart once the over voltage or under voltage fault is no longer present.

In the case of a global TSD event all of the TSD flags must be cleared or the ACT_OFF control bit must be reset to re-enable the Charge pump.

Any time the charge pump is enabled, re-enabled or restarted the drivers will not be available until after t_{set_CP} and the charge pump voltage exceeds the V_{CPLOW} threshold (see *Figure 3*).

In all cases the CPLOW bit will remain set indicating that the charge pump was low since the last read & clear of the register.

The charge pump frequency can be dithered to reduce the impact on radio frequency emissions. This option is set via bit DITHN in register 03H. By default DITHN=0 and dithering is enabled.

It is not recommended that the CP pin is used to power other circuits. The charge pump current capability is intended only for the IC and reverse battery MOSFET. This supply cannot be used for other circuits without potentially causing issues.

2.4 Output functionality

There are two groups with three drivers each. The three drivers in each group can be paralleled or driven independently.

The output configuration registers identify which outputs are tied together for driving and current regulation purposes.

The output configuration registers also provide for a range of current regulation levels and on-time durations.

The set up prior to command an actuation requires the following global commands. These are typically set at initialization and are not needed to be altered:

1. If initiating a timed actuation by SPI command:
   a) After power on reset, with all registers cleared, raise the EN_OUT pin. If the EN_OUT pin is hardwired no action needed.
2. Register 00H:
   a) Set the desired PWM regulation frequency.
3. Register 01H:
   a) No activity at this time.
4. Register 02H:
   a) Set the on-time duration for the actuation.
   b) Set the braking time duration after the actuation.
   c) Disable any outputs not using dynamic braking (typically, these outputs would not participate in the locking system).
5. Register 03H:
   a) Set the groups. This determines which outputs are in parallel (if any).
   b) Set the Thermal shutdown reaction (Global or individual).
   c) Set the PWM frequency dithering on/off. Dithering is automatically on (DITH=0).
   d) Set the Global fault indication bit if desired.
6. Register 04H and 05H
   a) Set the current regulation /PWM duty cycle levels for each of the outputs / groups. If two internal switches are driving both ends of a load then only one should be current regulating / PWMming.
7. Register 06H
   a) Set the Drain-Source monitoring parameters (amplitude and duration) for the external MOSFETs.

Commanding the outputs then requires:

1. Register 00H:
   a) Set the polarity of the internal switches (HS/LS)
2. Register 01H:
   a) Set the polarity of the external switches (HS/LS)
3. Initiate the timed actuation:
   a) If by SPI, then the OUT_ON bit may be set in register 01H. This can be done concurrently with programming register 01H (step 2 above) as long as the EN_OUT pin is high.
   b) If initiating timed actuation by the EN_OUT pin then raise the EN_OUT pin. Timed actuation will occur as long as the EN_OUT pin is high.

The unregulated side is protected by the overcurrent protection.

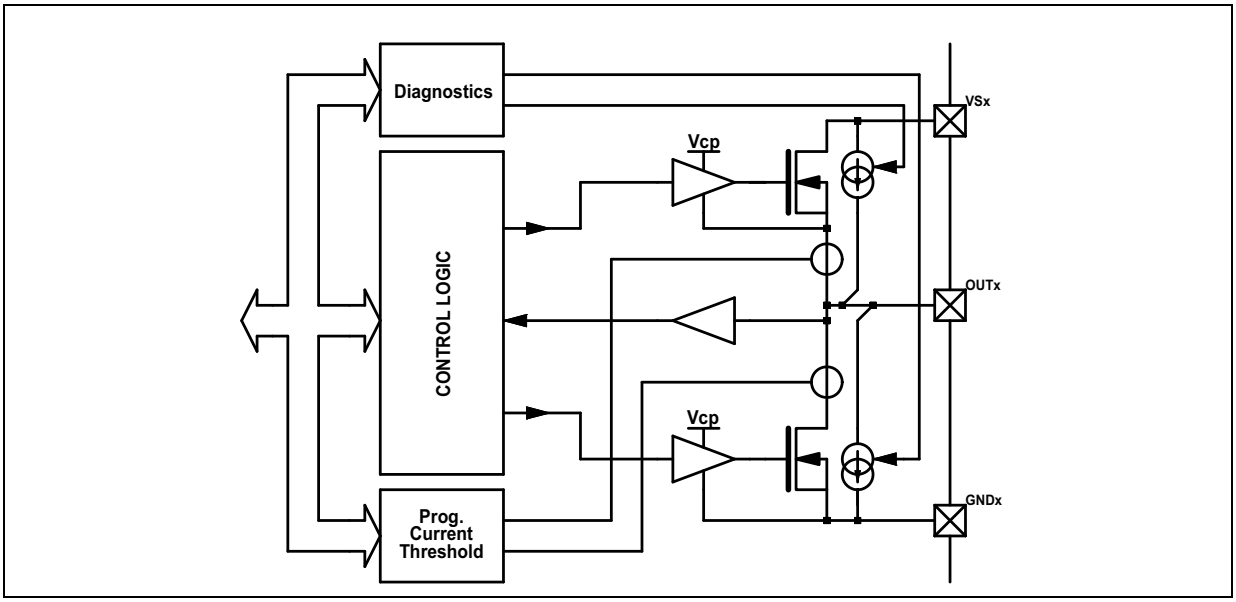
All outputs, internal and external, are driven with active circuitry. If indefinite dynamic braking is not enabled, once an actuation cycle is completed and all devices have been commanded off, the active circuitry is disabled after ~10 µs to reduce quiescent loading. All outputs are then in a passive off state that will keep the outputs off (gates tied to their sources) in the face of noise on the load or supply.

If indefinite braking is enabled, then the active circuitry will remain active for all outputs (even if dynamic braking is disabled for that output).

2.4.1 Integrated half bridge drivers (OUT1-OUT6)

These outputs are configured as switching drivers incorporating active recirculation to minimize power dissipation. The dead time between high and low side drivers is fixed within the functionality of the output drivers.

Figure 4. OUT1-6 block diagram



All the integrated outputs can be driven in timed voltage control (PWM duty cycle), timed current regulation control or on/off control.

These outputs have over current protection, under current detection, and off-state diagnostics. Off state diagnostics may provide for non-active detection of Lock motor status. The output rising and falling times are controlled to provide the lowest EMI while minimizing the switching losses. This is done by controlling the edges to smooth out the corners of the waveform while maintaining a fast transition from one level to the other.

Active freewheeling

Active freewheeling is an automatic function. Whenever the output voltage approaches the freewheeling rail, the freewheeling element becomes active. That is, when the High side is driving the load and the low side MOSFET is acting as the freewheeling element the low side MOSFET is only enabled when the voltage falls below $V_{DS\_ON\_LS}$ (50 mV typ). Conversely, if the low side MOSFET is the driving element the high side MOSFET is not active unless the voltage is above $V_{DS\_ON\_HS}$ (Vs-1 V typ).

This poses some limitation with respect to shorted load diagnostics. See *Limitations due to active freewheeling*.

Current regulation control

All integrated outputs can work in current regulation mode. Each power MOS has a configurable bidirectional current sense which provides an image of the load current during on mode and recirculation phase. This current image is compared to the target value written in the configuration register in a digital algorithm so that mean current value through the load is equal to the chosen value.

Figure 5. Current Control Loop

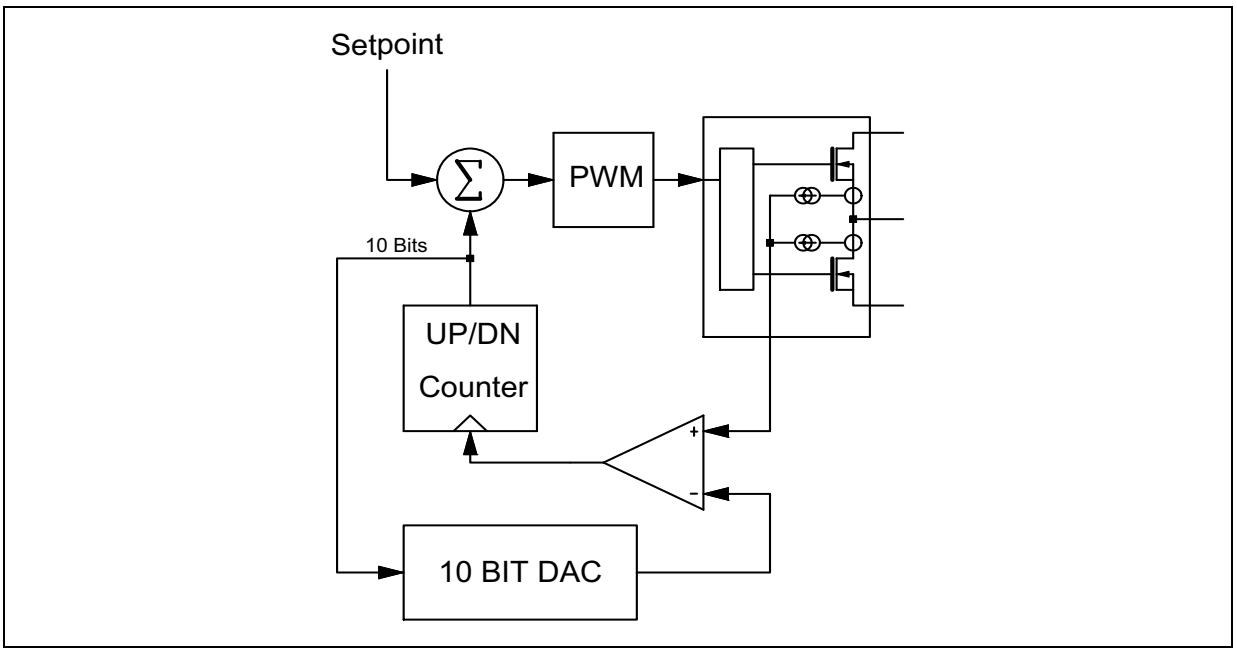


Figure 6. Unregulated door lock motor current

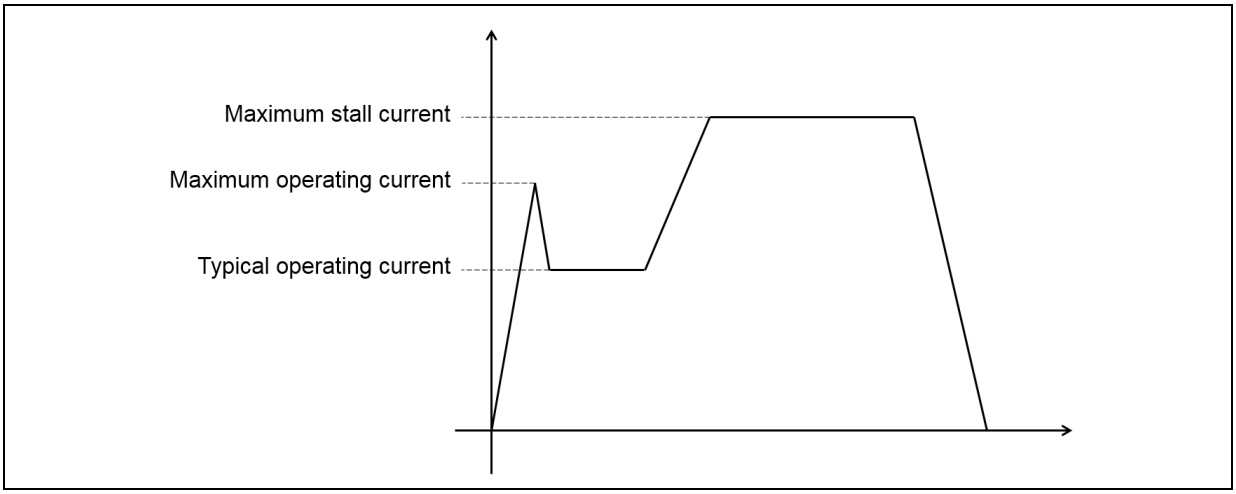


Figure 7. Slightly regulated door lock current

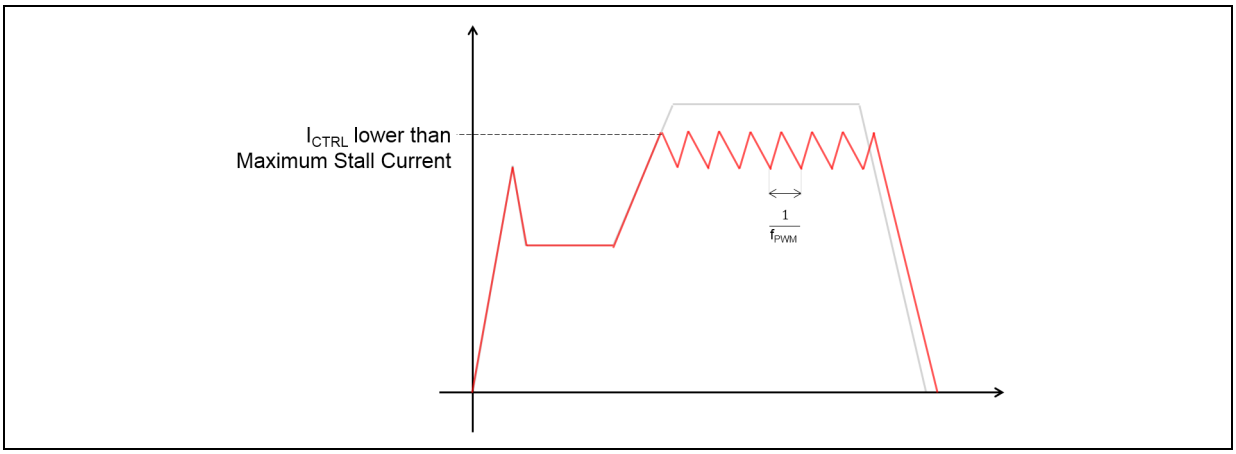
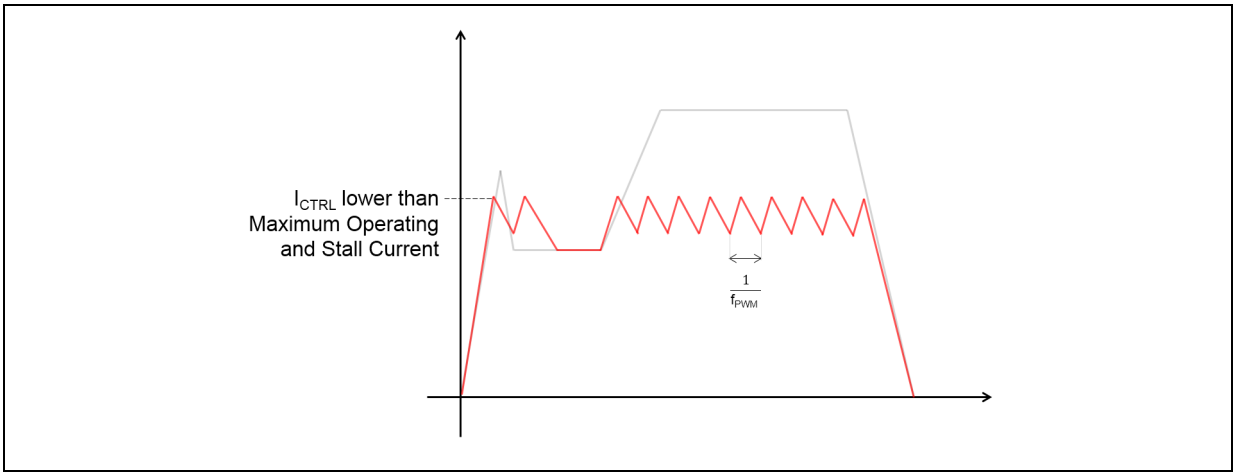


Figure 8. Heavily regulated door lock current



Control loop parameters

The control loop for the current regulation is programmable. There are two parameters that are adjustable through SPI. It should be noted that there is a default setting that will work for the most of the lock motor applications known. These parameters are provided to aid in any possible scenario. Typically, these parameters can be left alone:

- Integral Gain, Ki, (3 bits)
- Proportional Gain, Kp, (3 bits)

Integral and proportional gain settings are the standard control loop parameters for integral gain and proportional gain. The default settings for these parameters are Ki $=2^{-2}$ = 1/4, and Kp = 2^{6} = 64.

This register is set up for a nominal control loop. Most, if not all, applications will be stable enough to use this default setting.

Current regulation mode can be initiated via EN_OUT rising edge or via OUT_ON bit (register 01H) provided EN_OUT=1 and OUTx_on =0 for the timed output x. Once started, a timed actuation can be stopped only with EN_OUT=0, fault condition, Emergency mode or at the natural end of timers. No other time controlled output can be started when a timed actuation is ongoing.

Current feedback

The Integrated drivers can provide a 10 bit word representing the current regulation loop current value. This is done to provide load integrity information in addition to the CNR bit (a current not reached, CNR, bit is set if the current in the output does not reach the regulated current level during the entire on-time actuation).

This is a buffered value of the 10 bit up/down counter in the current regulation loop. This information is retrieved at the falling edge of CSN when accessing the appropriate current loop register.

The conversion of the 10 bit information found in registers 13h – 18h to a typical value of current is a simple equation:

$$\text{Typical Current} = \frac{\text{Reg}_x}{0\text{xA0h}}$$

The current feedback can be read during the actuation phase as well as during the dynamic braking. In the latter case, the current feedback cannot be read when the dynamic braking is disabled for that output (DBN_x bit). The current feedback can be read for any actuated integrated output regardless of its configuration (current mode, voltage mode and overridden).

In indefinite braking mode, the current feedback is disabled after the first 100ms.

PWM frequency adjustment

The current regulation or PWM control PWM frequency can be adjusted to optimize the motor current regulation. This is accomplished in 2 kHz intervals from 10 kHz to 24 kHz using three FPWMx bits in register 00H.

2.4.2 External FET controllers

The external FET controllers are designed to be drivers for MOSFETS configured as half bridges. Alternatively, each half bridge controller may be configured as a single high-side driver or a single low side MOSFET controller. These outputs are not intended to be PWMmed and are limited in their switching speed to aid in reducing EMC issues.

The external MOSFETS are protected by a programmable drain to source voltage (V_{DS}) monitor. Both the voltage threshold and reaction delay are programmable. The default setting is 1 V for 1 µs.

In the event of a Drain-Source fault the appropriate fault bit will be set as well as a fault bit in the Global Status Byte. A faulted driver will be switched off and is enabled again only after clearing fault bit (register 11H).

Since these outputs are not intended to be PWMmed there is no active recirculation option.

The external MOSFET control has off-state diagnostic capability as well.

The external MOSFETs can be driven in timed on/off control or purely on/off control.

External MOSFET dead time control

At the end of every timed actuation all outputs are pulled to ground for the off-time duration as determined in the control register 02H. This requires that the external H-Bridge controller have a dead time between when the high side MOSFET is commanded off and when the low side MOSFET is commanded on. This is a fixed value set to t_{DT} (6 µs).

2.4.3 DOUT

The Data OUT pin may provide the host processor with real time fault indication. The GSBN (Global Status Bit NOT) bit may be reflected on this pin when this feature is enabled. This feature may be enabled by setting the Global Fault Indication (GFI) bit found in the control register 03H (bit7).

2.4.4 EN_OUT

The output Enable pin has three states: It enables the output functionality while held high, and disables the outputs when held low. This pin can also be used to initiate an output timed actuation, based on programmed parameters, on a rising edge. There is a filter time on the rising edge of EN_OUT of t_{EN}. This is used to prevent noise from accidentally actuating a timed actuation.

2.4.5 Paralleling outputs

Up to three of the integrated outputs can be paralleled in two groups for the purpose of sharing higher current loads.

Some of the possible combinations:

- 2 groups of 3
- 2 groups of 2 and 2 single outputs
- 1 group of 2, 1 group of 3 and a single output
- 1 group of 3, and 3 single outputs
- 1 group of 2, and 4 single outputs
- 6 single outputs, no groups

Paralleled outputs have all their current regulation, protection, and diagnostic information tied together. Once a set of outputs are grouped then the master registers are used to command and diagnose that group. The master registers are output 1 for outputs 1 through 3 and output 4 for outputs 4 through 6.

When paralleling multiple half bridges all the channels in the group will provide the current monitoring for the master current regulation loop.

Current values programmed for each channel in the group are added to create the total current for the group. Each output can have different values (for ex; 1 A for ch1 and 1.2 A for ch2 to generate 2.2 A total current regulation for the group). The Slave outputs must be programmed as current regulating when using current regulation.

PWM values will be taken from the master registers only. The remaining slave registers will be ignored when in PWM mode. The Slave outputs must be programmed as PWM when using PWM mode.

All diagnostics in a group must be cleared prior to restarting that group. For grouped outputs, only the Master registers (OUT1 or OUT 4) contain the correct fault information for their respective groups. Any diagnostic information must be gleaned from the Master. Slave registers may or may not indicate faults.

2.4.6 Output override

The outputs can be driven directly, outside of a timed actuation, by the use of the Output Override bits (OUTx_on, EX_OUTx_on in register 01H). When any of these bits are high then the corresponding output(s) will be enabled according to the configuration settings (polarity only). Overridden outputs are fully protected. Emergency Override affects the protections for overridden outputs in the same manner as timed outputs.

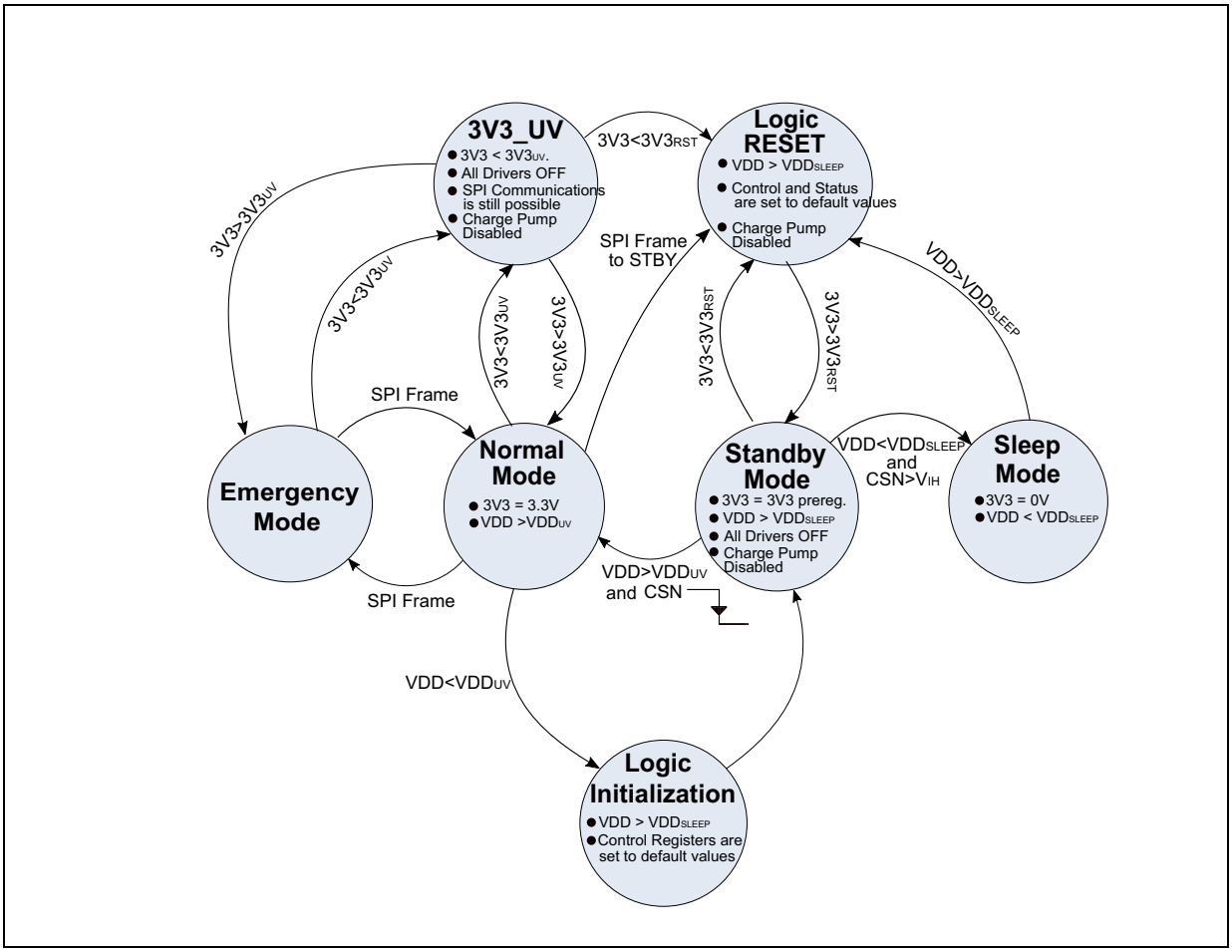
The overridden outputs will not current regulate nor will they be affected by a timed actuation.

Overridden outputs must not be modified (on, off, or polarity) at the initialization of (OUT_ON=1) or during a timed actuation unless an emergency override is enabled. Indefinite dynamic braking must be disabled prior to change any of the output override bits (OUTx_on and EX_OUTx_on in register 01H) or any of the overridden output polarities

2.5 Operating modes

We can distinguish among 4 different operating modes: Normal mode, Standby mode, Sleep mode and Emergency override mode. The L99UDL01 powers up in Standby mode by default.

Figure 9. State diagram



In Sleep mode no active circuitry is supplied. In standby mode logic is initialized but not operational. There is no function present in either modes in order to minimize the current consumption. Only wake-up circuitry is active in Standby mode.

2.5.1 Sleep mode

In sleep mode all circuitry is disabled. There is no charge pump or internal voltages. This is the lowest quiescent current mode.

Sleep mode is entered when the VDD input falls below VDD_{SLEEP_F}. Prior to entering sleep mode all control registers are reset to their default values. Sleep mode is exited when VDD rises above VDD_{SLEEP_R}. Sleep mode only exits into Standby mode.

To avoid anomalous behavior during transition into sleep mode, sleep mode should always be entered from standby mode. Entering sleep mode directly from any other mode is not supported.

2.5.2 Standby mode

Standby mode disables all circuitry except for the 3V3 pre-regulator and the circuitry related to watch for a wake-up event. Nothing else is active. The charge pump is off and the outputs are disabled.

Standby is entered by:

- SPI command from Normal Mode,
- When exiting Sleep Mode,
- When VDD falls below VDDUV
- When recovering from a 3V3 reset event.

Entering Standby by SPI command while in timed actuation, or when any output is active, is not supported. Doing this may cause adverse responses from the device.

In addition to Emergency override mode Standby is the only mode that Normal mode can be entered from. Transition to Standby Mode from Emergency Mode by SPI command is not supported.

To attain the low quiescent state in Standby mode, the EN_OUT pin must be held low.

2.5.3 Normal mode

The L99UDL01 will exit Standby mode to Normal mode when the CSN pin is pulled down as long as VDD>VDD_{UV}. There is a delay from the falling edge of CSN to when Normal mode is active (t_{Wake_up}). This delay is related to the charge pump and 3V3 regulator stabilization. When the 3V3 voltage has reached its proper level, the SDO pin is pulled low from a tri-stated condition. At that point, logic is operating, all circuits are activated and the SPI controller can be used to update the register configuration.

When coming out from Standby, the configuration registers are set to their default values. In this startup phase, the Charge Pump circuit starts working. In this case the drivers can be enabled after t_{set_CP} and the charge pump voltage exceeds the V_{CPLOW} threshold. An actuation can be initiated via EN_OUT pin or via an appropriate SPI frame. The CPLOW bit is not cleared until the register is read and cleared.

2.5.4 Emergency mode

Emergency mode is a crash override mechanism that will interrupt any current actuation command in progress and drives outputs according to the programmed values in the command and configuration registers.

This mode also overrides all protections. In an Emergency mode the device will not latch off if an overcurrent threshold is exceeded. Instead of latching off the driver and reporting a fault the output will continue to retry as in Normal mode.

All faults will be reported while not acted upon.

Emergency mode is initiated when (1, 0) is entered in the register containing the EMCY bits (register 01H). All other EMCY bit configurations result in normal mode.

When emergency is enabled any changes to the Output Override bits will be implemented and the current timed actuation activity will be stopped. To initiate a new timed actuation routine the OUT_ON bit must be set or the EN_OUT pin must be toggled.

While in Emergency mode the status bits (STAT [1:0]) will be automatically cleared whenever there is a write to CR01H.

2.6 Diagnostics and protections

2.6.1 Shorted load detection

All integrated drivers are protected for shorts to ground or supply by a simple over current detection and latch off strategy. At turn on there is a blanking time ($t_{OC\_BLANKING}$) where the output is given time to turn on. After the blanking time if the output current exceeds (I_{OC}) for longer than the filter time the faulted output(s) will be latched off.

If a shorted condition occurs after an output is active just the filtering time applies to the latch-off action.

The fault will be reported in the fault register (Register 10H). The Global fault Functional Error 1 bit (FE1) will also be set.

I_{OC} applies to a single output. Multiple outputs in parallel will multiply the I_{OC} value accordingly. Two outputs in parallel will garner a 2x increase in the I_{OC} value. The same concept applies in order to have three outputs in parallel.

Since this system relies on current limitation for normal running I_{OC} can occur in one of two ways. First, the I_{OC} threshold can occur if the current rise time is longer than the minimum on time ($t_{OC\_BLANKING}$) of the driver. This occurs as a shorted load has very little inductance.

The second method is when the integrated driver is programmed as a simple switch and does not provide the current regulation. Then I_{OC} is the only means of overcurrent protection.

The external half bridges are used as a simple switch (not current regulated). However, when both sides of the H-Bridge are set up by the use of integrated half bridges (outputs 1-6) then one of the integrated half bridges should be programmed as a simple switch. This is done by programming the output to be Voltage controlled (by setting the PWM_SW_x bit to 1) and setting the duty cycle to 100%.

This allows the other half bridge to provide the lock motor current regulation without confusion.

Shorted outputs may be detected in the off-state as well (see *Section 2.6.3*).

Limitations due to active freewheeling

Due to how active freewheeling is performed (see *Active freewheeling*) a short to the drive rail (a short to B+ for high side drive / low side freewheeling and vice versa) prior to activation is not detected. The freewheeling element is never active and cannot experience a shorted condition.

As a result, a shorted drive element during current regulation (C/PWM_SW_x=0) may appear as a CNR (current not reached). A shorted drive element cannot be detected if PWM control (C/PWM_SW_x=1) is selected.

A shorted driving element can be detected by reading the current feedback for that output or by an off state fault detection. Only if the short occurs while freewheeling, can a short be detected on the freewheeling element of the output.

External MOSFET protection

In case of the external half bridges Drain-Source voltage detection is implemented as an overload protection once the driver is active. The Drain-Source threshold, V_{DS_TH}, and duration, t_{VDS_BLANK}, are both programmable with a wide range to select from.

2.6.2 Thermal protection

There is a thermal sensor associated with each of the internal half bridges. There are two reported thermal thresholds. These are thermal warning, T_{Wx}, and thermal shutdown, T_{SDx}.

Thermal warning only provides a SPI register indication of the condition (T_{Wx}). Thermal shutdown either shuts down the offending half bridge or disables the entire device. This option is programmable via SPI command. Thermal shutdown is indicated in the SPI register via the T_{SDx} bits.

If more than one driver is linked in parallel the hottest driver will cause a thermal indication (T_{Wx} or T_{SDx}). All linked drivers have their diagnostic bits linked as well. That is, they will all demonstrate the same diagnostic state.

Drivers cannot be activated until its corresponding temperature is below thermal shutdown threshold and corresponding fault register bit is cleared.

2.6.3 Off state load detection

Along with the standard shorted load and thermal protections the L99UDL01 has the ability to verify load integrity without actuating loads.

This is done by incorporating enable-able weak pull-up (ODCHx) / pull-down (ODCLx) currents at each output. By using the weak pull-up/pull-down currents the following conditions can be determined:

- Shorted output to either ground or supply
- Open load

One method would be to first bias a motor node by either a weak pull-up or weak pull-down current then reading the Dynamic Output State (DOSx, DOS_EXTx) bits. A weak pull-up on one output should cause all nodes associated with that output to pull high. A weak pull-down on one output should cause all nodes associated with that output to pull low. An open circuit or shorted output would prevent either one or the other from happening.

2.6.4 Enable-able weak pull-up/down currents

The weak pull-up/pull-down currents are enable-able through SPI command (register 06H and 07H). Each output can have enabled a weak pull up current or a weak pull down current individually.

Activating a weak pull-up on one of a paralleled output and a weak pull-down in another of the same parallel group will be ignored and set a WRT_fail bit. Alternatively, activating a weak pull-up and a weak pull-down on the same output will be ignored and set a WRT_fail bit.

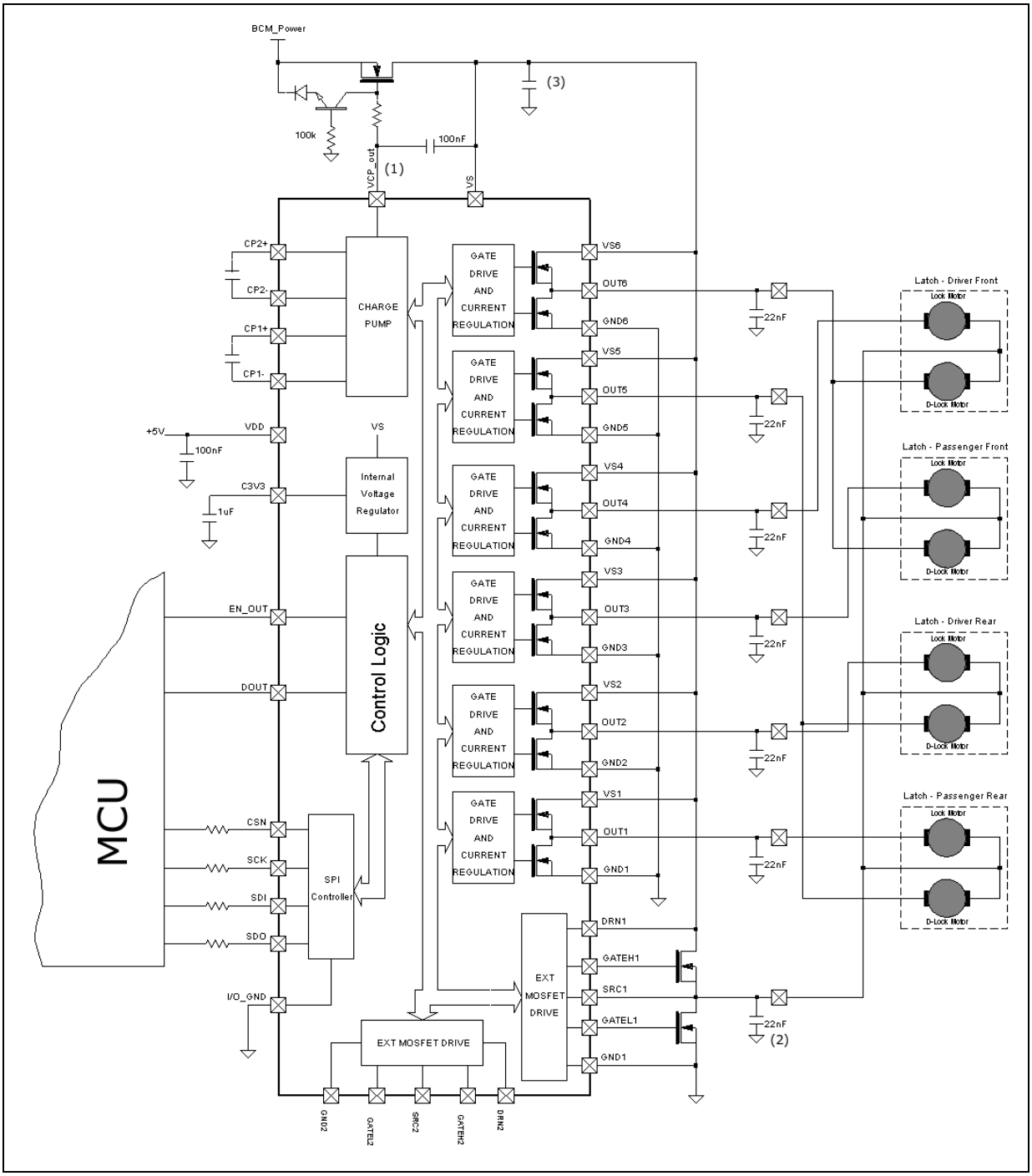
Weak pull-up/pull-down currents are available for both the integrated and the external Half-bridge controllers. This allows the user to determine if there is a short to ground or supply condition on these outputs prior to actuation.

2.6.5 Dynamic output state detection

All outputs, internal and external have the ability to detect if the output voltage is above or below a specific threshold (V_{OUT_th}). If the Output voltage at the time CSN falls is above the threshold the corresponding bit in Diagnostic register 11H is set high. If the output voltage is below the threshold then the corresponding bit is set low.

3 Application schematic

Figure 10. Typical application diagram example



1. Recommended VCP_out capacitors for optimum EMC performance. These capacitors need to be placed as close to the VS-VCP pins as possible to optimize their effectiveness at reducing EMC.
2. A 22 nF capacitor should be used on each output for ESD performance and output stability.
3. The Bulk capacitance should be dimensioned according to the user's design practices.

4 Electrical characteristics

4.1 Absolute maximum ratings

The absolute maximum ratings are the values at which if exceeded the device may become damaged.

Table 3. Absolute maximum ratings

PIN/Parameter Name	Parameter		Value		Unit
			min	max	
VS_X	Supply Voltage (Continuous)		-0.3	+28	V
VS_X	Supply Voltage 400 ms transient (Load Dump)		-0.3	+40	V
V_{CP}	High voltage signal pin	$V_S \le 26$ V	V_S-0.3 to V_S+14		V
		$V_S > 26$ V	V_S-0.3 to +40		V
VDD	VDD input		-0.3	+6	V
3V3	3.3 V regulator maximum allowable voltage			3.6	V
GNDx	Differential voltage between Grounds and TAB		-0.3	+0.3	V
DRNx	-		-0.3	V_S+0.3	V
SRCx	t < 200 ns		-5	V_S+0.3	V
	Continuous		-1		V
GATEHx	External high side MOSFET control		V_{SRCx} – 0.3	V_{SRCX} +12, V_{CP}+0.3(1)	V
GATELx	External low side MOSFET control		-0.3	12 V_{CP}+0.3(1)	V
DOUT, EN_OUT	-		-0.3	VDD+0.3	V
OUT_{X_max}	All half bridge outputs			V_S+0.3(1)	V
OUT_{X_min}	All internal half bridge outputs 4 A from ground, outputs inactive, t_{Recirc}<10 ms		-0.3		V
V_{CP1M},V_{CP2M}	High voltage signal pins		V_S-0.3 to V_S+0.3		V
V_{CP1P}	High voltage signal pins		V_S-0.3 to V_S+10		V
V_{CP2P}	High voltage signal pins		V_S-0.6 to V_S+10		V
CSN, SCK, SDI, DSO	-		-0.3	VDD+0.3	V
$T_{J(Operating)}$	Junction temperature		-40	175(2),(3),(4)	°C
$T_{J(Storage)}$	Storage temperature		-55	+150	°C

1. Of the values listed whichever is the lesser of them applies.
2. All parameters are guaranteed, and tested, in the temperature range -40°C to 130°C (unless otherwise specified). The L99UDL01 will still operate and be functional at temperatures up to 175°C.
3. Parameter limits at higher temperatures than 130°C may change with respect to what is specified as per the standard temperature range.
4. Device functionality at temperatures greater than 130°C are guaranteed by design.

4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value		Unit
		min	max	
$R_{th(j-a)}$	Thermal resistance Junction to Ambient(1). One output on.		18	°C/W
$R_{th(j-c)}$	Thermal resistance Junction to case. One output on		7	°C/W

1. On a 4-layer FR4 board with thickness of 1.5 mm +/- 10%, dimension 77 mm x 114 mm, Cu thickness 0,070 mm for outer layers, 0.0035 mm for inner layers, 5x4 thermal vias on 1.2x1.2 mm pads and clearance of 0.2 mm, thermal via diameter 0.3 mm ± 0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 6 mm x 6 mm.

4.3 Electrical characteristics

For an efficient and easy tracking, numbering has been added to each electrical parameter.

Device features are split into categories, see *Table 5*, and each of them is represented by a Letter (A, B, C, etc); all parameters will be completely identified by a letter and three digit number (e.g. B.125, C.096…) for their whole lifetime.

New inserted parameters will continue with the numbering of the related category, no matter of where they are placed.

To facilitate insertion, the last number inserted for each category is also reported in *Table 5*.

Table 5. Electrical parameters numbering

Category	Parameters numbering	Last Inserted
Analog I/O	A.xxx	A.040
Digital I/O	B.xxx	B.034
Voltage Regulators(1)	C.xxx	
Outputs	D.xxx	D.063
Transceivers (1)	E.xxx	
Others	F.xxx	F.005

1. Category not present in L99UDL01.

Due to these rules and taking into account that deleted parameter numbers will be no more reassigned, numbering inside each category may be not sequential.
All the electrical parameters reported in the following sections are evaluated with L99UDL01 in Normal Mode.

4.3.1 Supply

Table 6. Supply voltage parameters

Electrical characteristics (-40°C < T_J < 130°C, 6 V < V_S < 18 V unless otherwise specified)							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
A.001	VS_{OPER}	V_S Operating Supply Voltage		6		18	V
A.002	VS_{OPER_EXT}	Extended V_S Operating Supply Voltage(1)		5		26	V
A.003	$I_{Q(Vs)}$ on	V_S Supply current on-state	Sum of all VSx, DRNx and VS pins, All VSx = DRNx = VS = 13 V, OUTx floating		13	18	mA
A.004	$I_{Q(VSx)\ STBY}$	VSx supplies leakage current	Sum of all VSx pins VSx = 13 V, STBY bit = 1 OUTx floating -40°C to 25°C		1	6	µA
A.005			125°C			20	
A.006	$I_{Q(VSx)\ SLEEP}$	VSx supplies leakage current	Sum of all VSx pins VSx = 13 V, VDD<VDD_{SLEEP} OUTx floating -40°C to 25°C		1	6	µA
A.007			125°C			25	
A.008	$I_{Q(Vs)\ STBY}$	VS supply Standby consumption current in STBY mode	VS = 13 V, STBY bit = 1 VDD>VDD_{SLEEP} -40°C to 25°C		30		µA
A.009			125°C			50	
A.010	$I_{Q(Vs)\ SLEEP}$	VS supply Standby consumption current in Sleep mode	VS = 13 V VDD<VDD_{SLEEP} OUTx floating -40°C to 25°C		7		µA
A.011			125°C			15	
A.012	VDD_{OPER}	V_{DD} Operating Supply Voltage		2.5		5.5	V
A.013	VDD_{SLEEP_F}	VDD sleep threshold (falling).	A VDD below this threshold will force the L99UDL01 into Sleep mode. No supply is available at this time.	0.3	1.0	1.5	V

Table 6. Supply voltage parameters (continued)

Electrical characteristics (-40°C < T_J < 130°C, 6 V < V_S < 18 V unless otherwise specified)							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
A.014	VDD_{SLEEP_R}	VDD sleep threshold (rising).	Upon rising into the operating voltage range the L99UDL01 will enter Standby mode and the RSTB bit in the Global status register will be set.	0.4	1.3	1.9	V
A.015	VDD_{SLEEP_HYST}	VDD sleep threshold Hysteresis.			0.25		V
A.016	VDD_{UV}		Below this threshold the control registers are reset and the device enters standby. The RSTB bit in the Global status register will be set.	2		2.5	V
A.017	VDD_{UV_Hyst}				0.1		V
A.018	t_{VDDUV}	VDD Undervoltage filter time	Tested by scan		64		µs
A.019	V3V3	V3V3 Voltage	Device in RUN mode 220 nF cap on C3V3 pin	3.13	3.3	3.46	V
A.020	$V3V3_{RST\_F}$	V3V3 reset threshold (falling). Will cause a logic reset	3.3 V regulator voltage below this threshold will hold the L99UDL01 logic state machine into reset.	2.25		2.65	V
A.021	$V3V3_{RST\_R}$	V3V3 reset threshold (rising). Will cause a logic reset	Once in 3V3 reset (A.020), upon rising above $V3V3_{RST\_R}$ the L99UDL01 will enter Standby mode and the RSTB bit in the Global status register will be set.	2.4		2.95	V
A.022	$V3V3_{RST\_HYST}$	V3V3 reset threshold Hysteresis.			0.15		V
A.023	t_{3V3UV}	3V3 undervoltage filter time	Tested by scan		64		µs
A.024	$V3V3_{UV\_F}$	V3V3 undervoltage threshold (falling).	3.3 V regulator voltage below this threshold will disable all outputs internal and external and the V3V3UV bit in status register 13h will be set.	V3V3-0.3	V3V3-0.25	V3V3-0.1	V
A.025	$V3V3_{UV\_R}$	V3V3 undervoltage threshold (rising).	3.3 V regulator voltage upon rising into the operating voltage range the L99UDL01 will enter Normal and ready mode.	V3V3-0.25	V3V3-0.15	V3V3-0.05	V
A.026	$V3V3_{UV\_HYST}$				0.1		V

Table 6. Supply voltage parameters (continued)

Electrical characteristics (-40°C < T_J < 130°C, 6 V < V_S < 18 V unless otherwise specified)							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
A.027	$V3V3_{prereg}$	Preregulated Voltage	Device in Standby		2.95		V
A.028	$I_{VDD\ run}$	VDD Supply run current	– GFI enabled – SPI active (CSN low) – VDD = 5 V		1.05	1.3	mA
A.029	$I_{VDD\ inactive}$	VDD Supply inactive current	– GFI disabled – SPI inactive (CSN high)		60	120	µA
A.030	$I_{VDD\ STBY}$	VDD Supply STBY current	STBY bit = 1		2	5	µA

1. In the VS_{OPER_EXT} range, the functionality of the device is guaranteed by design and some parameters may shift (spec parameters are guaranteed only in the VS_{OPER} range).

4.3.2 Oscillator

Table 7. Oscillator

Electrical characteristics (-40°C < T_J < 130°C, 6 V < V_S < 18 V unless otherwise specified)							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
A.040	f_{clk}	Internal Oscillator frequency range		8	10	12	MHz

4.3.3 Turn-on/off timing

Table 8. On/Off timing parameters

Electrical characteristics (-40°C < T_J < 130°C, 6V < V_S < 18V unless otherwise specified)							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
F.001	$t_{ON\ RANGE}$	Typical Programmable on time duration	tON_x[4:0] Tested by scan	100		1040	ms
F.002	$t_{ON\ STEP}$	Typical Step Size per bit	tON_x[4 :0] ≤ F (Hex) Tested by scan		20		ms
F.003			tON_x[4 :0] > F (Hex) Tested by scan		40		
F.004	$t_{OFF\ RANGE}$	Typical Programmable off time duration	tOFF_x = [0:0], [0:1], [0:1] Tested by scan	0		200	ms
F.005	$t_{OFF\ STEP}$	Typical Step Size per bit	0 < tOFF_x[1:0] < 3 Tested by scan		100		ms

4.3.4 Integrated half bridge

Table 9. Integrated half-bridge DC parameters

Electrical characteristics (-40°C < T_J < 130°C, 6V < V_S < 18V unless otherwise specified)							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
D.001	Ron_HS	Static on resistance High side switch $R_{DS(on)}$	25°C, I_{OUT}=2 A		90		mΩ
D.002			-40°C < TJ < 125°C, I_{OUT}=2 A			180	
D.003	Ron_LS	Static on resistance Low side switch $R_{DS(on)}$	25°C, I_{OUT}=2 A		90		mΩ
D.004			-40°C < TJ < 125°C, I_{OUT}=2 A			180	
D.005	$I_{OUTLEAK}$	Output pulled to Ground	-40°C < TJ < 25°C, All outputs off			2	µA
D.006			25°C < TJ < 125°C, All outputs off			6	
D.007	$I_{OUTLEAK}$	Output pulled to Ground	At least one output on		180	250	µA
D.008	$I_{OUTLEAK}$	Output pulled to VSx	At least one output on		40	80	µA
D.009	$I_{OUTLEAK}$	Output pulled to VSx	-40°C < TJ < 125°C All outputs off	-55	-35		µA
D.012	V_{OUT_th}	Dynamic output voltage threshold		1.5	1.8	2.1	V
D.013	$I_{REG\ Range}$	Current regulation range	OCPx(0;3) = 0 to F One output only, Max ripple = 20%	1		4	A
D.014	I_{REG_STEP}	Current regulation step size			200		mA
D.015	I_{REG_TOL}	Current Regulation Tolerance	OCPx(0:3) = 7h	-15		15	%

4.3.5 Integrated half bridge current control loop

Table 10. Integrated half-bridge current control parameters

Electrical characteristics (-40°C < T_J < 130°C, 6V < V_S < 18V unless otherwise specified)							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
D.016	Ki	Integral gain factor 2^{Ki}	3 bits from 2^{-7} to 2^0 Tested by scan		2^X		
D.017	Kp	Proportional gain factor 2^{Kp}	3 bits from 2^1 to 2^8 Tested by scan		2^X		
D.018	K_{FB}	Current feedback conversion per LSB $Reg_{X[1-10]} \times K_{FB} = I_{measure}$	$Reg_{X[1-10]}$ = Values read in registers 13H- 18H		6.25		mA / bit
D.019	K_{FB_tol}	Current feedback conversion tolerance	Values read in registers 13H-18H	-15		+15	%

4.3.6 External half bridge

Table 11. External half-bridge parameters

Electrical characteristics (-40°C < T_J < 130°C, 6V < V_S < 18V unless otherwise specified)							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
D.020	V_{GATEH_on}	GATEH/EXTx output voltage when enabled	VCP > VCP_min, output commanded on	V_{SRCX} +5	V_{SRCX} +10	V_{SRCX} +13.5	V
D.021	I_{GATEH_on}	GATEH/EXTx rising current	Transition from off to on, VS=13.5 V, VSHx=0, VGHx=3 V	14	20		mA
D.022	I_{GATEH_off}	GATEH/EXTx falling current	Transition from on to off VS=13.5 V, VSHx=0, VGHx=3 V	14	20		mA
D.023	R_{GSHx}	GATEH/EXTx Gate-Source passive discharge resistance	Device in STBY (STBY bit=1)	10	15	20	kΩ
D.024	V_{GATEL_on}	GATEL/EXTx output voltage when enabled	Output commanded on	6		13.5	V
D.025	I_{GATEL_on}	GATEL/EXTx rising current	Transition from off to on VS=13.5 V, VGLx=3 V	15	20		mA
D.026	I_{GATEL_off}	GATEL/EXTx falling current	Transition from on to off VS=13.5 V, VGLx=3 V	15	20		mA
D.027	R_{GSLIx}	GATEL Gate-Source passive discharge resistance	Device in SLEEP mode	10	15	20	kΩ
D.028	t_{DT} (1)	Cross conduction dead time for external MOSFETs	Transitioning from either direction. Tested by scan		6		µs
D.029	V_{OUT_th}	Dynamic output voltage threshold		1.5	1.8	2.1	V
D.030	C_{max}	Maximum Capacitive load on Gate Drive pins	For cross conduction prevention.			1000	pF

1. t_{DT} typ. value is 10 µsec in the following cases:
   a. the external output is configured in overridden mode and the device is in emergency mode, or
   b. L99UDL01 is in Normal mode coming from Emergency mode without disabling and then enabling again the External Output (EX_OUTx_on) overridden control bit

4.3.7 Charge pump

Table 12. Charge pump parameters

Electrical characteristics (-40°C < T_J < 130°C, 6V < V_S < 18V unless otherwise specified)							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
A.031	V_{CP_LV}	Charge pump output voltage	Vs=6 V; I_{CP}=15 mA; C_{CPx}=100 nF; C_{CP}=100 nF	VS+6	VS+7		V
A.032	V_{CP}	Charge pump output voltage	Vs>10 V; I_{CP}=15 mA; C_{CPx}=100 nF; C_{CP}=100 nF	VS+11	VS+12	VS + 13.5	V
A.033	I_{CP}	Charge pump output current	VS=13.5 V; V_{CP}=VS+10 V; C_{CPx}= C_{CP}=100 nF	23			mA
A.034	I_{CP_lim}	Charge pump output current limit	VS= V_{CP}=13.5 V; C_{CPx}= C_{CP}=100 nF			70	mA
A.035	f_{CP}	Charge Pump Frequency	Tested by scan		400		kHz
A.036	f_{Dither}	Typical Charge pump frequency dither range	VS=13.5 V; V_{CP}=VS+10 V; DITH=1; Tested by scan	-75		75	kHz
A.037	t_{CP}	Charge pump filter time	Tested by scan		64		µs
A.038	V_{CPLOW}	Charge pump output low		VS + 4.5	VS + 5.0	VS + 5.5	V
A.039	t_{set_CP}	Delay time from Charge Pump Enable	Charge pump set-up Tested by scan	560	750	960	µs

4.3.8 Protections

Table 13. Protections

Electrical characteristics (-40°C < T_J < 130°C, 6V < V_S < 18V unless otherwise specified)							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
D.031	T_{SD}	Thermal Shutdown temperature threshold	OUT_X disabled after T_{SD}, Condition reported on SPI (TSDx bit latched)	160	175	190	°C
D.032	T_{SD_RES}	Thermal Shutdown Reset	Output can be reenabled after TSDx bit is read and cleared.		T_{SD}-10		°C
D.033	VS_{OVSD}	Overvoltage shutdown, rising edge	Above this threshold the integrated drivers are tri-stated and the external high side pre-drivers are turned off.	26		28	V
D.034	VS_{OVSD_HYST}	Supply voltage inhibit threshold Hysteresis			1.5		V
D.035	t_{VSOV}	Overvoltage filter time	Tested by scan		64		µs
D.036	VS_{LVI_F}	Supply voltage inhibit threshold	Falling edge	4.5	4.75	5	V

Table 13. Protections (continued)

Electrical characteristics (-40°C < T_J < 130°C, 6V < V_S < 18V unless otherwise specified)							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
D.037	VS_{LVI_R}	Supply voltage inhibit threshold	Rising edge	5	5.25	5.5	V
D.038	VS_{LVI_HYST}	Inhibit threshold Hysteresis			0.5		V
D.039	t_{VSLVI}	Low Voltage inhibit filter time	Tested by scan		64		µs
D.040	T_W	Thermal warning temperature threshold	Fault is reported in SPI register T_{Wx} bits only	140	150	160	°C
D.041	T_{W_RES}	Thermal warning Reset	Fault can be read and cleared.		T_W-10		°C
D.042	V_{DS_TH}	Typical Drain to Source overvoltage voltage range	This parameter is programmable in 0.25 V increments. See V_{DS} Protection programming register 06H	0.25		2	V
D.043	$V_{DS\_TH\ Step\ size}$	Programmed step size			0.25		V
D.044	$V_{DS\_TH\ Step\ tolerance}$	VDS Programming step size tolerance	Voltage tolerance per bit change	-15	0	+15	%
D.063			Voltage tolerance per bit change (only for EXTx_VDSx = 1000)	-67.5		+67.5	mV
D.045	t_{VDS_BLANK}	VDS fault blanking time range	Start from turn on command This is a programmable parameter. Refer to Register 06H Tested by scan	1		4	µs
D.046	t_{VDS_STEP}	VDS Fault blanking time step size	Step size per bit (EXTx_VDt_y) Refer to Register 06H Tested by scan		1		µs
D.047	t_{VDS_FILTER}	VDS fault filter time	Tested by scan		1		µs
D.048	I_{DIAG}	Diagnostic current	ODCLx/ODCHx bit set Source		-0.5		mA
D.049			Sink		2.5		
D.050	I_{DIAG_EXT}	Diagnostic current	HBDCLx/HBDCHx bit set Source		-0.5		mA
D.051			Sink		2.5		
D.052	I_{OC_HS}	Overcurrent(1)	Single output commanded high VOUTx = 0 V	5.3			A
D.053	I_{OC_LS}	Overcurrent(1)	Single output commanded low VOUTx = VS	5.3			A

Table 13. Protections (continued)

Electrical characteristics (-40°C < T_J < 130°C, 6V < V_S < 18V unless otherwise specified)							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
D.054	$t_{OC\_BLANKING}$	Integrated driver Blanking time during switching	Duration from output commanded on to start of fault current detection Output commanded to opposite rail of short connection Tested by scan		3		µs
D.055	t_{OC_FILTER}	Filter time to avoid false overcurrent detections during current spikes	Tested by scan		1.5		µs
D.056	$V_{DS\_ON\_LS}$	Low side active freewheeling threshold	Active Freewheeling enabled current is freewheeling through the low side internal MOSFET	-50		150	mV
D.057	$V_{DS\_ON\_HS}$	High side active freewheeling threshold	Active Freewheeling enabled current is freewheeling through the high side internal MOSFET	Vs-1.3	Vs-1.1	Vs-0.9	V

1. This current is for one output on. If outputs are grouped this value is multiplied by the number of outputs in the group.

4.3.9 Integrated half bridge AC characteristics

Table 14. Integrated half bridge AC characteristics

Electrical characteristics (-40°C < T_J < 130°C, 6 V < V_S < 18 V unless otherwise specified.)							
Req ID	**Symbol**	**Parameter**	**Test condition**	**Min.**	**Typ.**	**Max.**	**Unit**
D.058	t_r	Output rise time	One output on, R_{LOAD}=6.5 Ohm, VS=13 V 20% to 80% VS	5		20	V/µs
D.059	t_f	Output fall time	One output on, R_{LOAD}=6.5 Ohm, VS=13 V 80% to 20% VS	5		20	V/µs
D.060	$f_{PWM\ TOL}$	PWM frequency tolerance		-20	10	20	%
D.061	$f_{PWM\ STEP}$	PWM frequency Step size	Frequency difference per bit (register 00H) Tested by scan		2.0		kHz
D.062	$f_{PWM\ RANGE}$	Typical frequency range	3 bits @ 2kHz per bit Tested by scan	10		24	kHz

4.3.10 I/O and SPI

Table 15. I/O Parameters, CLK, SDO, SDI, CSN, EN_OUT, DOUT

Electrical characteristics (-40°C < T_J < 130°C, 6V < V_S < 18V unless otherwise specified)							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
B.001	V_{IL}	Input Low Voltage	CLK, SDI, CSN, EN_OUT	1.0	1.45		V
B.002	V_{IH}	Input High voltage	CLK, SDI, CSN, EN_OUT		1.85	2.3	V
B.003	$V_{I(HYST)}$	Input Threshold Hysteresis	CLK, SDI, CSN, EN_OUT	0.2	0.4		V
B.004	t_{EN}	EN_OUT filter time	Rising and falling edge of EN_OUT Tested by scan		64	82	µs
B.005	t_{CSN_EN}	Output enable delay from rising edge of CSN	CSN rising on command register 01H with OUT_ON bit high Tested by scan		11		µs
B.006	R_{pu_csn}	CSN pull up resistance		35	70	140	kΩ
B.007	$R_{pd\_EN\_OUT}$	EN_OUT pull down resistance	V_{EN_OUT} = 1.5V		40		kΩ
B.008	I_{PD_SDI}	Pull down current	V_{SDI} = 1V		50		µA
B.009	I_{PD_CLK}	Pull down current	V_{CLK} = 1V		50		µA
B.010	I_{DOLK}	Tri-state SDO leakage current	0V < V_{DO} < VDD, V_{CSN}=VDD	-10		10	µA
B.011	C_{DO}	Tri-state SDO input capacitance	Guaranteed by design		10	15	pF
B.012	V_{OL}	SDO, DOUT Output low voltage	I_{OUT}<4mA,	0		0.5	V
B.013	t_{CSN}	CSN Timeout	CSN held low	20	35	50	ms
B.014	V_{OH}	SDO, DOUT Output high voltage	I_{OUT}<4 mA,	VDD-0.5		VDD	V
B.015	f_{IN}	Signal Frequency Range	I_{OUT}<25 µA, CL<60 pF	DC		4	MHz
B.016	t_{rise}	CLK, SDI, CSN rise time				25	ns
B.017	t_{fall}	CLK, SDI, CSN fall time				25	ns

4.3.11 SPI timing

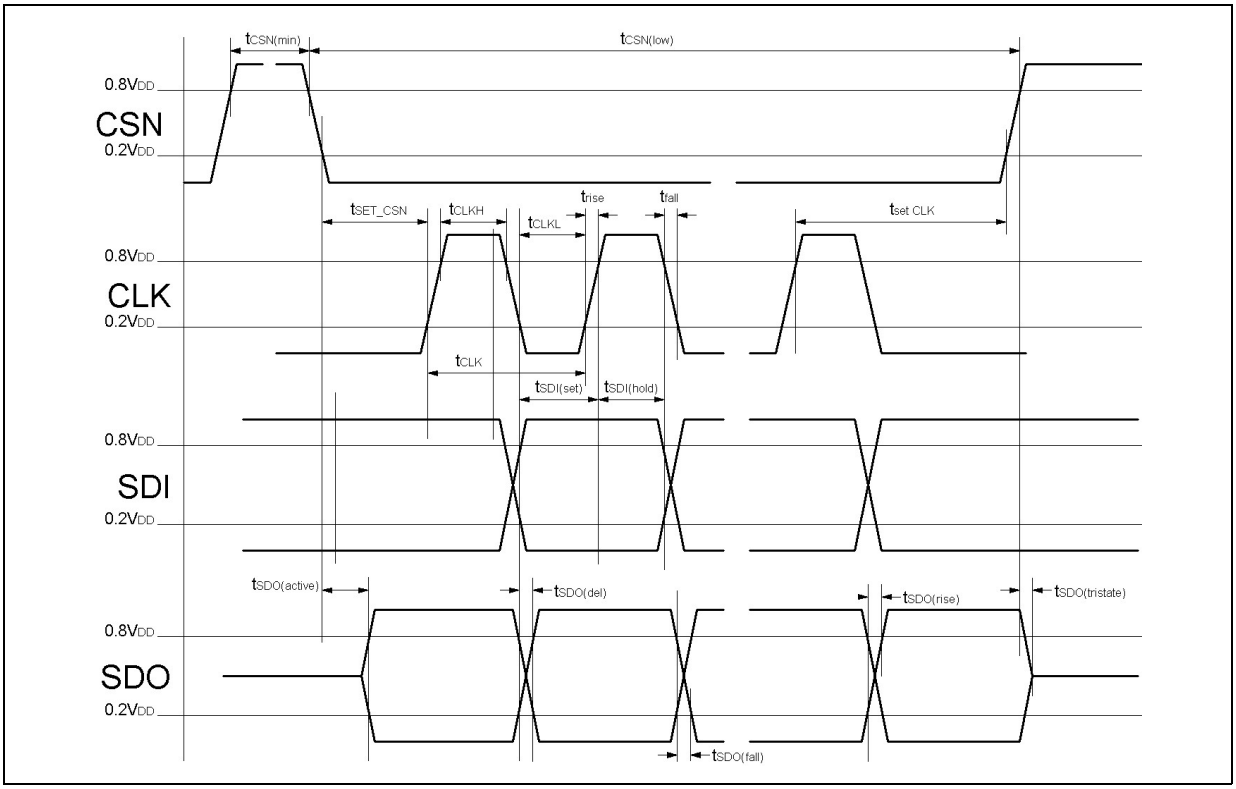
Table 16. SPI timing parameters

Electrical characteristics (-40°C < T_J < 130°C, 6V < V_S < 18V unless otherwise specified)							
SPI Timing Parameters							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
B.018	t_{CLK}	CLK period		250			ns
B.019	t_{CLKH}	Minimum CLK high time		100			ns
B.020	t_{CLKL}	Minimum CLK low time		100			ns
B.021	$t_{set\ CSN}$	CSN setup time, CSN low before CLK rising	Active device in Normal Mode, not in STBY	150			ns
B.022	t_{wake_up}	Minimum CSN low pulse timing needed before the first SPI access	Wake up from Standby to Normal mode	150			µs
B.023	$t_{set\ CLK}$	CLK setup time before CSN rising		150			ns
B.024	$t_{SDI(set)}$	SDI setup time before CLK rising		25			ns
B.025	$t_{SDI(hold)}$	SDI hold time		25			ns
B.026	$t_{SDO(rise)}$	Rise time of SDO	CL=50 pF; guaranteed by design			25	ns
B.027	$t_{SDO(fall)}$	Fall time of SDO	CL=50 pF; guaranteed by design			25	ns
B.028	$t_{en\ DO\ tri\ H}$	CSN falling until SDO high	C_L = 50 pF, SDO=HZ t1": I_{LOAD}=-1 mA; Pull-down load to GND; Active device in Normal Mode		50	100	ns
B.029	$t_{en\ DO\ tri\ L}$	CSN falling until SDO low	SDO=HZ t0": I_{LOAD}=1 mA; Pull-up load to VCC; Active device in Normal Mode		50	100	ns
B.030	$t_{SDO(wake)}$	CSN falling until SDO valid	C_L = 50 pF, I_{LOAD}=-1 mA Pull-down load to GND	0.15		1	ms
B.031	$t_{dis\ DO\ H\ tri}$	CSN rising until SDO from high to tristate	C_L = 50 pF, I_{LOAD}=-4 mA Pull-down load to GND Active device in Normal Mode		50	100	ns
B.032	$t_{dis\ DO\ L\ tri}$	CSN rising until SDO from low to tristate	C_L = 50 pF, I_{LOAD}=4 mA Pull-up load to VDD Active device in Normal Mode		50	100	ns

Table 16. SPI timing parameters (continued)

Electrical characteristics (-40°C < T_J < 130°C, 6V < V_S < 18V unless otherwise specified)							
SPI Timing Parameters							
Req ID	**Symbol**	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
B.033	$t_{CSN(min)}$	Minimum CSN high time		6			µs
B.034	$t_{SDO(del)}$	SDO delay time	V_{DO} < 0.3VDD, V_{DO} > 0.7VDD C_L = 50 pF Active device in Normal Mode		30	60	ns

Figure 11. SPI timing diagram



4.4 ESD protection

Table 17. ESD protection

Parameter	Value	Unit
All pins(1)	+/-2	kV
Power Output pins(2): OUT1-6, GND1-6, VS1-6, DRN1-2, SRC1-2, GNDEXT1-2, GATEH1-2, GATEL1-2, VS and GND	+/-4	kV
All pins(3)	+/-500	V
Corner pins(3)	+/-750	V

1. HBM (Human Body Model, 100 pF, 1.5 kΩ) according to joint standard ANSI/ESDA/JEDEC JS-001-2014.
2. HBM with all none zapped pins grounded.
3. Charge Device Model (AEC_Q100-011).

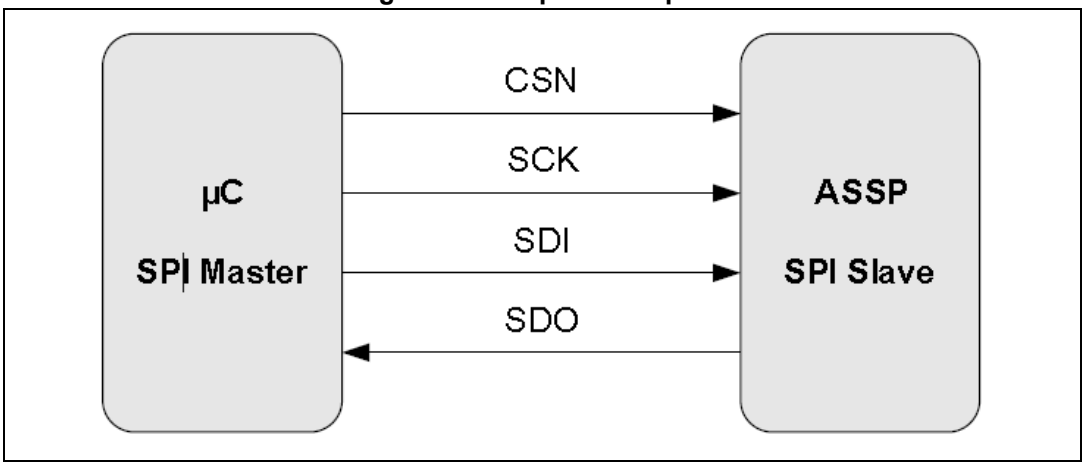
5 Serial communications

5.1 General information

The ST-SPI is a common serial peripheral interface protocol used in ST's Automotive ASSP devices. ST-SPI uses an in-frame response protocol for all communications providing for a global status byte to be communicated for every SPI transmission.

5.1.1 Physical Layer

Figure 12. SPI pin description



5.2 Signal description

5.2.1 Chip Select Not (CSN)

The communication interface is deselected, when this input signal is logically high. A falling edge on CSN enables and starts the communication while a rising edge finishes the communication and the sent command is executed when a valid frame was sent. During communication start and stop the Serial Clock (SCK) has to be logically low. The Serial Data-Out (SDO) is in high impedance when CSN is high or a communication timeout was detected (refer to CSN timeout).

5.2.2 Serial Clock (SCK)

This SCK provides the clock of the SPI. Data present at Serial Data Input (SDI) is latched on the rising edge of Serial Clock (SCK) into the internal shift registers while on the falling edge data from the internal shift registers are shifted out to Serial-Data-Out (SDO).

5.2.3 Serial Data Input (SDI)

This input is used to transfer data serially into the device. Data is latched on the rising edge of Serial Clock (SCK).

5.2.4 Serial Data Output (SDO)

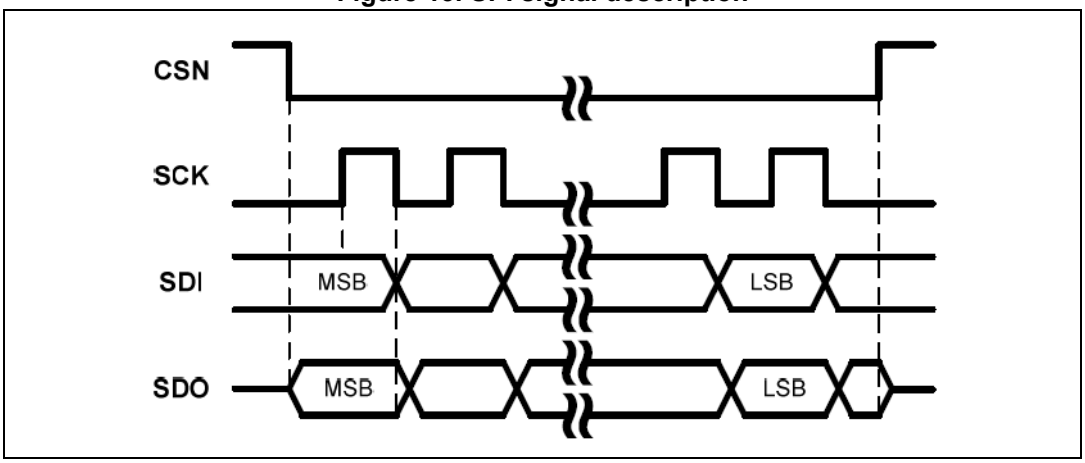
This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK).

5.3 Clock and data characteristics

The ST-SPI can be driven by a microcontroller with its SPI peripheral running in following mode:

- CPOL = 0 and CPHA = 0.

Figure 13. SPI signal description



The communication frame starts with the falling edge of the CSN (Communication Start). SCK has to be low. The SDI data is then latched at all following rising SCK edges into the internal shift registers.

After Communication Start the SDO will leave Tristate mode and present the MSB of the data shifted out to SDO. At all following falling SCK edges data is shifted out through the internal shift registers to SDO.

The communication frame is finished with the rising edge of CSN. If a valid communication took place (e.g. correct number of SCK cycles), the requested operation by the OpCode will be performed (Write or Clear operation).

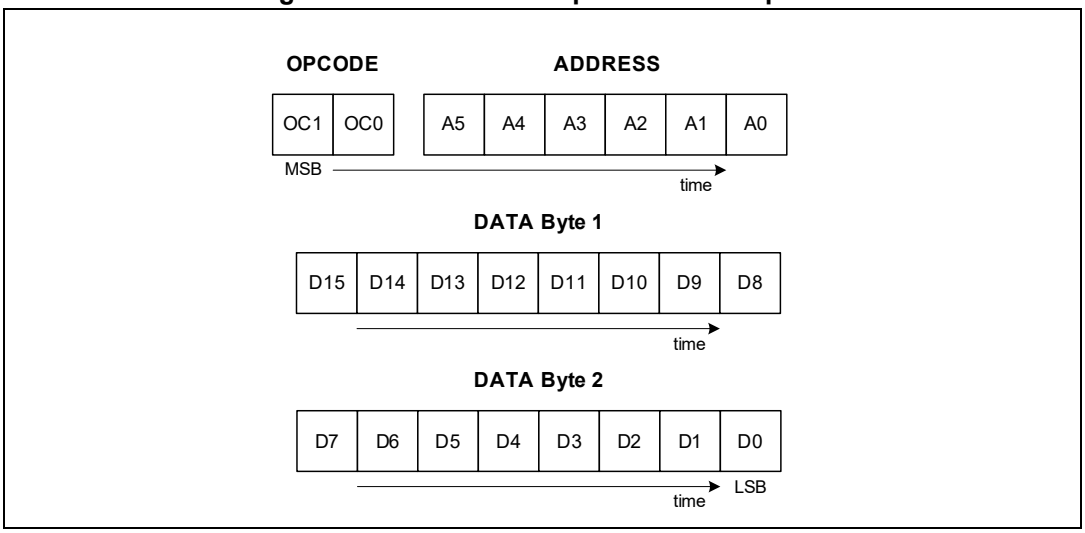
5.4 Protocol

The Data-In Frame consist of 24 bits (OpCode + Address + Data1 + Data2) (see *Figure 12: SPI pin description*). The first two transmitted bits (OC1, OC2) contain the Operation Code which represents the instruction that will be performed. The following 6 bits (A5 to A0) represent the address on which the operation will be performed.

The subsequent 2 bytes (D15 – D0) contain the payload data.

All data are written and read using within the same 24 bit frame.

Figure 14. SPI command protocol description



5.5 Operating codes

The operating code is used to distinguish different modes in the registers of the slave device.

Table 18. Op code description

OC1	OC0	Description
0	0	Write operation
0	1	Read operation
1	0	Read & clear operation
1	1	Read device information

A *Write Operation* will lead to a modification of the addressed data by the payload if a write access is allowed (e.g. Control Register, valid data). Beside this a shift out of the content (data present at Communication Start) of the registers is performed.

A *Read Operation* shifts out the data present in the addressed register at Communication Start. The payload data will be ignored and internal data will not be modified.

A *Read & Clear Operation* will lead to a clear of addressed status bits. The bits to be cleared are defined first by address, second by payload bits set to ‘1’. Beside this a shift out of the content (data present at Communication Start) of the registers is performed.

Note: Status registers which change status during communication could be cleared by the actual Read & Clear Operation and are neither reported in actual communication nor in the following communications. To avoid a loss of any reported status it is recommended to just clear status registers which are already reported in the previous communication (Selective Bitwise Clear).

5.5.1 Advanced operation codes

There are two Advanced Operation Codes that can be used to set all control registers to the default value or to clear all status registers. These are available along with the separate write of all control registers and the bitwise clear of all status registers.

To execute a ‘set all control registers to default’ command, an OpCode ‘11’ at address b’111111 is written to the SPI bus. (This is equivalent to the Read-Access to the ROM area 3FH: [11][111111]=0xFF)

To execute a ‘clear all status registers’ command, an OpCode ‘10’ at address b’111111 is written on the SPI bus. (This is equivalent to the Read & Clear to the RAM area 3FH: [10][111111]=0xBF)

Please note that dynamic status registers or ongoing status indications (e.g. thermal warning or thermal shutdown) may be re-set even after being cleared by this command.

5.6 Register change during communication

From implementation point of view it is guaranteed that no register change gets lost during communication. In case a register value was changed during a communication it will be reported with the next communication frame.

5.7 GSB and payload inconsistency

Due to internal implementation strategy it may occur that data reported in the GSB does not match with data reported in the payload in case the data was changed during GSB shift out. In this case the payload data is the status quo as it was loaded later into the SPI’s shift register.

5.8 Address

The two bits OpCode togheter with the six Address bits are a fixed part of the communication frame. The six bits, in combination with the OpCode, allow to access to a 2 x 64 wide address range.

Table 19. Control register addresses

Control registers		
RAM ADDR	**Register**	**RWC**
09H	Spare Control Register (Not used)	R/W
08H	Control Register 08H	R/W
...	...	...
02H	Control Register 02H	R/W
01H	Control Register 01H	R/W
00H	Control Register 00H	R/W
00h	Device commands	RWC

Table 20. Status registers addresses

Status registers		
RAM ADDR	**Register**	**RWC**
18H	Status register 18H	R
...	...	...
13H	Status register 13H	R(1)
12H	Status register 12H	R/R&C
11H	Status register 11H	R/R&C
10H	Status register 10H	R/R&C

1. Just the V3V3UV flag can be cleared

5.9 Data-In payload

The Payload (Data Byte 1 and Data byte 2) is the data transferred to the L99UDL01 with every SPI communication. The Payload always follows the OpCode and the Address bits.

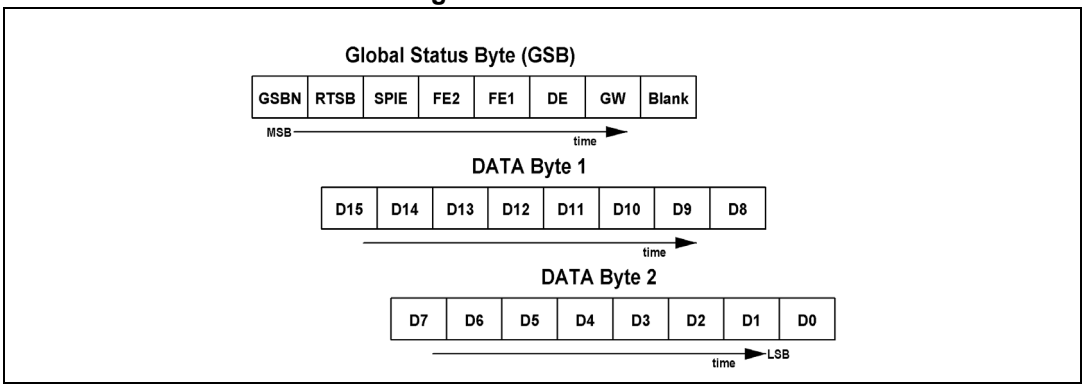
For write accesses, the Payload represents the new data written to the addresses registers. For Read & Clear operations the Payload indicates which bits to clear in the Status Register. For every payload bit set to a “1” the corresponding Status bit is cleared.

For a Read Operation the Payload bits are not used. For functional safety reasons it is recommended to set the unused Payload bits to ‘0’.

5.10 SDO frame

The Data-Out Frame consist of a Frame length 24 bits (GSB+Data1+Data2). The first eight transmitted bits contain device related status information and are latched into the shift register at the time of the Communication Start (falling edge of CSN). These 8 bits are called the Global Status Byte (GSB) and are transmitted at every SPI transaction.

Figure 15. SDO frame



The subsequent bytes contain the payload data and are latched into the shift register with every eighth positive SCK edge. This could lead to an inconsistency of data between the GSB and Payload due to different shift register load times. It should be noted that no

unwanted Status Register clear should occur, as status information is only cleared with a dedicated bit clear after read.

5.11 Global status byte

The global status byte is a read only register that appears on every SPI transmission on the SDO pin. Bit definition can be found in the programmers guide.

5.12 Parity

To ensure proper communication every SPI frame has a parity bit (odd). If a parity error is detected, then the data is discarded and the SPI Error (SPIE) bit in the Global Status Byte is set. Parity is checked on all incoming frames (SDI) and is generated for all outgoing frames (SDO).

5.13 Clock monitor

The number of clock pulses for each frame is counted. If this number is incorrect then the data is discarded and the SPI Error bit in the Global Status Byte as well as the SPI_FAIL bit in register 10H are set. Note: This feature prevents this SPI bus from being daisy chained.

Providing no SCK edge during a CSN low to high phase is not recognized as an SPIE.

For a SPI Burst Read also the SPI Data Length plus multiple numbers of Payload SCK edges are assumed as a valid communication.

5.14 CSN timeout, (t_{CSN})

By pulling CSN low the SDO is set active and leaves its Tristate condition. To ensure communication between other SPI devices within the same bus even in case of CSN stuck @ low a CSN timeout is implemented. By pulling CSN low an internal timer is started. After timer end is reached the actual communication is rejected and the SDO is set to tri-state condition. This error (CSN timeout, t_{CSN}) is not reported in any specific status register.

5.15 Burst read

Burst read is used to perform a device internal memory dump to the SPI Master. The start of the Burst Read is like a normal Read Operation. The difference is, that after the SPI Data Length the CSN is not pulled high and the SCK will be continuously clocked. When the normal SCK max count is reached (SPI Data Length) the consecutive addressed data will be latched into the shift register. This procedure is performed every time the SCK payload length is reached.

Burst Read will not overrun 3FH. SCK cycles that extend the address beyond 3FH will read the contents of address 3FH until the transmission is terminated by rising CSN.

The SPI Burst Read is limited by the CSN low timeout.

5.16 Device Information Registers

The Device Information Registers can be read by using OpCode ‘11’. After shifting out the GSB the 8bit wide payload will be transmitted. The remaining 8 bits shifted out the SDO will be ‘0’s

Table 21. Device information registers

ROM Addr.	Description	RWC	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20H	<SPI CPHA test>	R	0	1	0	1	0	1	0	1
10H	<SPI mode>	R	A1H							
...										
0AH	<Silicon Ver.>	R	Major revision				Minor revision			
...										
05H	<Device No. 4>	R	03H							
04H	<Device No. 3>	R	5AH							
03H	<Device No. 2>	R	41H							
02H	<Device No. 1>	R	55H							
01H	<Device Family>	R	01H							
00H	<Company Code>	R	00H							

5.16.1 Device Identification Registers (00H => 0AH)

These registers represent a unique signature to identify the device and silicon version.

<Company Code>: 00H (STMicroelectronics)

<Device Family>: 01H (BCD Power Management)

<Device No. 1>: 55H (ASCII code for U)

<Device No. 2>: 41H (ASCII code for A)

<Device No. 3>: 5AH (ASCII code for Z)

<Device No. 4>: 03H (3)

SPI modes

By reading out the <SPI Mode> register general information of SPI usage of the Device Application Registers can be read.

Table 22. SPI modes register

Bit No.	BIT 7	BIT 6	BIT 5	BIT4	BIT 3	BIT 2	BIT 1	BIT 0
Definition	BR	DL2	DL1	DL0	0	0	S1	S0
Default	1	0	1	0	0	0	0	1

**Burst Read bit
**

The SPI Burst Read bit indicates if a burst read operation is implemented.(See Burst Read). This bit is set.

SPI Data Length <DLx>

The SPI Data Length value indicates the counts the SCK count monitor requires for valid accesses to the Device Application Registers. In case a communication frame with an SCK count is not equal to that value (24 for the L99UDL01) SPI Error will be reported and the data will be rejected.

The Frame Length is specified using 3 bits. The L99UDL01 has a 24 Bit SPI using a 16 Bit payload (0,1,0).

Table 23. SPI data length

Bit 6 DL2	Bit 5 DL1	Bit 4 DL0	Description
0	0	0	Invalid
0	0	1	16 Bit SPI (8 Bit payload)
0	1	0	24 Bit SPI (16 Bit payload)
...	...	...	...
1	1	1	64 Bit SPI (56 Bit payload)

Data consistency check (Parity/CRC)

For some devices a Data Consistency Check is required. Therefore either a parity-check or for very sensitive systems a CRC may be implemented.

Table 24. Data consistency bit definition

Bit 1	Bit0	Description
0	0	Not used
0	1	Odd parity used
1	0	CRC used
1	1	Invalid

It is defined on 2 bits, in SPI Mode register located in ROM Part. A check is then applied on the incoming frame (SDI) while a calculation elaborated on one/multiple bits is done and integrated on the outgoing frame (SDO). The L9UDL01 uses standard odd parity.

5.17 SPI registers

5.17.1 SPI control register description

The SPI Command word consists of an OpCode (2 bits) a Parity (1 bit), address (6 bits), and C
The following descriptions are done by SPI address.

5.17.2 Control register overview

Table 25. Control register overview

Bit			23	22	21	20	19	18
Global Status			GSBN	RSTB	SPIE	FE2	FE1	DE
Control Reg								
Addr		Bit	15	14	13	12	11	10
			7	6	5	4	3	2
0x00	CR0	MSB	FPWM2	FPWM1	FPWM0	HSD6	HSD5	HSD4
		LSB	HSD1	LSD6	LSD5	LSD4	LSD3	LSD2
0x01	CR1	MSB	EX_OUT2_on	EX_OUT1_on	OUT6_on	OUT5_on	OUT4_on	OUT3_on
		LSB	EMCY1	EMCY0	EXT2_HSD	EXT1_HSD	EXT2_LSD	EXT1_LSD
0x02	CR2	MSB	DBN_EX2	DBN_EX1	DBN_6	DBN_5	DBN_4	DBN_3
		LSB	tON_4	tON_3	tON_2	tON_1	tON_0	tOFF _1
0x03	CR3	MSB	RES	RES	RES	RES	RES	RES
		LSB	GFI	TSD_ACT	DITHN	GRP2_6	GRP2_5	GRP1_3
0x04	CR4	MSB	C/PWM_SW_3	OCP3_3	OCP3_2	OCP3_1	OCP3_0	C/PWM_SW_2
		LSB	OCP2_1	OCP2_0	C/PWM_SW_1	OCP1_3	OCP1_2	OCP1_1
0x05	CR5	MSB	C/PWM_SW_6	OCP6_3	OCP6_2	OCP6_1	OCP6_0	C/PWM_SW_5
		LSB	OCP5_1	OCP5_0	C/PWM_SW_4	OCP4_3	OCP4_2	OCP4_1
0x06	CR6	MSB	HBDCL2	HBDCH2	STBY1	EXT2_VDt_1	EXT2_VDt_0	EXT1_VDt_1
		LSB	EXT2_VDS_2	EXT2_VDS_1	EXT2_VDS_0	EXT1_VDS_3	EXT1_VDS_2	EXT1_VDS_1
0x07	CR7	MSB	HBDCL1	HBDCH1	STBY2	ODCL6	ODCH6	ODCL5
		LSB	ODCH4	ODCL3	ODCH3	ODCL2	ODCH2	ODCL1
0x08	CR8	MSB	RES	RES	RES	RES	RES	RES
		LSB	RES	KI_2	KI_1	KI_0	KP_2	KP_1

5.17.3 Output configuration registers

GRPx registers

There are 2 sets of registers that define what outputs are set to work in parallel. This is necessary to share current regulation functionality when paralleling outputs. The definitions provide 2 different groups of outputs (GRP_1-GRP_2). Those outputs not in groups can be driven individually. They should not be driven in parallel with another output if they are not in a parallel grouping.

Current/voltage regulation registers

There are 6 separate current / voltage regulation parameters. One parameter for each of the integrated half bridges.

These parameters define the regulation current or the duty cycle for any of the six integrated half bridge outputs

5.18 SPI status register definitions

5.18.1 Status register overview

Table 26. Status register overview

Bit			23	22	21	20	19	18
Global Status			GSBN	RSTB	SPIE	FE2	FE1	DE
Control Reg								
Addr		Bit	15	14	13	12	11	10
			7	6	5	4	3	2
0x10	SR0	MSB	SPI_Fail	WRT_Fail	RD_Fail	FLT6_1	FLT6_0	FLT5_1
		LSB	FLT4_0	FLT3_1	FLT3_0	FLT2_1	FLT2_0	FLT1_1
0x11	SR1	MSB	VDDUV	STAT1	STAT0	DOS_EXT2	DOS_EXT1	DOS6
		LSB	DOS3	DOS2	DOS1	EXTF2_1	EXTF2_0	EXTF1_1
0x12	SR2	MSB	CPLOW	VSLVI	VSOVSD	TSD6	TSD5	TSD4
		LSB	TSD1	TW6	TW5	TW4	TW3	TW2
0x13	SR3	MSB	V3V3UV	RES	RES	RES	RES	CF1_9
		LSB	CF1_6	CF1_5	CF1_4	CF1_3	CF1_2	CF1_1
0x14	SR4	MSB	RES	RES	RES	RES	RES	CF2_9
		LSB	CF2_6	CF2_5	CF2_4	CF2_3	CF2_2	CF2_1
0x15	SR5	MSB	RES	RES	RES	RES	RES	CF3_9
		LSB	CF3_6	CF3_5	CF3_4	CF3_3	CF3_2	CF3_1
0x16	SR6	MSB	RES	RES	RES	RES	RES	CF4_9
		LSB	CF4_6	CF4_5	CF4_4	CF4_3	CF4_2	CF4_1
0x17	SR7	MSB	RES	RES	RES	RES	RES	CF5_9
		LSB	CF5_6	CF5_5	CF5_4	CF5_3	CF5_2	CF5_1
0x18	SR8	MSB	RES	RES	RES	RES	RES	CF6_9
		LSB	CF6_6	CF6_5	CF6_4	CF6_3	CF6_2	CF6_1

5.18.2 Diagnostics

The L99UDL01 has an high level diagnostic capability. There are general global faults and specific output faults. The following are faults reported for each of the integrated outputs, both high side and low side individually:

- Overcurrent
- Undercurrent
- Open load
- Output State
- Thermal warning
- Thermal shutdown

6 Programmers guide

This programmer's guide is a reference section intended to help in the L99UDL01 interface software development. The L99UDL01 uses SPI messaging for all its communication into or out the device. The Command registers are written to the L99UDL01 by the MASTER μC and the corresponding Status registers are read from the L99UDL01 by the MASTER μC.

6.1 Output Control Registers

The control registers are registers written to the L99UDL01 by the MASTER μC to actuate the L99UDL01 outputs. Each command consists of an address, data bits, and a parity bit. The information written to these registers can either set up or initiate the lock/unlock functionality. The outputs are set up for actuation or can be actuated by these registers.

All writable registers can be written while the device is in timed actuation mode, but not all the data. New information placed in registers 00H through 05H while in timed actuation mode will not be acted upon until after a timed actuation mode is completed. If these registers are written during a timed actuation mode, their contents will be used on a subsequent actuation. Register 06H through 08H are acted upon immediately after the rising edge of CSN.

The device does not support any changes to the output override function during a timed actuation. It means that the output override bits in registers 01H as well as the related output control bits in register 00H must not be modified during a timed actuation. Further, Output Override bits in register 01H cannot be changed while the OUT_ON bit is high. This action is not supported.

6.1.1 Register 00H (Integrated driver control registers)

This register sets up the polarity of the integrated outputs upon actuation. These values will remain in this register even after actuation.

This register also sets up the PWM frequency for the integrated drivers using 3 bits.

This register can be read or written at any time. New data are not acted upon if programmed while in timed actuation. New data will be used in subsequent timed actuations.

Figure 16. Register 00H Integrated output commands

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 0	0 1	0	0	0	0	0	0	FPWM2	FPWM1	FPWM0	HSD6	HSD5	HSD4	HSD3	HSD2	HSD1	LSD6	LSD5	LSD4	LSD3	LSD2	LSD1	Parity
Default Values								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X

Table 27. 00H Command description

Bit#	Command	Description
15	FPWM2	PWM Frequency selection bit 2
14	FPWM1	PWM Frequency selection bit 1

Table 27. 00H Command description

Bit#	Command	Description
13	FPWM0	PWM Frequency selection bit 0
12	HSD6	Hbridge HSD 6 Enable
11	HSD5	Hbridge HSD 5 Enable
10	HSD4	Hbridge HSD 4 Enable
9	HSD3	Hbridge HSD 3 Enable
8	HSD2	Hbridge HSD 2 Enable
7	HSD1	Hbridge HSD 1 Enable
6	LSD6	Hbridge LSD 6 Enable
5	LSD5	Hbridge LSD 5 Enable
4	LSD4	Hbridge LSD 4 Enable
3	LSD3	Hbridge LSD 3 Enable
2	LSD2	Hbridge LSD 2 Enable
1	LSD1	Hbridge LSD 1 Enable
0	Parity	

LSDx, HSDx

These bits determine the polarity of an output. Only a low side driver or a high side driver for a single output can be on at a time. If both a low side driver and a high side driver for a specific output are enabled simultaneously the output will be tri-stated.

Table 28. Polarity command bits

Output polarity		
LSDx	**HSDx**	**Polarity**
0	0	Tristate
0	1	High Side on
1	0	Low Side on
1	1	Tristate

FPWM_x PWM frequency selection

These three bits provide PWM frequency selection to optimize the current regulation / PWM frequency for the loads. This is a global command. All integrated drivers will use the selected frequency to provide PWM voltage control or PWM current control.

Table 29. PWM frequency select bits

PWM Frequency selector			
FPWM_2	**FPWM_1**	**FPWM_ 0**	**Frequency (kHz)**
0	0	0	10.240
0	0	1	12.288
0	1	0	14.336
0	1	1	16.384
1	0	0	18.432
1	0	1	20.480
1	1	0	22.528
1	1	1	24.576

6.1.2 Register 01H (external driver control registers and Output On override bits)

This register sets up the polarity of the external MOSFET controller outputs upon actuation and can actuate these drivers as in register 00H. These values will remain in this register even after actuation.

This register can be read or written. New data is not acted upon if programmed while in timed actuation. New data will be used in subsequent timed actuations.

Figure 17. 01H External driver commands

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 0	0 1	0	0	0	0	0	1	EX_Out2_on	EX_Out1_on	Out6_on	Out5_on	Out4_on	Out3_on	Out2_on	Out1_on	EMCY1	EMCY0	EXT2_HSD	EXT1_HSD	EXT2_LSD	EXT1_LSD	OUT_ON	Parity
Default Values								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X

Table 30. 01H Command description

Bit#	Command	Description
15	EX_OUT2_on	External output 2 override
14	EX_OUT1_on	External output 1 override
13	OUT6_on	Output 6 on override
12	OUT5_on	Output 5 on override
11	OUT4_on	Output 4 on override
10	OUT3_on	Output 3 on override
9	OUT2_on	Output 2 on override

Table 30. 01H Command description (continued)

Bit#	Command	Description
8	OUT1_on	Output 1 on override
7	EMCY1	Emergency override Bit 1
6	EMCY0	Emergency override Bit 0
5	EXT2_HSD	External H-Bridge 2 Output High Enable
4	EXT1_HSD	External H-Bridge 1 Output High Enable
3	EXT2_LSD	External H-Bridge 2 Output Low Enable
2	EXT1_LSD	External H-Bridge 1 Output Low Enable
1	OUT_ON	If set will actuate ALL outputs on CSN rising
0	Parity	

OUT_ON

If the OUT_ON bit is not set when writing to this register then the outputs will be initiated or actuated per the programming on the rising edge of EN_OUT. If the OUT_ON bit in the register is set, then upon the rising edge of CSN the outputs are actuated per the programmed sequence, provided that EN_OUT=1. It should be noted that writing OUT_ON=1 during a timed actuation outside of an Emergency mode is NOT supported and is not recommended.

It needs to take care there are many registers that set up polarity and actuation parameters. When not in timed actuation the OUT_ON bit will initiate actuation upon the rising edge of CSN (provided that EN_OUT=1) using the information that is in all registers. If the OUT_ON bit is set before the other registers are programmed, erroneous behavior may result.

In emergency mode (and EN_OUT=1) the rising edge of CSN will actuate what is in the registers if the OUT_ON bit is set regardless any timed actuation in progress.

OUTx_on / EX_OUTx_on

These bits will override the programmed timed outputs. If this bit is set, it will turn on the indicated output according to the output configuration (high side / low side) indefinitely. This will occur on the rising edge of CSN regardless of the state of the OUT_ON bit or any other register, provided that EN_OUT=1. The output will remain on until the corresponding OUTx_on/ EX_OUTx_on bit is reset or EN_OUT=0. Disengaging an output override only disables that output.

OUTx_on and EX_OUTx_on bits must not be changed at the initiation of or during a timed actuation. Indefinite dynamic braking must be disabled before changing any of the output override bits (OUTx_on, EX_OUTx_on in register 01H) or any of the overridden outputs polarities.

OUTx_on works for paralleled outputs as well. To actuate a group of outputs using OUTx_on first assign the appropriate outputs to be in parallel, then drive the master OUTPUT for that group (OUT1 or OUT4) using the OUTx_on bit. OUTx_on will not work when an output is grouped and an output, other than a master output, is commanded on. For instance:

If OUT1 and OUT2 are grouped (GRP1_2 bit is set in register 03H) OUT1_on can be used to command these two outputs on. OUT2_on will be ignored if used.

In normal mode, all overridden outputs (internal and external) will experience a ~6us pause at each write access to register 01h that does not set the OUT_ON control bit. In emergency mode, all overridden outputs (internal and external) will experience a ~10 µs pause at each write access to register 01h regardless of the OUT_ON control bit value. Once back in normal mode from the emergency one, the behavior will remain the one described in emergency mode, unless the overridden outputs are disabled and then enabled again.

EMCYx

Emergency mode overrides any current actuation command in progress and drives outputs according to the programmed values in the registers. If OUT_ON is low on the rising edge of CSN then all timed actuation activity (if a timed actuation is in progress) will stop and wait for an actuation.

While in Emergency mode the status bits (STAT[1:0]) will be automatically cleared whenever there is a write to CR01H.

This command also overrides all protections such as thermal shutdown and overcurrent latch off. In Emergency mode the device will not latch off if an overcurrent threshold is exceeded. Instead of latching off the driver and reporting a fault the output will continue to retry as in Normal mode. All faults will be reported while not acted upon.

Emergency mode is initiated when a (1, 0) is entered in the EMCY bits. All other EMCY bit configurations result in Normal mode. Emergency mode is exited by initiating another actuation where the EMCY bits are different from (1,0) or because of $V3V3_{RST}$ event.

Table 31. 01H emergency command description

EMGCY bits		
Bit 1	**Bit 0**	**Mode**
0	0	Normal mode
0	1	Normal mode
1	0	Emergency mode
1	1	Normal mode

At the initiation of an emergency mode timed actuation a ~10 µs pause will be experienced on all overridden outputs (internal and external). In case of indefinite braking, at the initiation of an emergency mode timed actuation a ~10 µs pause will be experienced on all outputs (internal overridden, external overridden and time actuated)

EXTx_LSD, EXTx_HSD

These bits determine the polarity of an output, i.e. they specify which is the driver switched on, High Side or Low Side. External drivers cannot be PWMmed.

Table 32. External output polarity bits

Output polarity		
EXTx_LSD	**EXTx_HSD**	**Polarity**
0	0	Tri-state
0	1	High Side on
1	0	Low Side on
1	1	Tri-state

6.2 Output configuration registers

The Configuration Registers are registers written to the L99UDL01 by the MASTER μC to configure the actuation of the L99UDL01 outputs. Each command consists of an address, data bits, and a parity bit. The information written in these register sets up timing and regulation parameters during lock / unlock actuation.

6.2.1 Register 02H (Driver configuration register 1).

This register sets up the on-time and off-time durations of the lock / unlock actuations as well as enables/disables the braking function. The information of this register remain even after actuation.

This register can be read or written. New data is not acted upon if programmed while in timed actuation. New data will be used in subsequent timed actuations.

Figure 18. 02H Driver configuration register 1

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 0	0 1	0	0	0	0	1	0	DBN_EX2	DBN_EX1	DBN_6	DBN_5	DBN_4	DBN_3	DBN_2	DBN_1	ON_TIME_4	ON_TIME_3	ON_TIME_2	ON_TIME_1	ON_TIME_0	OFF_TIME_1	OFF_TIME_0	Parity
Default Values								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X

Table 33. 02H Configuration bit description

Bit#	Command	Description
15	DBN_EX2	Dynamic Braking disable for external bridge driver 2
14	DBN_EX1	Dynamic Braking disable for external bridge driver 1
13	DBN_6	Dynamic Braking disable for Internal bridge 6
12	DBN_5	Dynamic Braking disable for Internal bridge 5
11	DBN_4	Dynamic Braking disable for Internal bridge 4
10	DBN_3	Dynamic Braking disable for Internal bridge 3
9	DBN_2	Dynamic Braking disable for Internal bridge 2

Table 33. 02H Configuration bit description (continued)

Bit#	Command	Description
8	DBN_1	Dynamic Braking disable for Internal bridge 1
7	tON_4	Latch on-time duration bit 4
6	tON_3	Latch on-time duration bit 3
5	tON_2	Latch on-time duration bit 2
4	tON_1	Latch on-time duration bit 1
3	tON_0	Latch on-time duration bit 0
2	tOFF _1	Dynamic braking duration bit 1
1	tOFF _0	Dynamic braking duration bit 0
0	Parity	

tOFF_x

These bits set up the dynamic braking mode duration. Dynamic braking occurs immediately after the on-time actuation is complete. Dynamic braking is active on all outputs except where overridden (Output Override) or disabled (Dynamic Braking Disable). During dynamic braking, low side drivers (internal and external) are turned on for the duration commanded by the tOFF_x bits. When the indefinite dynamic braking mode, [1:1], is selected a new actuation cannot start until after an initial 100ms of dynamic braking time.

Table 34. Brake duration bits

tOFF _1	tOFF _0	Duration (ms)
0	0	0
0	1	100
1	0	200
1	1	100 + Indefinite

Indefinite braking can be stopped by appropriately programming register CR02H (tOFF bits [1,2]) and initiating an actuation (i.e. setting OUT_ON=1). One example would be programing tOFF=tON=0, disabling all timed and unused outputs in CR00H and CR01H and initiating an actuation. Entering in Emergency mode with OUT_ON=0 stops the indefinite braking

tON_x

Three bits set up the on-time duration during lock / unlock actuation. These bit are global since they act upon all appropriate outputs together.

Table 35. Run time duration bits

Run time						Step
tON_4	tON_3	tON_2	tON_1	tON_0	Duration (ms)	Size (ms)
0	0	0	0	0	100	20
0	0	0	0	1	120	20
0	0	0	1	0	140	20
0	0	0	1	1	160	20
0	0	1	0	0	180	20
0	0	1	0	1	200	20
0	0	1	1	0	220	20
0	0	1	1	1	240	20
0	1	0	0	0	260	20
0	1	0	0	1	280	20
0	1	0	1	0	300	20
0	1	0	1	1	320	20
0	1	1	0	0	340	20
0	1	1	0	1	360	20
0	1	1	1	0	380	20
0	1	1	1	1	400	20
1	0	0	0	0	440	40
1	0	0	0	1	480	40
1	0	0	1	0	520	40
1	0	0	1	1	560	40
1	0	1	0	0	600	40
1	0	1	0	1	640	40
1	0	1	1	0	680	40
1	0	1	1	1	720	40
1	1	0	0	0	760	40
1	1	0	0	1	800	40
1	1	0	1	0	840	40
1	1	0	1	1	880	40
1	1	1	0	0	920	40
1	1	1	0	1	960	40
1	1	1	1	0	1000	40
1	1	1	1	1	1040	40

DBN_x

The DBN_X bits disable the braking mode on specific outputs. When this bit is set the dynamic braking function does not work for that output. This allows the selected output to be used for other functions besides door lock.

6.2.2 Register 03H (Driver configuration register 2)

This register sets up the groups for paralleling outputs as well as a few other functions. This information remains in the register even after actuation.

This register can be read or written. While new data can be written to the register it will not become effective while in timed actuation or while in indefinite braking mode. The new data will become effective:

- If the data is changed during a timed actuation, then the new data value will become effective at the end of the timed actuation (ton + toff).
- If the data is changed during indefinite braking or during a timed actuation with programmed indefinite braking, then the new data value will be taken into account only after a write operation on to register 01H occurs or unless a new timed actuation is triggered by EN_OUT rising edge.
- If the data is changed outside of a timed actuation and outside of indefinite braking, then the new data value will become effective upon at the rising edge of CSN.

Figure 19. 03H Driver config register 2

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 0	0 1	0	0	0	0	1	1	Reserved								GFI	TSD_ACT	DITH	GRP2_6	GRP2_5	GRP1_3	GRP1_2	Parity
Default Values								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X

Table 36. 03H register bit description

Bit#	Command	Description
15	Reserved	—
14	Reserved	—
13	Reserved	—
12	Reserved	—
11	Reserved	—
10	Reserved	—
9	Reserved	—
8	Reserved	—
7	GFI	Global Fault indication on DOUT
6	TSD_ACT	Thermal Shutdown action (0=Output only, 1=Gloal)
5	DITHN	Disables Dither frequency to Charge Pump osc.

Table 36. 03H register bit description (continued)

Bit#	Command	Description
4	GRP2_6	Group 2 assignment bit for Output 6
3	GRP2_5	Group 2 assignment bit for Output 5
2	GRP1_3	Group 1 assignment bit for Output 3
1	GRP1_2	Group 1 assignment bit for Output 2
0	Parity	

GRPx_y

These bits assign outputs to one of two groups for the purpose of paralleling. When grouped, the outputs behave as one.

There are two groups that can associate outputs together. Group 1 can only associate outputs 1 through 3. Group 2 can only associate outputs 4 through 6. Group 1 must have Output 1 in the group. Also, group 2 must have Output 4 in the group.

Table 37. Grouping configuration bits

Group configuration				
GRP2_6	GRP2_5	GRP1_3	GRP1_2	Group assignments
0	0	0	0	No group
x	x	0	1	Group 1, 2
x	x	1	0	Group 1, 3
x	x	1	1	Group 1, 2, 3
0	1	x	x	Group 4, 5
1	0	x	x	Group 4, 6
1	1	x	x	Group 4, 5, 6

Configuring these bits alters how the current regulation/PWM bits are used. In PWM control (C_PWM_SWx = 1), only the master is used to configure outputs associated together. Master outputs are output 1 for outputs 1 through 3 and output 4 for outputs 4 through 6. All C_PWM_SWx bits in the associated group must be at the same setting.

When in current regulation control, all outputs in the group are configured. All currents are added to give a total regulated current value. See Section 2.4.9 as well as Control registers 04H and 05H for more detail.

Any unassociated outputs are driven or configured normally.

DITHN

This bit disables the dither frequency to the charge pump oscillator. Disabling the dither function will stop the charge pump oscillator from constantly shifting in frequency within a specified range of frequencies.

TSD_ACT

This bit determines the reaction to a thermal shutdown event on an output. If reset the thermal shutdown action is limited to the individual output OUTx (x=1...6). If set, all of the internal outputs OUTx (x=1...6), the external outputs EX_OUTx (x=1, 2) and the charge pump are disabled in a thermal shutdown event. No data is lost during a thermal shutdown event.

GFI

This bit enables the DOUT pin to be a reflection of the GSBN bit in the Global Status Byte. When enabled, the DOUT pin will go low if there is any fault indication in the Global Status Byte or will remain high under no fault condition. When this bit is not set the DOUT pin is tri-stated.

6.2.3 Register 04H and 05H (Driver configuration registers 1 through 3, and 4 through 6)

These registers set up the current / PWM regulation for Output/Group 1, Output 2 and Output 3 in register 04H and Output 4/Group 2, Output 5 and Output 6 in register 05H

These registers can be read or written to. New data is not acted upon if programmed while in timed actuation. New data will be used in subsequent timed actuations.

Register 04H (Outputs 1-3)

Figure 20. 04H driver configuration register 3

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 0	0 1	0	0	0	1	0	0	C/PWM_SW_3	OCP3_3	OCP3_2	OCP3_1	OCP3_0	C/PWM_SW_2	OCP2_3	OCP2_2	OCP2_1	OCP2_0	C/PWM_SW_1	OCP1_3	OCP1_2	OCP1_1	OCP1_0	Parity
Default Values								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X

Table 38. 04H register bit description

Bit#	Command	Description
15	C/PWM_SW_3	Out 3 Current / PWM enable bit
14	OCP3_3	Out 3 Curr/PWM CNTL bit 3
13	OCP3_2	Out 3 Curr/PWM CNTL bit 2
12	OCP3_1	Out 3 Curr/PWM CNTL bit 1
11	OCP3_0	Out 3 Curr/PWM CNTL bit 0
10	C/PWM_SW_2	Out 2 Current / PWM enable bit
9	OCP2_3	Out 2 Curr/PWM CNTL bit 3
8	OCP2_2	Out 2 Curr/PWM CNTL bit 2
7	OCP2_1	Out 2 Curr/PWM CNTL bit 1

Table 38. 04H register bit description (continued)

Bit#	Command	Description
6	OCP2_0	Out 2 Curr/PWM CNTL bit 0
5	C/PWM_SW_1	Out 1/GRP 1 Current / PWM enable bit
4	OCP1_3	Out 1 Curr/PWM CNTL bit 3
3	OCP1_2	Out 1 Curr/PWM CNTL bit 2
2	OCP1_1	Out 1 Curr/PWM CNTL bit 1
1	OCP1_0	Out 1 Curr/PWM CNTL bit 0
0	Parity	Parity bit

Register 05H (Outputs 4-6)

Figure 21. 05H driver configuration register 4

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 0	0 1	0	0	0	1	0	1	C/PWM_SW_6	OCP6_3	OCP6_2	OCP6_1	OCP6_0	C/PWM_SW_5	OCP5_3	OCP5_2	OCP5_1	OCP5_0	C/PWM_SW_4	OCP4_3	OCP4_2	OCP4_1	OCP4_0	Parity
Default Values								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X

Table 39. 05H register bit description

Bit No.	Function	Level
15	C/PWM_SW_6	Out 6 Current / PWM enable bit
14	OCP6_3	Out 6 Curr/PWM CNTL bit 3
13	OCP6_2	Out 6 Curr/PWM CNTL bit 2
12	OCP6_1	Out 6 Curr/PWM CNTL bit 1
11	OCP6_0	Out 6 Curr/PWM CNTL bit 0
10	C/PWM_SW_5	Out 5 Current / PWM enable bit
9	OCP5_3	Out 5 Curr/PWM CNTL bit 3
8	OCP5_2	Out 5 Curr/PWM CNTL bit 2
7	OCP5_1	Out 5 Curr/PWM CNTL bit 1
6	OCP5_0	Out 5 Curr/PWM CNTL bit 0
5	C/PWM_SW_4	Out 4/GRP 2 Current / PWM enable bit
4	OCP4_3	Out 4 Curr/PWM CNTL bit 3
3	OCP4_2	Out 4 Curr/PWM CNTL bit 2
2	OCP4_1	Out 4 Curr/PWM CNTL bit 1

Table 39. 05H register bit description (continued)

Bit No.	Function	Level
1	OCP4_0	Out 4 Curr/PWM CNTL bit 0
0 LSB	Parity	

When the C/PWM_SW_x bit is set the OCPx_y bits set up the PWM level for Output1-3 or Group 1 according to the following table.

Table 40. Current / duty cycle bit description

Current / PWM bit selection				Bit	%Duty
OCPx_3	OCPx_2	OCPx_1	OCPx_0	Value	Cycle
0	0	0	0	0	6.25
0	0	0	1	1	12.5
0	0	1	0	2	18.75
0	0	1	1	3	25
0	1	0	0	4	31.25
0	1	0	1	5	37.5
0	1	1	0	6	43.75
0	1	1	1	7	50
1	0	0	0	8	56.25
1	0	0	1	9	62.5
1	0	1	0	10	68.75
1	0	1	1	11	75
1	1	0	0	12	81.25
1	1	0	1	13	87.5
1	1	1	0	14	93.75
1	1	1	1	15	100

When the C/PWM_SW_x bit is set to “0” then the OCPx_y bits determine the current regulation levels according to the following table (for bit values see *Figure 21: 05H driver configuration register 4*):

Table 41. Current bit description

	One output		Two outputs		Three outputs	
	Sum of 1 only	Current	Sum of 1+2	Current	Sum of 1+2+3	Current
One output	0	1 A	0	2 A	0	3 A
	1	1.2 A	1	2.2 A	1	3.2 A
	2	1.4 A	2	2.4 A	2	3.4 A
	3	1.6 A	3	2.6 A	3	3.6 A
	4	1.8 A	4	2.8 A	4	3.8 A
	5	2 A	5	3 A	5	4 A
	6	2.2 A	6	3.2 A	6	4.2 A
	7	2.4 A	7	3.4 A	7	4.4 A
	8	2.6 A	8	3.6 A	8	4.6 A
	9	2.8 A	9	3.8 A	9	4.8 A
	10	3 A	10	4 A	10	5 A
	11	3.2 A	11	4.2 A	11	5.2 A
	12	3.4 A	12	4.4 A	12	5.4 A
	13	3.6 A	13	4.6 A	13	5.6 A
	14	3.8 A	14	4.8 A	14	5.8 A
	15	4 A	15	5 A	15	6 A
Two outputs			16	5.2 A	16	6.2 A
			17	5.4 A	17	6.4 A
			18	5.6 A	18	6.6 A
			19	5.8 A	19	6.8 A
			20	6 A	20	7 A
			21	6.2 A	21	7.2 A
			22	6.4 A	22	7.4 A
			23	6.6 A	23	7.6 A
			24	6.8 A	24	7.8 A
			25	7 A	25	8 A
			26	7.2 A	26	8.2 A
			27	7.4 A	27	8.4 A
			28	7.6 A	28	8.6 A
			29	7.8 A	29	8.8 A
			30	8 A	30	9 A

Table 41. Current bit description (continued)

	One output		Two outputs		Three outputs	
	Sum of 1 only	Current	Sum of 1+2	Current	Sum of 1+2+3	Current
Three outputs					31	9.2 A
					32	9.4 A
					33	9.6 A
					34	9.8 A
					35	10 A
					36	10.2 A
					37	10.4 A
					38	10.6 A
					39	10.8 A
					40	11 A
					41	11.2 A
					42	11.4A
					43	11.6 A
					44	11.8 A
					45	12 A

C/PWM_SW_x

The Current PWM Switch bit determines if the output will regulate the motor current directly or just impose a specific PWM duty cycle (voltage regulation) per the OCPx_y bits above.

Table 42. Current / duty cycle switch bit description

C/PWM_SW_x	Regulation type
0	Current Regulation
1	Voltage Regulation

As the driving component, the driver is either regulating to a current level or is PWMming to a specified duty cycle.

This only applies to the 6 internal half bridges. The external half bridges are not PWMmable.

6.2.4 Register 06H (external bridge VDS monitor and control)

This register sets up the drain source monitoring for the two external half bridges.

This register can be read or written to. All new data programmed into this register will be acted upon the rising edge of CSN even during a timed actuation.

Figure 22. 06H external bridge VDS monitor and control register

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 0	0 1	0	0	0	1	1	0	HBDCL2	HBDCH2	STBY1	EXT2_VDt_1	EXT2_VDt_0	EXT1_VDt_1	EXT1_VDt_0	EXT2_VDS_3	EXT2_VDS_2	EXT2_VDS_1	EXT2_VDS_0	EXT1_VDS_3	EXT1_VDS_2	EXT1_VDS_1	EXT1_VDS_0	Parity
Default Values								0	0	0	0	0	0	0	1	0	1	1	1	0	1	1	X

Table 43. 06H Register bit description

Bit No.	Function	Level
15	HBDCL2	H-Bridge 2 diagnostic current Sink
14	HBDCH2	H-Bridge 2 diagnostic current Source
13	STBY1	Standby Activation bit 1
12	EXT2_VDt_1	External Bridge 2 VDS Blanking time bit 1
11	EXT2_VDt_0	External Bridge 2 VDS Blanking time bit 0
10	EXT1_VDt_1	External Bridge 1 VDS Blanking time bit 1
9	EXT1_VDt_0	External Bridge 1 VDS Blanking time bit 0
8	EXT2_VDS_3	External Bridge 2 Drain-Source threshold bit 3
7	EXT2_VDS_2	External Bridge 2 Drain-Source threshold bit 2
6	EXT2_VDS_1	External Bridge 2 Drain-Source threshold bit 1
5	EXT2_VDS_0	External Bridge 2 Drain-Source threshold bit 0
4	EXT1_VDS_3	External Bridge 1 Drain-Source threshold bit 3
3	EXT1_VDS_2	External Bridge 1 Drain-Source threshold bit 2
2	EXT1_VDS_1	External Bridge 1 Drain-Source threshold bit 1
1	EXT1_VDS_0	External Bridge 1 Drain-Source threshold bit 0
0 LSB	Parity	

EXTx_VDSx

These bits set up the Drain-Source voltage fault threshold for the external bridges. If the Drain-Source voltage exceeds the programmed value (EXTx_VDSx, see *Table 43*) for longer than the VDS filtering time (t_{VDS_FILTER}) the output is disabled and a fault code is set. *Table 43* contains only typical values. Refer to parameter V_{DS_TH} Step tolerance (D.044) for worst case tolerances. The default setting is 1011 (1.0V).

At turn on, there is an additional programmable VDS fault blanking time (EXTx_VDtx). In this case, starting from a turn on command, the delay includes the VDS fault filter time plus the programmed blanking time (i.e. t_{VDS_FILTER} + EXTx_VDtx).

Table 44. VDS threshold bit description

VDS threshold				
Bit 8 / Bit 4	**Bit 7 / Bit 3**	**Bit 6 / Bit 2**	**Bit 5 / Bit 1**	**Threshold (typical)**
0	0	0	0	OFF
1	0	0	0	0.25 V
1	0	0	1	0.5 V
1	0	1	0	0.75 V
1	0	1	1	1.0 V
1	1	0	0	1.25 V
1	1	0	1	1.5 V
1	1	1	0	1.75 V
1	1	1	1	2.0 V

STBY1

Standby is entered when bit 13 in this register and bit 13 in register 07H are set in order. First STBY1 must be set and then STBY2 must be set for standby to be initiated. Upon the rising edge of CSN, when setting the second of the two bits, the device will enter standby. Setting only one of the bits or setting the bits out of order will not cause the device to enter standby.

Once entering Standby no communication can occur without waking the device up (CSN falling edge).

HBDCL2

See register 07H below for description.

EXTx_VDtx

These bits set up the blanking time for VDS fault detection for the external bridges. If at turn on the Drain-Source voltage exceeds the programmed EXTx_VDSx value during the blanking time programmed by these bits, the fault is not triggered. The VDS fault can be triggered after this blanking time if it persists for more than t_{VDS_FILTER} time (1 µs). The VDS timer default setting is 1 µs.

Table 45. VDS timer bit description

VDS timer		
Bit 12 / Bit 10	**Bit 11 / Bit 9**	**Duration**
0	0	1 µs
0	1	2 µs
1	0	3 µs
1	1	4 µs

6.2.5 Register 07H (diagnostic monitoring control)

This register controls the diagnostic current enable and polarity.

This register can be read or written to. All new data programmed into this register will be acted upon the rising edge of CSN even during a timed actuation.

Figure 23. 07H diagnostic monitoring control register

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 0	0 1	0	0	0	1	1	1	HBDCL1	HBDCH1	STBY2	ODCL6	ODCH6	ODCL5	ODCH5	ODCL4	ODCH4	ODCL3	ODCL3	ODC21	ODCH2	ODCL1	ODCH1	Parity
Default Values								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X

Table 46. 07H Register bit description

Bit No.	Function	Level
15	HBDCL1	H-Bridge 1 diagnostic current Sink
14	HBDCH1	H-Bridge 1 diagnostic current Source
13	STBY2	Standby Activation bit 2
12	ODCL6	Output 6 diagnostic current Sink
11	ODCH6	Output 6 diagnostic current Source
10	ODCL5	Output 5 diagnostic current Sink
9	ODCH5	Output 5 diagnostic current Source
8	ODCL4	Output 4 diagnostic current Sink
7	ODCH4	Output 4 diagnostic current Source
6	ODCL3	Output 3 diagnostic current Sink
5	ODCH3	Output 3 diagnostic current Source
4	ODCL2	Output 2 diagnostic current Sink
3	ODCH2	Output 2 diagnostic current Source
2	ODCL1	Output 1 diagnostic current Sink
1	ODCH1	Output 1 diagnostic current Source
0 LSB	Parity	Parity bit

ODCHx / ODCLx – HBDCHx/HBDCLx

These bits set the output diagnostic current. When the corresponding bit is set there is a current imposed (I_{DIAG}) on the integrated drivers (ODCH/Lx) or external drivers (HBDCH/Lx). A sink and a source current cannot be enabled simultaneously.

It is not recommended to use the diagnostic currents when the outputs are being used. That is during timed actuation or during output override.

STBY2

Standby is entered when bit 13 in this register and bit 13 in register 06H are set in order. First STBY1 must be set and then STBY2 must be set for standby to be initiated. Upon the rising edge of CSN, when setting the second of the two bits, the device will enter standby. Setting only one of the bits or setting the bits out of order will not cause the device to enter standby.

Once entering Standby no communication can occur without waking the device up (CSN falling edge)

6.2.6 Register 08H (current regulation loop control).

This register provides the option of adjusting the control loop P-I parameters. These parameters are set to a typical default setting that will fit most applications.

This register can be read or written to. All new data programmed into this register will be acted upon the rising edge of CSN even during a timed actuation.

Figure 24. 08H Current regulation loop control register

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 0	0 1	0	0	1	0	0	0	Reserved									KI_2	KI_1	KI_0	KP_2	KP_1	KP_0	Parity
Default Values								0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	X

Table 47. 08H Register bit description

Bit No.	Function	Level
15	Reserved	—
14	Reserved	—
13	Reserved	—
12	Reserved	—
11	Reserved	—
10	Reserved	—
9	Reserved	—
8	Reserved	—
7	Reserved	—
6	KI_2	Integral gain of regulation loop bit 2
5	KI_1	Integral gain of regulation loop bit 1
4	KI_0	Integral gain of regulation loop bit 0
3	KP_2	Proportional gain of regulation loop bit 2
2	KP_1	Proportional gain of regulation loop bit 1

Table 47. 08H Register bit description (continued)

Bit No.	Function	Level
1	KP_0	Proportional gain of regulation loop bit 0
0 LSB	Parity	Parity bit

KP_X

These bits set the current control loop proportional gain. The shaded area is the default setting (during a POR or a software reset).

Table 48. KP Gain settings

KP_2	KP _1	KP _0	Gain setting
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

KI_X

These bits set the current control loop integral gain. The shaded area is the default setting.

Table 49. KI gain settings

KI_2	KI _1	KI _0	Gain setting
0	0	0	$^1/_{128}$
0	0	1	$^1/_{64}$
0	1	0	$^1/_{32}$
0	1	1	$^1/_{16}$
1	0	0	$^1/_{8}$
1	0	1	¼
1	1	0	½
1	1	1	1

Register 09H (Spare control register-unused)

Figure 25. 09 H spare control register

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 0	0 1	0	0	1	0	0	1	Reserved															Parity
Default Values								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X

Table 50. 09H register bit description

Bit No.	Function	Level
15	Reserved	—
14	Reserved	—
13	Reserved	—
12	Reserved	—
11	Reserved	—
10	Reserved	—
9	Reserved	—
8	Reserved	—
7	Reserved	—
6	Reserved	—
5	Reserved	—
4	Reserved	—
3	Reserved	—
2	Reserved	—
1	Reserved	—
0 LSB	Parity	Parity bit

6.3 SPI diagnostic registers

Fault indications will not be cleared unless asked to do so by op-code. It is recommended, if a read and clear operation is performed, that all bits in the diagnostic register be cleared. Otherwise there could be confusion as to the reported fault.

6.3.1 Global Status byte

This byte consists of 8 bits. This information is returned while the command byte is sent.

Figure 26. Global Status byte

D7	D6	D5	D4	D3	D2	D1	D0
GSBN	RSTB	SPIE	FE2	FE1	DE	GW	N/A
0	1	0	0	0	0	0	0

Table 51. GSB bit description

Global Status byte		
Bit#	**Data Bit**	**Description**
7	GSBN	Global Status Bit NOT (active low)
6	RSTB	RESET bit
5	SPIE	SPI Error
4	FE2	Functional Error bit 2
3	FE1	Functional Error bit 1
2	DE	Device Error
1	GW	Global Warning
0	Blank	Not used

Global Status Bit Not (GSBN)

The GSBN is a logically NOR combination of Bit 0 to Bit 6. This bit can also be used as Global Status Flag without starting a complete communication frame as it is present directly after pulling CSN low.

Reset Bit (RSTB)

The RSTB indicates a device reset. In case this bit is set, all internal Control Registers have been set to their default values and kept in that state until the bit is cleared. This bit is automatically cleared by any valid SPI communication.

SPI Error (SPIE)

The SPIE is a logical OR combination of errors related to a wrong SPI communication. The SPIE bit will not be automatically cleared by a valid SPI communication. This includes:

- SCK count
- SDI stuck @
- Write fail
- Read fail
- Parity error.

Functional Error 2 (FE2)

The FE2 indicates logical OR combination of errors coming from supply monitoring type faults as seen in Diagnostic Register 12H. These include:

- Low voltage on VS
- Over voltage on VS
- Low voltage on VDD
- Low voltage on 3V3
- Charge Pump Low voltage

Functional Error 1 (FE1)

The FE1 is a logical OR combination of errors coming from output type faults. These faults can be found in Diagnostic register 10H. These include:

- Overcurrent fault
- VDS fault

Device Error (DE)

The DE is a logical OR combination of errors related to device related to thermal events such as thermal shutdown for each output as seen in Diagnostic register 02H.

Global Warning (GW)

The GW is a logical OR combination of all warning flags implemented in the design. These include:

- Thermal Warning

6.3.2 Register 10H Integrated H-Bridge diagnostic status register

This register contains the fault diagnostic information for the integrated H-Bridges.

This register can be read or read and cleared. Fault indications will not be cleared unless asked to do so by op-code.

Figure 27. 10H integrated driver Diagnostic status register

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 1	1 0	0	1	0	0	0	0	SPI_Fail	WRT_Fail	RD_Fail	FLT6_1	FLT6_0	FLT5_1	FLT5_0	FLT4_1	FLT4_0	FLT3_1	FLT3_0	FLT2_1	FLT2_0	FLT1_1	FLT1_0	Parity
Default Values								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X

Table 52. 10H register bit description

Bit No.	Function	Level	State after Read & Clear	Default (after POR)
15	SPI_Fail	SCK count, SDI Stuck@ or parity error fails	Cleared	0
14	WRT_Fail	Data write fail	Cleared	0

Table 52. 10H register bit description (continued)

Bit No.	Function	Level	State after Read & Clear	Default (after POR)
13	RD_Fail	Read fail	Cleared	0
12	FLT6_1	Output 6 Fault diagnostic bit 1	Cleared (1)	0
11	FLT6_0	Output 6 Fault diagnostic bit 0	Cleared (1)	0
10	FLT5_1	Output 5 Fault diagnostic bit 1	Cleared (1)	0
9	FLT5_0	Output 5 Fault diagnostic bit 0	Cleared (1)	0
8	FLT4_1	Output 4 Fault diagnostic bit 1	Cleared (1)	0
7	FLT4_0	Output 4 Fault diagnostic bit 0	Cleared (1)	0
6	FLT3_1	Output 3 Fault diagnostic bit 1	Cleared (1)	0
5	FLT3_0	Output 3 Fault diagnostic bit 0	Cleared (1)	0
4	FLT2_1	Output 2 Fault diagnostic bit 1	Cleared (1)	0
3	FLT2_0	Output 2 Fault diagnostic bit 0	Cleared (1)	0
2	FLT1_1	Output 1 Fault diagnostic bit 1	Cleared (1)	0
1	FLT1_0	Output 1 Fault diagnostic bit 0	Cleared (1)	0
0 LSB	Parity	Parity bit		1

1. It is recommended, if a read and clear operation is performed, that all bits for that output (or paralleled outputs) be cleared. Otherwise there could be confusion as to the reported fault.

FLTx_y

Each integrated output has 2 bits assigned to communicate status.

- Each current regulation loop provides information about an output going under current regulation. This information is reported in fault register at the end of the Ton phase (just before the braking phase).
- An overcurrent flag occurs if the internal switch exceeds the maximum current allowed (I_{OC_HS}/I_{OC_LS}). Due to how the active freewheeling circuit is activated, overcurrent fault may only occur on the driving MOSFET. The freewheeling MOSFET will only show an overcurrent if there is a short across the driving element while freewheeling.
- Once an overcurrent fault is detected no CNR fault can be reported until the register is reset with a read & clear command. An overcurrent event will latch off an output until this register is read and cleared. An overcurrent fault has priority over CNR fault regardless of the age of the fault.A CNR flag can be set if the driver is shorted. To determine if a load is missing or the output is shorted an off-state diagnostic should be performed.
- CNR flag will not disable an output
- CNR is not available when DBN_x = 1 (x = 1...6)

Table 53. Output status bit description

Output diagnostic		
FLTx_1	**FLTx_0**	**Diagnostic**
0	0	No Fault
0	1	Overcurrent
1	0	CNR
1	1	Not used

Due to the nature of the active freewheeling, a short across the regulated switch may show up as a CNR. It is recommended that if a CNR is detected that an off-state load diagnostic be performed using the dynamic output voltage detect (DOSx Register 11H) with the weak pull-up/down currents (ODCxy in register 07H).

A PWM controlled output may not detect a shorted driving element. The output current may be read or an off state load diagnostic may be performed to verify the load integrity.

For grouped outputs only the Master status bits (OUT1 or OUT 4) contain the correct fault information for their respective groups. Slave status bits may be ignored.

It is recommended that all of the status bits, single or paralleled, be completely cleared to guarantee proper operation.

RD_Fail

If a read command is given for a register that is non-existent a read fail bit will be set. The SPIE bit in the global status byte will also be set. There will be no effect on the function of the IC as a result of a Read Fail event. The data will be ignored.

SPI_Fail

A SPI Fail bit is set if the clock count is incorrect or the SDI pin is stuck high or low or if a parity error is detected. A clock count error occurs when the clock count between the falling and rising edge of the CSN pin is not 24 (not burst read mode). For a SPI Burst Read the SPI Data Length plus multiple numbers of Payload SCK edges are assumed as a valid communication (e.g. 8+ n x 16 where n = the number of additional payloads read). Anything outside of that count would be considered a SPI Fail.

A SPI failure does not change the behavior of the device. That is, if a SPI fail occurs no registers will change their value as a result of that attempted SPI transmission.

WRT_Fail

A write fail occurs if incorrect data is written to an existing command or configuration register (06H-07H). The data will be transferred to the register and the WRT_Fail flag will be set and latched until the correct data is written followed by a read and clear command. A write fail can also occur if the address used is not one of the command or configuration registers (00H – 09H).

6.3.3 Register 11H (dynamic output state register)

This register can be read (or read and cleared for diagnostic bits). This register reports the dynamic state of an output as seen at the falling edge of CSN as well as the External MOSFET controller fault status.

Figure 28. 11H dynamic output status register

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 1	1 0	0	1	0	0	0	1	VDDUV	STAT1	STAT0	DOS_EXT2	DOS_EXT1	DOS6	DOS5	DOS4	DOS3	DOS2	DOS1	EXTF2_1	EXTF2_0	EXTF1_1	EXTF1_0	Parity
Default Values								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X

Table 54. 11H register bit description

Bit No.	Function	Level	State after SPI Read & Clear	Default (After POR)
15	VDDUV	VDD Under voltage	Cleared	
14	STAT1	Device status bit 1	Cleared(1)	0
13	STAT0	Device status bit 0	Cleared(1)	0
12	DOS_EXT2	Dynamic Output State External Output 2	Read Only	0
11	DOS_EXT1	Dynamic Output State External Output 1	Read Only	0
10	DOS6	Dynamic Output State Output 6	Read Only	0
9	DOS5	Dynamic Output State Output 5	Read Only	0
8	DOS4	Dynamic Output State Output 4	Read Only	0
7	DOS3	Dynamic Output State Output 3	Read Only	0
6	DOS2	Dynamic Output State Output 2	Read Only	0
5	DOS1	Dynamic Output State Output 1	Read Only	0
4	EXTF2_1	External Output 2 Fault diagnostic bit 1	Cleared	0
3	EXTF2_0	External Output 2 Fault diagnostic bit 0	Cleared	0
2	EXTF1_1	External Output 1 Fault diagnostic bit 1	Cleared	0
1	EXTF1_0	External Output 1 Fault diagnostic bit 0	Cleared	0
0 LSB	Parity	Parity bit		1

1. It is recommended, if a read and clear operation is performed, that both the bits 14 and 13 are cleared at the same time.

EXTFx_y

These bits provide fault diagnostic information for the external MOSFET drivers. Fault indication is limited to drain source faults. A VDS (drain-source voltage) fault is indicated if the Drain-Source voltage exceeds the programmed value (EXTx_VDSx) for longer than the VDS filtering time (t_{VDS_FILTER}) the output is disabled and a fault code is set.

At turn on, there is an additional programmable VDS fault blanking time (EXTx_VDtx). In this case, starting from a turn on command, the delay includes the VDS fault filter time plus the programmed blanking time (i.e. t_{VDS_FILTER} + EXTx_VDtx).

Table 55. EXT output status register

Output diagnostic		
EXTFx_1	**EXTFx_0**	**Diagnostic**
0	0	No Fault
0	1	LSD VDS Fault
1	0	HSD VDS Fault
1	1	Not used

DOSx / DOS_EXTx

The Dynamic output state bits provide the state of the output either above or below a threshold (V_{OUT_th}). The outputs are examined at the falling edge of CSN. If the output is above V_{OUT_th} the bit is set. If the output is below V_{OUT_th} the bit is reset. This is a dynamic condition. If the output is being PWMmed then the bit may be set or reset depending on when during the PWM duty cycle the CSN pin went low.

The advantage of this feedback is for off-state diagnosis in conjunction with the weak pull-up/down currents. Between these two features the quality of the load (short to battery, short to ground, open circuit) can be determined before an output is enabled.

STATx

The device status bits tell of the actuation status of the device. There are 4 states. These only apply to outputs being controlled by the state machine and not being overridden (Output Override). Overridden outputs are not considered with respect to the status bits.

- Ready: The device is in inactive state ready for use
- Actuating: The device is in the process of actuation but has not entered Braking mode
- Braking: The device has finished actuating and is now braking.
- Complete: The device has completed actuation and braking modes. Status bits remain at “Complete” until a read and clear command is sent and status is reset to Ready. It should be noted that when the indefinite braking duration is selected (tOFF_x=[1;1]) the “Complete” status will appear 100 ms after dynamic braking has started.

Table 56. Device status bits

Status bits		
STAT1	**STAT0**	**Mode**
0	0	Ready
0	1	Actuating
1	0	Braking
1	1	Complete

The Device status bits must be read and cleared to be able to read subsequent changes in the status. The device status bits will remain at “Complete” [1:1] until cleared. It is recommended that both status bits be cleared to avoid confusion as to the status of the device.

While in Emergency Override mode the status bits will be automatically cleared whenever there is a write to CR01H.

VDDUV

The VDDUV bit will be set when the L99UDL01 VDD falls below the under voltage threshold, VDD_{UV}. It will only be cleared by a read and clear. This bit affects the FE2 bit in the Global Status byte.

6.3.4 Register 12H (General Fault information)

This register reports the thermal faults as well as some supply faults.

Figure 29. 12H General fault information register

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 1	1 0	0	1	0	0	1	0	CPLOW	VSLVI	VSOVSD	TSD6	TSD5	TSD4	TSD3	TSD2	TSD1	TW6	TW6	TW4	TW3	TW2	TW1	Parity
Default Values								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X

Table 57. 12H register bit description

Bit No.	Function	Level	State after SPI Read & Clear	Default (after POR)
15	CPLOW	Charge pump low state	Cleared	0
14	VSLVI	VS low Voltage Inhibit indication	Cleared	0
13	VSOVSD	VS overvoltage indication	Cleared	0
12	TSD6	Over temperature Shutdown Out 6	Cleared	0
11	TSD5	Over temperature Shutdown Out 5	Cleared	0
10	TSD4	Over temperature Shutdown Out 4	Cleared	0
9	TSD3	Over temperature Shutdown Out 3	Cleared	0
8	TSD2	Over temperature Shutdown Out 2	Cleared	0
7	TSD1	Over temperature Shutdown Out 1	Cleared	0
6	TW6	Thermal Warning Out 6	Cleared	0
5	TW5	Thermal Warning Out 5	Cleared	0
4	TW4	Thermal Warning Out 4	Cleared	0
3	TW3	Thermal Warning Out 3	Cleared	0
2	TW2	Thermal Warning Out 2	Cleared	0

Table 57. 12H register bit description (continued)

Bit No.	Function	Level	State after SPI Read & Clear	Default (after POR)
1	TW1	Thermal Warning Out 1	Cleared	0
0 LSB	Parity	Parity bit		1

TWx

These bits indicate which outputs have temperatures over the thermal warning threshold (T_W). They will remain set as long as the junction temperature is above the thermal warning reset threshold (T_{W_RES}). Once the junction temperature is below the thermal warning reset threshold they can only be cleared by a Read & Clear command.

TSDx

These bits indicate which outputs have exceeded the over temperature shutdown threshold. There are two reactions to a thermal shutdown. The individual output can be disabled or the entire IC can be disabled by setting TSD_ACT bit to 1 (Register 03H).

The TSDx bits will remain set as long as the junction temperature is above the thermal shutdown reset threshold (T_{SD_RES}). Once the junction temperature is below the thermal shutdown reset threshold they can only be cleared by a Read & Clear command.

Offending outputs will remain latched off until their respective TSD_X bits are Read & Cleared.

VSOV

VS overvoltage bit is set when the device has exceeded the VSOVSD threshold

VSLVI

VS under voltage inhibit bit is set when the VS voltage has dropped below the VS_{LVI_F} threshold.

CPLOW

CPLOW will remain set indicating that the charge pump was low, below V_{CPLOW} threshold. When CPLOW is set (i.e. the Charge Pump is low), the EXTFx_y bits (in register 11H) and the FLTx_y bits (in register 10H) may be set too.

6.3.5 Register 13H-(regulated current feedback out 1-6)

Figure 30. 13H through 18H Regulated current feedback registers

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 1	1 0	0	1	0 0 0 0 0 1	0 1 1 1 1 0	1 0 1 1 1 0	1 0 1 0 1 0	V3V3UV(1)	RES				CFx_9	CFx_8	CFx_7	CFx_6	CFx_5	CFx_4	CFx_3	CFx_2	CFx_1	CFx_0	Parity
Default Values								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X

Table 58. 13H through 18H register bit description

Bit No.	Function	Level	State after SPI Read&Clear	Default (After POR)
15	V3V3UV(1)	3V3 under voltage	Cleared	0
14	Reserved			0
13				0
12				0
11				0
10	CFx_9	Current control Feedback loop bit 9	Read only	0
9	CFx_8	Current control Feedback loop bit 8	Read only	0
8	CFx_7	Current control Feedback loop bit 7	Read only	0
7	CFx_6	Current control Feedback loop bit 6	Read only	0
6	CFx_5	Current control Feedback loop bit 5	Read only	0
5	CFx_4	Current control Feedback loop bit 4	Read only	0
4	CFx_3	Current control Feedback loop bit 3	Read only	0
3	CFx_2	Current control Feedback loop bit 2	Read only	0
2	CFx_1	Current control Feedback loop bit 1	Read only	0
1	CFx_0	Current control Feedback loop bit 0	Read only	0
0 LSB	Parity	Parity bit		1

1. Found in register 13H only.

CFx_x

These bits in these 6 registers provide a 10 bit binary digital reflection of the current regulation loop internal value. This value is periodically sampled and filtered to show what the current regulation loop is measuring. Taking bits 1 – 10 and multiplying by KFB (6.25 mA/bit see Table 9) provides the value of the current being measured.

Regx[1-10] x KFB = Imeasure

For register 13H please remove bit 15 prior to calculating the current. For all registers the parity bit must also be stripped off prior to calculation (shift the data right by one bit).

V3V3UV

The V3V3UV bit is only in register 13H. This bit is set when the V3V3 voltage regulator voltage falls below the $V3V3_{UV\_F}$ threshold. It is only reset by a read and clear command. This fault is also reported in the FE2 bit in the Global Status byte.

6.3.6 Register 19H-1CH silicon test traceability data

This data indicated when the device was manufactured and tested.

Figure 31. 19H through 1CH silicon traceability data

OC1	OC2	A5	A4	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	1	0	1	1	0	0	1	Reserved							X DIE Coordinate								Parity
				1	0	1	0	Reserved							Y DIE Coordinate								Parity
				1	0	1	1	Reserved										Wafer number					Parity
				1	1	0	0	Reserved															Parity

7 Package and packing information

7.1 ECOPACK

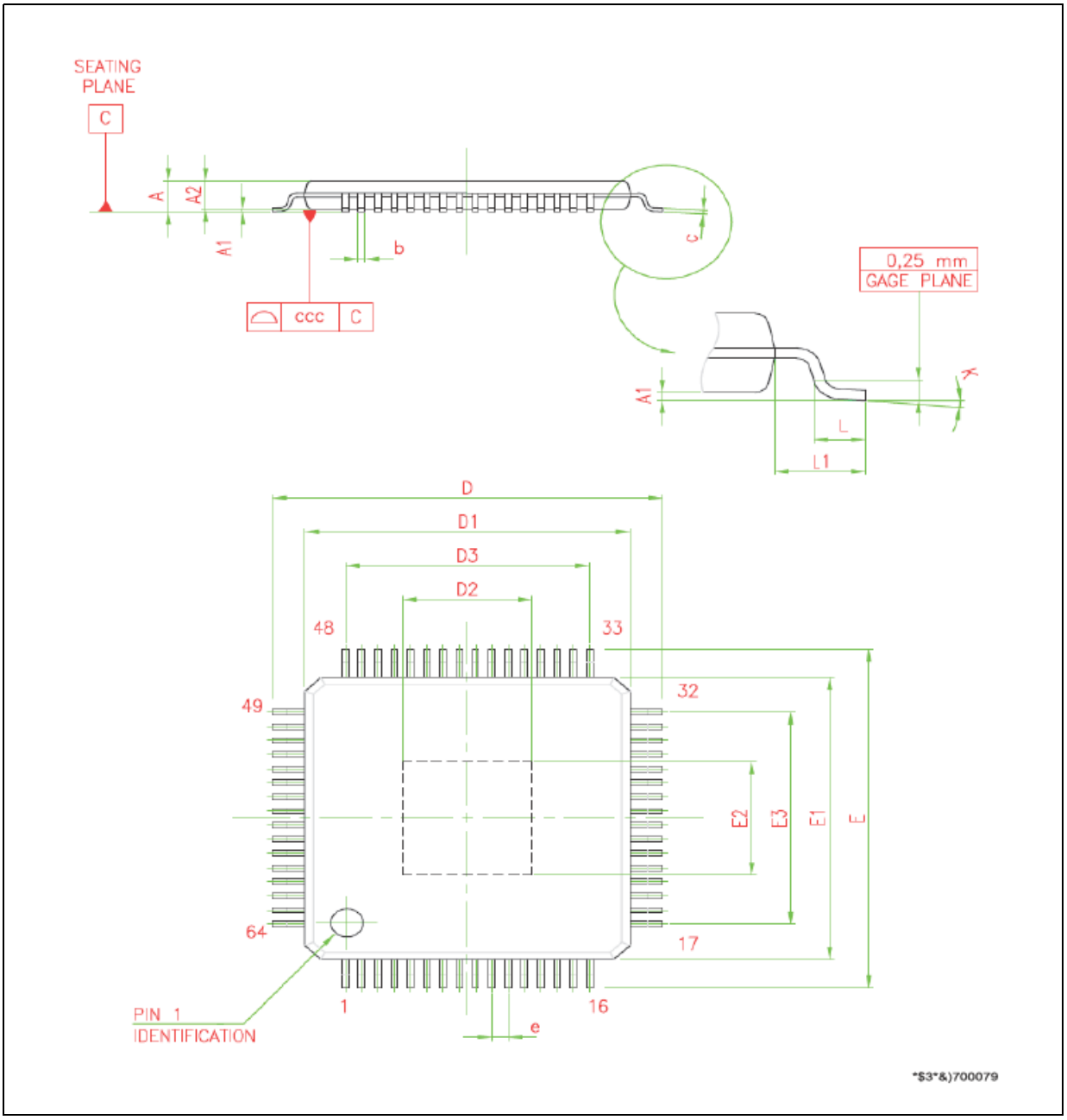
In order to meet environmental requirements, ST offers these devices in different grades of *ECOPACK* packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.2 TQFP-64 mechanical data

Table 59. TQFP-64 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1,20
A1	0,05		0,15
A2	0,95	1,00	1,05
b	0,17	0,22	0,27
c	0,09		0,20
D	11,80	12,00	12,20
D1	9,80	10,00	10,20
D2(1)	5,85	6,00	6,15
D3		7,50	
E	11,80	12,00	12,20
E1	9,80	10,00	10,20
E2(1)	5,85	6,00	6,15
E3		7,50	
e		0,50	
L	0,45	0,60	0,75
L1		1,00	
k	0°	3,50°	7°
ccc			0,08

Figure 32. TQFP-64 package dimensions



8 Revision history

Table 60. Document revision history

Date	Revision	Changes
05-Nov-2018	1	Initial release.
18-Dec-2018	2	Minor text changes. Updated: – Pins 30, 31 and 57 in *Table 2: Pin description*; – Pin 30 in *Figure 2: Pin connection diagram on page 13*; – *Section 2.1: Overview* – *Section 2.4: Output functionality*; – *Section 2.5.3: Normal mode*; – *Figure 10: Typical application diagram example*; – *Section 5.8: Address*; – Updated Figures from *Figure 16* to *Figure 25* and from *Figure 27* to *Figure 30*.
15-May-2019	3	Updated: – *Section 2.2.4: 3V3 monitoring*; – *Section 2.6.3: Off state load detection*; – *Table 3: Absolute maximum ratings on page 28*; – *Table 5: Electrical parameters numbering*; – *Table 6: Supply voltage parameters* ; – *Table 9: Integrated half-bridge DC parameters*; – *Table 10: Integrated half-bridge current control parameters*; – *Table 11: External half-bridge parameters*; – *Table 12: Charge pump parameters*; – *Table 13: Protections*; – *FLTx_y on page 77*.
10-Oct-2019	4	Updated: – *Table 6: Supply voltage parameters* – *Table 12: Charge pump parameters* – *Table 13: Protections*
12-Oct-2020	5	Updated *Table 11: External half-bridge parameters* (D.023 and D.027 Req ID)

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