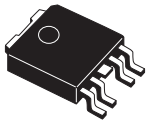
LD39080

Ultra low drop BiCMOS voltage regulator

Datasheet - production data



PPAK

Features

- 0.8 A guaranteed output current
- Ultra low-dropout voltage (150 mV typ. @ 0.8 A load, 20 mV typ. @150 mA load)
- Very low quiescent current (1 mA typ. @ 0.8 A load, 1 µA max.@ 25 °C in off mode)
- Logic-controlled electronic shutdown
- Current and thermal internal limit
- ±1.5% output voltage tolerance @ 25 °C
- ADJ output voltage: 1.22 V to 5.0 V
- Temperature range: - 40 to 125 °C
- Fast dynamic response to line and load changes
- Stable with ceramic capacitor
- Available in PPAK

Applications

- Microprocessor power supply
- DSP power supply
- Post regulators for switching suppliers
- High efficiency linear regulator

Description

The LD39080 is a fast, ultra low drop linear regulator which operates from 2.5 V to 6 V input supply.

A wide range of output options is available. The low drop voltage, low noise, and ultra low quiescent current make it suitable for low voltage microprocessors and memory applications. The device is developed on the BiCMOS process which allows the low quiescent current operation regardless of the output load current.

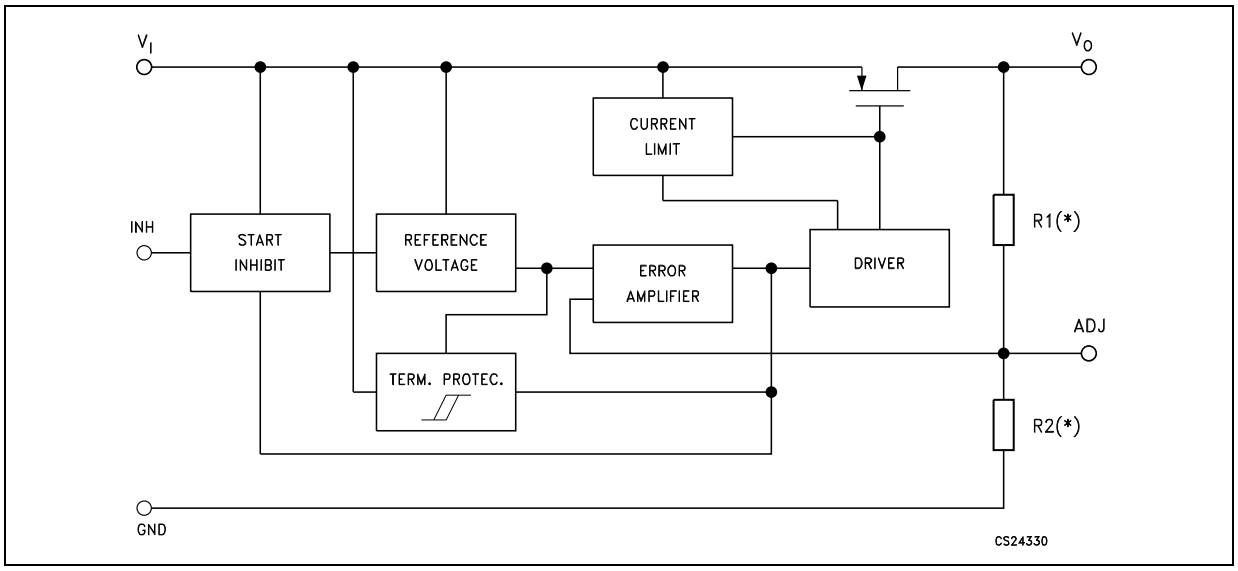
Table 1. Device summary

PPAK (tape and reel)	Output voltage
LD39080PT-R	ADJ from 1.22 to 5.0 V

Contents

1 Diagram

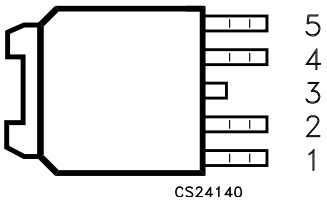
Figure 1. Block diagram



(*) Not present on ADJ version.

2 Pin configuration

Figure 2. Pin connections (top view)



PPAK

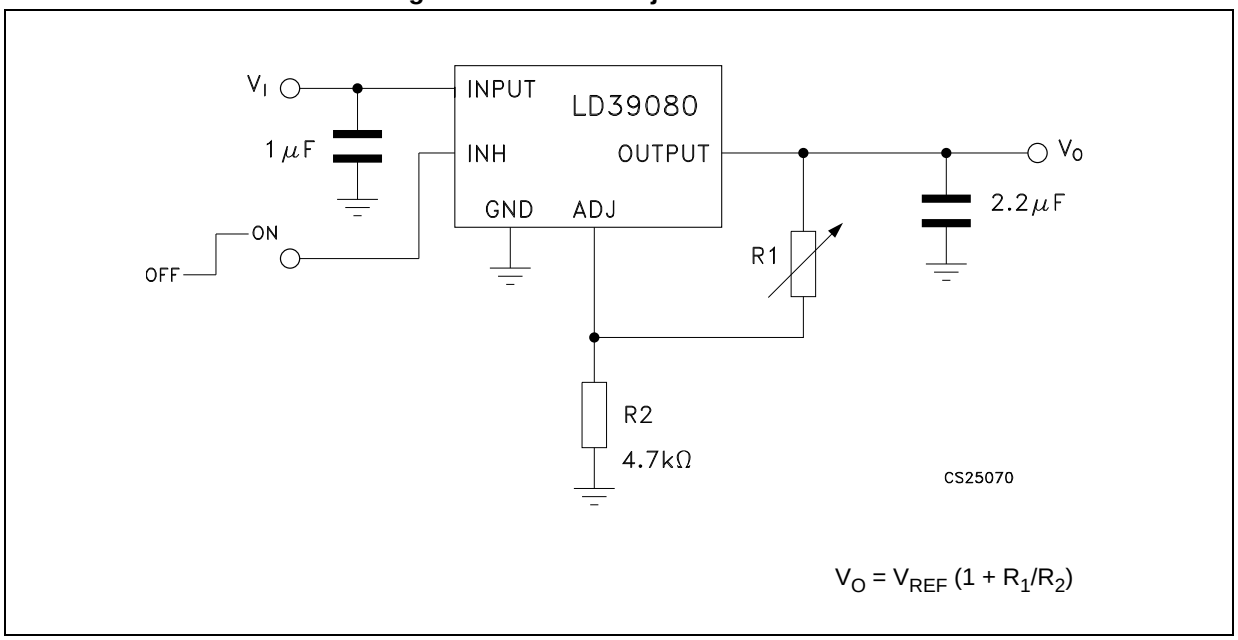
Table 2. Pin description

Pin	Symbol	Note
5	ADJ	Error amplifier input pin for V_O from 1.22 to 5.0 V
2	V_I	LDO input voltage: V_I from 2.5 V to 6 V, C_I=1 µF not farther than 1 cm from input pin
4	V_O	LDO output voltage pins, with minimum C_O = 2.2 µF needed for stability (refer to C_O vs ESR stability chart)
1	V_{INH}	Inhibit input voltage: on mode when $V_{INH} \geq 2$ V, off mode when $V_{INH} \leq 0.3$ V (do not leave it floating, not internally pulled down/up)
3	GND	Common ground

3 Typical application circuits

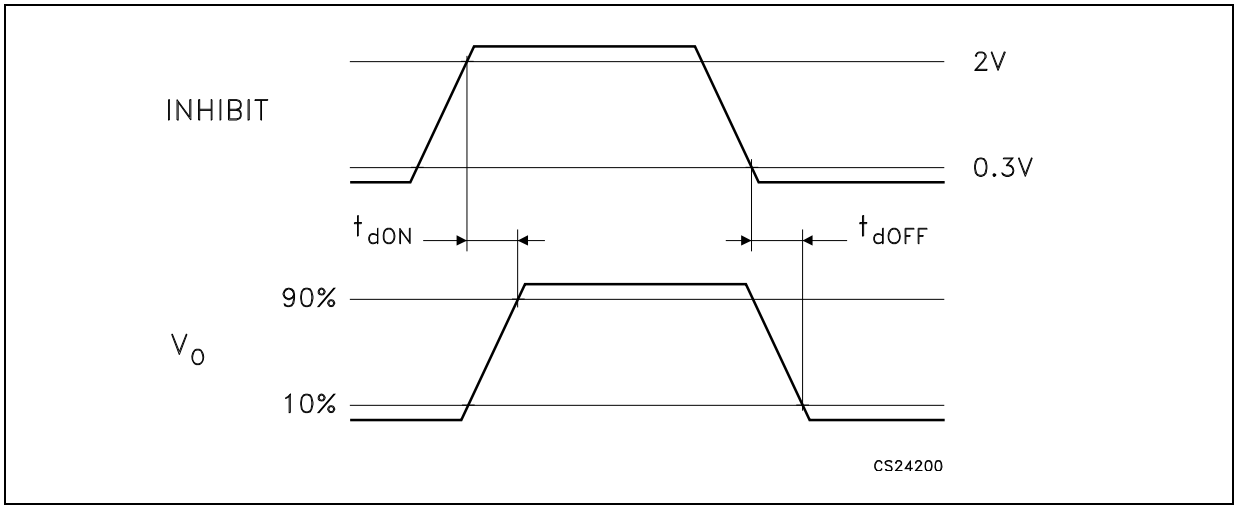
(C_I and C_O capacitors have to be placed as closer as possible to the IC pin).

Figure 3. LD39080 adjustable version



Note: Set R2 as closer as possible to 4.7 KΩ.

Figure 4. Timing diagram



4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC input voltage	-0.3 to 6.5	V
V_{INH}	Inhibit input voltage	-0.3 to V_I +0.3 (6.5 V max.)	V
V_O	DC output voltage	-0.3 to V_I +0.3 (6.5 V max.)	V
V_{ADJ}	ADJ pin voltage	-0.3 to V_I +0.3 (6.5 V max.)	V
I_O	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	-50 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	100	°C/W
R_{thJC}	Thermal resistance junction-case	8	°C/W

5 Electrical characteristics

T_J = 25 °C, V_I = V_O+1 V, C_I = 1 µF, C_O = 2.2 µF, I_{LOAD} = 10 mA, V_{INH} = 2 V, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_I	Operating input voltage			2.5		6	V
V_O	Output voltage tolerance	V_I = V_O+1 V, I_{LOAD} = 10 mA to 0.8 A		-1.5		1.5	% of $V_{O(NOM)}$
		V_I = V_O+1 V to 6 V, I_{LOAD} = 10 mA to 0.8 A T_J = -40 to 125 °C		-3		3	
V_{REF}	Reference voltage				1.22		V
ΔV_O	Output voltage line regulation	V_I = V_O+1 V to 6 V			0.04		%
		V_I = V_O+1 V to 6 V, T_J = -40 to 125 °C			0.1	0.2	%
$\Delta V_O/\Delta I_{LOAD}$	Output voltage load regulation	I_{LOAD} = 10 mA to 0.8 A			0.06		%/A
		I_{LOAD} = 10 mA to 0.8 A, T_J = -40 to 125 °C			0.2	0.4	
V_{DROP}	Dropout voltage (V_I - V_O)	I_{LOAD} = 150 mA, T_J=-40 to 125 °C			20	40	mV
		I_{LOAD} = 0.8 A, T_J = -40 to 125 °C			150	300	
I_Q	Quiescent current: on mode	I_{LOAD} = 10 mA to 0.8 A, V_{INH} = 2 V T_J = -40 to 125 °C			1	2.5	mA
	Quiescent current: off mode	V_{INH} = 0.3 V				1	µA
		V_{INH} = 0.3 V, T_J = -40 to 125 °C				5	
Short-circuit protection							
I_{SC}	Short-circuit protection	R_L = 0			1.6		A
Inhibit Input							
V_{INH}	Inhibit threshold low	V_I = 2.5 to 6 V off T_J = -40 to 125 °C				0.3	V
	Inhibit threshold high			2			
T_{D-OFF}	Current limit	I_{LOAD} = 0.8 A, V_O = 3.3 V			15		µs
T_{D-ON}	Current limit	I_{LOAD} = 0.8 A, V_O = 3.3 V			15		
I_{INH}	Inhibit input current (1)	V_I = 6 V, V_{INH} = 0 to 6 V			±0.1	±1	µA
AC parameters							
SVR	Supply voltage rejection	V_I = 4.5 ± 1 V, V_O = 3.3 V, I_{LOAD} = 10 mA,	f = 120 Hz		65		dB
			f = 1 kHz		55		

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
e_N	Output noise voltage	B_W = 10 Hz to 100 kHz, C_O = 2.2 µF, V_O = 2.5 V			100		$µV_{RMS}$
T_{SHDN}	Thermal shutdown off				170		°C
	Hysteresis				10		

1. Guaranteed by design.

6 Typical performance characteristics

T_J = 25 °C, $V_I = V_O$+1 V, C_I = 1 µF, C_O = 2.2 µF, I_{LOAD} = 10 mA, $V_{INH} = V_I$, unless otherwise specified.

Figure 5. Output voltage vs temperature

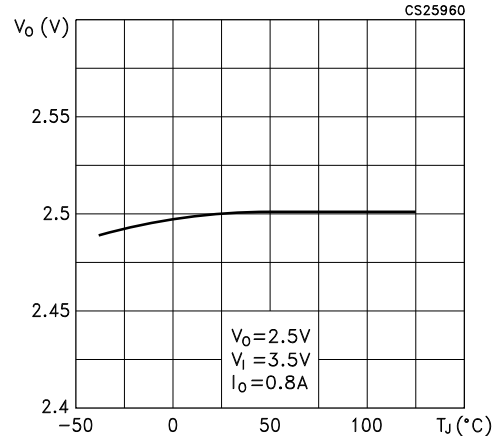


Figure 6. Dropout voltage vs temperature

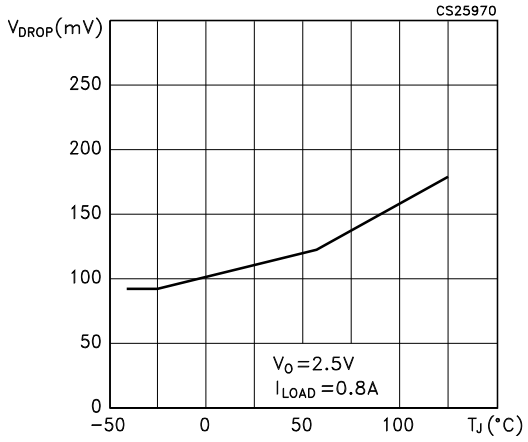


Figure 7. Dropout voltage vs output current

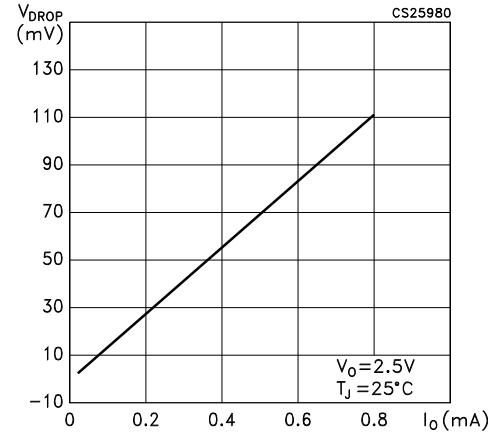


Figure 8. Quiescent current vs output current

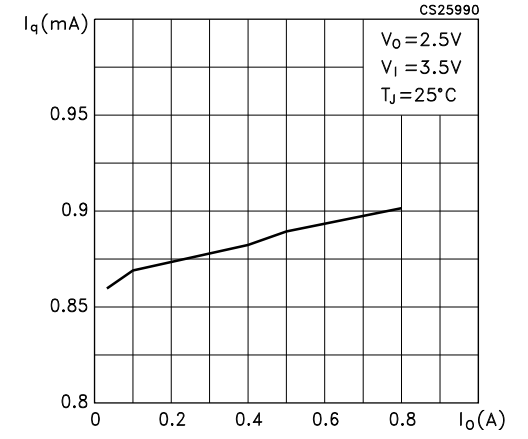


Figure 9. Quiescent current vs supply voltage

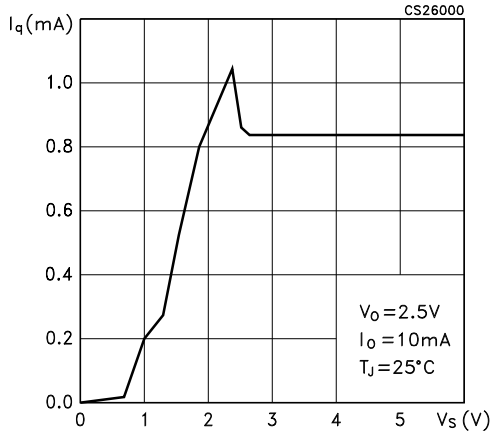


Figure 10. Off-state current vs temperature

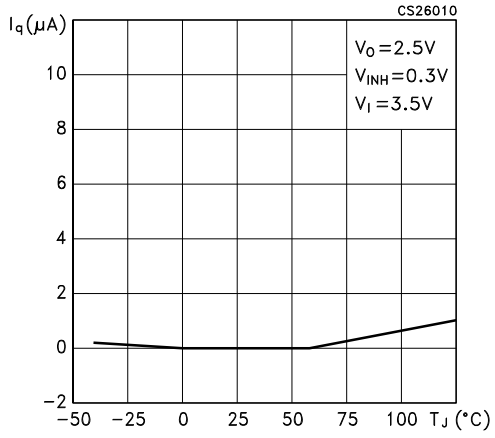


Figure 11. Quiescent current vs temperature

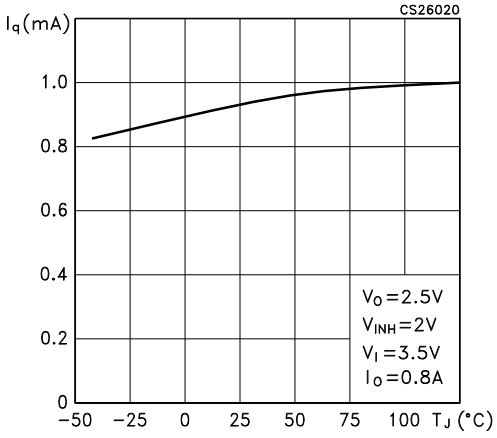


Figure 12. Short-circuit current vs temperature

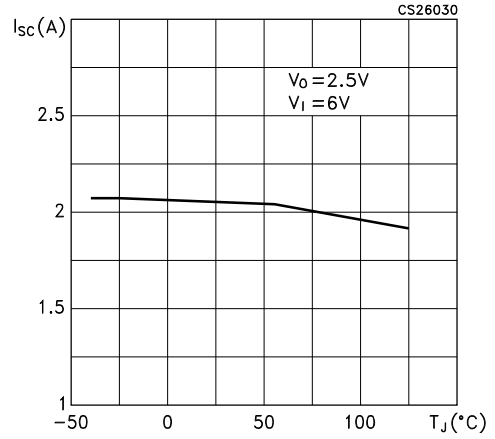


Figure 13. Output voltage vs input voltage

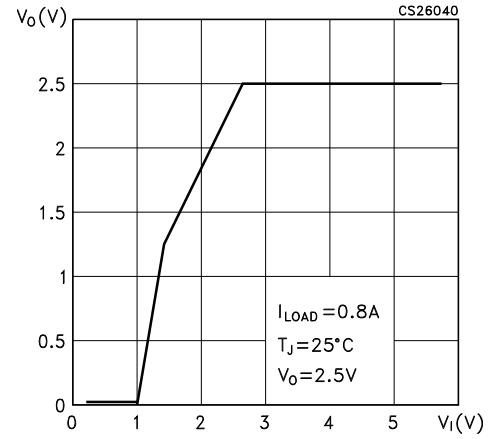


Figure 14. Supply voltage rejection vs temperature

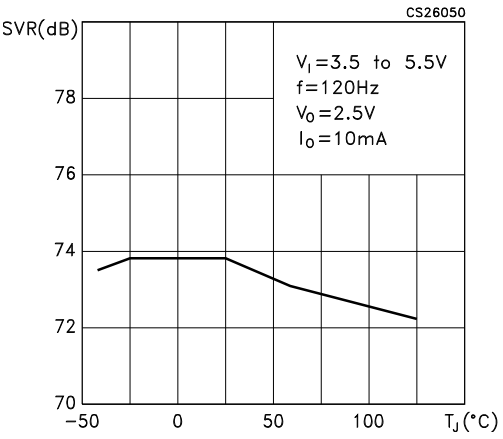


Figure 15. Stability region vs Co and ESR (at 100 kHz)

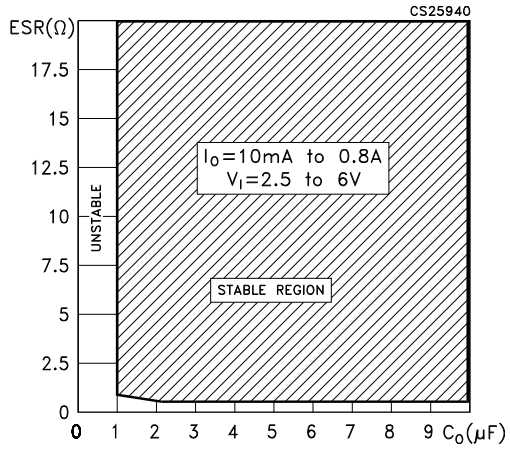


Figure 16. Stability region vs Co and low ESR (at 100 kHz)

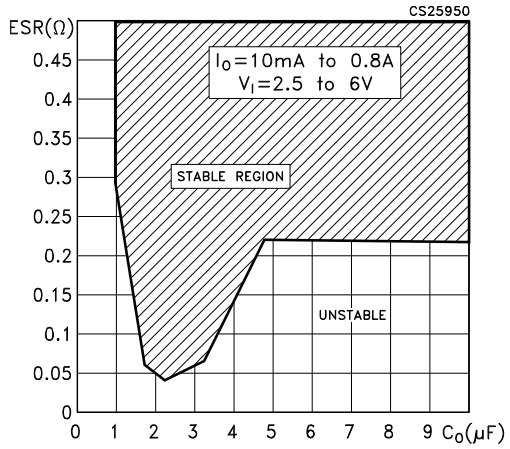


Figure 17. Load transient

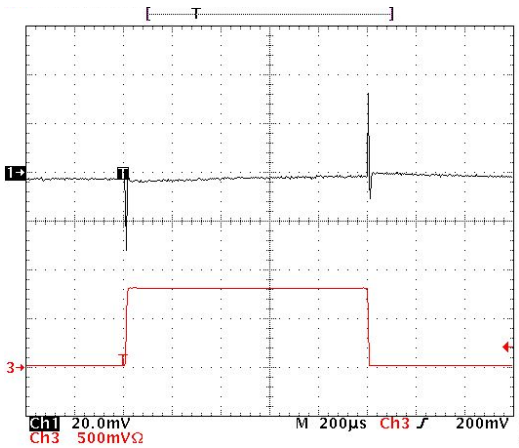
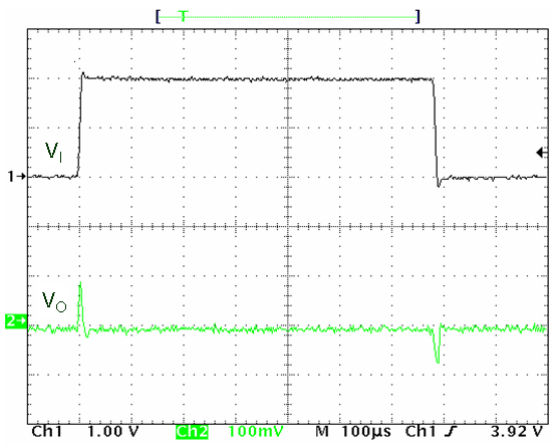


Figure 18. Line transient



7 Application notes

7.1 External capacitor

The LD39080 requires external capacitors to assure the stability. These capacitors have to meet the requirements of minimum capacitance and equivalent series resistance (see *Figure 16 Figure 17*). The input/output capacitors cannot be farther than 1 cm from the relative pins and have to be connected directly to the input/output ground pins using traces without any current flowing through them. Ceramic or electrolytic capacitors can be used.

7.2 Input capacitor

An input capacitor, whose minimum value is 1 µF, is required (the amount of capacitance can be increased without any limit). This capacitor cannot be farther than 1 cm from the input pin of the device and has to return to clean analog ground. Ceramic, tantalum or film capacitors can be used.

7.3 Output capacitor

Ceramic or tantalum capacitors can be used but the output capacitor has to meet the requirements of minimum capacitance and ESR (equivalent series resistance) value. A minimum capacitance of 2.2 µF is a good choice to guarantee the stability of the regulator. Anyway, other C_O values can be used as per *Figure 16 Figure 17*, where the allowable ESR range is seen as a function of the output capacitance. The curve represents the stability region over the full temperature and I_O range.

7.4 Thermal note

The output capacitor has to maintain its ESR in the stable region over the operating temperature range to assure the stability. Besides, capacitor tolerance and temperature variation have to be taken into account to assure the minimum amount of capacitance all time.

7.5 Inhibit input operation

The inhibit pin can be used to turn off the regulator when pulled down, therefore by reducing the current consumption below 1 µA. When the inhibit feature is not used, this pin has to be tied to V_I to turn on the regulator output all the time. To assure the right operation, the signal source, used to drive the inhibit pin, has to swing above and below the specified thresholds listed in *Section 5: Electrical characteristics* (V_{IH} V_{IL}). The inhibit pin must not be left floating because it is not internally pulled down/up.

8 Package mechanical data

Figure 19. PPAK drawings

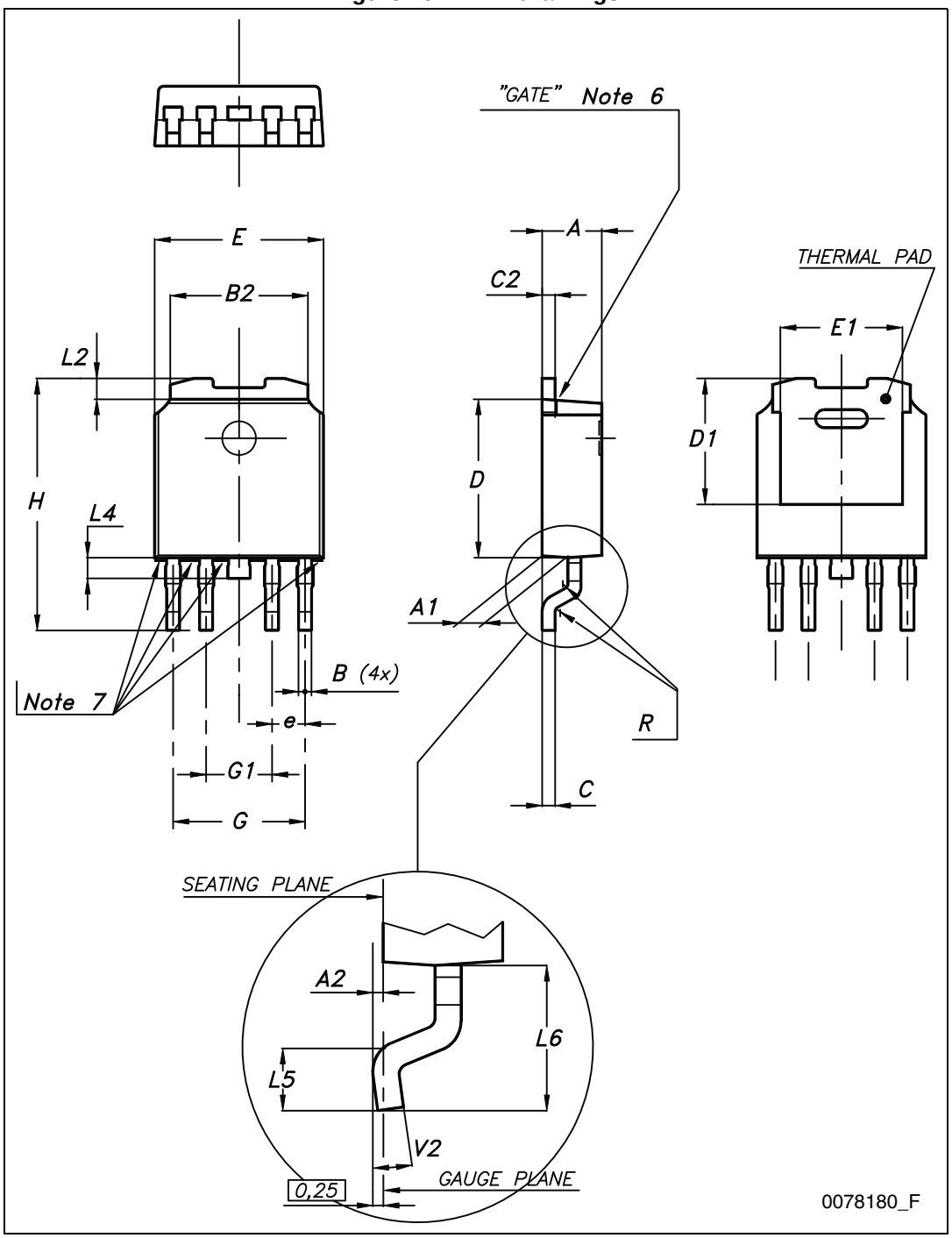


Table 6. PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A2	0.03		0.23
B	0.4		0.6
B2	5.2		5.4
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
D1		5.1	
E	6.4		6.6
E1		4.7	
e		1.27	
G	4.9		5.25
G1	2.38		2.7
H	9.35		10.1
L2		0.8	1
L4	0.6		1
L5	1		
L6		2.8	
R		0.20	
V2	0°		8°

9 Packaging mechanical data

Figure 20. PPAK tape

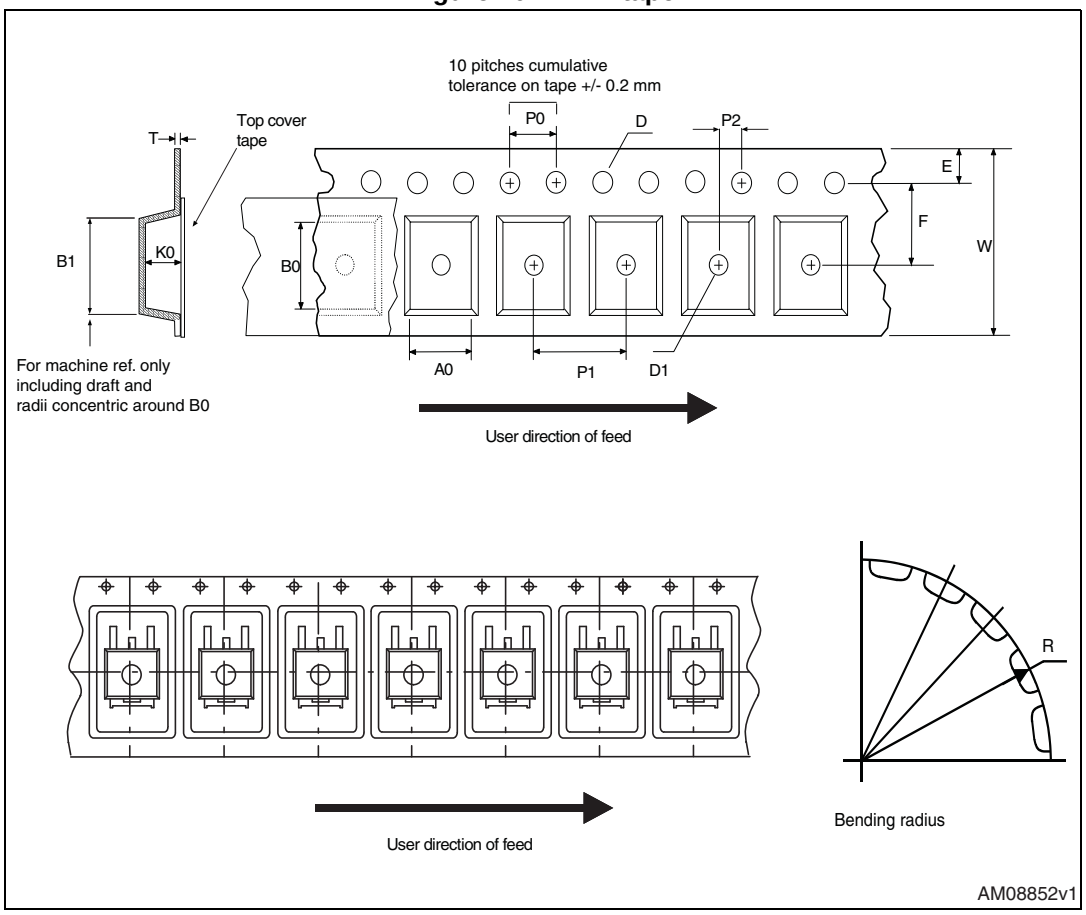


Figure 21. PPAK reel

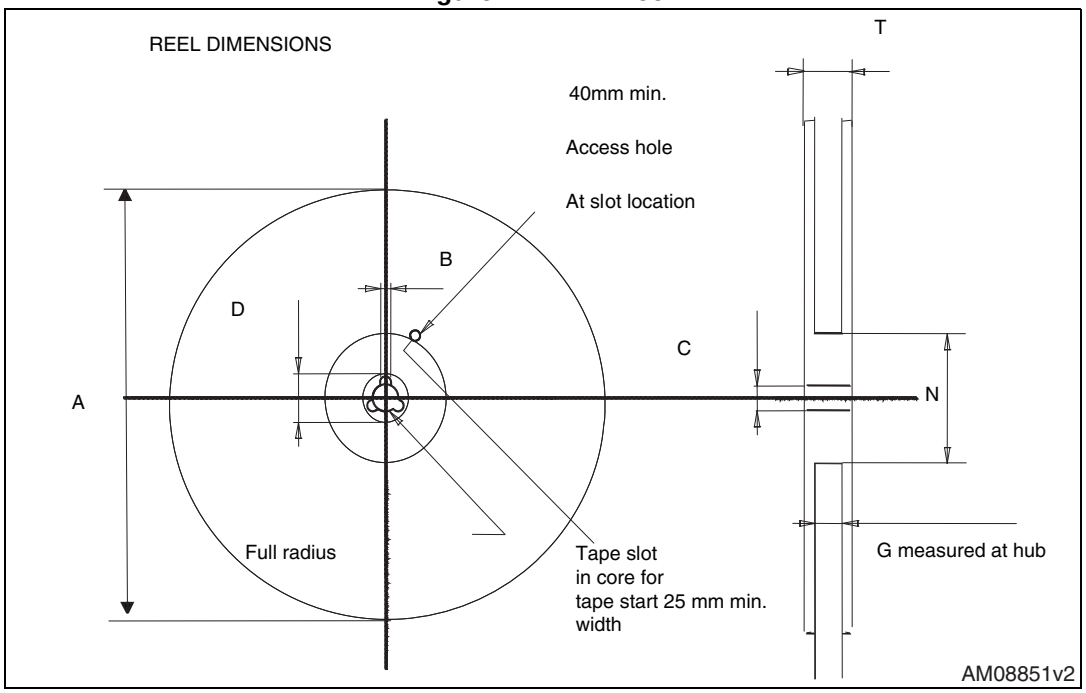


Table 7. PPAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

10 Revision history

Table 8. Document revision history

Date	Revision	Changes
26-Jan-2007	1	Initial release.
25-Mar-2014	2	Updated features in cover page, *Section 5: Electrical characteristics, Section 6: Typical performance characteristics, Section 7: Application notes, Section 8: Package mechanical data*. Added *Section 9: Packaging mechanical data.* Minor text changes.
01-Aug-2017	3	Updated *Table 1: Device summary* on the cover page.

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