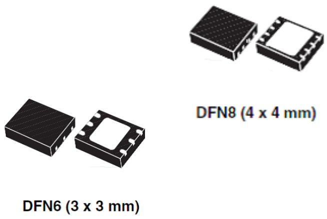
LD39200

Datasheet

2 A high PSRR ultra low drop linear regulator with reverse current protection



Maturity status link
LD39200

Features

- Input voltage from 1.25 V to 6.0 V
- Ultra low drop: 130 mV (typ.) at 2 A load
- 1 % output accuracy at 25 °C, 2 % in full temperature range
- High PSRR: 70 dB at 1 kHz
- Reverse current protection
- 2 A guaranteed output current
- Available in fixed and adjustable output voltage version from 0.5 V with 100 mV step
- Power Good
- Internal current and thermal limit
- Operating junction temperature range: -40 °C to 125 °C
- DFN6 (3 x 3 mm) and DFN8 (4 x 4 mm) packages

Applications

- Telecom infrastructure
- Medium power POL

Description

The LD39200 provides 2 A of maximum current with an input voltage range from 1.25 V to 6.0 V, and a typical dropout voltage of 130 mV.

It is stable with ceramic capacitors on the output (10 µF).

Typical power supply rejection ratio is 70 dB at 1 kHz and starts to roll off at 20 kHz.

The enable logic control function puts the LD39200 in shutdown mode, reducing the total current consumption to 10 nA (typ.).

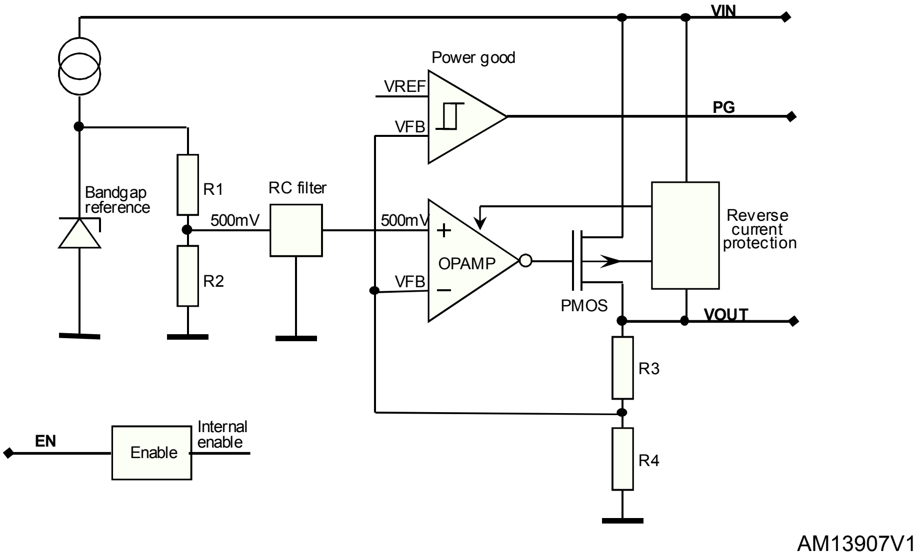
Power Good flag is available on a dedicated pin.

The device also includes reverse current protection, short-circuit constant current limit and thermal protection.

Typical applications are for Telecom infrastructure and consumer.

1 Block diagram

Figure 1. Block diagram



2 Pin configuration and description

Figure 2. Pin configuration (top view)

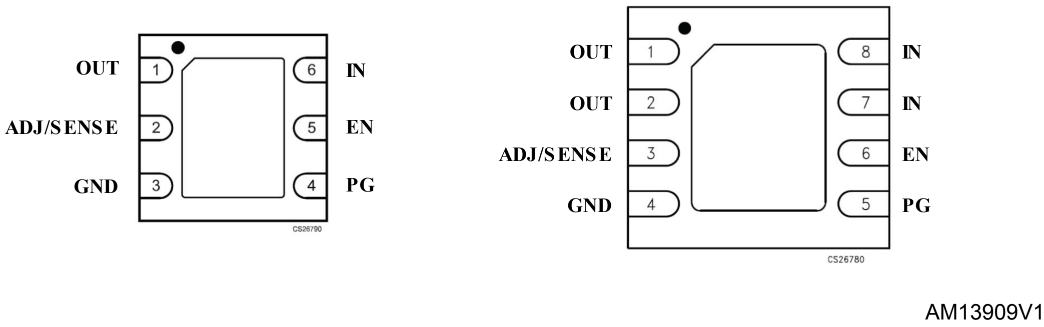


Table 1. DFN6 (3 x 3 mm) package pin description

Pin name	Pin number	Description
IN	6	Input voltage
GND	3	Ground
EN	5	Enable pin. The device is in OFF state when this pin is pulled low
ADJ/sense (1)	2	Adjustable pin on ADJ version can be connected to external resistor divider to set the output voltage. Output sense pin on the fixed version has to be connected to V_{OUT}
OUT	1	Output voltage
PG	4	Power Good
GND	Exposed pad	Exposed pad should be connected to GND

1. *The output sense pin of the fixed version has to be connected to the output pin for proper operation.*

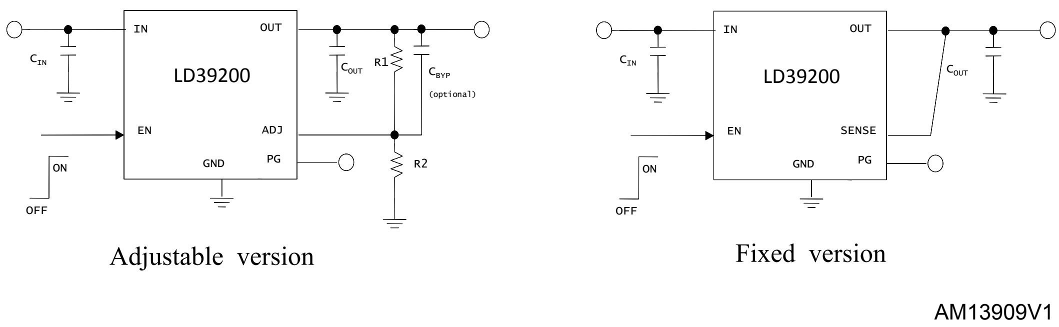
Table 2. DFN8 (4 x 4 mm) package pin description

Pin name	Pin number	Description
IN (1)	7, 8	Input voltage
GND	4	Ground
EN	6	Enable pin. The device is in OFF state when this pin is pulled low
ADJ/sense (2)	3	Adjustable pin on ADJ version can be connected to external resistor divider to set the output voltage. Output sense pin on the fixed version has to be connected to V_{OUT}
OUT (3)	1, 2	Output voltage
PG	5	Power Good
GND	Exposed pad	Exposed pad should be connected to GND

1. *Both of input pins have to be connected together on the board.*
2. *The output sense pin of the fixed version has to be connected to the OUT pin for proper operation.*
3. *Both of output pins have to be connected together on the board.*

3 Typical application

Figure 3. LD39200 typical application schematic



Note: *R1 and R2 are calculated according to the following formula: R1 = R2 x (V_{OUT} / V_{ADJ} - 1). Recommended value for C_{IN} and C_{OUT} is 10 µF.*

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input supply voltage	-0.3 to 7	V
V_{ADJ}	Adjustable voltage	-0.3 to 2	V
V_{OUT} /V_{SENSE}	Output voltage/output sense voltage	-0.3 to 7	V
I_{OUT}	Output current	Internally limited	A
EN	Enable pin voltage	-0.3 to 7	V
PG	Power Good pin voltage	-0.3 to 7	V
P_D	Power dissipation	Internally limited	W
ESD	Charge device model	±500	V
	Human body model	±2000	
T_{J-OP}	Operating junction temperature	-40 to 125	°C
T_{J-MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature	-55 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	DFN6 (3 x 3 mm)	DFN8 (4 x 4 mm)	Unit
R_{THJC}	Junction-to-case thermal resistance	10	4	°C/W
R_{THJA}	Junction-to- ambient thermal resistance	55	40	

5 Electrical characteristics

(T_J = 25 °C, V_{IN} = V_{OUT}+1 V; V_{OUT} = V_{ADJ}; C_{IN} = 10 µF; C_{OUT} = 10 µF; I_{OUT} = 10 mA; V_{EN} = V_{IN})

Table 5. Electrical characteristics, adjustable version

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		1.25		6.0	V
V_{ADJ}	Adjustable pin voltage			0.5		V
	Adjustable pin voltage accuracy	T_J = 25 °C	-1.0		1.0	%
		-40 °C < T_J < 125 °C	-2.0		2.0	
I_{ADJ}	Adjustable pin current	-40 °C < T_J < 125 °C		100		nA
ΔV_{ADJ}%/ Δ_{VIN}	Static line regulation	V_{OUT} + 1 V < V_{IN} < 6.0 V; T_J = 25 °C		0.01		%/V
		-40 °C < T_J < 125 °C			0.2	
ΔV_{ADJ}%/ Δ_{IOUT}	Static load regulation	0 mA < I_{OUT} < 2 A; T_J = 25 °C		0.1		%/A
		-40 °C < T_J < 125 °C			0.4	
V_{DROP}	Dropout voltage (1)	V_{IN} = 1.4 V; I_{OUT} = 1 A; -40 °C < T_J < 125 °C		120	250	mV
		V_{IN} = 2.5 V; I_{OUT} = 2 A; -40 °C < T_J < 125 °C		135	250	
		V_{IN} = 5.3 V; I_{OUT} = 2 A; -40 °C < T_J < 125 °C		110	250	
eN	Output noise voltage	V_{OUT} = V_{ADJ} ; f = 10 Hz to 100 kHz		45		μV_{RMS} / V_{OUT}
eN	Output noise voltage	V_{IN} = V_{OUT} + 0.4 V, I_{OUT} = 700 mA; C_{IN} = C_{OUT} = 10 µF, R2 = 10 kΩ, R1 = (V_{OUT} – 0.5) x 20 kΩ, C_{byp} = 470 nF		24		μV_{RMS}
SVR	Supply voltage rejection	V_{OUT} = 1.8 V; V_{IN} = V_{OUT}+0.5 V; C_{OUT} = 10 µF; I_{OUT} = 10 mA; T_J = 25 °C; f = 1 kHz		70		dB
		V_{OUT} = 1.8 V; V_{IN} = V_{OUT} + 0.5 V; C_{OUT} = 10 µF; I_{OUT} = 10 mA; T_J = 25 °C; f = 100 kHz		50		
		V_{OUT} = 1.8 V; V_{IN} = V_{OUT} + 0.5 V; C_{OUT} = 10 µF; I_{OUT} = 10 mA; T_J = 25 °C; f = 500 kHz		50		dB
		V_{OUT} = 1.8 V; V_{IN} = V_{OUT} + 0.5 V; C_{OUT} = 10 µF; I_{OUT} = 10 mA; T_J = 25 °C; f = 1 MHz		40		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_Q	Quiescent current	I_{OUT} = 0 A		100		µA
		I_{OUT} = 0 A; -40 °C < T_J < 125 °C			300	
		I_{OUT} = 2 A;		1		mA
		I_{OUT} = 2 A; -40 °C < T_J < 125 °C			3	
	Shutdown current	Ven = 0, Vin = 6 V		10		nA
I_{SC}	Short-circuit current	V_{OUT} = 0 V		3.5		A
I_{MIN}	Minimum output current				0	A
V_{EN}	Enable input logic low	1.25 V < V_{IN} < 6.0 V			0.5	V
	Enable input logic high	-40 °C < T_J < 125 °C	1.2			
I_{EN}	Enable pin input current	V_{EN} = V_{IN}; 1.25 < V_{IN} < 6.0 V		10		nA
PG	Power Good output threshold	Rising edge		0.92* V_{out}		V
		Falling edge		0.8*V_{out}		
	Power Good output voltage low	Isink = 6 mA open drain output			0.4	
T_{SHDN}	Thermal shutdown			170		°C
	Hysteresis			20		

1. *Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value; this specification does not apply to nominal output voltages below 1.2 V.*

(T_J = 25 °C, V_{IN} = V_{OUT}+1 V; C_{IN} = 10 µF; C_{OUT} = 10 µF; I_{OUT} = 10 mA; V_{EN} = V_{IN})

Table 6. Electrical characteristics, fixed version

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		1.25		6.0	V
V_{OUT}	Output voltage accuracy	T_J = 25 °C	-1.0		1.0	%
		-40 °C < T_J < 125 °C	-2.0		2.0	
$\Delta V_{ADJ\%}/\Delta V_{IN}$	Static line regulation	V_{OUT} + 1 V < V_{IN} < 6.0 V; T_J = 25 °C		0.01		%/V
		-40 °C < T_J < 125 °C			0.1	
$\Delta V_{ADJ\%}/\Delta I_{OUT}$	Static load regulation	0 mA < I_{OUT} < 2 A; T_J = 25 °C		0.05		%/A
		-40 °C < T_J < 125 °C			0.4	
V_{DROP}	Dropout voltage	V_{OUT} = 3.3 V; I_{OUT} = 2 A; -40 °C < T_J < 125 °C		130	250	mV
eN	Output noise voltage	V_{OUT} = 2.5 V; f = 10 Hz to 100 kHz		40		$\mu V_{RMS}/V_{OUT}$

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection	V_{OUT} = 1.8 V; V_{IN} = V_{OUT} + 0.5 V; C_{OUT} = 10 µF; I_{OUT} = 10 mA; T_J = 25 °C; f = 1 kHz		70		dB
		V_{OUT} = 1.8 V; V_{IN} = V_{OUT} + 0.5 V; C_{OUT} = 10 µF; I_{OUT} = 10 mA; T_J = 25 °C; f = 100 kHz		50		
		V_{OUT} = 1.8 V; V_{IN} = V_{OUT} + 0.5 V; C_{OUT} = 10 µF; I_{OUT} = 10 mA; T_J = 25 °C; f = 500 kHz		50		
		V_{OUT} = 1.8 V; V_{IN} = V_{OUT} + 0.5 V; C_{OUT} = 10 µF; I_{OUT} = 10 mA; T_J = 25 °C; f = 1 MHz		40		
I_Q	Quiescent current	I_{OUT} = 0 A		100		µA
		I_{OUT} = 0 A; -40 °C < T_J < 125 °C			300	
		I_{OUT} = 2 A;		1		mA
		I_{OUT} = 2 A; -40 °C < T_J < 125 °C			3	
	Shutdown current	Ven = 0, Vin = 6 V		50		nA
I_{SC}	Short-circuit current	V_{OUT} = 0 V		3.5		A
I_{MIN}	Minimum output current				0	A
V_{EN}	Enable input logic low	1.25 V < V_{IN} < 6.0 V			0.5	V
	Enable input logic high	-40 °C < T_J < 125 °C	1.2			
I_{EN}	Enable pin input current	V_{EN} = V_{IN}; 1.25 < V_{IN} < 6.0 V		10		nA
PG	Power Good output threshold	Rising edge		0.92*V_{OUT}		V
		Falling edge		0.8*V_{OUT}		
	Power Good output voltage low	Isink = 6 mA open drain output			0.4	
T_{SHDN}	Thermal shutdown			170		°C
	Hysteresis			20		

6 Application information

6.1 Thermal and short-circuit protections

The LD39200 is self-protected from short-circuit conditions and overtemperature. When the output load is higher than the one supported by the device, the output current rises until the limit of typically 3.5 A is reached; at this point the current is kept constant even when the load impedance is zero. The thermal protection acts when the junction temperature reaches 170 °C. The IC enters the shutdown status. As soon as the junction temperature falls again below 150 °C the device starts working again. In order to calculate the maximum power the device can dissipate, keeping the junction temperature below $T_{J\text{-}OP}$, the following formula is used:

$$P_{DMAX} = \left(125 - T_{AMB}\right) / R_{THJ-A} \quad (1)$$

6.2 Output voltage setting for ADJ version

In the adjustable version, the output voltage can be set from 0.5 V up to the input voltage minus the voltage drop across the pass transistor (dropout voltage), by connecting a resistor divider between the ADJ pin and the output, allowing remote voltage sensing. The resistor divider can be selected using the following equation:

$$V_{OUT} = V_{ADJ}\left(1 + R1/R2\right), with\, V_{ADJ} = 0.5\,V\,(typ.) \quad (2)$$

6.3 Enable pin

The LD39200 features an enable function. When the EN voltage is higher than 1.2 V the device is ON, and if it is lower than 0.5 V the device is OFF. In shutdown mode, the total current consumption is 10 nA (typ). The EN pin does not have an internal pull-up, therefore it cannot be left floating if it is not used.

6.4 Power Good pin (PG)

Some applications require a flag showing that the output voltage is in the correct range. Power Good threshold depends on the output voltage. When the output voltage is higher than 0.92 * $V_{OUT(nom)}$, the PG pin goes to high impedance. If the output voltage is below 0.80 * $V_{OUT(nom)}$ the PG pin goes to low impedance. If the device works well, the PG pin is at high impedance.

6.5 Reverse current protection

The device avoids the reverse current to flow from the output to the input during any operating condition (EN = 0 or EN = 1, $V_{IN} > V_{OUT} + V_{DROP}$). During fast turn-on/off this function prevents a big current from flowing to the input. Moreover it is used to avoid the reverse current to flow from the output pin to the input one, when other power supplies, providing a voltage higher than the input voltage, are connected to the output pin. If a power supply, providing a voltage lower than LDO output voltage, is connected to OUT pin, LDO works in current protection, causing high power dissipation inside the device.

When the device is disabled (EN = low) and V_{OUT} > 0 V, a small current (few µA) is sunk from the OUT pin.

7 Typical performance characteristics

(The following plots are referred to the typical application circuit and, unless otherwise noted, at T_A = 25 °C)

Figure 4. Dropout voltage vs. temperature (Vin = 1.3 V, Iout = 1 A)

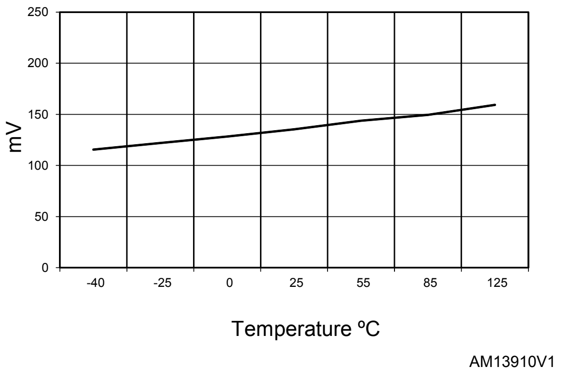


Figure 5. Dropout voltage vs. temperature (Vin = 1.4 V, Iout = 1 A)

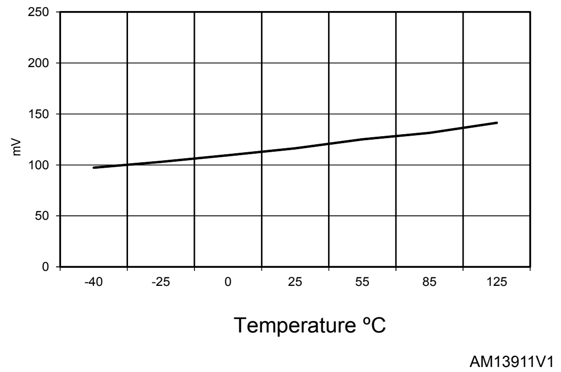


Figure 6. Dropout voltage vs. temperature (Vin = 1.4 V, Iout = 2 A)

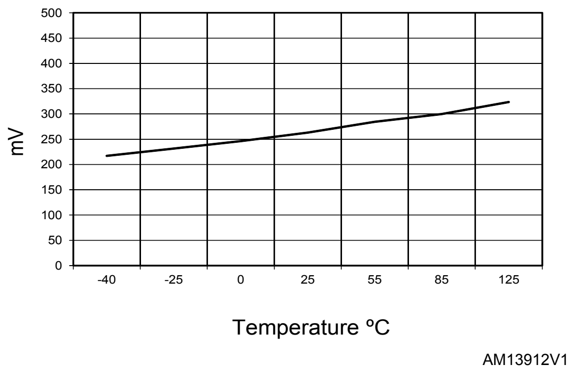


Figure 7. Dropout voltage vs. temperature (Vin = 1.5 V, Iout = 1 A)

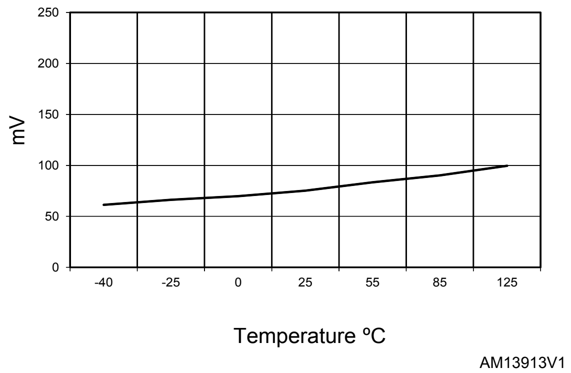
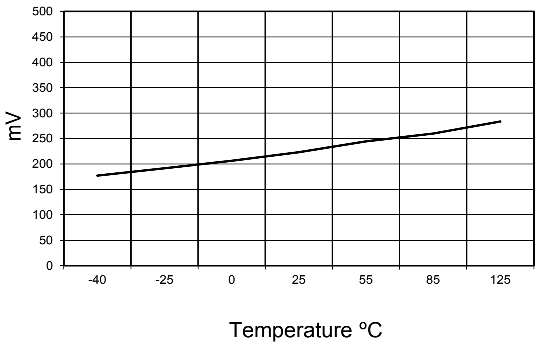
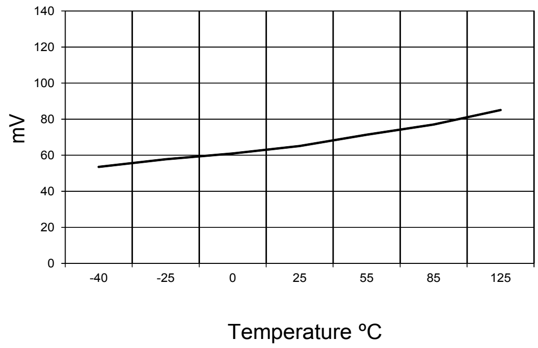


Figure 8. Dropout voltage vs. temperature (Vin = 1.5 V, Iout = 2 A)



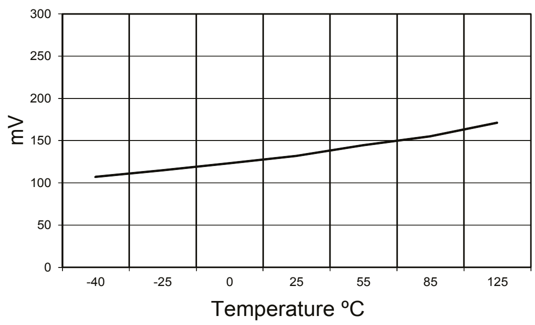
AM13914V1

Figure 9. Dropout voltage vs. temperature (Vin = 2.5 V, Iout = 1 A)



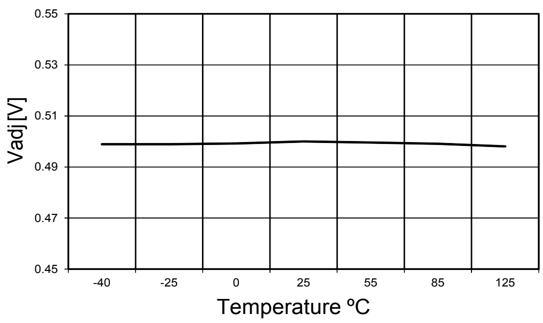
AM13915V1

Figure 10. Dropout voltage vs. temperature (Vin = 2.5 V, Iout = 2 A)



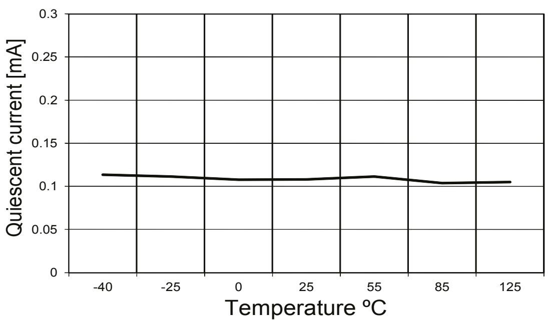
AM13916V1

Figure 11. Reference voltage vs. temperature (Vin = 1.5 V, Iout = 10 mA)



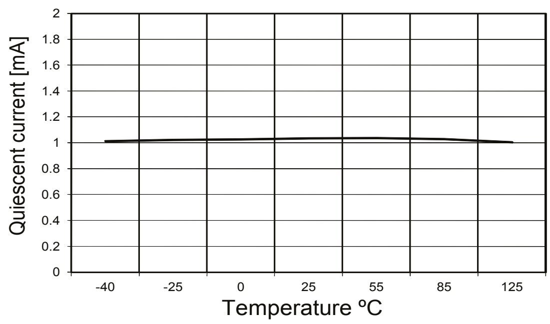
AM13917V1

Figure 12. Quiescent current vs. temperature (Vin = 1.5 V, Iout = 0 mA)



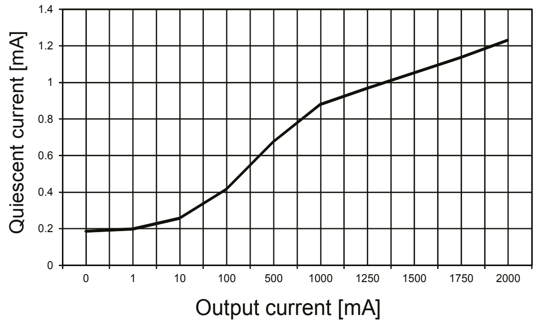
AM13918V1

Figure 13. Quiescent current vs. temperature (Vin = 1.5 V, Iout = 2 A)



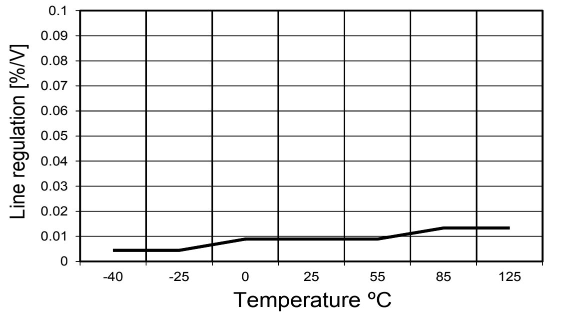
AM13919V1

Figure 14. Quiescent current vs. output current



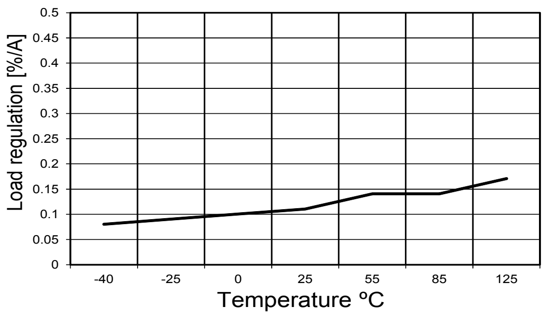
AM13920V2

Figure 15. Line regulation vs. temperature (1.5 V ≤ Vin ≤ 6 V, Iout = 10 mA)



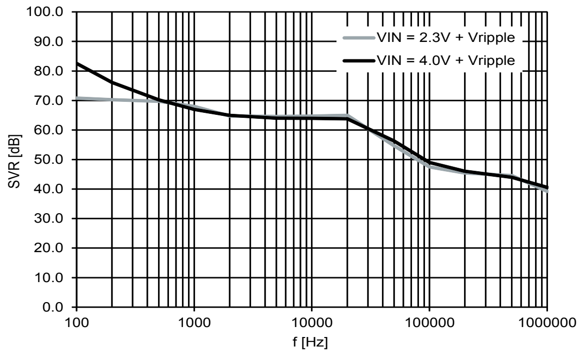
AM13920V1

Figure 16. Load regulation vs. temperature (Vin = 1.5 V, 0 < Iout < 2 A)



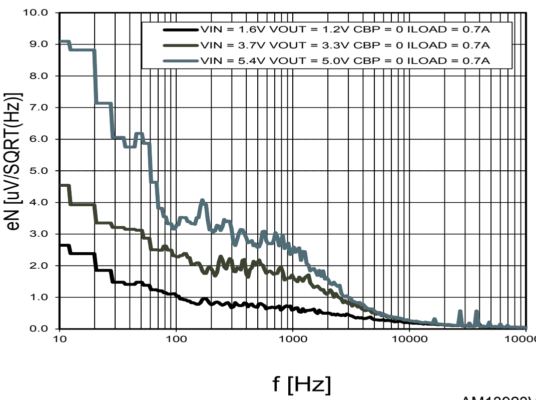
AM13921V1

Figure 17. SVR vs. frequency



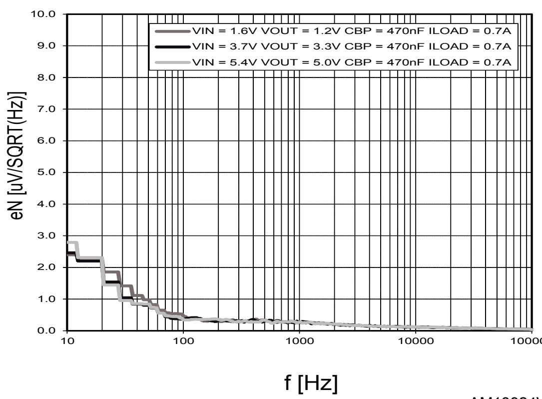
AM13922V1

Figure 18. Noise spectral density (no Cbyp)



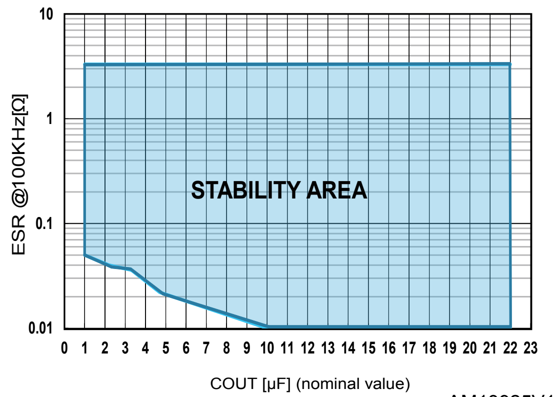
AM13923V1

Figure 19. Noise spectral density (Cbyp = 470 nF)



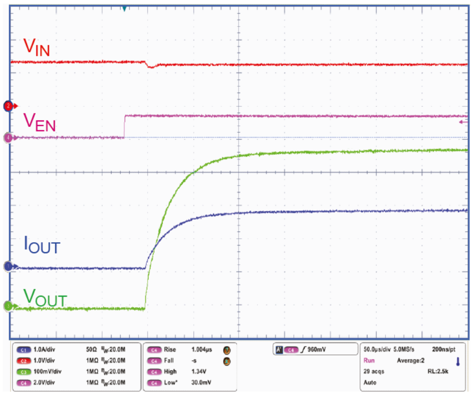
AM13924V1

Figure 20. Stability plan



AM13925V1

Figure 21. Enable startup, Vin = 1.25 V, Iout = 2 A



V_{IN} = 1.25 V, V_{EN} = from 0 to V_{IN}, I_{OUT} = 2 A, V_{OUT} = V_{ADJ}, C_{IN} = C_{OUT} = 10 µF, C_{BYP} = 0 nF

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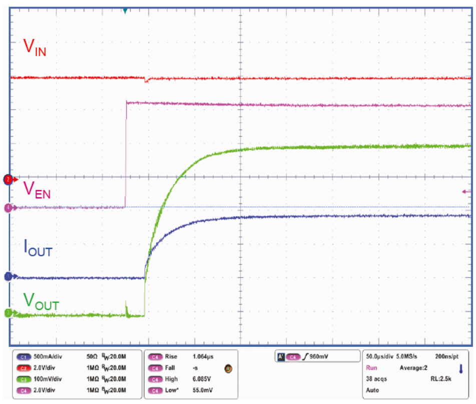
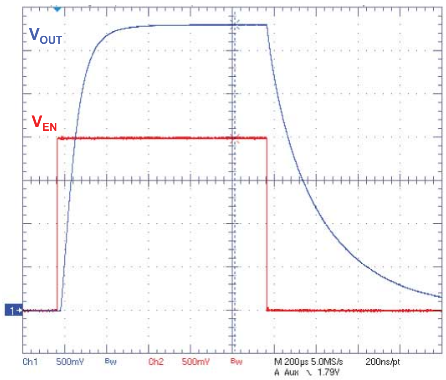
Figure 22. Enable startup, Vin = 6 V, Iout = 2 A



V_{IN} = 6 V, V_{EN} = from 0 to V_{IN}, I_{OUT} = 1 A, V_{OUT} = V_{REF}, C_{IN} = C_{OUT} = 10 µF, C_{BYP} = 0 nF

GIPG080420141423MT

Figure 23. Enable startup, no Cbyp



V_{IN} = 3.7 V, V_{EN} = from 0 to 2 V, I_{OUT} = 100 mA, V_{OUT} = 3.3 V, C_{IN} = C_{OUT} = 10 µF, C_{BYP} = 0

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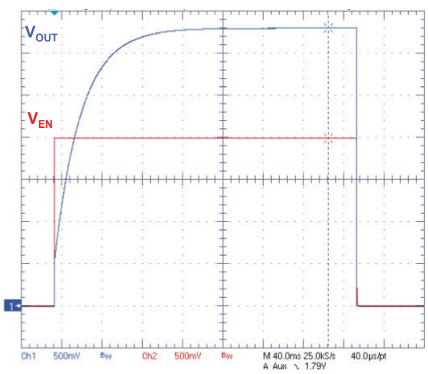
Figure 24. Enable startup, Cbyp = 470 nF



V_{IN} = 3.7 V, V_{OUT} = 3.3 V, V_{EN} = from 0 to 2V, I_{OUT} = 100 mA, C_{IN} = C_{OUT} = 10 µF, C_{BYP} = 470

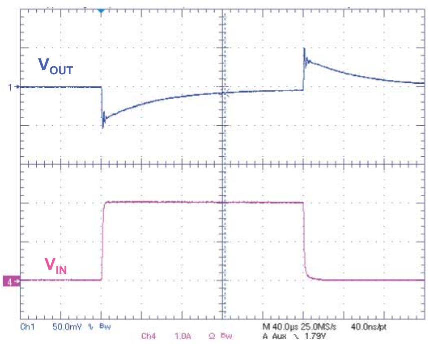
GIPG080420141552MT

Figure 25. Line transient

V_{IN} = V_{EN} = from 1.5 to 5.5 V, I_{OUT} = 10 mA, N_O C_{IN} = C_{OUT} = 10 µF, T_{RISE} = T_{FALL} = 10 µs

GIPG140420141401MT

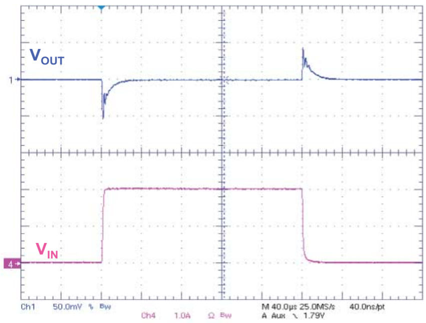
Figure 26. Load transient, no Cbyp



V_{IN} = 3.7 V, V_{OUT} = 3.3 V, I_{LOAD} = 10 mA to 2 A, C_{BYP} = 0

GIPG140420141403MT

Figure 27. Load transient, Cbyp = 470 nF



V_{IN} = 3.7 V, V_{OUT} = 3.3 V, I_{LOAD} = 10 mA to 2 A, C_{BYP} = 470 nF

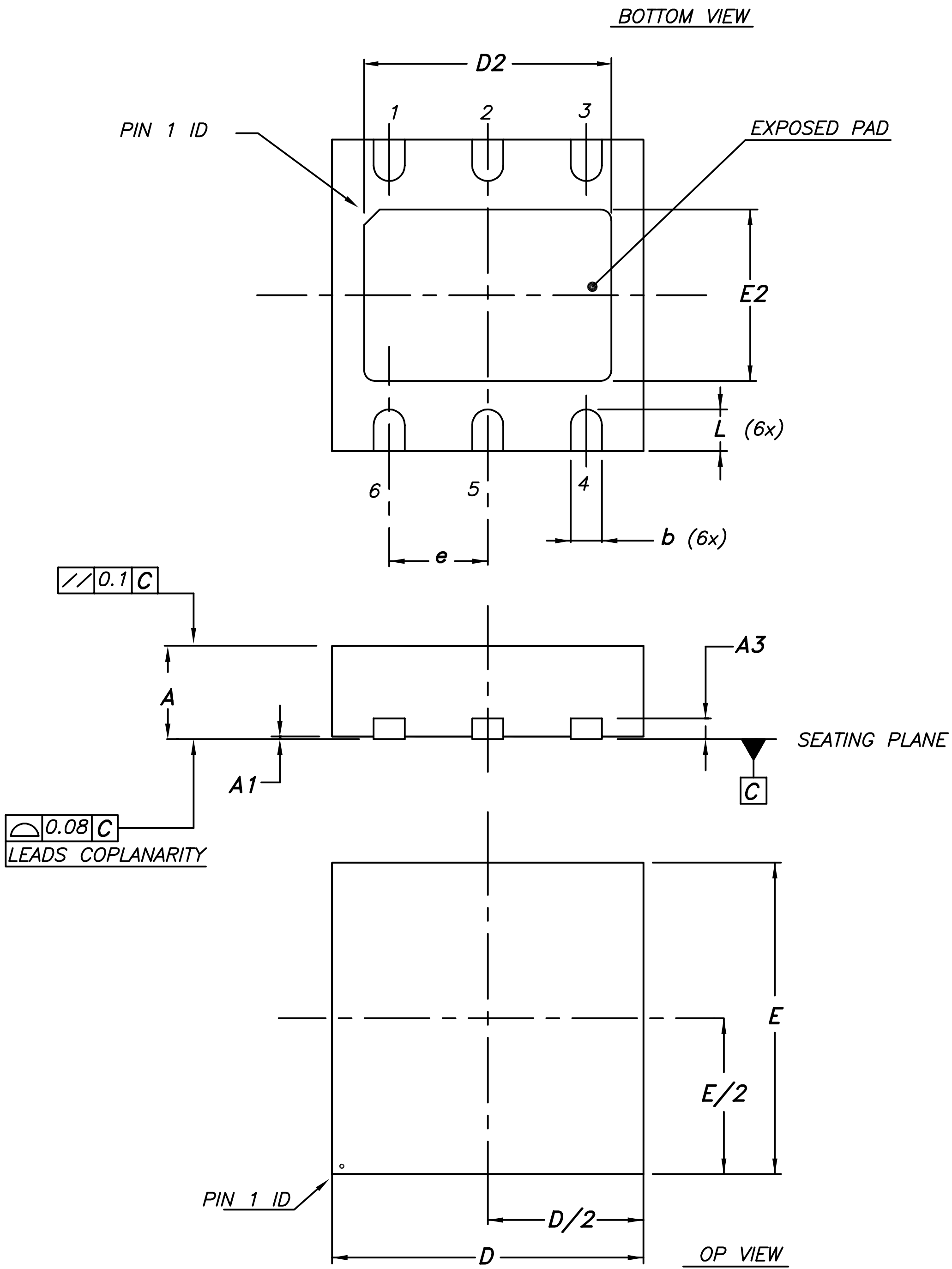
GIPG140420141405MT

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 DFN6 (3 x 3 mm) mechanical data

Figure 28. DFN6 (3 x 3 mm) package outline

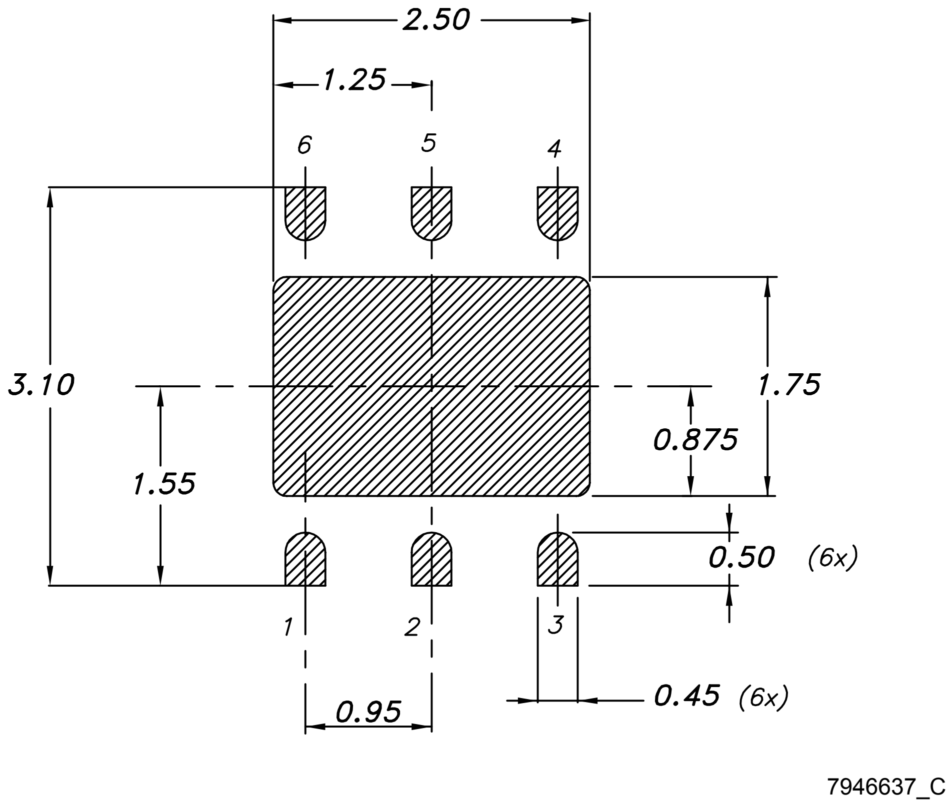


7946637_C

Table 7. **DFN6 (3 x 3 mm) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1
A1	0	0.02	0.05
A3		0.20	
b	0.23		0.45
D	2.90	3	3.10
D2	2.23		2.50
E	2.90	3	3.10
E2	1.50		1.75
e		0.95	
L	0.30	0.40	0.50

Figure 29. **DFN6 (3 x 3 mm) recommended footprint (all dimensions are in mm)**



8.2 DFN6 (3 x 3 mm) tape and reel mechanical data

Figure 30. **DFN6 (3 x 3 mm) tape outline**

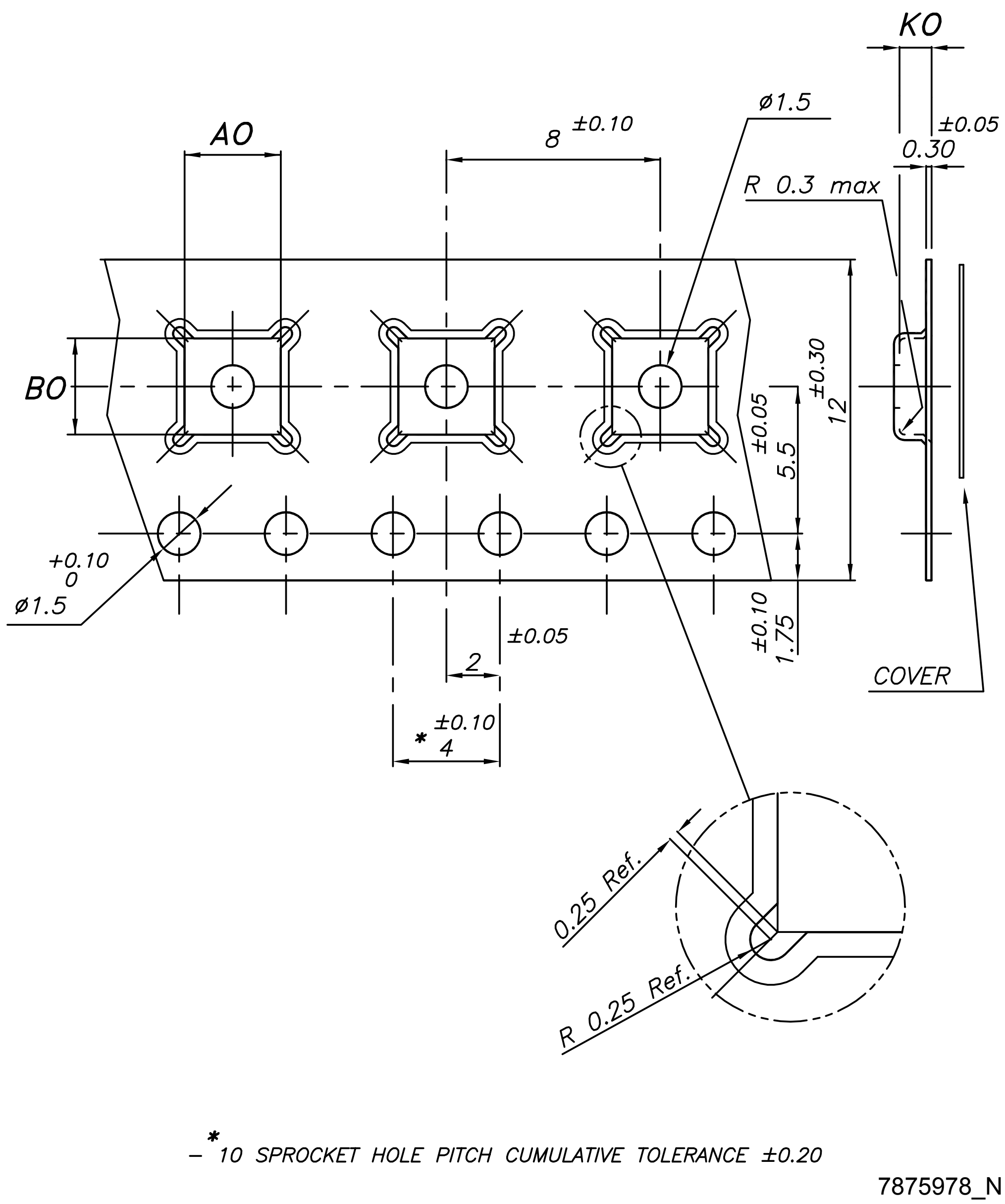
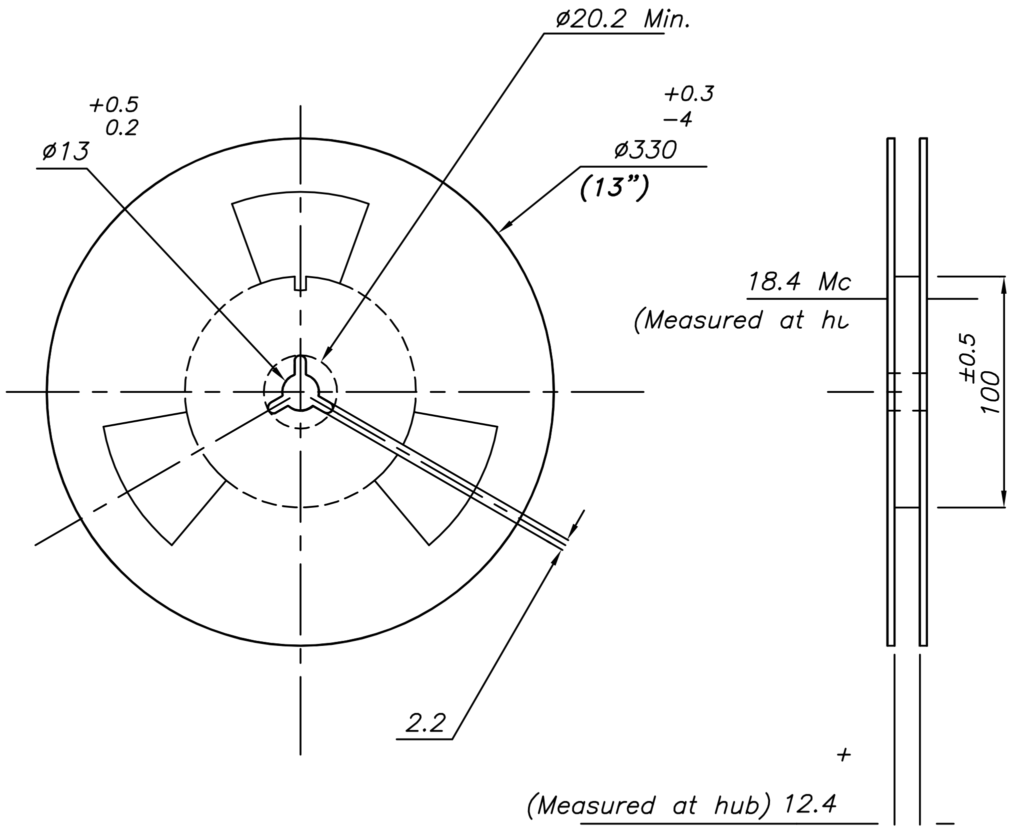


Figure 31. **DFN6 (3 x 3 mm) reel outline**



7875978_N

Table 8. **DFN6 (3 x 3 mm) tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

8.3 DFN8 (4 x 4 mm) mechanical data

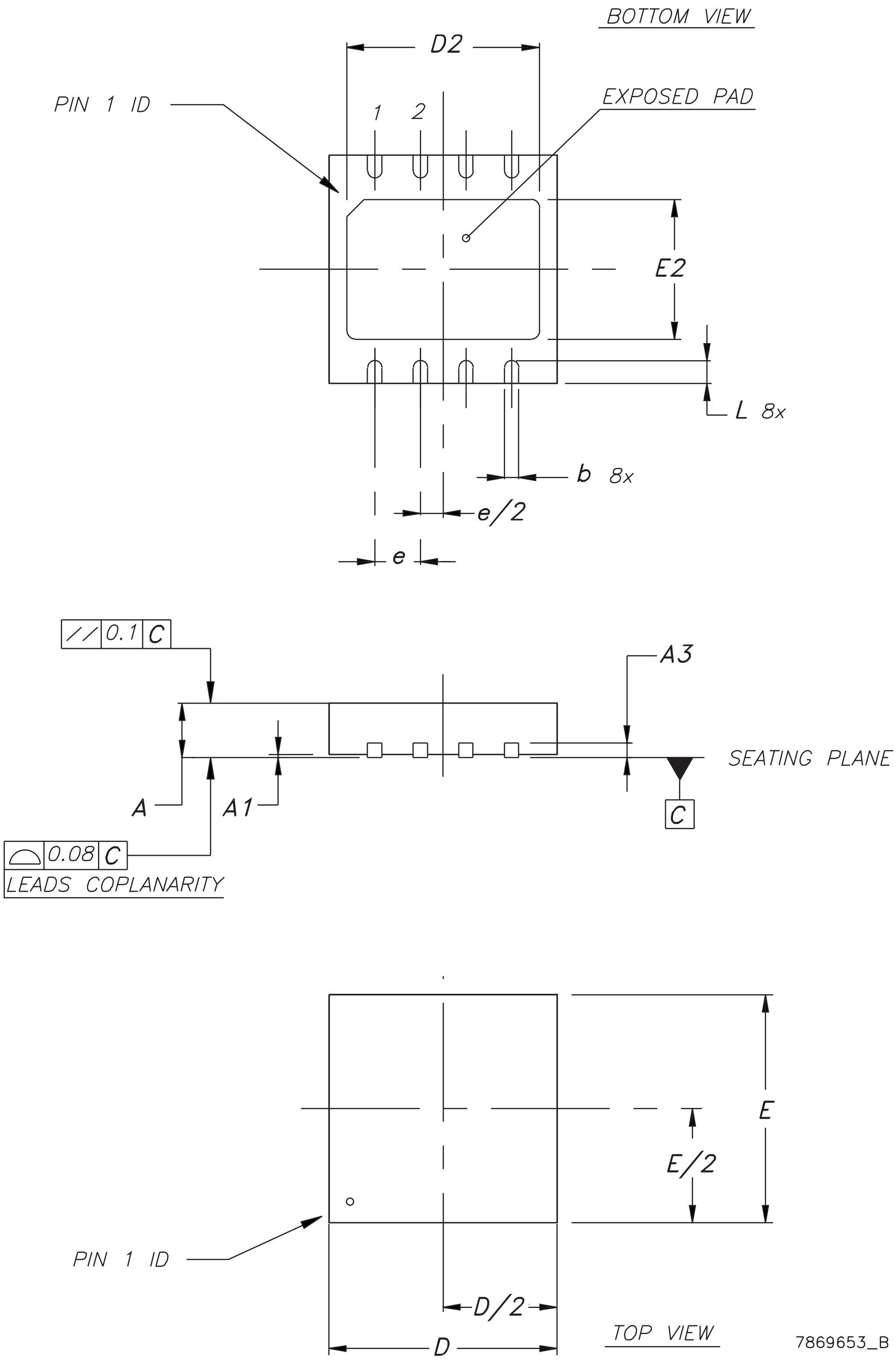
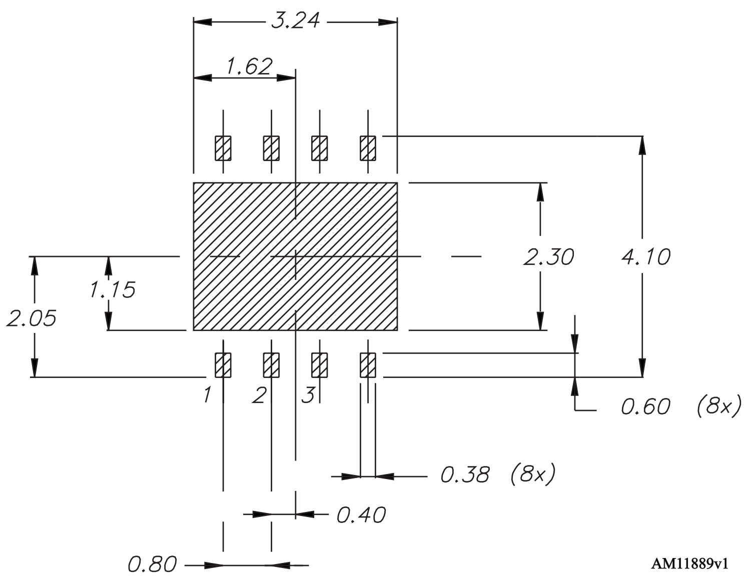


Figure 32. DFN8 (4 x 4 mm) package outline

Table 9. DFN8 (4 x 4 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1
A1	0	0.02	0.05
A3		0,20	
b	0.23	0.30	0.38
D	3.90	4	4.10
D2	2.82	3	3.23
E	3.90	4	4.10
E2	2.05	2.20	2.30
e		0.80	
L	0.40	0.50	0.60

Figure 33. DFN8 (4 x 4 mm) recommended footprint (all dimensions are in mm)



8.4 DFN8 (4 x 4 mm) reel mechanical data

Figure 34. DFN8 (4 x 4 mm) tape outline (all dimensions are in mm)

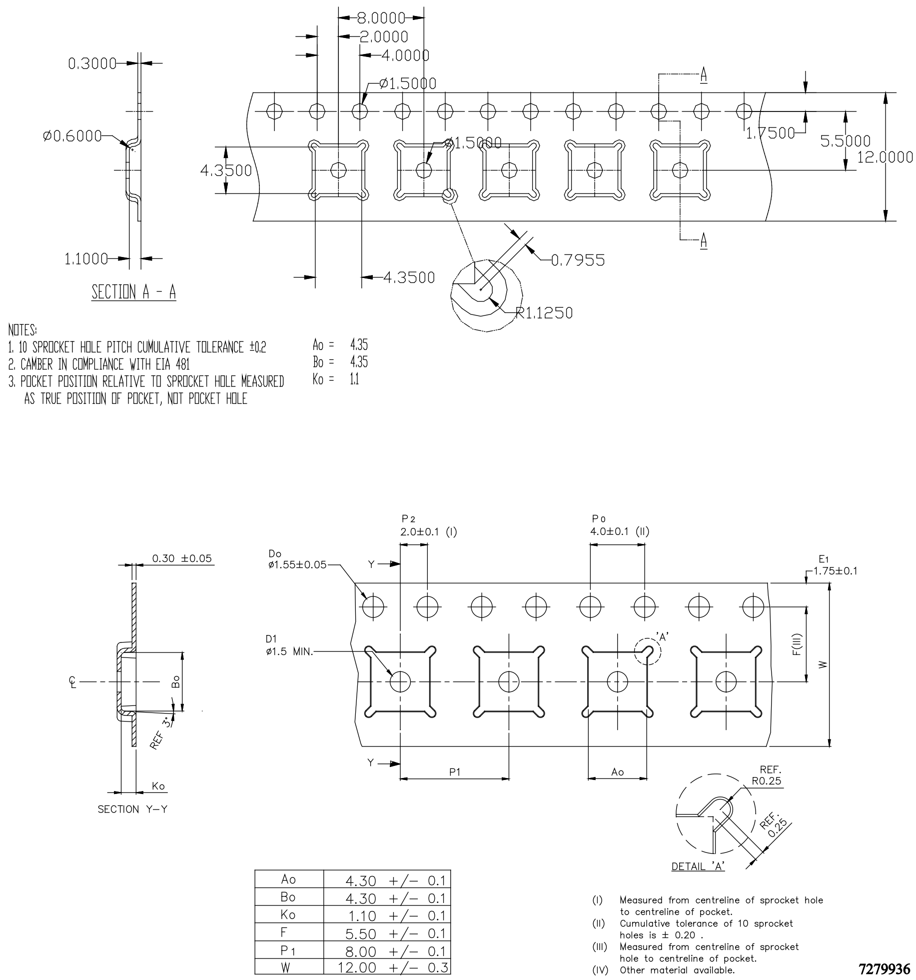


Figure 35. DFN8 (4 x 4 mm) reel outline

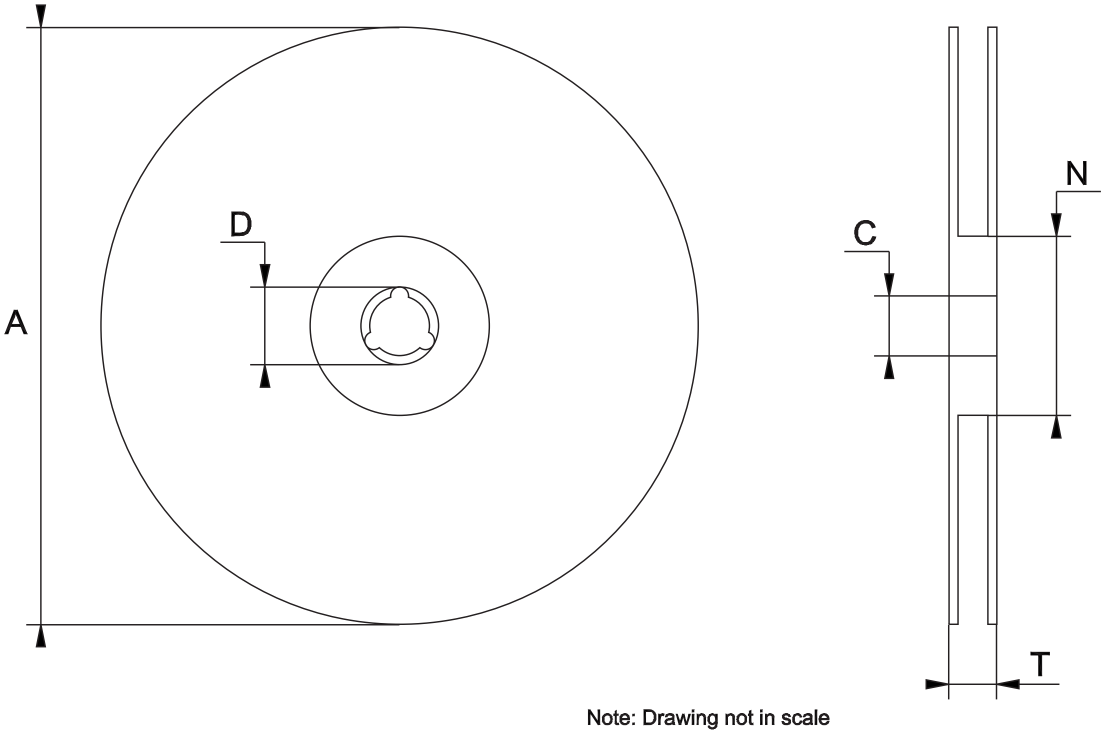


Table 10. DFN8 (4 x 4 mm) reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8	13.0	13.2
D	20.2		
N	60		
T			22.4

9 Ordering information

Table 11. Order codes

DFN6 (3 x 3 mm)	DFN8 (4 x 4 mm)	Output voltage
LD39200PUR	LD39200DPUR	ADJ
LD39200PU33R		3.3 V

Revision history

Table 12. Document revision history

Date	Revision	Changes
08-Jul-2014	1	Initial release.
06-Jul-2017	2	Updated Table 11: "Order codes". Minor text changes.
17-Sep-2018	3	Updated note Section 3 Typical application.

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