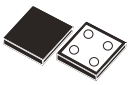
LDLN025

Datasheet

250 mA ultra low noise LDO



Flip-Chip4

DFN4-1x1

SOT23-5L

Maturity status link
LDLN025

Features

- Ultra low output noise: 6.5 μV_{RMS}
- Operating input voltage range: 1.5 V to 5.5 V
- Output current up to 250 mA
- Very low quiescent current: 12 µA at no-load
- Controlled I_q in dropout condition
- Very low-dropout voltage: 250 mV at 250 mA
- Very high PSRR: 80 dB@100 Hz, 60 dB @ 100 kHz
- Output voltage accuracy: 2% across line, load and temperature
- Output voltage versions: from 1 V to 5 V, with 50 mV step
- Logic-controlled electronic shutdown
- Output discharge feature
- Internal soft-start
- Overcurrent and thermal protections
- Temperature range: from -40 °C to +125 °C
- Packages: Flip-Chip4, DFN4-1x1, SOT23-5L

Applications

- Smartphones/tablets
- Image sensors
- Instrumentation
- VCO and RF modules

Description

The LDLN025 is a 250 mA low-dropout voltage regulator, able to work with an input voltage range from 1.5 V to 5.5 V.

The typical dropout voltage at 250 mA load is 120 mV.

The very low quiescent current, which is just 12 µA at no-load, extends battery-life of applications requiring very long standby time.

Thanks to its ultra low noise value and high PSRR, the LDLN025 provides a very clean output, suitable for ultra-sensitive loads. It is stable with ceramic capacitors.

The enable logic control function puts the device into shutdown mode allowing a total current consumption lower than 1 µA.

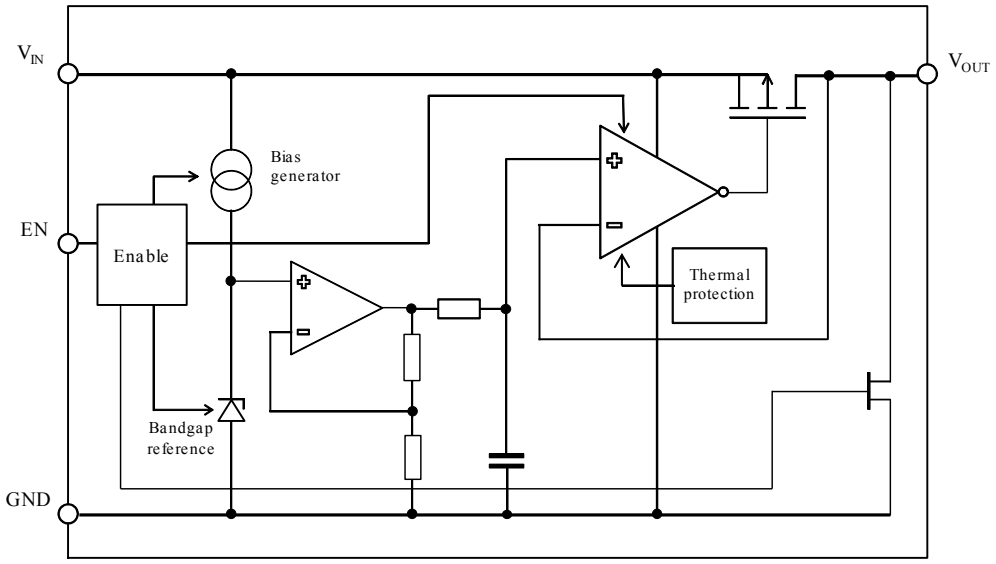
The device also includes short-circuit and thermal protection.

Typical applications are noise sensitive loads such as ADC, VCO in mobile phones and tablets, wireless LAN devices. The LDLN025 is designed to keep the quiescent current under control and at a low value also during dropout operation, extending the operating time of battery-powered devices.

Several small package options are available.

1 Block diagram

Figure 1. **Block diagram**



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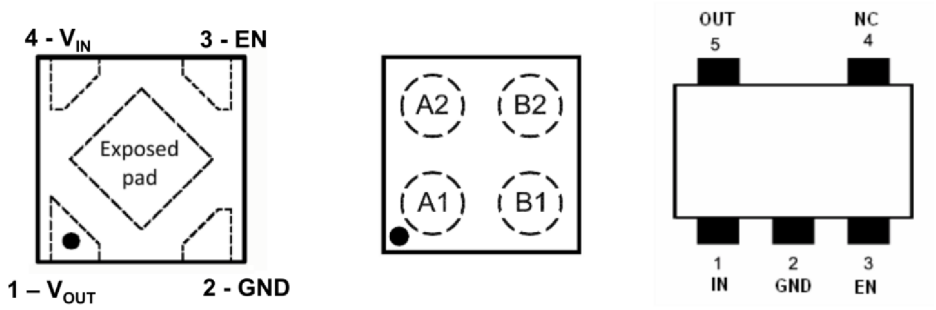
2 Pin configuration

Figure 2. **Pin configuration**



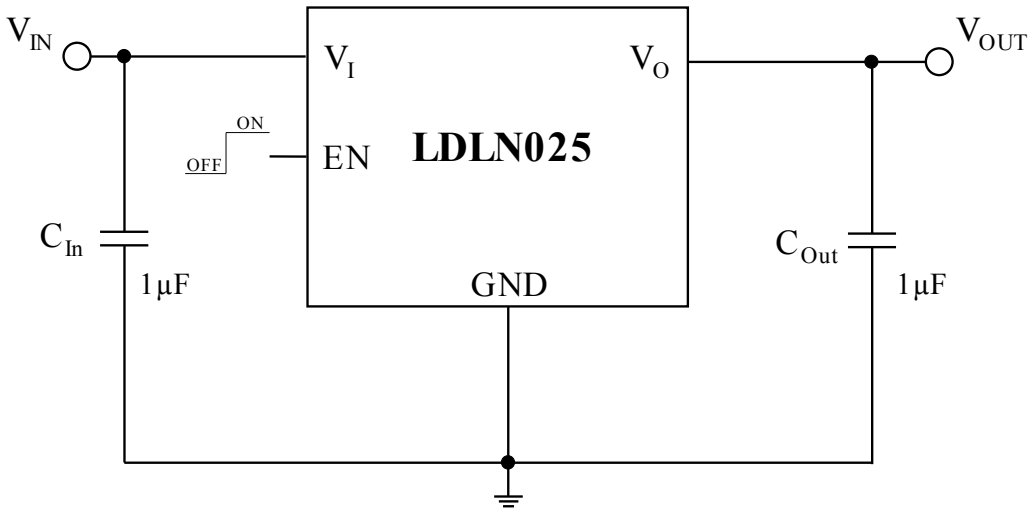
DFN4-1x1 (marking view) | Flip-Chip4 (marking view) | SOT23-5L (top view)

Table 1. **Pin description**

Symbol	DFN4-1x1	Flip-Chip4	SOT23-5L	Description
V_{IN}	4	A1	1	LDO Supply voltage
V_{OUT}	1	A2	5	LDO Output voltage
GND	2	B2	2	Ground
EN	3	B1	3	Enable input: set V_{EN} = high to turn on the device; V_{EN} = low to turn off the device
				This pin is internally pulled down via 1 MΩ resistor
NC	-	-	4	Not internally connected: can be connected to GND
Exposed pad	Exposed pad	-	-	Must be connected to GND

3 Typical application diagram

Figure 3. **Typical application diagram**



4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input supply voltage	-0.3 to 7	V
V_{OUT}	Output voltage	-0.3 to V_{IN} +0.3	V
I_{OUT}	Output current	Internally limited	A
EN	Enable pin voltage	-0.3 to V_{IN} +0.3	V
P_D	Power dissipation	Internally limited	W
ESD	Charge device model	±1000	V
	Human body model	±2000	
T_{J-OP}	Operating junction temperature	-40 to 125	°C
T_{J-MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature	-55 to 150	°C

Table 3. Thermal data

Symbol	Parameter	DFN4-1x1	Flip-Chip4	SOT23-5L	Unit
R_{thja}	Thermal resistance, junction-to-ambient	220	210	200	°C/W

5 Electrical characteristics

(T_J = 25 °C, V_{IN} = $V_{OUT(nom)}$ + 1 V or 1.5 V, whichever is greater; V_{EN} = 1.2 V; C_{IN} = 1 µF; C_{OUT} = 1 µF; I_{OUT} = 1 mA)

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		1.5		5.5	V
V_{OUT}	Output voltage accuracy (Flip-Chip package)	V_{OUT} + 1 V < V_{IN} < 5.5 V, (1) 1 mA < I_{OUT} < 0.25 A, V_{OUT} ≥ 1.8 V, -40 °C < T_J < 125 °C	-2.0		+2.0	%
		V_{OUT} + 1 V < V_{IN} < 5.5 V,(1) 1 mA < I_{OUT} < 0.25 A, V_{OUT} < 1.8 V, -40 °C < T_J < 125 °C	-3.0		+3.0	
V_{OUT}	Output voltage accuracy (DFN and SOT23 packages)	V_{OUT} + 1 V < V_{IN} < 5.5 V,(1) 1 mA < I_{OUT} < 0.25 A, V_{OUT} ≥ 1.8 V, -40 °C < T_J < 125 °C	-2.0		+2.0	%
		V_{OUT} + 1 V < V_{IN} < 5.5 V,(1) 1 mA < I_{OUT} < 0.25 A, V_{OUT} < 1.8 V, -40 °C < T_J < 125 °C	-4.0		+4.0	
$\Delta V_{OUT}/\Delta V_{IN}$	Static line regulation	V_{OUT} + 1 V < V_{IN} < 5.5 V(1)		0.02		%/V
		-40 °C < T_J < 125 °C			0.06	
	Line transient (2)	ΔV_{IN} = +/- 0.6 V, t_{rise} = t_{fall} = 30 µs	-1		+1	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Static load regulation	1 mA < I_{OUT} < 0.25 A, V_{OUT} ≥ 1.8 V		0.002		%/mA
		-40 °C < T_J < 125 °C, V_{OUT} ≥ 1.8 V			0.007	
		1 mA < I_{OUT} < 0.25 A, V_{OUT} < 1.8 V		20		mV
	Load transient(2)	ΔI_{OUT} = 1 mA to 250 mA and back, t_{rise} = t_{fall} = 10 µs	-40		+40	mV
ΔV_{OUT}	Overshoot on startup(2)	Percentage of $V_{OUT(nom)}$			5	%
V_{DROP}	Dropout voltage(3)	I_{OUT} = 0.1 A		50		mV
		I_{OUT} = 0.25 A		120		
		I_{OUT} = 0.25 A, -40 °C < T_J < 125 °C (Flip-Chip4)			200	
		I_{OUT} = 0.25 A, -40 °C < T_J < 125 °C (DFN4-1x1)			250	
eN	Output noise voltage (2)	f = 10 Hz to 100 kHz; I_{OUT} = 1 mA		10		μV_{RMS}
		f = 10 Hz to 100 kHz; I_{OUT} = 250 mA		6.5		
SVR	Supply voltage rejection(2)	f = 100 Hz; I_{OUT} = 20 mA		80		dB
		f = 1 kHz; I_{OUT} = 20 mA		80		
		f = 10 kHz; I_{OUT} = 20 mA		75		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection(2)	f = 100 kHz; I_{OUT} = 20 mA		60		dB
I_Q	Quiescent current(4)	I_{OUT} = 0 A		12		µA
		I_{OUT} = 0 A; -40 °C < T_J < 125 °C			25	
		I_{OUT} = 0.25 A		250		µA
		I_{OUT} = 0.25 A; -40 °C < T_J < 125 °C			425	
	Shutdown current	V_{EN} = 0 V		0.2	1	µA
I_{SC}	Short-circuit current	V_{OUT} = 0 V	250	500		mA
R_{LOW}	Output discharge resistance	V_{EN} = 0 V		230		Ω
V_{EN}	V_{IL}, enable input logic low	V_{OUT} + 1 V < V_{IN} < 5.5 V -40 °C < T_J < 125 °C(1)			0.4	V
	V_{IH}, enable input logic high		1.2			
I_{EN}	Enable pin input current	V_{IN} = V_{EN} = 5.5 V		5.5		µA
		V_{IN} = 5.5 V; V_{EN} = 0 V		0.001		
t_{ON}	Turn-on time(2)	From V_{EN} > V_{IH} to V_{OUT} = 95 % of $V_{OUT(nom)}$		80	150	µs
T_{SHDN}	Thermal shutdown(2)	I_{OUT} > 1 mA		160		°C
	Hysteresis			20		

1. *V_{IN} = V_{OUT} + 1 V or 1.5 V, whichever is greater. Not applicable for 5 V output voltage versions.*
2. *Guaranteed by design.*
3. *Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.*
4. *The quiescent current is defined as I_{IN}-I_{OUT} and does not include the EN pin current.*

Table 5. Recommended input and output capacitors

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input capacitance	Stability	0.7	1		µF
C_{OUT}	Output capacitance		0.7	1	10	
ESR	Output/input capacitance		5		500	mΩ

6 Typical characteristics

(The following plots are referred to LDLN025J2925R in the typical application circuit and, unless otherwise noted, at T_A = 25 °C).

Figure 4. Output voltage vs. temperature (V_{IN} = 3.925 V)

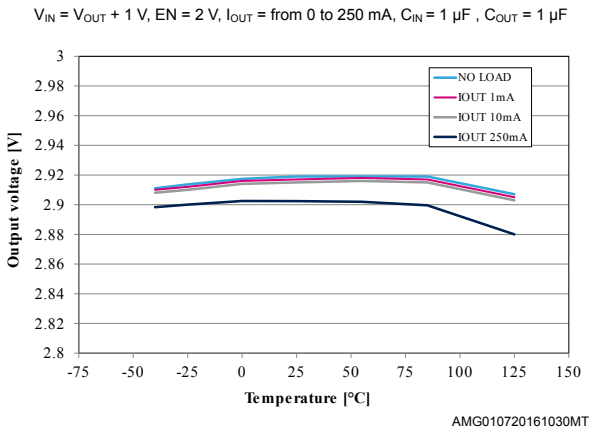


Figure 5. Output voltage vs. temperature (V_{IN} = 5.5 V)

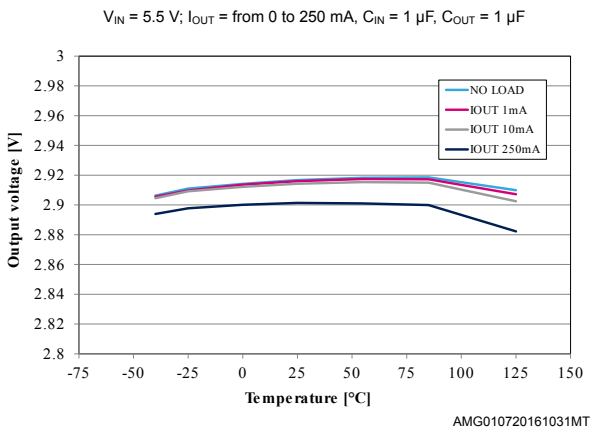


Figure 6. Load regulation vs. temperature

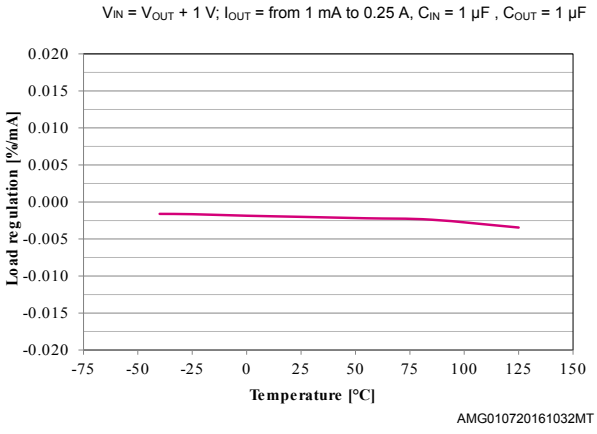


Figure 7. Line regulation vs. temperature

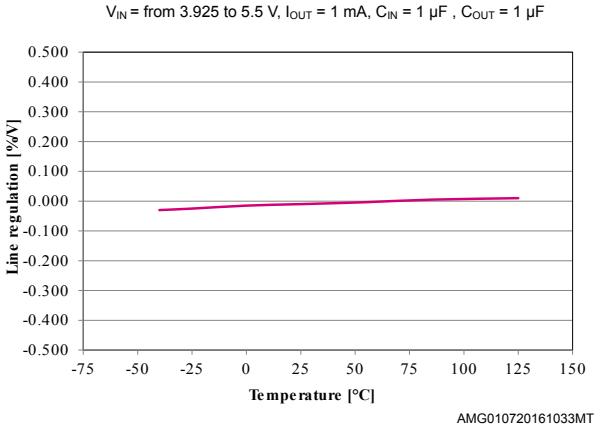


Figure 8. Quiescent current vs. temperature (I_{OUT} = 0 mA)

$V_{IN} = V_{OUT} + 1$ V, V_{EN} = 1.2 V, I_{OUT} = 0 A, C_{IN} = 1 µF , C_{OUT} = 1 µF

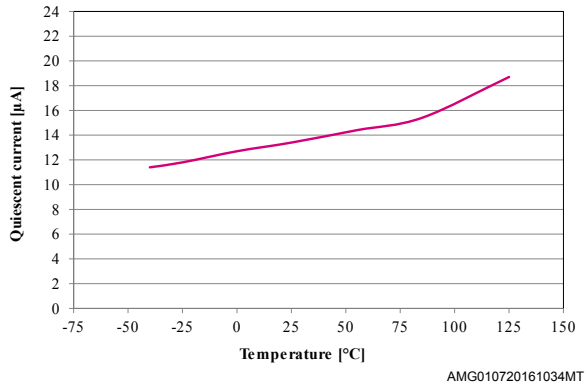


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Figure 9. Quiescent current vs. temperature (I_{OUT} = 250 mA)

$V_{IN} = V_{OUT} + 1$ V, V_{EN} = 1.2 V, I_{OUT} = 250 mA, C_{IN} = 1 µF , C_{OUT} = 1 µF

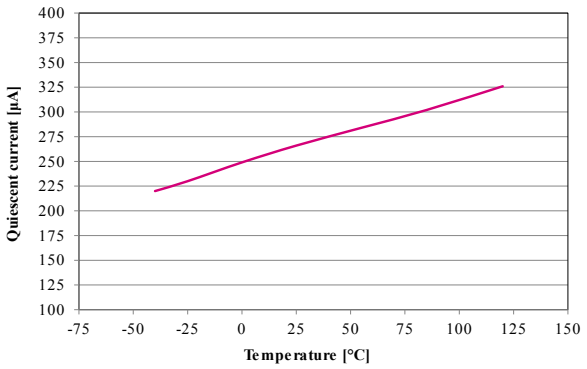

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Figure 10. GND current vs. input voltage

V_{IN} = EN = from 0 to 6 V, I_{OUT} = 0 A, C_{IN} = 1 µF , C_{OUT} = 1 µF

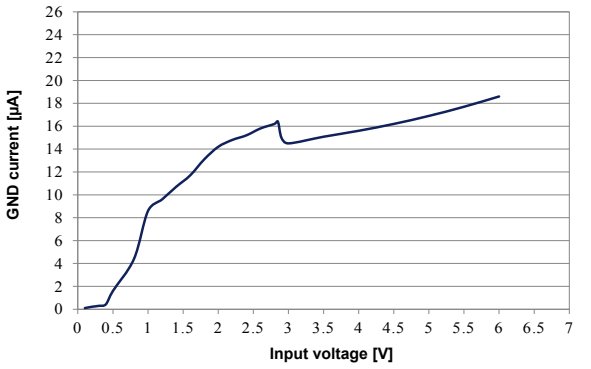

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Figure 11. Off-state current vs. temperature

$V_{IN} = V_{OUT} + 1$ V, I_{OUT} = 0 A, C_{IN} = 1 µF , C_{OUT} = 1 µF

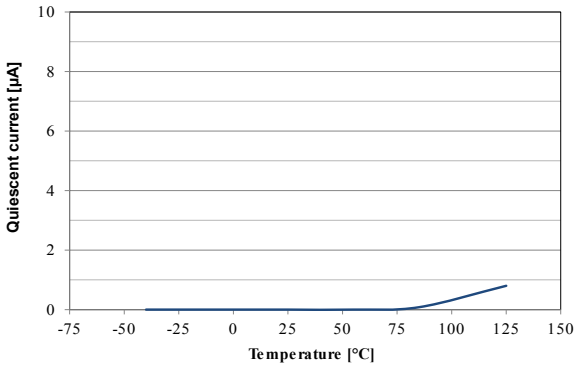

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Figure 12. Quiescent current vs. output current

V_{EN} = 1.2 V, I_{OUT} = from 0 to 250 mA, C_{IN} = 1 µF , C_{OUT} = 1 µF

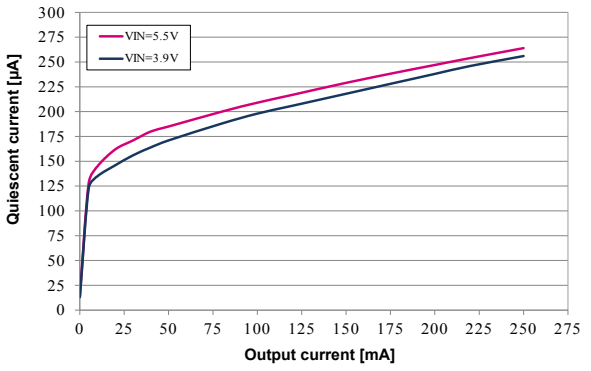

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Figure 13. Quiescent current vs. output current (zoom)

V_{EN} = 1.2 V, I_{OUT} = from 0 to 5 mA, C_{IN} = 1 µF , C_{OUT} = 1 µF

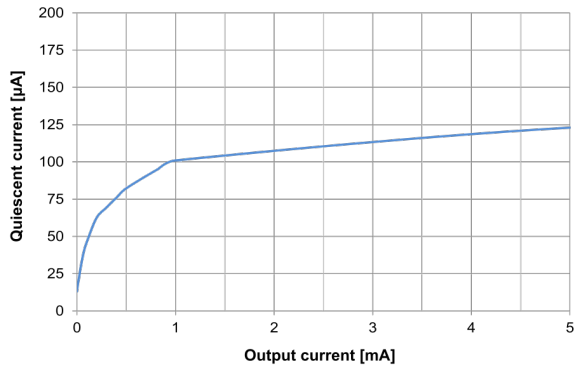

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Figure 14. Dropout voltage vs. temperature

V_{OUT} = 2.8 V, I_{OUT} = 0.25 A, C_{IN} = 1 µF , C_{OUT} = 1 µF

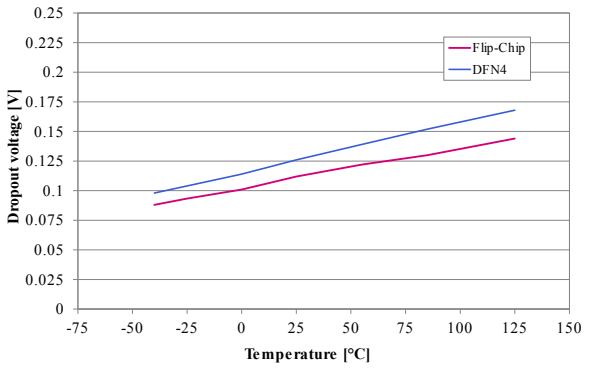

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Figure 15. Dropout voltage vs. load current

V_{OUT} = 2.8 V, C_{IN} = 1 µF , C_{OUT} = 1 µF

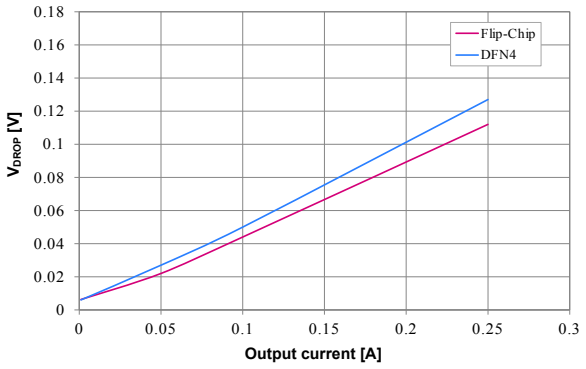

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Figure 16. Output voltage vs. input voltage

V_{IN} = V_{EN} = from 0 to 5.5 V, V_{OUT} = 2.75 V, I_{OUT} = 250 mA, C_{IN} = 1 µF , C_{OUT} = 1 µF

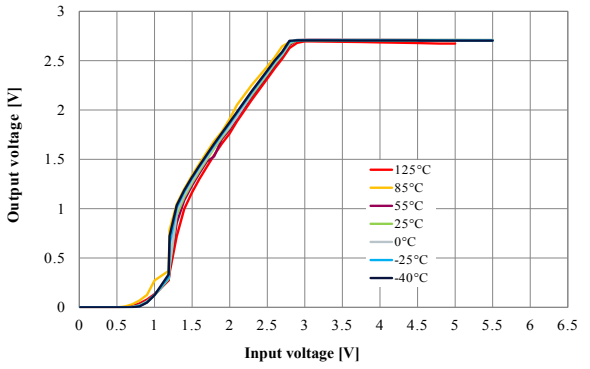

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Figure 17. Short circuit current vs. dropout voltage

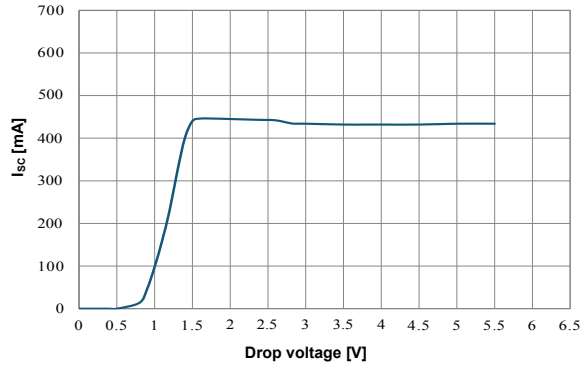

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Figure 18. Enable threshold vs. temperature

V_{IN} = 3.925 V, I_{OUT} = 1 mA, C_{IN} = 1 µF , C_{OUT} = 1 µF

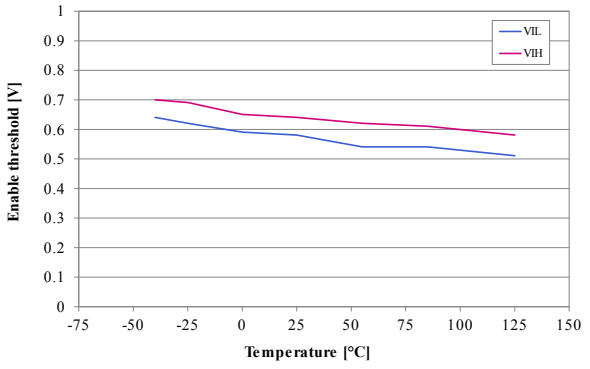

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Figure 19. Stability region vs. C_{OUT} and ESR

V_{IN} = V_{OUT} + $V_{drop(max)}$ to 5.5 V, I_{OUT} = from 1 mA to 250 mA, T= 25 °C, C_{IN} = 1 µF

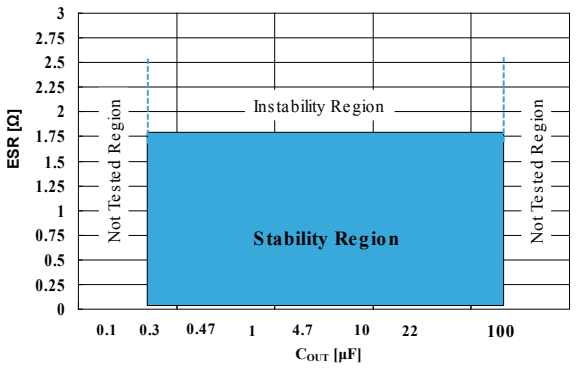

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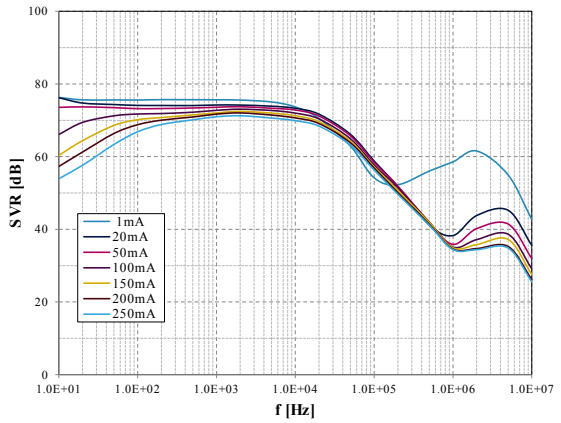
Figure 20. PSRR vs. frequency (V_{OUT} = 2.75 V)



V_{IN} = 3.75 V + V_{ripple}, V_{OUT} = 2.75 V, no C_{IN}, C_{OUT} = 1 µF, V_{EN} = 1.2 V

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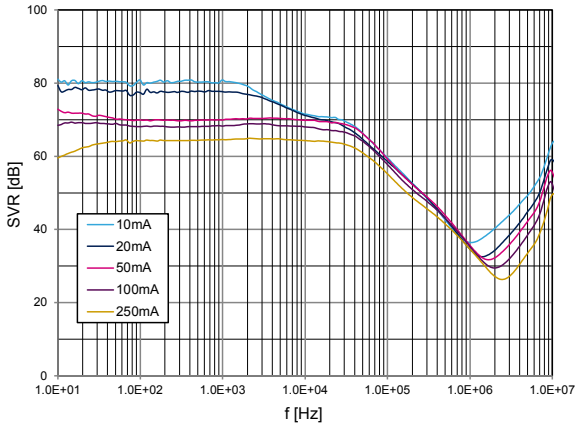
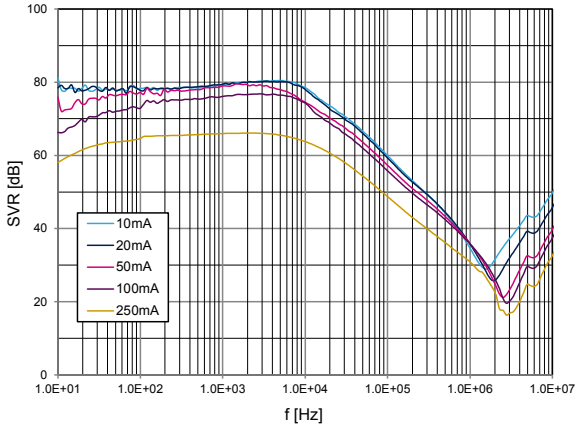
Figure 21. PSRR vs. frequency (V_{OUT} = 1.8 V)



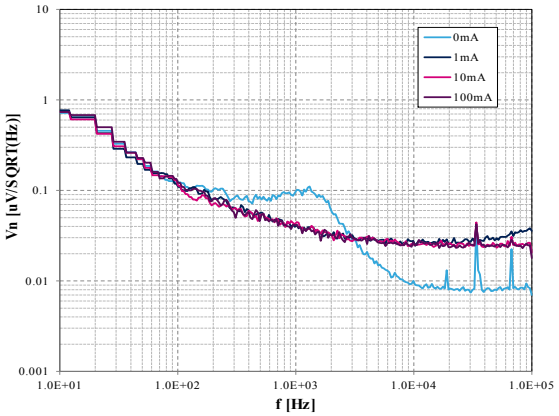
V_{IN} = 2.5 V + V_{ripple}, V_{OUT} = 1.8 V, no C_{IN}, C_{OUT} = 1 µF, V_{EN} = 1.2 V

Figure 22. PSRR vs. frequency (V_{OUT} = 5 V)



V_{IN} = 5 V + V_{ripple}, V_{OUT} = 5 V, no C_{IN}, C_{OUT} = 1 µF, V_{EN} = 1.2 V

Figure 23. Noise density



V_{IN} = 3.75 V, V_{OUT} = 2.75 V, C_{IN} = C_{OUT} = 1 µF

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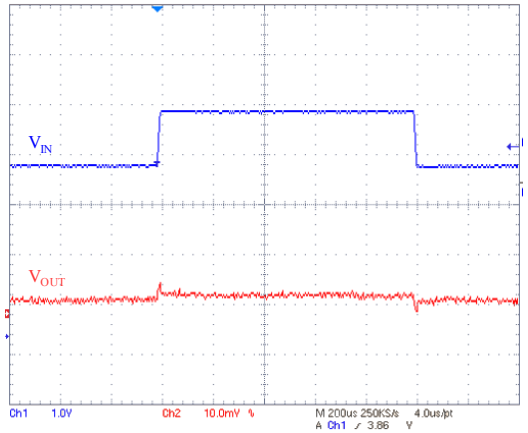
Figure 24. Line transient (I_{OUT} = 1 mA)



V_{IN} = from 3.4 V to 4.4 V, I_{OUT} = 1 mA, t_r = 10 µs, C_{IN} = C_{OUT} = 1 µF (X7R)

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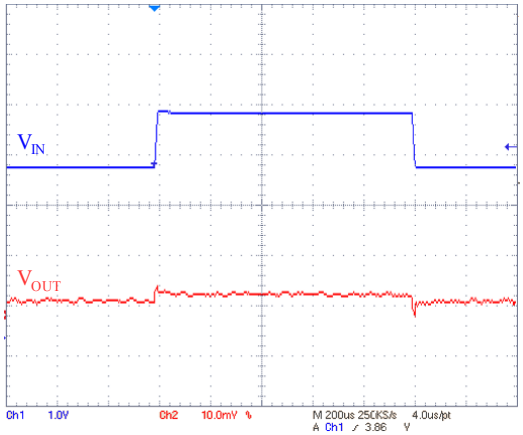
Figure 25. Line transient (I_{OUT} = 250 mA)



V_{IN} = from 3.4 V to 4.4 V, I_{OUT} = 250 mA, t_r = 10 µs, C_{IN} = C_{OUT} = 1 µF (X7R)

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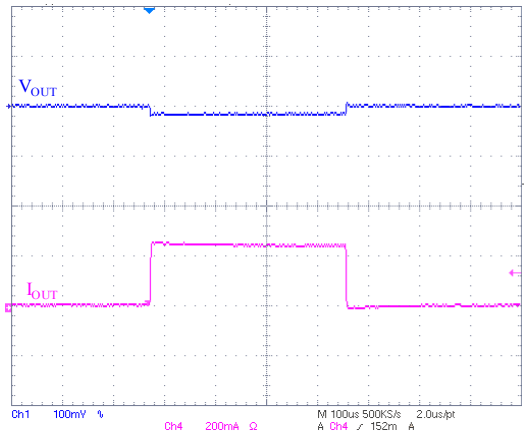
Figure 26. Load transient



I_{OUT} = from 0 mA to 250 mA, t_r = 10 µs, C_{IN} = C_{OUT} = 1 µF (X7R)

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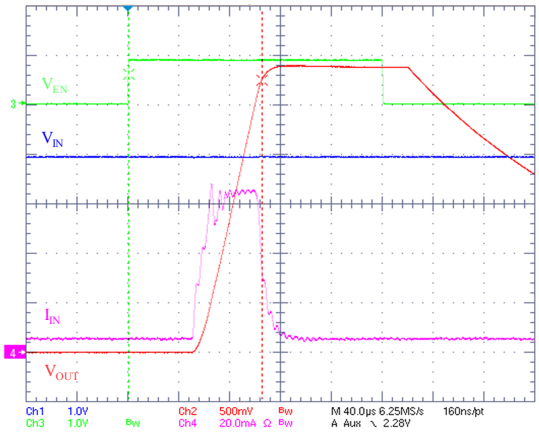
Figure 27. Inrush current



V_{IN} = 4 V, I_{OUT} = 0 mA, C_{IN} = C_{OUT} = 1 µF (X7R)

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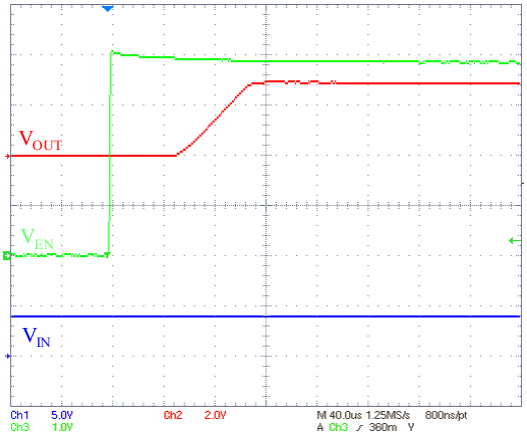
Figure 28. Enable transient (I_{OUT} = 0 mA)



V_{IN} = 3.925 V, V_{EN} = from 0 V to 3.925 V, I_{OUT} = 0 mA, t_r = 1 µs, C_{IN} = C_{OUT} = 1 µF (X7R)

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Figure 29. Enable transient (I_{OUT} = 250 mA)

V_{IN} = 3.925 V, V_{EN} = from 0 V to 3.925 V, I_O = 250 mA, t_r = 1 µs, C_{IN} = C_{OUT} = 1 µF (X7R)

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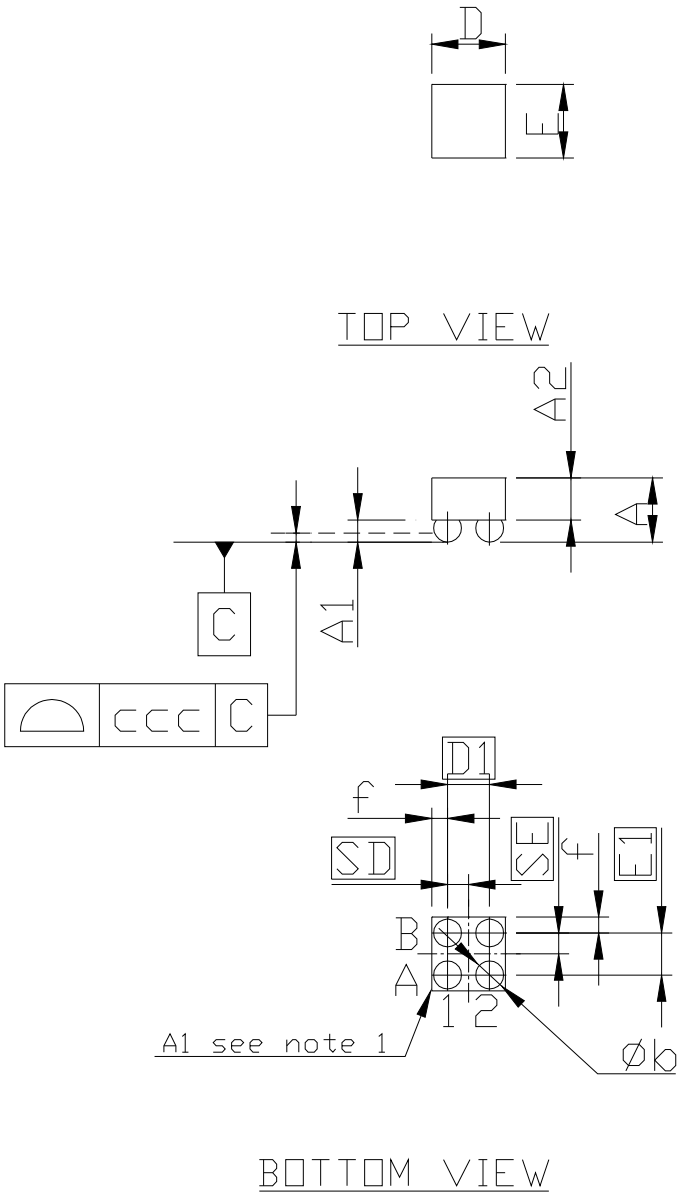
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 Flip-Chip4 package information

Figure 30. Flip-Chip4 package outline



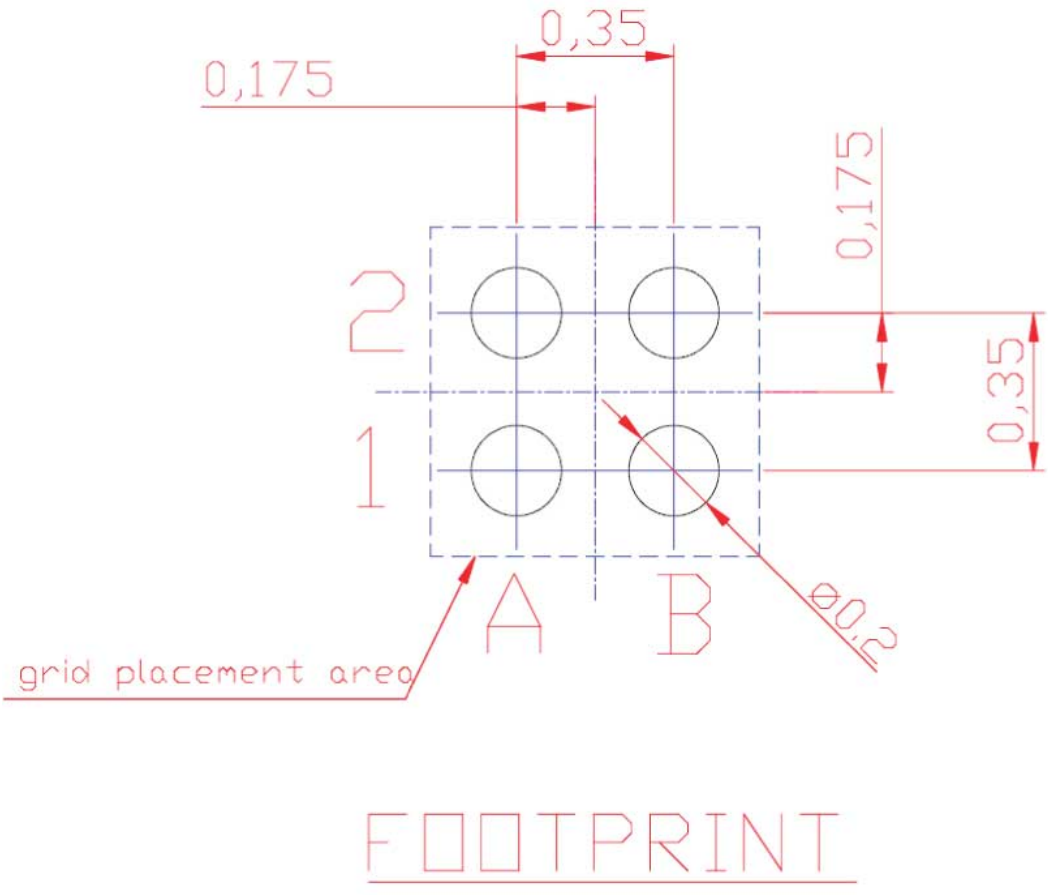
8387748 option F

Table 6. Flip-Chip4 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.375	0.410	0.445
A1	0.145	0.160	0.175
A2 (1)	0.230	0.250	0.270
b	0.189	0.210	0.231
D	0.598	0.628	0.658
D1		0.350	
E	0.598	0.628	0.658
E1		0.350	
SD		0.175	
SE		0.175	
f		0.139	
ccc		0.075	

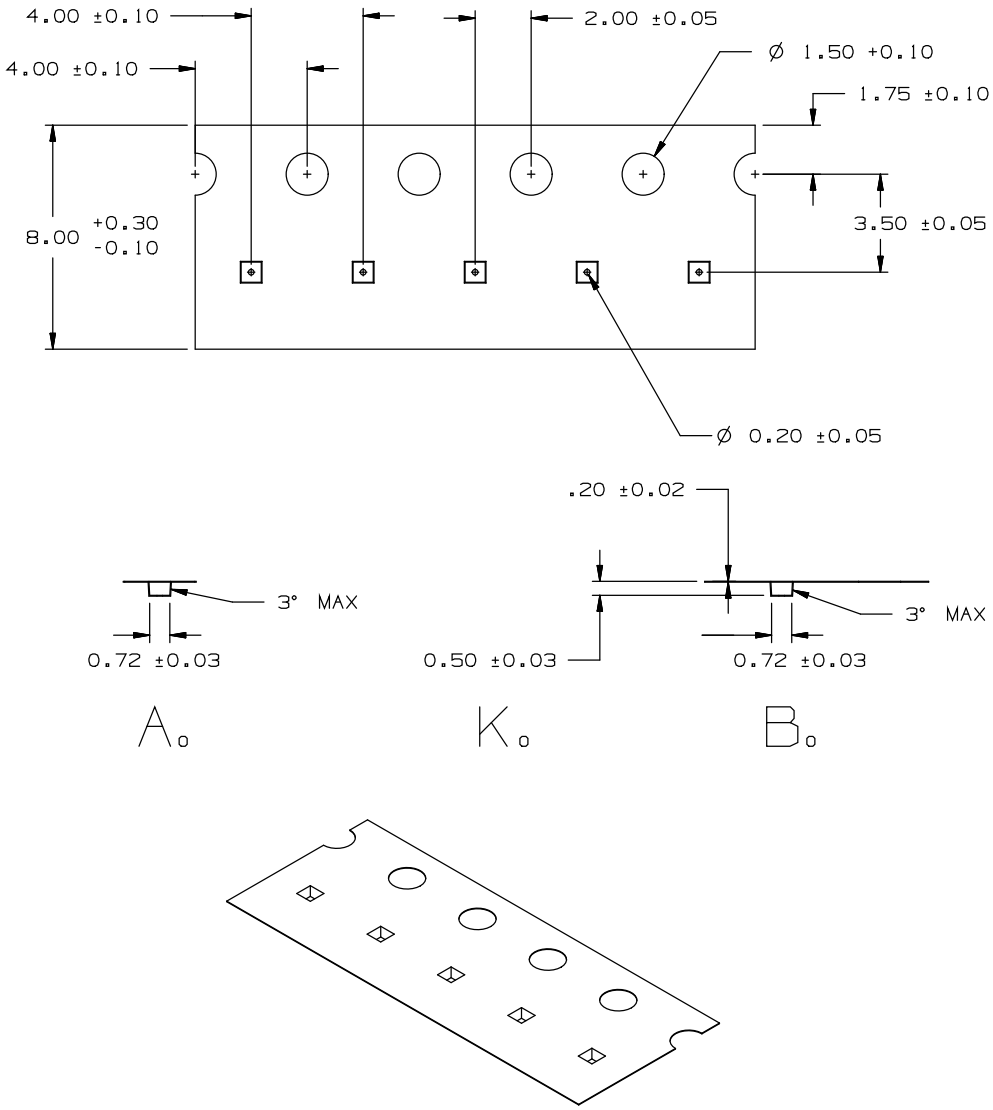
1. *Including back coating.*

Figure 31. Flip-Chip4 recommended footprint



7.2 Flip-Chip4_160304-47_carrier_tape

Figure 32. **Flip-Chip4 carrier tape**



7.3 DFN4-1x1 package info

Figure 33. **DFN4-1x1 package outline**

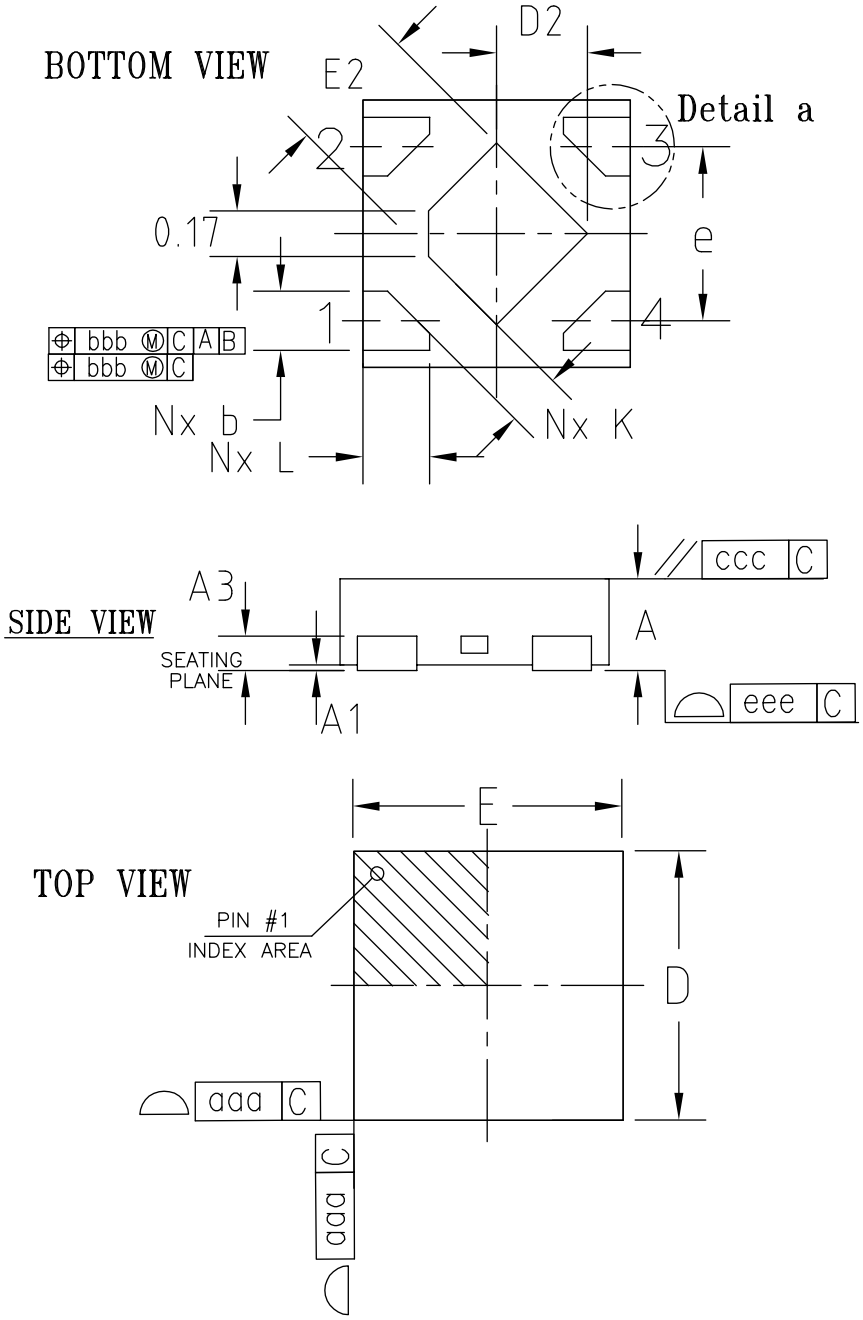
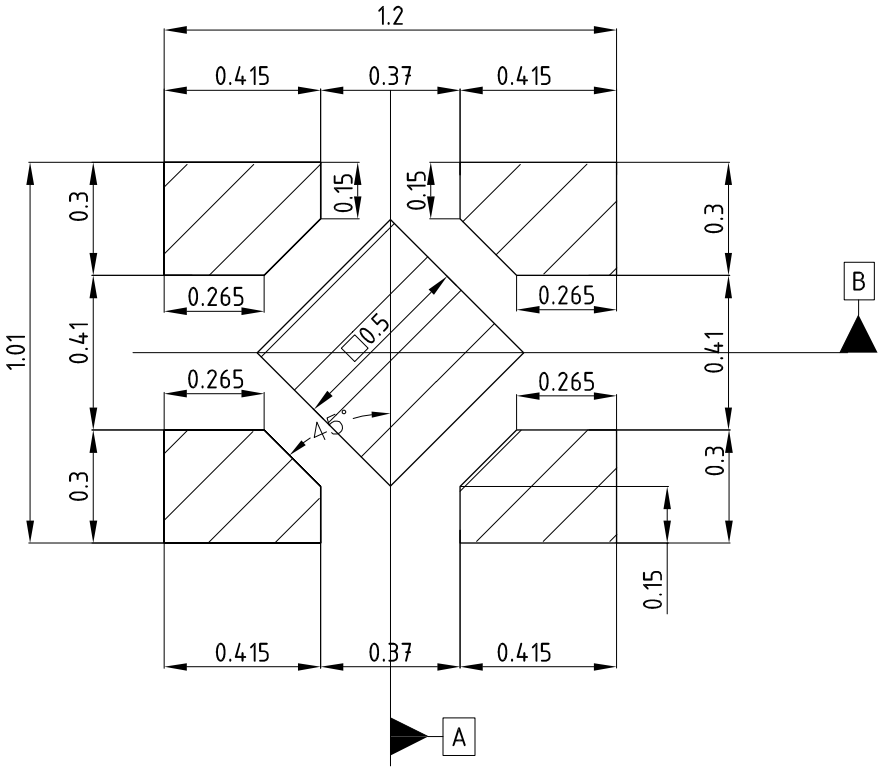


Table 7. **DFN4-1x1 package mechanical data**

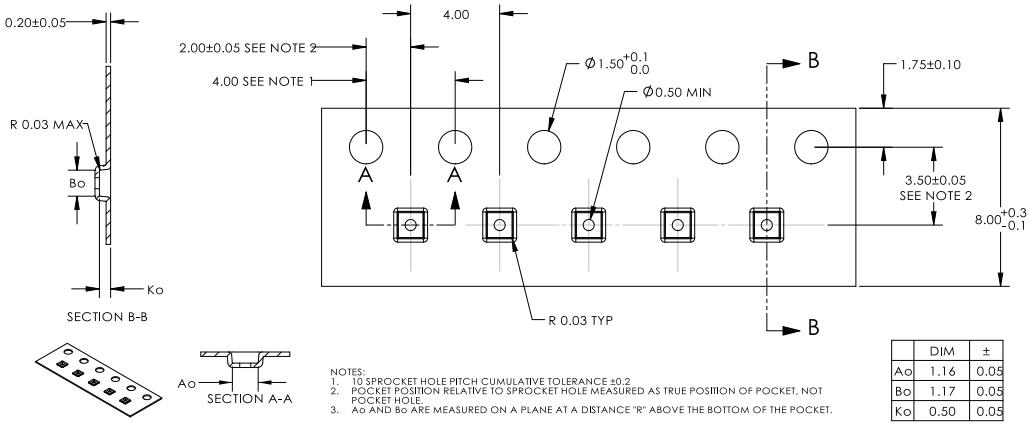
Dim.	mm		
	Min.	Typ.	Max.
A	0.34	0.37	0.40
A1	0.00	0.02	0.05
A3		0.127 REF.	
b	0.17	0.22	0.27
D	0.95	1.00	1.05
E	0.95	1.00	1.05
e		0.65 BSC	
D2	0.43	0.48	0.53
E2	0.43	0.48	0.53
K	0.15		
L	0.20	0.25	0.30
N		4	
ND		2	

Figure 34. **DFN4-1x1 recommended footprint**



7.4 DFN4_1x1x0.38_pitch_4mm_carrier_tape

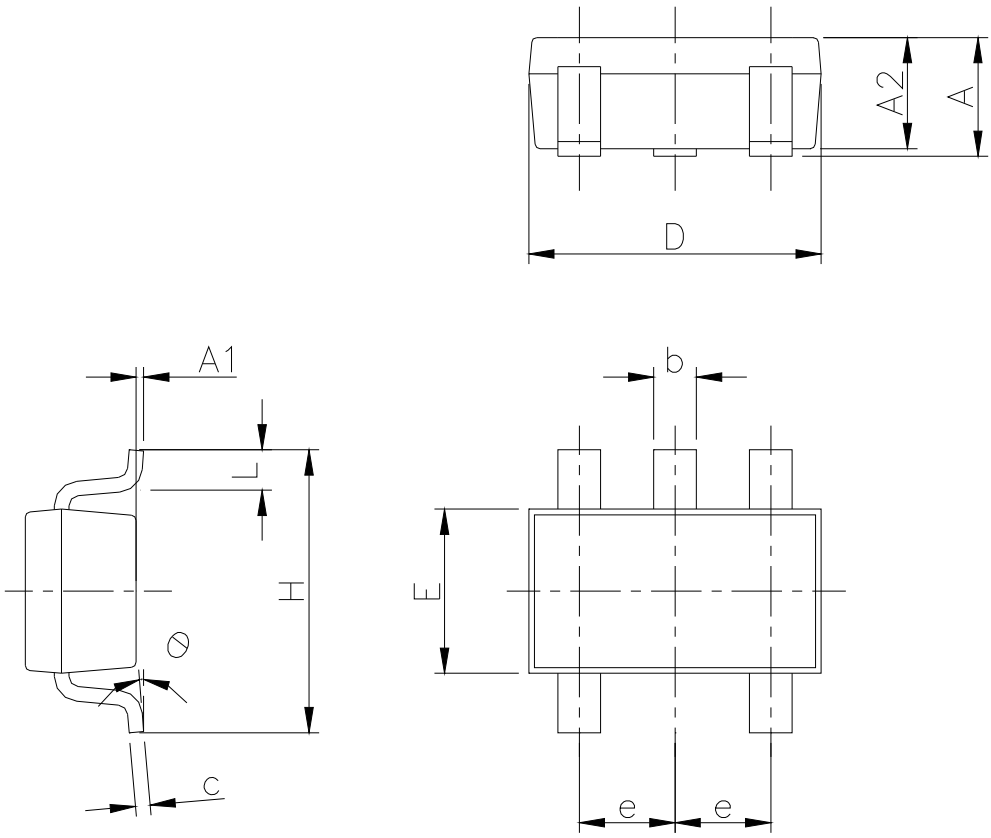
Figure 35. DFN4 (1x1x0.38 pitch 4 mm) carrier tape



	DIM	±
Ao	1.16	0.05
Bo	1.17	0.05
Ko	0.50	0.05

7.5 SOT23-5L mechanical data

Figure 36. **SOT23-5L package outline**

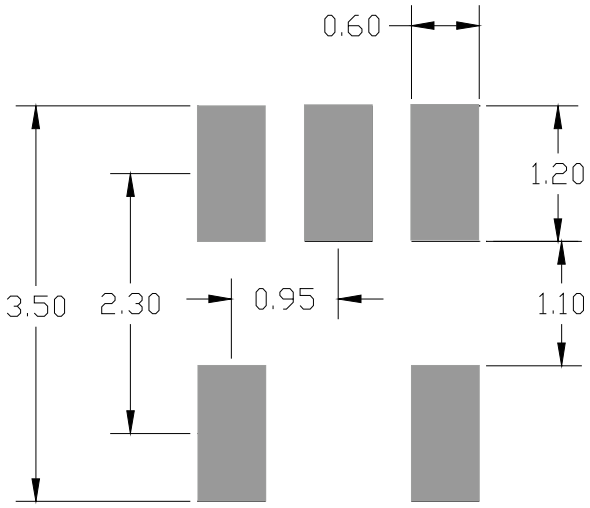


7049676_k

Table 8. **SOT23-5L package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.90		1.45
A1	0		0.15
A2	0.90		1.30
b	0.30		0.50
c	0.09		0.20
D		2.95	
E		1.60	
e		0.95	
H		2.80	
L	0.30		0.60
θ	0°		8°

Figure 37. **SOT23-5L recommended footprint**



Note: Dimensions are in mm

8 Ordering information

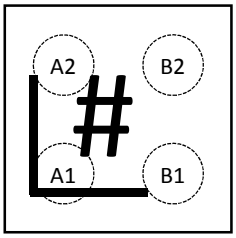
Table 9. **Order code**

Order code	Package	Output voltage (V)	Marking	Packing
LDLN025PU12R	DFN4-1x1	1.2	12	Tape and reel
LDLN025PU18R		1.8	18	
LDLN025PU25R		2.5	25	
LDLN025PU275R		2.75	2Z	
LDLN025PU28R		2.8	28	
LDLN025PU29R		2.9	29	
LDLN025PU30R		3.0	30	
LDLN025PU32R		3.2	32	
LDLN025PU33R		3.3	33	
LDLN025PU50R		5.0	50	
LDLN025J12R	Flip-Chip4	1.2	M	
LDLN025J18R		1.8	E	
LDLN025J25R		2.5	H	
LDLN025J28R		2.8	I	
LDLN025J29R		2.9	S	
LDLN025J2925R		2.925	K	
LDLN025J30R (1)		3.0	G	
LDLN025J32R		3.2	N	
LDLN025J33R		3.3	F	
LDLN025J50R		5.0	P	
LDLN025M12R	SOT23-5L	1.2	LN12	
LDLN025M15R		1.5	LN15	
LDLN025M18R		1.8	LN18	
LDLN025M25R		2.5	LN25	
LDLN025M28R		2.8	LN28	
LDLN025M30R		3.0	LN30	
LDLN025M33R		3.3	LN33	
LDLN025M45R		4.5	LN45	

1. *Part number in development. Contact our sales office.*

8.1 Marking information

Figure 38. **Flip-Chip marking composition (marking view)**



AMG260720161100MT

Note: the symbol # indicates the marking digit, as per Table 9. Order code.

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
03-Aug-2016	1	First release.
01-Sep-2016	2	Updated Table 8: “Order code”. Minor text changes.
24-Oct-2016	3	Updated Table 2: "Absolute maximum ratings". Minor text changes.
17-Nov-2016	4	Updated Section 9: “Ordering information”. Minor text changes.
12-Jul-2017	5	Added SOT23-5L package. Modified silhouette, features, Figure 1: "Block diagram", Section 2: "Pin configuration" and Table 4: "Electrical characteristics". Added Section 7.5: "SOT23-5L package information". Updated Table 9: "Order code". Minor text changes.
09-Oct-2018	6	Added Figure 21. PSRR vs. frequency (VOUT = 1.8 V), Figure 22. PSRR vs. frequency (VOUT = 5 V), new order codes LDLN025PU12R and LDLN025J29R in Table 9. Order code.
08-May-2019	7	Added footnote on A2 parameter in Table 6. Flip-Chip4 mechanical data..
16-Jul-2021	8	Update Figure 33. DFN4-1x1 package outline and Table 7. DFN4-1x1 package mechanical data

Contents

List of tables

List of figures

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