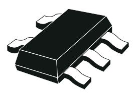
LDLN030

Datasheet

300 mA ultra low-noise LDO with Power Good and soft-start



TSOT23-5L

Features

- Ultra-low output noise: 7.5 μV_{RMS}
- Operating input voltage range: 1.6 V to 5.5 V
- Undervoltage lockout
- Output current up to 300 mA
- Very low quiescent current:16 µA at no-load
- Controlled Iq in dropout condition
- Very low dropout voltage: 100 mV at 200 mA, 150 mV at 300 mA
- Very high PSRR: 80 dB @ 100 Hz, 60 dB @ 100 kHz
- Output voltage accuracy: 2% across line, load and temperature
- Output voltage versions: from 1 V to 5 V, with 50 mV step
- Logic-controlled electronic shutdown
- Power Good
- Output discharge feature
- Internal soft-start to limit the in-rush current
- Overcurrent and thermal protections
- Temperature range: from -40 °C to +125 °C
- Package: TSOT23-5L

Maturity status link	
LDLN030	
Device summary	
Order code	LDLN030G33R
Package	TSOT23-5L
Output voltage	3.3 V
Marking	KN33
Packing	Tape and reel

Applications

- Smartphones/tablets
- Image sensors
- Instrumentation
- VCO and RF modules
- HDD and SSD
- Portable and other battery powered devices

Description

The LDLN030 is a 300 mA very low-dropout voltage regulator, able to work with an input voltage ranging from 1.6 V to 5.5 V.

The typical dropout voltage at 300 mA load is 150 mV.

The very low quiescent current, which is just 16 µA at no load, extends battery-life of applications requiring very long standby time.

Thanks to its ultra low-noise value and high PSRR the device provides a very clean output, suitable for ultra-sensitive loads. It is stable with ceramic capacitors.

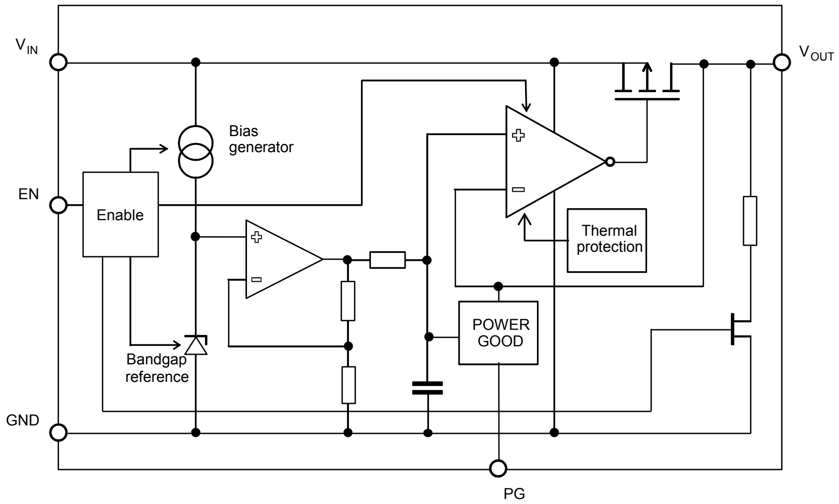
The enable logic control function puts the LDLN030 into shutdown mode allowing a total current consumption lower than 1 µA.

The device also includes short-circuit constant current limiting, undervoltage lockout, soft-start, Power Good and thermal protection.

Typical applications are noise sensitive loads such as ADC, VCO in mobile phones and tablets, wireless lan devices. The LDLN030 is designed to keep the quiescent current under control and at a low value also during dropout operation, helping to extend even more the operating time of battery-powered devices.

1 Diagram

Figure 2. Block diagram



2 Pin configuration

Figure 3. Pin connection (top view)

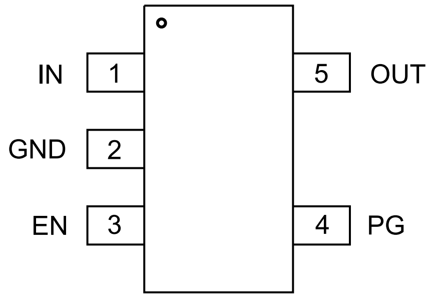
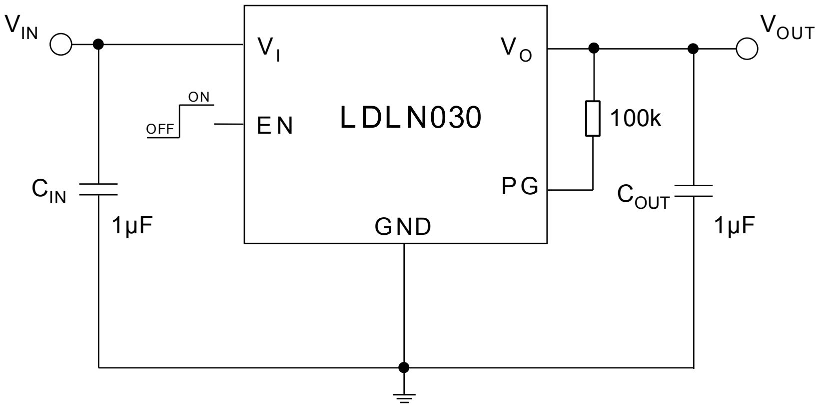


Table 1. Pin description

Symbol	TSOT23-5L	Description
V_{IN}	1	LDO supply voltage
V_{OUT}	5	LDO output voltage
GND	2	Ground
EN	3	Enable input: set V_{EN} = high to turn on the device; V_{EN} = low to turn off the device. Do not left floating.
PG	4	Power Good

3 Typical application diagram

Figure 4. Application diagram



4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input supply voltage	-0.3 to 7	V
V_{OUT}	Output voltage	-0.3 to V_{IN} + 0.3	V
I_{OUT}	Output current	Internally limited	A
EN	Enable pin voltage	-0.3 to V_{IN} + 0.3	V
P_D	Power dissipation	Internally limited	W
ESD	Charge device model	± 1000	V
	Human body model	± 2000	
$T_{J\text{-}OP}$	Operating junction temperature	- 40 to 125	°C
$T_{J\text{-}MAX}$	Maximum junction temperature	150	°C
T_{STG}	Storage temperature	- 55 to 150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	202	°C/W

5 Electrical characteristics

- 40 °C < T_J < 125 °C , typical values refer to T_J = 25 °C, $V_{IN} = V_{OUT (nom)}$ + 1 V or 1.6 V, whichever is greater; V_{EN} = 1.2 V; C_{IN} = 1 µF; C_{OUT} = 1 µF; I_{OUT} = 1 mA.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range	T_J = 25 °C	1.6		5.5	V
V_{UVLO}	Undervoltage lockout	V_{IN} rising	1.3	1.4	1.5	V
V_{OUT}	Output voltage accuracy (1)	V_{OUT} + 1 V < V_{IN} < 5.5 V,1 mA < I_{OUT} < 0.25 A, V_{OUT} ≥ 1.8 V	-2.0		+2.0	%
		V_{OUT} + 1 V < V_{IN} < 5.5 V, 1mA < I_{OUT} < 0.25 A, V_{OUT} < 1.8 V	-3.0		+3.0	
$\Delta V_{OUT} / \Delta V_{IN}$	Static line regulation (1)	V_{OUT} + 0.3 V < V_{IN} < 5.5 V;		300	1500	µV/V
	Line transient (2)	ΔV_{IN} = +/- 0.6 V, $t_{rise} = t_{fall}$ = 30 µs		+/-1		mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Static load regulation	0 mA < I_{OUT} < 0.2 A;		50	240	µV/mA
		1 mA < I_{OUT} < 0.3 A		0.002	0.007	%/mA
	Load transient (2)	I_{OUT} = 1 mA to 200 mA and back $t_{rise} = t_{fall}$ = 1 µs		+/-90		mV
V_{DROP}	Dropout voltage (3)	I_{OUT} = 0.1 A; V_{OUT} = 3.3 V		50		mV
		I_{OUT} = 0.2A; V_{OUT} = 3.3 V		100	180	
		I_{OUT} = 0.3 A; V_{OUT} = 3.3 V		150	230	
eN	Output noise voltage (2)	f = 10 Hz to 100 kHz; I_{OUT} = 1 mA		10		μV_{RMS}
		f = 10 Hz to 100 kHz; I_{OUT} = 0.2 A		7.5	20	
		f = 10 Hz to 100 kHz; I_{OUT} = 0.3 A		7.5		
SVR	Supply voltage rejection (2)	f = 100 Hz; I_{OUT} = 20 mA		80		dB
		f = 1 kHz ; I_{OUT} = 20 mA		80		
		f = 10 kHz ; I_{OUT} = 20 mA		75		
		f = 100 kHz ; I_{OUT} = 20 mA		60		
		f = 100 Hz; I_{OUT} = 150 mA		70		
		f = 1 kHz ; I_{OUT} = 150 mA		68		
		f = 10 kHz ; I_{OUT} = 150 mA		53		
I_Q	Quiescent current	I_{OUT} = 0 A, including enable current		16	30	µA
		I_{OUT} = 0.2 A		200	350	
		I_{OUT} = 0.3 A		240	360	
	Shutdown current	V_{EN} = 0 V		0.2	1	µA
I_{SC}	Short-circuit current	V_{OUT} = 0 V	300	500		mA
R_{LOW}	Output discharge resistance	V_{EN} = 0 V, de-assert V_{EN} from V_{EN_HI} to V_{EN_LO}		300	500	Ω
V_{EN}	V_{IL}, enable input logic low	V_{OUT} + 1 V (1) < V_{IN} < 5.5 V			0.4	V
	V_{IH}, enable input logic high		1.2			

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{EN}	Enable pin input current	V_{IN} = V_{EN} = 5.5 V (pull-down)		5		µA
t_{ON1}	Rise time (SS) (2)	I_{OUT} = 0 mA to 200 mA for V_{OUT} = 10% $V_{OUT(nom)}$ to 95% $V_{OUT(nom)}$		200		µs
t_{ON2}	Turn-on time (2)	I_{OUT} = 0 mA to 200 mA, from V_{EN} assertion to 95% of $V_{OUT(nom)}$		450	550	µs
T_{SHDN}	Thermal shutdown (2)	I_{OUT} > 1 mA	130	160	200	°C
	Hysteresis (2)			20		
V_{PG-}	Power Good threshold voltage	V_{OUT} decreasing	90	92	94	%V_{OUT}
V_{PG+}		V_{OUT} increasing	92	94	96	
PG_{HYS}	Power Good hysteresis	Measured at V_{OUT}		2		%V_{OUT}
PG_L	Power Good output low	De-assert V_{EN} from V_{EN_HI} to V_{EN_LO}		0.1	0.4	V
PG_{IL}	Power Good pin leakage current (2)	Measured at V_{OUT}		0.002	1	µA
PG_{RT}	Power Good reaction time (2)			2	10	µs
PG_{RD}	Power Good delay (2)			2	10	µs

1. *V_{IN} = V_{OUT} + 1 V or 1.6 V, whichever is greater. Not applicable for 5 V output voltage versions.*
2. *Performance guaranteed by design and/or characterization, and not production tested.*
3. *Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.*

Note: Performance guaranteed over the indicated operating temperature range by design and/or characterization, and/or production tested at T_J = T_A = 25 °C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

Table 5. Recommended input and output capacitors

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input capacitance	Stability	0.7	1		µF
C_{OUT}	Output capacitance		0.7	1	10	
ESR	Output/input capacitance		5		500	mΩ

6 Typical characteristics

The following plots are referred to LDLN030 in the typical application circuit and, unless otherwise noted, at T_A = 25°C.

Figure 5. Output voltage vs. temperature (V_{IN} = 4.3 V, I_{OUT} = 1 mA)

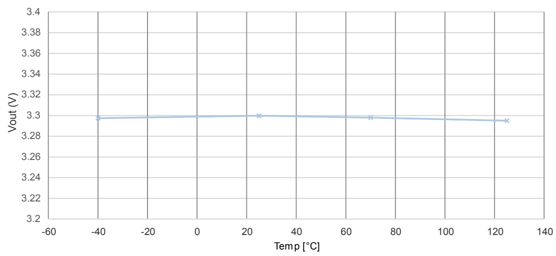


Figure 6. Output voltage vs. temperature (V_{IN} = 4.3 V, I_{OUT} = 300 mA)

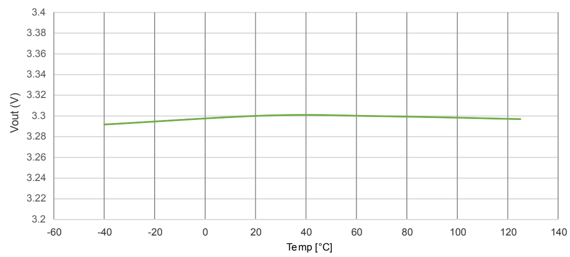


Figure 7. Load regulation vs. temperature (V_{IN} = 4.3 V, I_{OUT} from 1 mA to 300 mA)

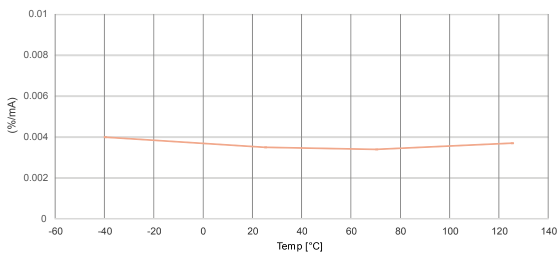


Figure 8. Line regulation vs. temperature (V_{IN} from 4.3 V to 5.5 V, I_{OUT} = 1 mA)

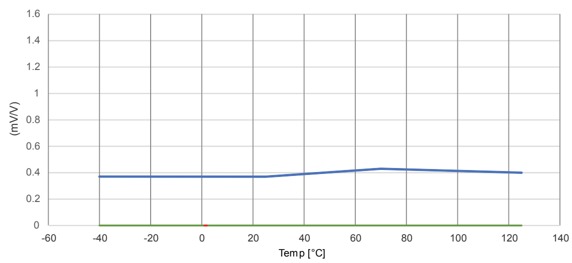


Figure 9. Quiescent current vs. temperature, (I_{OUT} = 0 mA)

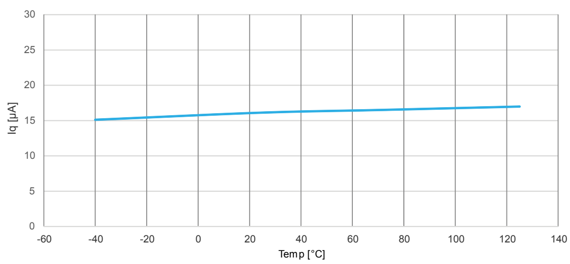
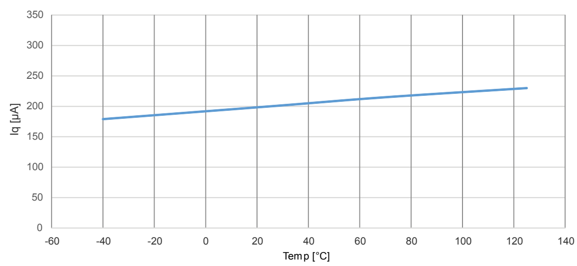


Figure 10. Quiescent current vs. temperature, (I_{OUT} = 200 mA)



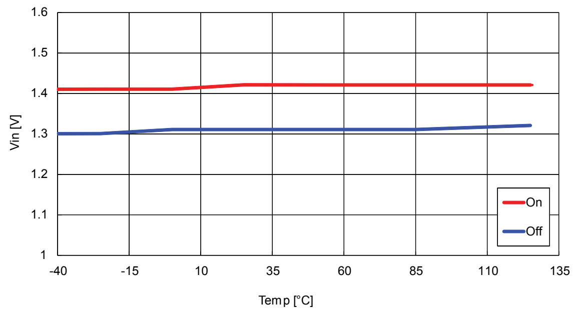


Figure 11. UVLO vs. temperature

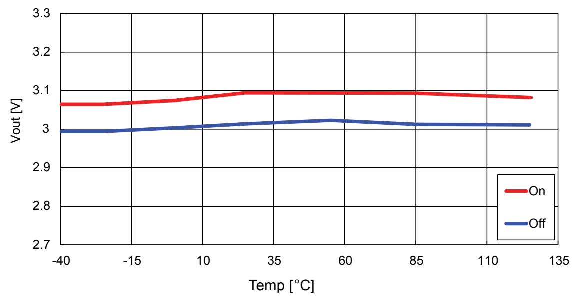


Figure 12. PG threshold vs. temperature

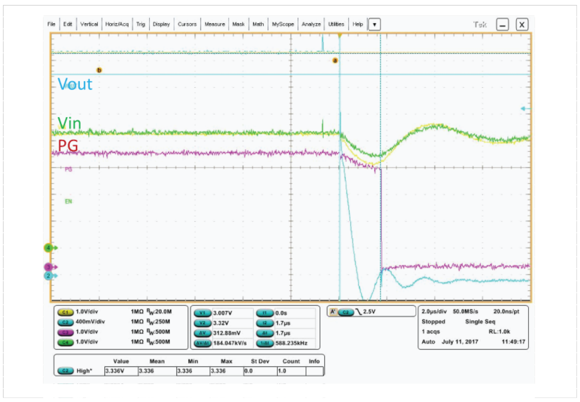


Figure 13. Power Good transient

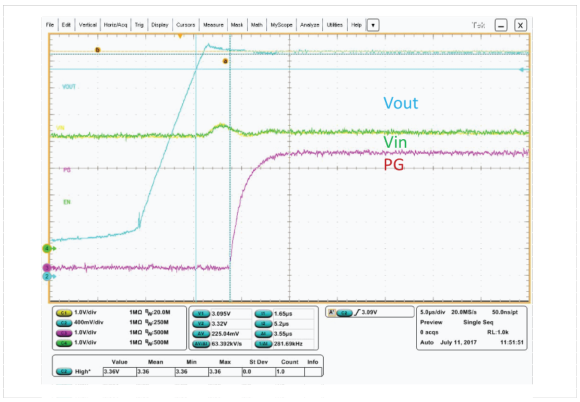


Figure 14. Power Good transient

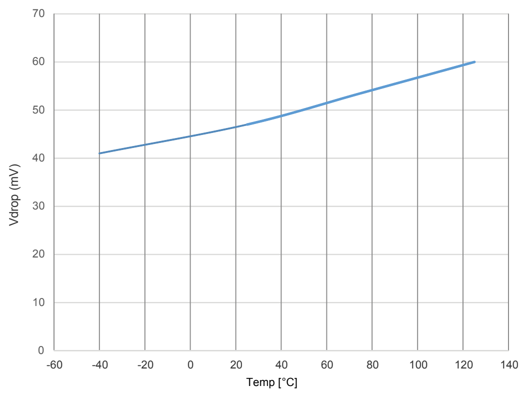


Figure 15. Dropout voltage vs. temperature I_{OUT} = 100 mA

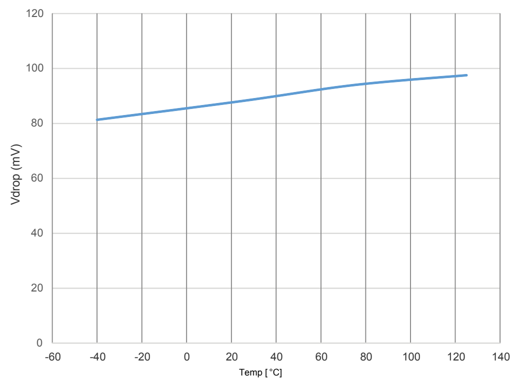


Figure 16. Dropout voltage vs. temperature I_{OUT} = 200 mA

Figure 17. Output voltage vs. input voltage

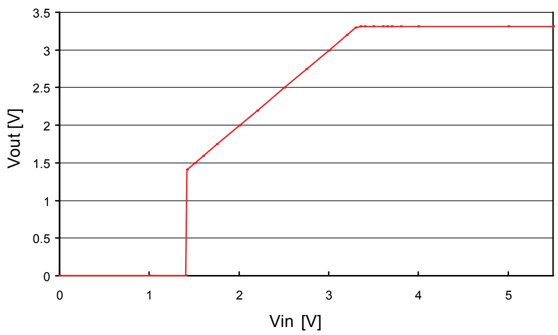


Figure 18. Short-circuit current vs. temperature

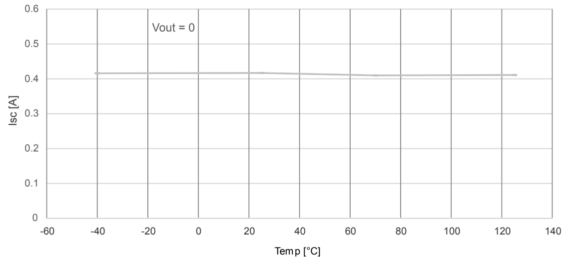


Figure 19. $R_{discharge}$ vs. temperature

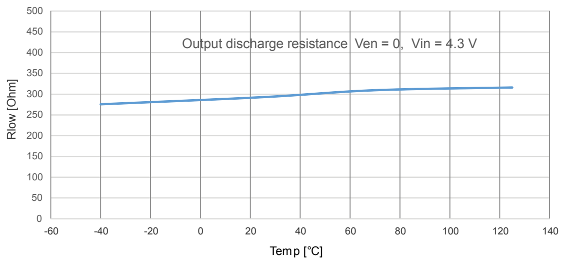


Figure 20. Stability region vs. C_{OUT} and ESR

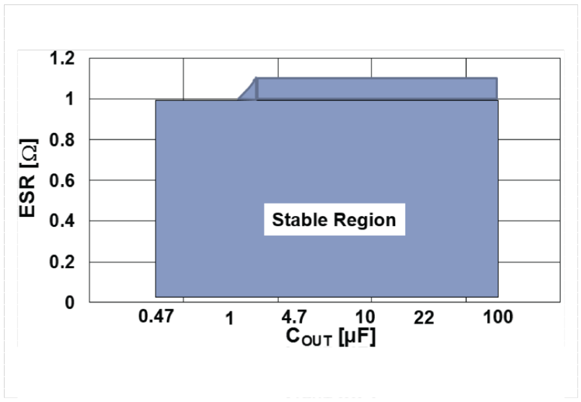


Figure 21. PSRR vs. frequency

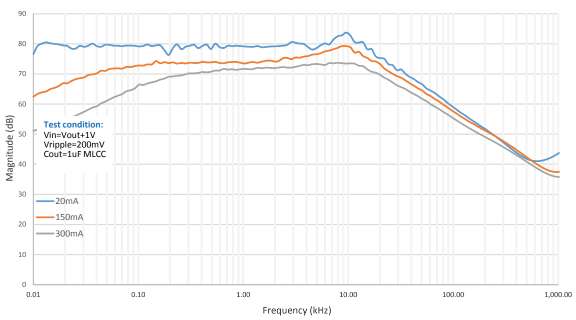


Figure 22. Noise density vs. frequency

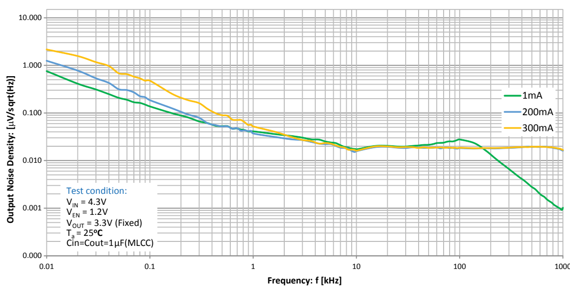


Figure 23. Line transient

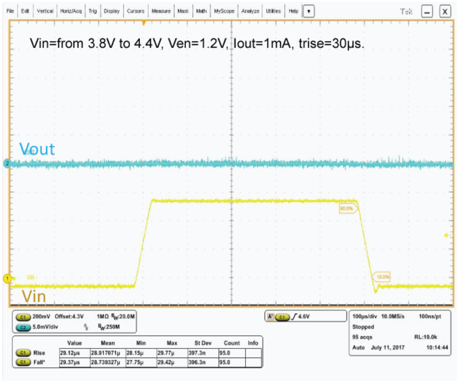


Figure 24. Load transient

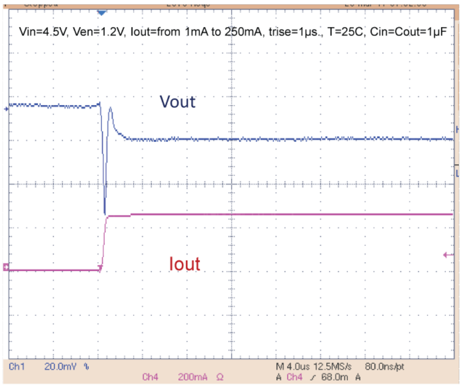


Figure 25. Load transient

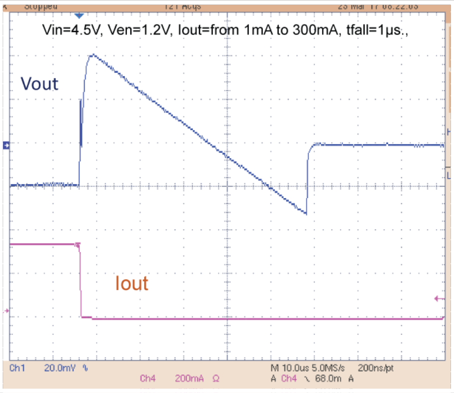


Figure 26. Inrush current

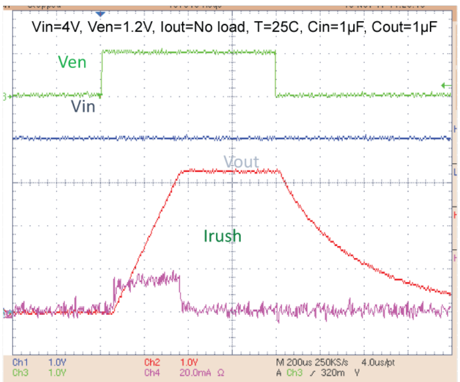


Figure 27. Enable transient

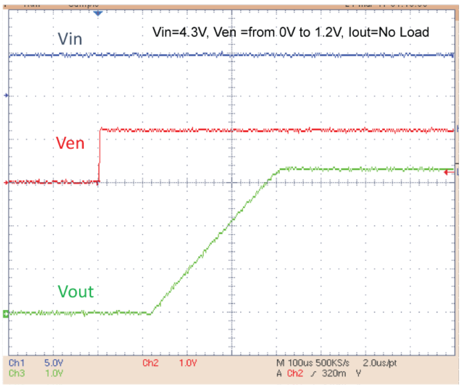
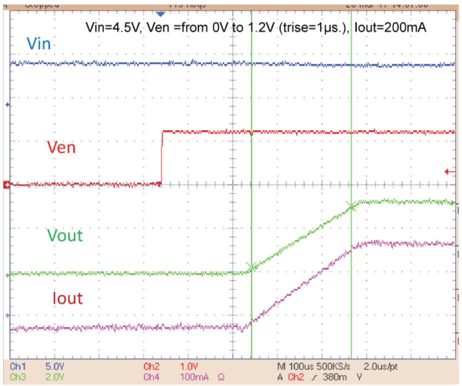


Figure 28. Enable transient



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 TSOT23-5L package information

Figure 29. TSOT23-5L package outline

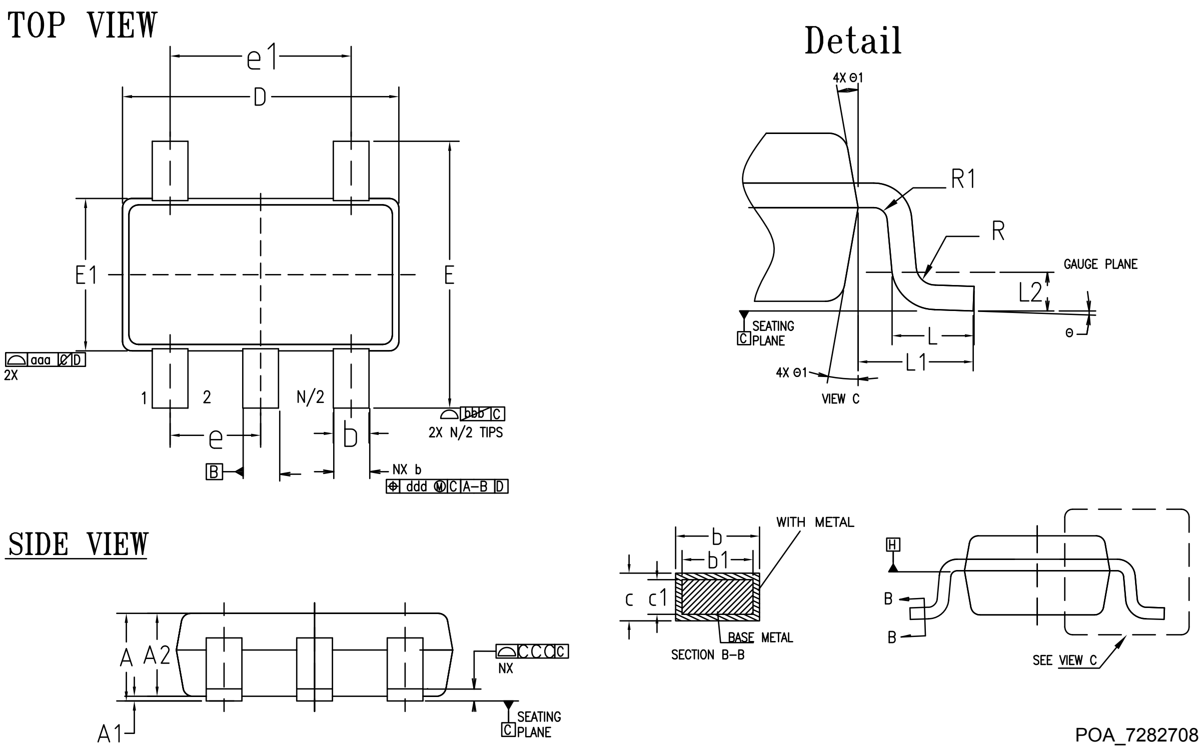


Table 6. TSOT23-5L mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.00
A1	0.01	0.05	0.10
A2	0.84	0.87	0.90
b	0.30		0.45
b1	0.31	0.35	0.39
e		0.95 BSC	
e1		1.90 BSC	
c	0.12	0.15	0.20
c1	0.08	0.13	0.16
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
L	0.30	0.40	0.50
L1		0.60 REF	
L2		0.25 BSC	

Dim.	mm		
	Min.	Typ.	Max.
R	0.10		
R1	0.10		0.25
ɵ	0°	4°	8°
ɵ1	4°	10°	12°
N	5		

Figure 30. **TSOT23-5L tape and reel drawing**

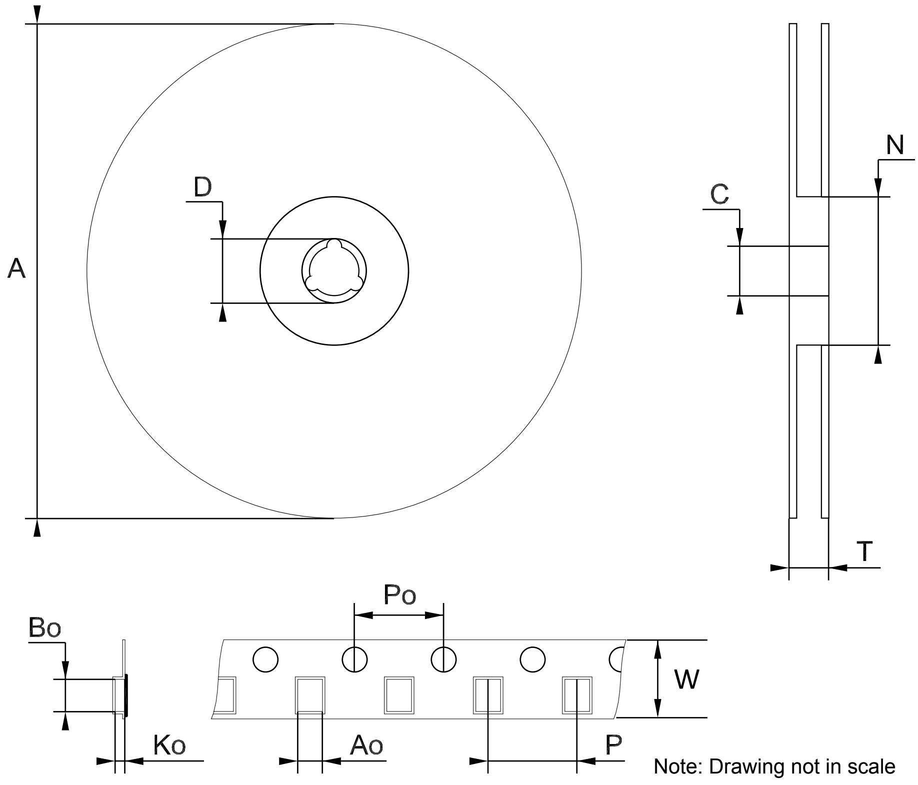
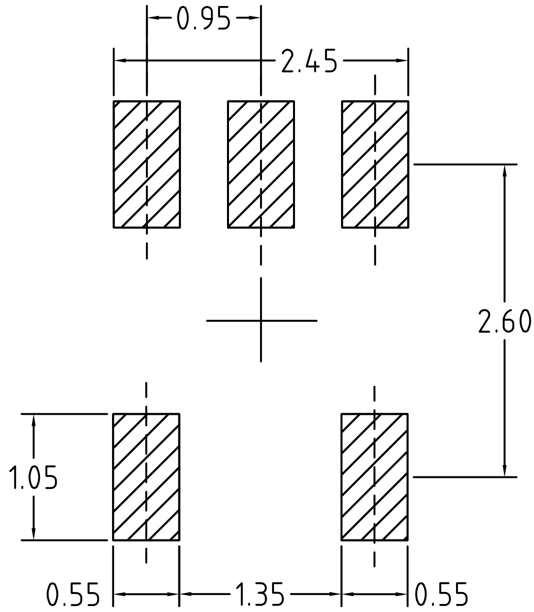


Table 7. **TSOT23-5L tape and reel**

Dim.	mm		
	Min.	Typ.	Max.
A			180
C	12.8	13.0	13.2
D	20.2		
N	60		
T			14.4
Ao	3.13	3.23	3.33
Bo	3.07	3.17	3.27
Ko	1.27	1.37	1.47

Dim.	mm		
	Min.	Typ.	Max.
Po	3.9	4.0	4.1
P	3.9	4.0	4.1
W		8.0	

Figure 31. TSOT23-5L footprint data (dimensions are in mm)



Revision history

Table 8. **Document revision history**

Date	Revision	Changes
08-Feb-2018	1	Initial release.

Contents

List of tables

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