LET9120

RF power transistor from the LdmoST family of n-channel enhancement-mode lateral MOSFETs

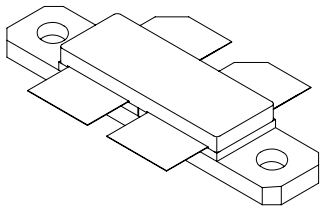
Preliminary data

Features

- Excellent thermal stability
- Common source configuration push-pull
- P_{OUT} = 120 W with 18 dB gain @ 860 MHz
- BeO-free package

Description

The LET9120 is a common source n-channel enhancement-mode lateral field-effect RF power transistor designed for broadband commercial and industrial applications at frequencies up to 1.6 GHz.



M246
Epoxy sealed

Figure 1. Pin connection

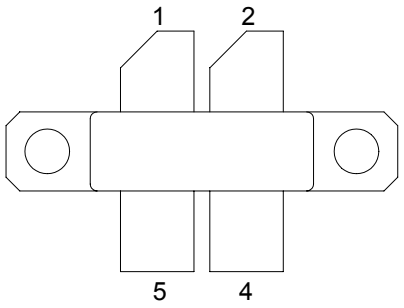


Table 1. Device summary

Order code	Package	Branding
LET9120	M246	LET9120

Contents

1 Electrical data

1.1 Maximum ratings

T_{CASE} = 25 °C

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	- 0.5 / + 15	V
I_D	Drain current	18	A
P_{DISS}	Power dissipation (@ T_C = 70 °C)	200	W
T_J	Max. operating junction temperature	200	°C
T_{STG}	Storage temperature	- 65 to + 150	°C

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.65	°C/W

2 Electrical characteristics

T_{CASE} = + 25 °C

2.1 Static

Table 4. Static (per section)

Symbol	Test conditions			Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	V_{GS} = 0 V	I_{DS} = 10 mA		80			V
I_{DSS}	V_{GS} = 0 V	V_{DS} = 28 V				1	µA
I_{GSS}	V_{GS} = 5 V	V_{DS} = 0 V				1	µA
$V_{GS(Q)}$	V_{DS} = 28 V	I_D = 100 mA		2.0		5.0	V
$V_{DS(ON)}$	V_{GS} = 10 V	I_D = 3 A			0.9	1.2	V
G_{FS}	V_{DS} = 10 V	I_D = 3 A		2.5			mho
C_{ISS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		58		pF
C_{OSS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		30		pF
C_{RSS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		0.7		pF

2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	V_{DD} = 32 V I_{DQ} = 400 mA P_{IN} = 2.5 W	120	150	-	W
G_{PS}	V_{DD} = 32 V I_{DQ} = 400 mA P_{OUT} = 150 W	16	18		dB
η_D	V_{DD} = 32 V I_{DQ} = 400 mA P_{OUT} = 150 W	60	70		%
Load Mismatch	V_{DD} = 32 V I_{DQ} = 400 mA P_{OUT} = 160 W @ 860 MHz All phase angles		20:1		VSWR

Table 6. Impedance data

Frequency Mhz	Z source Ω (As measured in the circuit gate to gate)	Z load Ω (As measured in the circuit drain to drain)
860	1.5 + j 2.2	6.2 + j 5.2

3 Typical performance

Figure 2. Gain & efficiency vs. output power

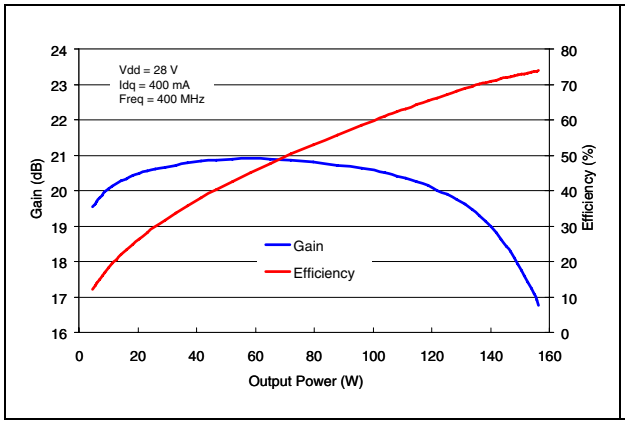


Figure 3. Gain vs. output power & bias current

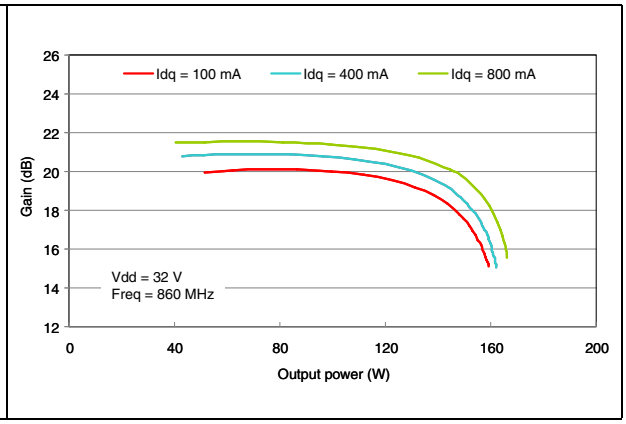


Figure 4. Output power & efficiency vs. input power

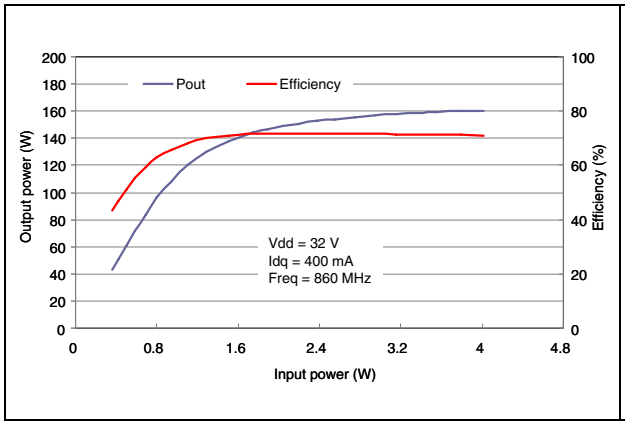
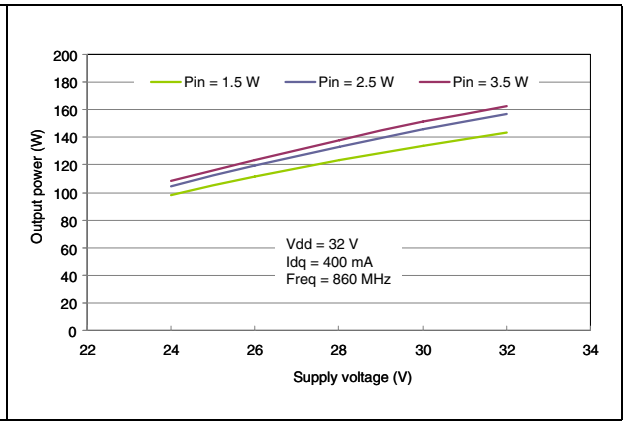


Figure 5. Output power vs. drain supply voltage



4 Test circuit

Figure 6. Test circuit schematic - 860 MHz

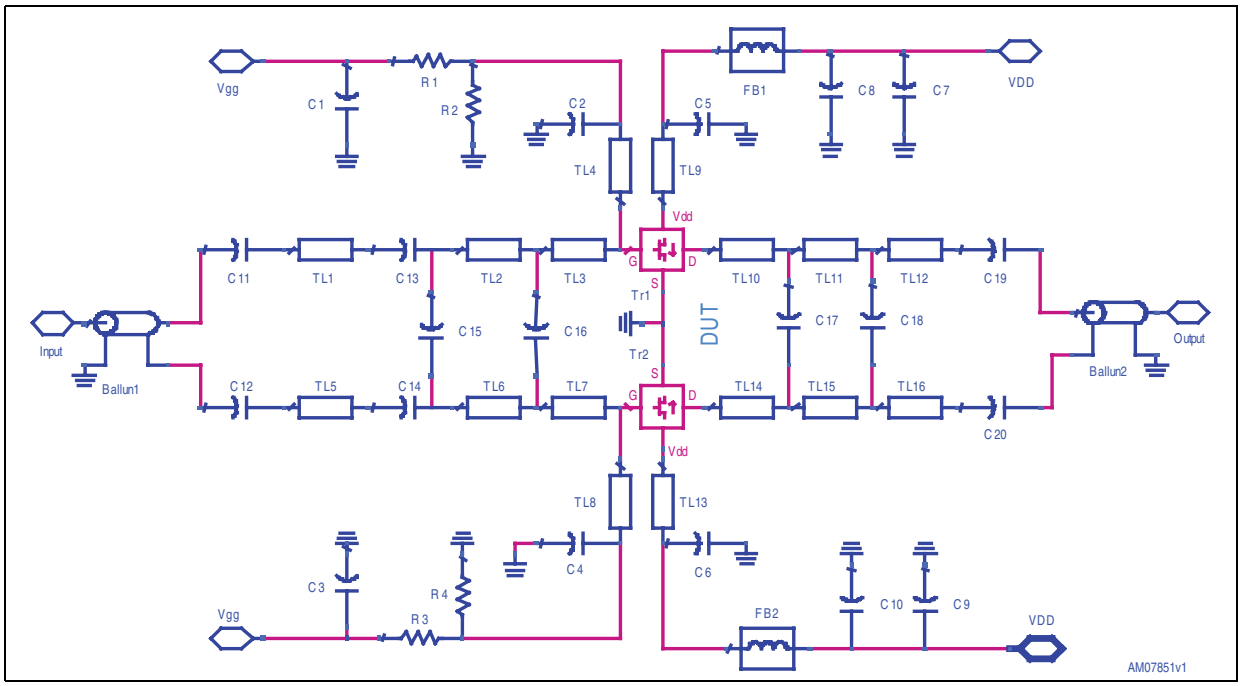


Table 7. Circuit component list

Item	Q.ty	Part number	Vender	Description
R1, R3	2	CR1206-8W-130JB	VENKEL	13 Ω, 1/8 W surface mount chip resistor
R2, R4	2	CR1206-8W-122JB	VENKEL	1.2 kΩ, 1/8 W surface mount chip resistor
R5, R6	2	CR1206-8W-250JB	VENKEL	25 Ω, 1/8 W surface mount chip resistor
B1, B2	2	2743021447	FAIR-RITE CORP	Surface mount EMI shield bead
C1, C3, C7, C9	4			100 µF, 63 V electrolytic capacitor
C2, C4, C5, C6	4	ATC100B910XXXX	ATC	91 pF chip capacitor
C8, C10	2	C1812X7R501-104KNE	VENKEL	0.1 F 500 V surface mount ceramic chip capacitor
C11, C12	2	ATC100B620XXXX	ATC	62 pF chip capacitor
C13, C14	2	ATC100B151XXXX	ATC	150 pF chip capacitor
C15	1	ATC100B110XXXX	ATC	11 pF chip capacitor
C16	1	ATC100B7R5XXXX	ATC	7.5 pF chip capacitor
C17	1	ATC100B1R1XXXX	ATC	1.1 pF chip capacitor
C18	1	27291PC	JOHANSON	0.8 - 8 pF giga trim variable capacitor

Table 7. Circuit component list (continued)

Item	Q.ty	Part number	Vender	Description
C19, C20	2	ATC100B101XXXX	ATC	100 pF chip capacitor
TL1, TL5				L= 0.250in [6.35mm] W=0.214in [5.44mm]
TL2, TL6				L= 0.182in [4.62mm] W=0.284in [7.21mm]
TL3, TL7				L= 0.318in [8.08mm] W=0.284in [7.21mm]
TL4, TL8, TL9, TL13				L= 2.37in [60.19mm] W=0.082in [2.08mm]
TL10, TL14				L= 0.314in [7.97mm] W=0.230in [5.84mm]
TL11, TL15				L= 0.460in [11.68mm] W=0.230in [5.84mm]
TL12, TL16				L= 0.280in [7.11mm] W=0.230in [5.84mm]
Board 3X5	1		Rogers Corp	Er=2.55 t=0.0026in h=0.030in

5 Package mechanical data

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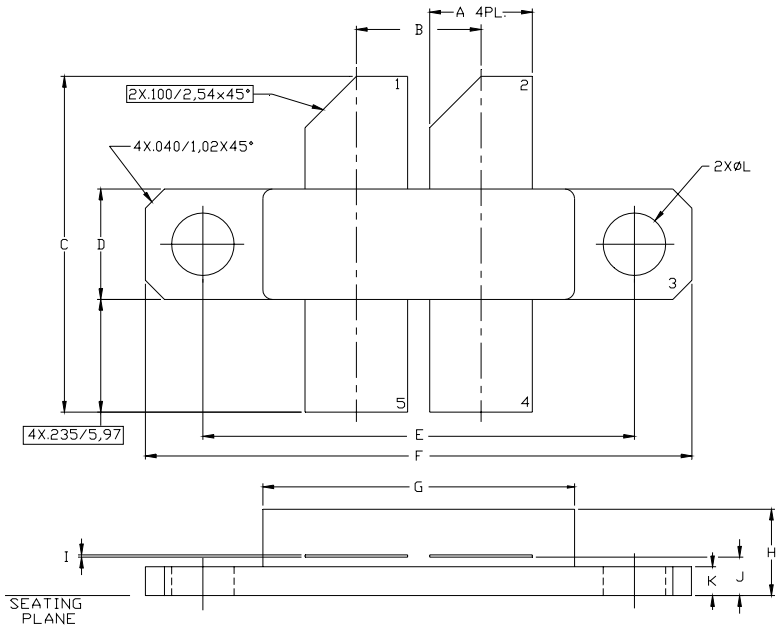
Table 8. M246 (0.230 x 0.650 WIDE 4/L BAL N/HERM W/FLG) mechanical data

Dim.	mm.			Inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	5.33		5.59	0.210		0.220
B	6.48		6.73	0.255		0.265
C	17.27		18.29	0.680		0.720
D	5.72		5.97	0.225		0.235
E		22.86			.900	
F	28.83		29.08	1.135		1.145
G	16.26		16.76	0.640		0.660
H	4.19		5.08	0.165		0.200
I	0.08		0.15	0.003		0.006
J	1.83		2.24	0.072		0.088
K	1.40		1.65	0.055		0.065
L	3.18		3.43	0.125		0.135

Figure 7. Package dimensions



Controlling dimension: Inches

Ref. 7145054A

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
10-Mar-2009	1	First Issue.
22-Jul-2009	2	Updated document's title.
18-Nov-2009	3	Updated V_{GS} in *Table 2*.
11-Feb-2010	4	Changed test condition for $V_{(BR)DSS}$ in *Table 4: Static (per section)*.
22-Oct-2010	5	Added: *Typical performance on page 5* and *Test circuit on page 6*.

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