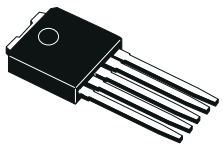
LNBP8L, LNBP9L
LNBP10L, LNBP11L

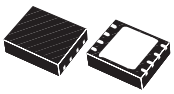
LNB supply and control voltage regulator

Features

- Simplest integrated solution for LNB remote supply and control
- 500 mA guaranteed output current
- Dual input supply for reducing power dissipation (DFN package)
- 3-state function to enable/disable and select the output voltage level through a single pin
- Fast oscillator startup for DiSEq™ encoding (LNBP9L/11L versions)
- External 22 kHz modulation input pin (LNBP8L/10L versions)
- Cable length compensation, LLC pin (LNBP10L, LNBP11L versions)
- Short-circuit and over-temperature protection
- LNB overload and short-circuit dynamic protection (LNBP10L, LNBP11L versions)
- Available in DFN8 (5 x 6 mm) and IPPAK packages



IPPAK



DFN8 (5 x 6 mm)

Description

Intended for analog and digital satellite receivers, the LNBP is a monolithic linear voltage regulator, assembled in the DFN8 (5 x 6) and IPPAK packages, specifically designed to provide the powering voltages and the interfacing signals to the LNB down-converter. The regulator output can be logic controlled for 13 V or 18 V (typ.) by means of the EN/VSEL 3-state pin for remotely controlling the LNB. When the IC is powered and put in standby (EN/VSEL pin at high impedance), the regulator output is disabled. In order to reduce power dissipation, the LNBP10L/11L versions (on DFN package) feature 2 supply inputs: V_{CC1} and V_{CC2}. These pins must be powered, respectively, at 15 V (min.) and 22 V (min.), and an internal switch will automatically select the appropriate supply voltage according to the selected output voltage. The LNBP8L/9L versions (in the IPPAK package) have only one supply input pin, which must be supplied at 22 V (min.). Additionally, the LNBP10L/11L versions have the LLC pin to increment the selected output voltage value by 1 V (typ.) to compensate for the excess voltage drop along the coaxial cable (LLC pin HIGH). An analog 22 kHz modulation input pin (EXTM) is available in the LNBP8L and LNBP10L versions. An appropriate DC blocking capacitor must be used to couple the modulating signal source to the EXTM pin. The LNBP10L/11L versions are also equipped with over-current dynamic protection: as soon as an overload is detected the output is shut down for the time T_{OFF}, which is determined by the capacitor connected between the CEXT pin and GND. After the time has elapsed, the output is resumed for a time $T_{ON} = (1/12)*T_{OFF}$ (typ.). If the overload is still present, the protection circuit will cycle again through T_{OFF} and T_{ON} until the overload is removed. A typical $T_{ON}+T_{OFF}$ value is 1100 ms when a 4.7 µF external capacitor is used on the C_{EXT}. This dynamic operation can greatly reduce the power dissipation in short-circuit condition, while ensuring excellent power-on startup even with highly capacitive loads on the LNB outputs. The device is packaged in the IPPAK for through-hole mounting and in the DFN8 (5 x 6) for surface mounting. Both package solutions are offered in two versions: with ten pins (LNBP9L/11L) to use with the integrated 22 kHz tone generator, or with the EXTM pin (LNBP8L/10L) to use external 22 kHz sources. All versions have built-in thermal protection to prevent overheating damage.

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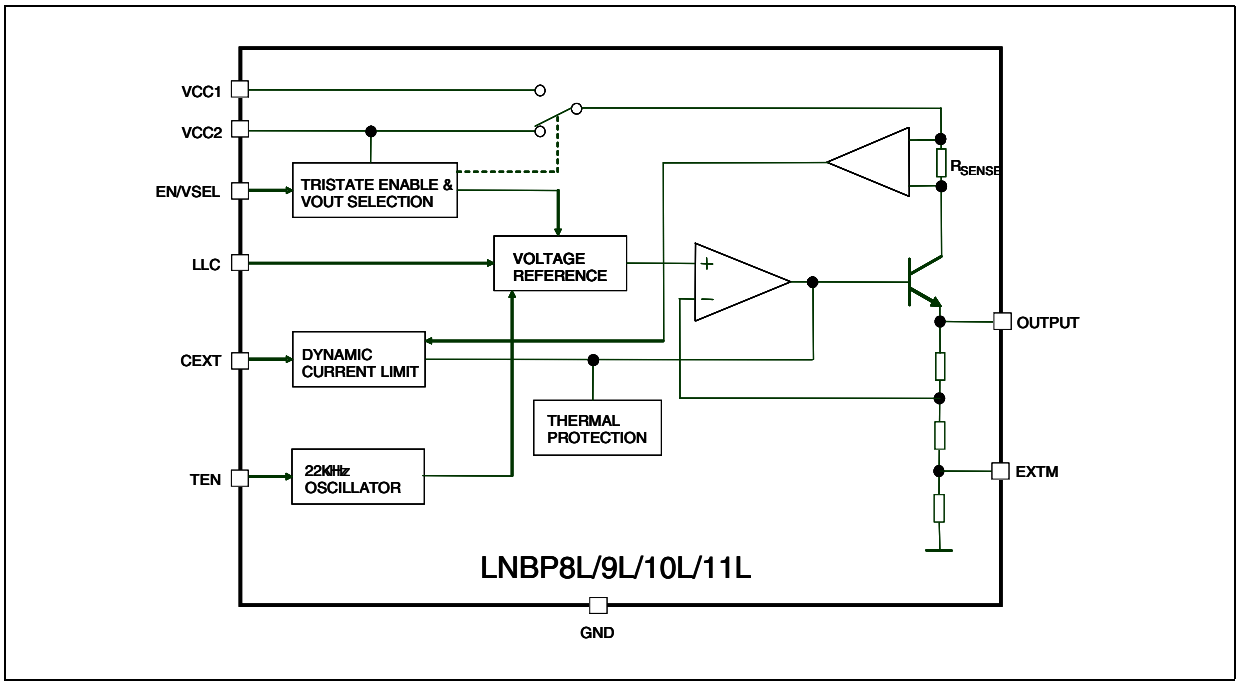
1 Diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin connections (top view for IPPAK, bottom view for DFN8)

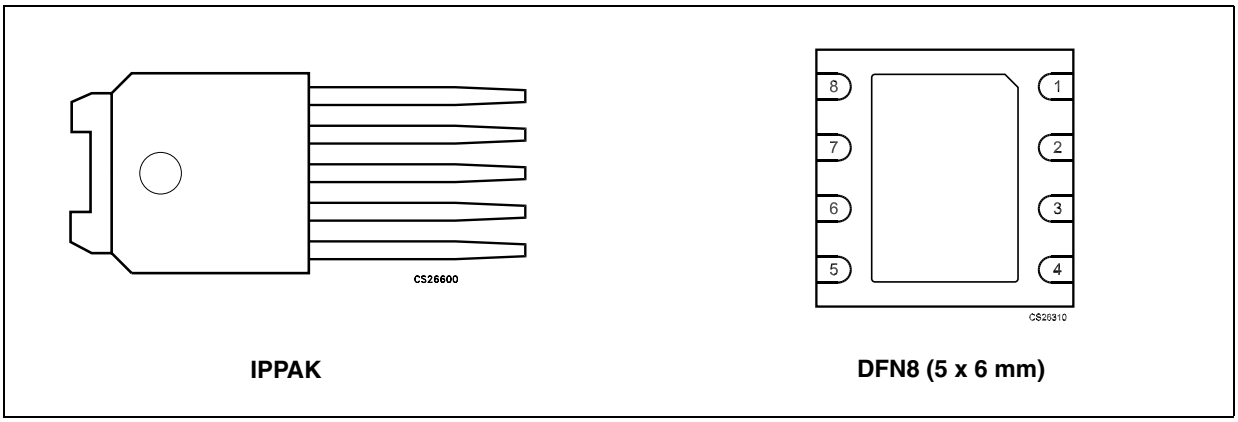


Table 1. Pin description

Pin n° (DFN) LNBP10/11L	Pin n° (IPPAK) LNBP8/9L	Name	Pin function
1	-	VCC1 (not available for IPPAK)	**Supply input 1:** 15 V to 25 V supply. For DFN package it is automatically selected when V_{OUT} = 13 V. For IPPAK package V_{CC1} and V_{CC2} are internally connected together to pin 1 to be supplied at 22 V min.
2	1	VCC2 (V_{CC} pin for IPPAK)	**Supply input 2:** 22 V to 25 V supply. For DFN package it is automatically selected when V_{OUT} = 18 V. For IPPAK package V_{CC1} and V_{CC2} are internally connected together to the pin 1 to be supplied at 22 V min.
3	2	OUTPUT	**Output:** regulator output. It is 13 V typ when EN/VSEL LOW and 18 V typ when EN/VSEL HIGH.
4, ePAD	3, ePAD	GROUND	GROUND
6	4	EN/VSEL	**Enable and output voltage selection 3-state pin:** logic control input 3-state pin for the remote controlling of the LNB; if LOW V_{OUT} = 13 V, when HIGH V_{OUT} = 18 V, if left at high impedance the IC is set in shut down mode (V_{OUT} = 0 V)
5	5	EXTM/TEN	**Tone enable (LNBP9-11):** logic control input to enable internal tone generator. **External modulation (LNBP8-10):** Needs DC decoupling to the AC source. If not used can be left floating.
8	NA	LLC	**LLC:** logic control input to add 1 V typ.
7	NA	C_{EXT}	**C_{EXT}:** timing capacitor used by the dynamic overload protection. Typical application is 4.7 µF for a 1100 ms cycle

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC1, VCC2	Input voltages	-0.3 to 28	V
VCC1-OUTPUT	VCC1 voltage with respect to OUTPUT voltage (1)	-0.3 to 25	V
VCC2-OUTPUT	VCC2 voltage with respect to OUTPUT voltage (1)	-0.3 to 25	V
EN/VSEL, TEN, LLC	Logic input voltage	-0.3 to 7	V
EXTM	External modulation input voltage	-0.3 to 1	V
OUTPUT	Output voltage	-0.3 to 25	V
T_{STG}	Storage temperature range	-50 to 150	°C
ESD DFN package	ESD rating with human body model (HBM) for all pins except 1, 2, 6	2	kV
	ESD rating with human body model (HBM) for pins 1, 2, 6	1.5	
ESD IPPAK package	ESD rating with human body model (HBM) for all pins except 1, 4	2	kV
	ESD rating with human body model (HBM) for pins 1, 4	1.5	

1. Exposure beyond the VCC1 and VCC2 with respect to OUTPUT absolute-maximum-rated voltages during OUTPUT pin overload or short-circuit to GROUND may cause permanent damage to the device.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to network ground terminal unless otherwise stated.

Table 3. Operating ratings

Symbol	Parameter	Value	Unit
T_J	Operating junction temperature range	0 to 125	°C
VCC1	Input voltage	15 to 25	V
VCC2	Input voltage	22 to 25	V

Table 4. Thermal data

Symbol	Parameter	IPPAK	DFN8	Unit
R_{thJA}	Thermal resistance junction-ambient		35 (mounted on PCB 2s2p)	°C/W
R_{thJC}	Thermal resistance junction-case	8		°C/W

4 Electrical characteristics

Refer to the typical application circuits in *Figure 3* and *Figure 4*, V_{CC1} = 16 V, V_{CC2} = 23 V (1), EN/VSEL = LOW, TEN = LLC = LOW, EXTM = FLOATING, I_{OUT} = 50 mA, T_J = 0 °C to 85 °C, unless otherwise stated. Typical values are referred to T_J = 25 °C.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC1}	V_{CC} supply input 1 (1)	I_{OUT} = 500 mA, TEN=HIGH, EN/VSEL=LOW, LLC=LOW	15		25	V
		I_{OUT} = 500 mA, TEN=HIGH, EN/VSEL=LOW, LLC= HIGH	16		25	
V_{CC2}	V_{CC} supply input 2 (1)	I_{OUT} = 500 mA, TONE=HIGH, EN/VSEL=HIGH, LLC=LOW	22		25	V
		I_{OUT} = 500 mA, TONE=HIGH, EN/VSEL=HIGH, LLC= HIGH	23		25	
V_{OUT}	Output voltage	I_{OUT} = 500 mA, EN/VSEL=LOW	12.5	13.25	14	V
		I_{OUT} = 500 mA, EN/VSEL=HIGH	17	18	19	V
		I_{OUT} = 500 mA, EN/VSEL=LOW, LLC=HIGH (2)		14.25		V
		I_{OUT} = 500 mA, EN/VSEL=LLC=HIGH (2)		19		V
ΔV_{OUT}	Line regulation (1)	V_{CC1} from 15 V to 18 V, EN/VSEL=LOW or HIGH		5	40	mV
ΔV_{OUT}	Load regulation	V_{CC1} = V_{CC2} = 22 V, I_{OUT} from 50 mA to 500 mA, EN/VSEL=LOW or HIGH		50	150	mV
I_{MAX}	Output current limiting		550	700	850	mA
F_{TONE}	Tone frequency	TEN=High	20	22	24	kHz
A_{TONE}	Tone amplitude	TEN=High	0.4	0.65	0.9	V_{PP}
D_{TONE}	Tone duty cycle	TEN=High	40	50	60	%
t_r, t_f	Tone Rise and Fall Time	TEN=High (3)	5	10	15	µs
G_{EXTM}	External modulation Gain	$\Delta V_{OUT}/\Delta V_{EXTM}$, freq. from 10 kHz to 40 kHz	4.5	5.5	6.5	
V_{EXTM}	External modulation input voltage	AC Coupling			400	mV_{PP}
Z_{EXTM}	External modulation impedance	Freq. from 10 kHz to 40 kHz		400		Ω
V_{ILT}	Control input logic LOW threshold for 3-state pin	EN/VSEL	0.8	1	1.2	V
V_{IHT}	Control input logic HIGH threshold for 3-state pin	EN/VSEL	1.8	2	2.2	V
I_{IHT}	3-state control pin input current HIGH	V_{IHT} = 5 V, EN/VSEL		-400		µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ILT}	3-state control pin input current LOW	V_{ILT} = 0 V, EN/VSEL		+180		µA
V_{IL}	Control input logic LOW	TEN, LLC			0.8	V
V_{IH}	Control input logic HIGH	TEN, LLC	2.5			V
I_{IH}	Control pins input current	V_{IH} = 5 V, TEN, LLC		20		µA
I_{CC}	Supply current	Output disabled EN/VSEL=High impedance (floating)		1.7	2.4	mA
		Output enabled EN/VSEL=HIGH, TEN=HIGH, I_{OUT} = 500 mA		3.7	6.3	mA
T_{OFF}	Dynamic overload protection OFF time	Output shorted, C_{EXT} = 4.7 µF (2)		1000		ms
T_{ON}	Dynamic overload protection ON time	Output shorted, C_{EXT} = 4.7 µF (2)		T_{OFF} /12		ms
I_{OBK}	Output backward current	Output forced to 21 V		6		mA
T_{SHDN}	Thermal shutdown threshold			165		°C
ΔT_{SHDN}	Thermal shutdown hysteresis			25		°C

1. For IPPAK package V_{CC1} and V_{CC2} are internally connected to the pin 1 (V_{CC}) to be supplied in the range from 22 V up to 25 V
2. Only DFN package
3. Guaranteed by design

5 Typical application circuits

Figure 3. Single input supply voltage solution for IPPAK package versions

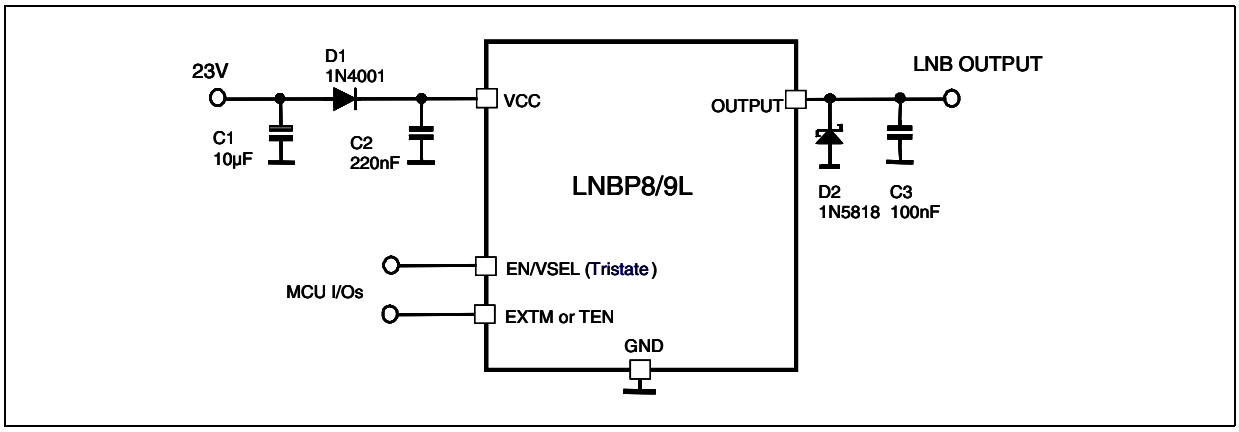


Figure 4. Dual input supply voltage solution for DFN8 (5 x 6 mm) package versions

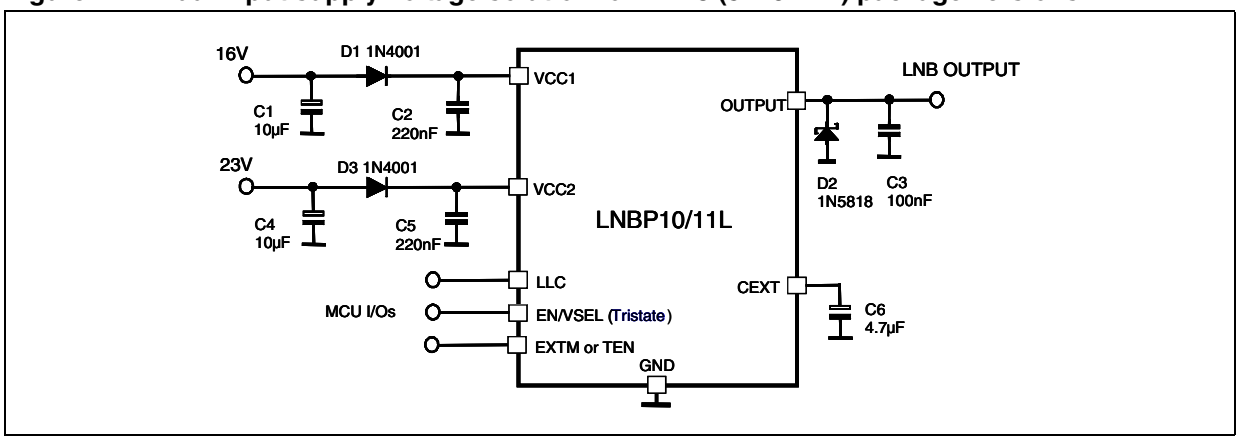
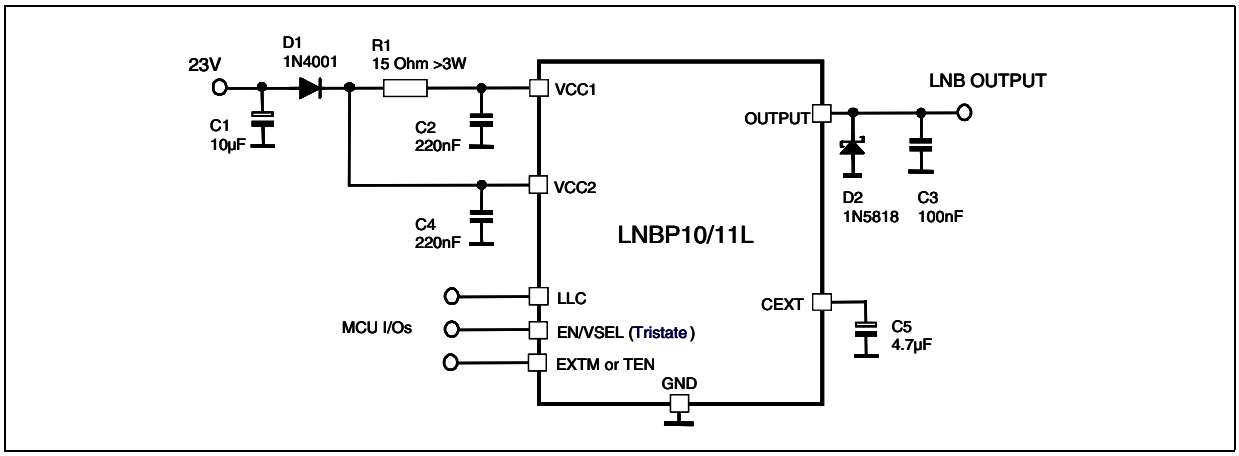


Figure 5. Single input supply voltage solution for DFN8 (5 x 6 mm) package versions



Note: In a single supply configuration with the DFN package, an R_1 resistor in the 12-15 Ω range is recommended to reduce device power dissipation during the 13 V output condition. The resistor can be omitted, but the power dissipation will increase.

6 Detailed description and application hints

The LNBPxx is made up of several functional blocks (see *Figure 1 on page 3*), as described below:

1. The oscillator is activated by setting the ENT pin (enable tone) = H, and is factory-trimmed at 22 kHz ± 2 kHz, eliminating the need to use external trimming. The rising and falling edges are maintained in the 5 to 15 µs range (10 µs typ.), to avoid RF pollution of the receiver. The duty cycle is 50% typ. It modulates the DC output with a ± 0.325 V typ. amplitude and 0 V average. The presence of this signal usually gives the LNB information about the band to be received.
2. The 3-state enable & V_{OUT} selection block, selects the two output voltages or sets the IC to shutdown mode, depending on the voltage applied on the EN/VSEL pin.
   When EN/VSEL is set high (EN/VSEL > 2.2 V), an 18 V output voltage is selected; when the EN/VSEL is set low (EN/VSEL < 0.8 V), a 13 V output voltage is selected.
   If the EN/VSEL pin is left floating (high impedance) or if the pin is set in a range from 1.2 V to 1.8 V (1.5 V typ.), the IC goes into shutdown mode and the output voltage will be set to 0 V.
   This feature changes the LNB polarization type. The LNB switches to horizontal or vertical polarization depending on the supply voltage it gets from the receiver.
3. For the DFN package, in order to keep the power dissipation of the device as low as possible, the input selector automatically selects V_{CC1}; that is, the lowest input voltage, when 13 V output is selected (i.e. EN/VSEL is low). If the 18 V output is selected (i.e. EN/VSEL is high), the V_{CC2} input pin is selected. For example, power dissipation at I_{OUT} = 350 mA is:

P_D = (23 - 18) x 0.35 = 1.75 W

with V_{CC2} = 23 V (voltage on the V_{CC2} pin) and V_{OUT} = 18 V, and

P_D = (16 - 13) x 0.35 = 1.05 W

with V_{CC1} = 16 V (voltage on the V_{CC1} pin) and V_{OUT} = 13 V

For IPPAK package, V_{CC1} and V_{CC2} are internally connected and must be supplied from a single input voltage line (22 V min.) to the V_{CC} pin. In this case the worst case power dissipation is 13 V output. For example: at I_{OUT} = 350 mA and V_{CC} = 23 V (voltage on the V_{CC} pin):

P_D = (23 - 13) x 0.35 = 3.5 W

4. The line length compensation function is useful when the antenna is connected to the receiver by a long coaxial cable that adds a considerable DC voltage drop. When the LCC pin is H, the output voltage selected is increased by about 1 V. This function is available for the DFN package only.
5. The reference drives all the internal blocks that require a high-precision thermally compensated voltage source.
6. The LNBPxx has two different protection features, and both turn off the outputs. The first one protects against overheating (i.e. for $T_J \geq 150$ °C), and the second against overload conditions (i.e. for output current > 550 mA) or short-circuit:
   a) In the thermal protection case the output is disabled until the chip temperature has fallen below 140 °C typ. and the LNBPxx output is restored.
   b) The overload protection case occurs when output current request is ≥ 500 mA. For the DFN package only, the IC features dynamic overload and short-circuit protection. When an overload occurs the device limits the output current for the

time T_{ON} depending on the C_{EXT} value (see *Figure 24* and *Figure 25*). When T_{ON} has elapsed, the output goes low for a time of T_{OFF} = 12 x T_{ON}. This keeps the power dissipated by the device low in overload conditions, and avoids the need for an oversized heat sink in this condition. For the IPPAK package, when the overload or the short-circuit occurs, the device clamps the output current in a range between 550 mA and 850 mA.

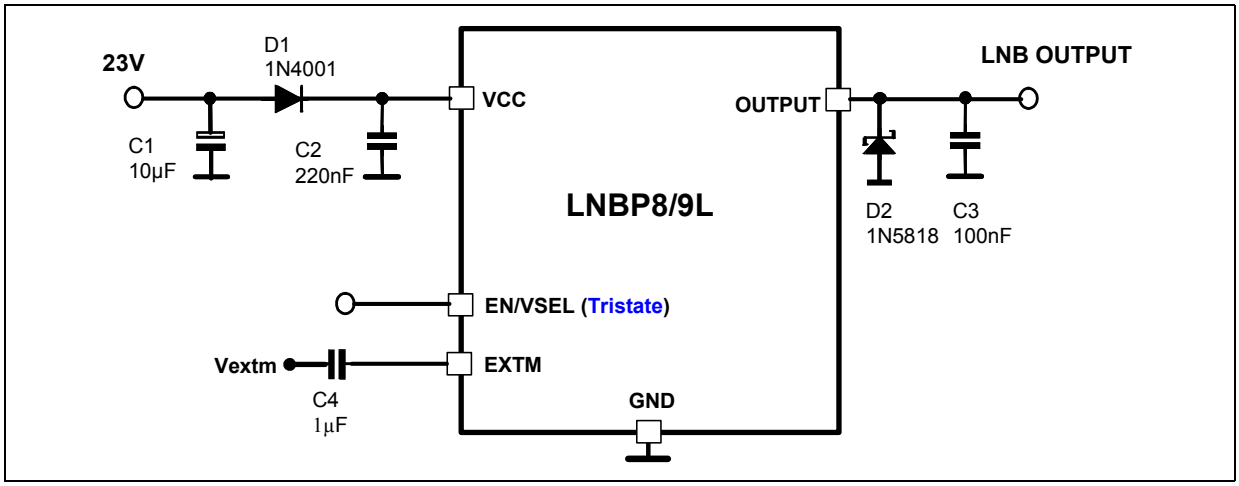
7. EXTM modulates the V_{OUT} by means of a capacitor connected in series (see *Figure 6*). The following equation is used to calculate the peak-to-peak voltage of V_{OUT}:

Equation 1

$$V_{OUT}(AC) = V_{EXTM}(AC) \times G_{EXTM}$$

where $V_{OUT}(AC)$ and $V_{EXTM}(AC)$ are, respectively, the peak-to-peak voltage of V_{OUT} and V_{EXTM}. G_{EXTM} is the external modulation gain.

Figure 6. EXTM application circuit



6.1 Input voltage protection

In some cases two or more receivers share the same coaxial cable, rendering their outputs hard-paralleled, so the same voltage is present at the outputs of the receivers. If a receiver is not disconnected at the mains, a current will flow from the OUTPUT to the V_{CC1} or V_{CC2} pins, depending the EN/VSEL pin setting. To avoid this, two diodes (only one for the IPPAK package) in series are recommended at input pins V_{CC1} and V_{CC2} (see *Figure 3*). These diodes do not cause a change at V_{OUT}, but only a voltage drop, which can be minimized by using Schottky diodes. Diodes used in *Figure 4* and *Figure 5* must withstand a continuous current of almost 1 A and a breakdown voltage of 30 V (suggested type is 1N4001 or BYV10-30). Be aware that the minimum voltage needed at the V_{CC} pins must be respected, considering the voltage drop across the input diodes).

6.2 Single supply for the DFN package

If only one power supply source is available, the V_{CC1} and V_{CC2} pins can be powered by the same power source without affecting the performance of other circuits, at the cost of higher power losses in the device and higher heat sink surface. Also, in order to reduce the power dissipation in the device, an appropriate-value resistor can be inserted in series with the

V_{CC1} line (see *Figure 5*). This resistor must be dimensioned considering that the minimum voltage on the V_{CC1} pin must be >= 16 V (15 V if LLC is not used).

For example, with I_{OUT} = 500 mA:

Equation 2

$$R \leq \frac{(23 - V_f - 16)}{500 \times 10^{-3}} \cong 12\ \Omega$$

Where V_f is the forward voltage of the input diode D1 (see *Figure 5*).

Power dissipated in this resistor is:

Equation 3

$$P_D = R * I_{OUT}^2 = 12 * \left(500 * 10^{-3}\right)^2 = 3\ W$$

It is recommended to bypass the V_{CC1} and V_{CC2} pins using 220 nF electrolytic capacitors.

6.3 IPPAK mounting and thermal considerations

First, it should be noted that the tab is directly connected to the GND pin, so care must be taken when the device is connected to a heat-sink. If the heat sink is at a different voltage than the ground, an electrical insulator must be added between the tab and the heat sink at the cost of an increase in the thermal resistance. For better thermal performance, an isolated heat sink or connection to ground is recommended.

Several clips can be used depending on the heat sink type:

- Saddle clips (*Figure 7*) for slim heat sinks
- U-clips (*Figure 8*) for thick heat sinks
- Dedicated clips for special shaped heat sinks

Figure 7. IPPAK mounted with a saddle clip

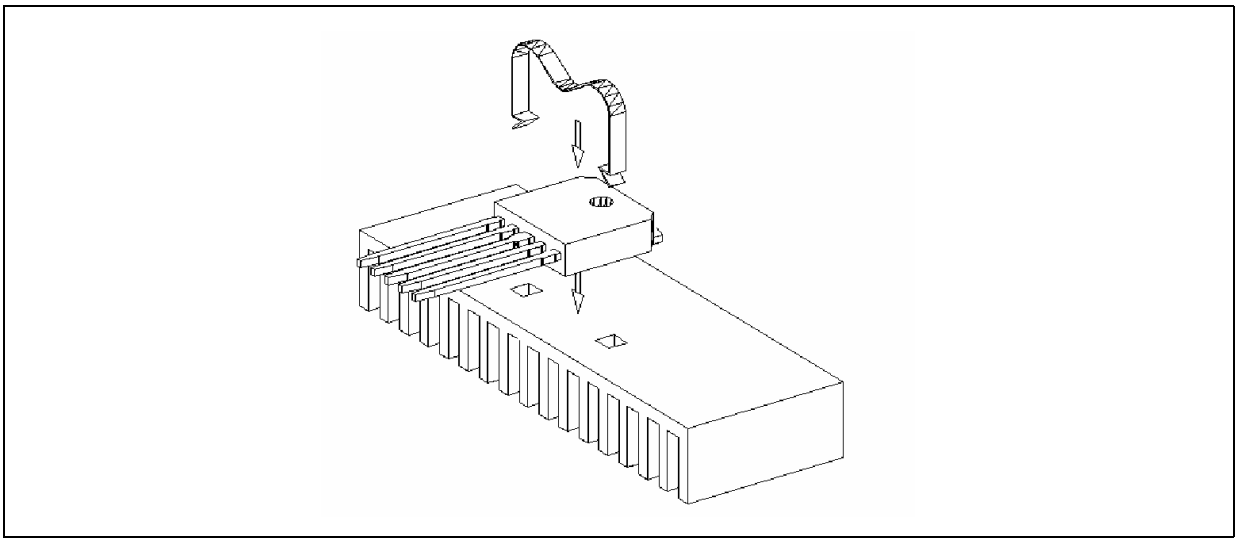
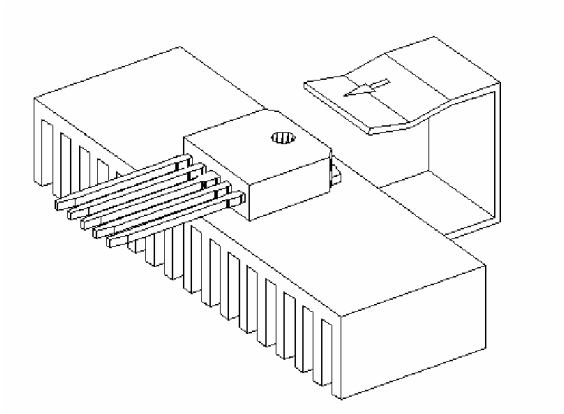


Figure 8. IPPAK mounted with a U-clip



Note that the thickness of the IPPAK package (2.3 +/- 0.1 mm) is similar to that of the SOT-32 and SOT-82 (2.55 +/- 0.15 mm). The same clips can also be used for these packages.

The junction-to-ambient thermal resistance for the IPPAK can be calculated as follows:

Equation 4

$R_{TH\text{-}JA} = R_{TH\text{-}JC} + R_{TH\text{-}CH} + R_{TH\text{-}HA}$

where: $R_{TH\text{-}JC}$ is the junction-to-case thermal resistance of the IPPAK (see *Table 4: Thermal data*), $R_{TH\text{-}CH}$ is the case-to-heat sink thermal resistance and the $R_{TH\text{-}HA}$ is the heat sink-to-air thermal resistance.

7 Typical performance characteristics

Refer to the typical application circuit, T_J from 0 to 85 °C. Typical values are referred to T_J = 25 °C.

Figure 9. Output voltage vs. temperature

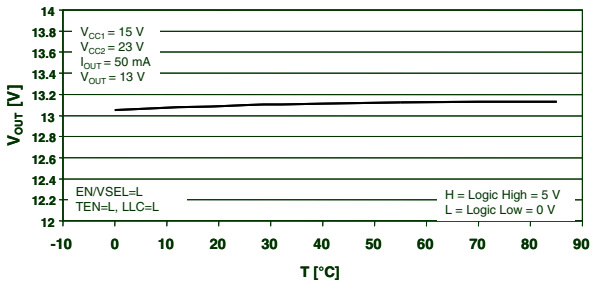


Figure 10. Output voltage vs. temperature

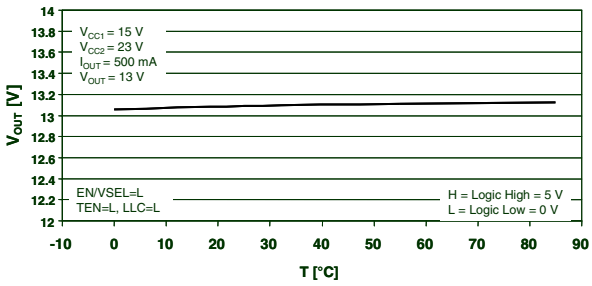


Figure 11. Output voltage vs. temperature

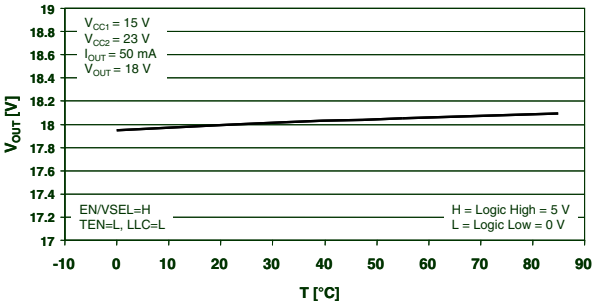


Figure 12. Output voltage vs. temperature

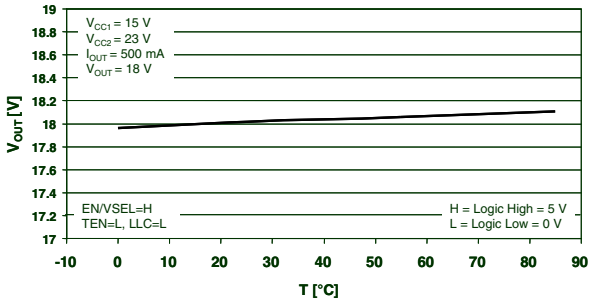


Figure 13. Line regulation vs. temperature

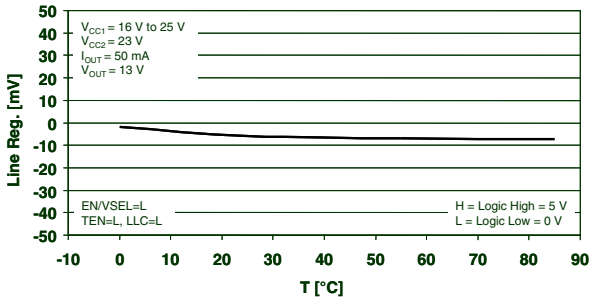


Figure 14. Load regulation vs. temperature

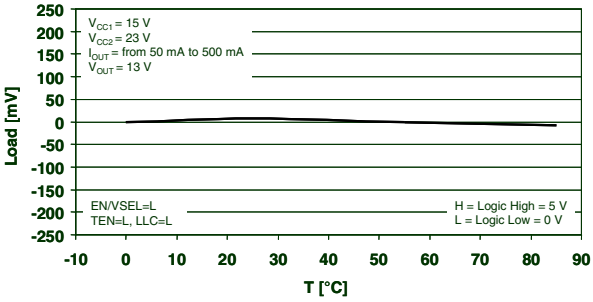


Figure 15. Load regulation vs. temperature

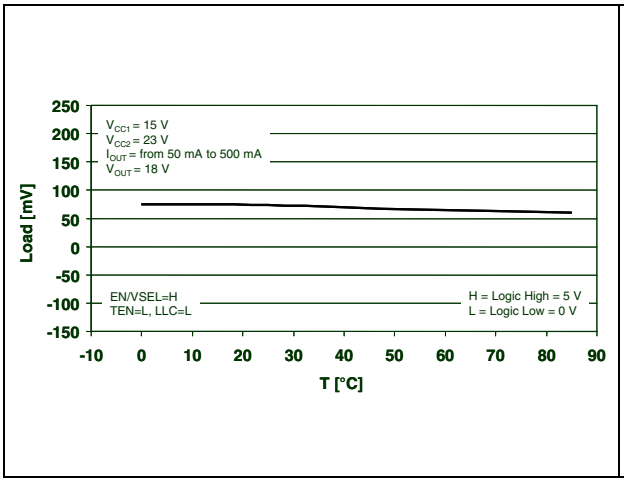


Figure 16. Output current limiting vs. temperature

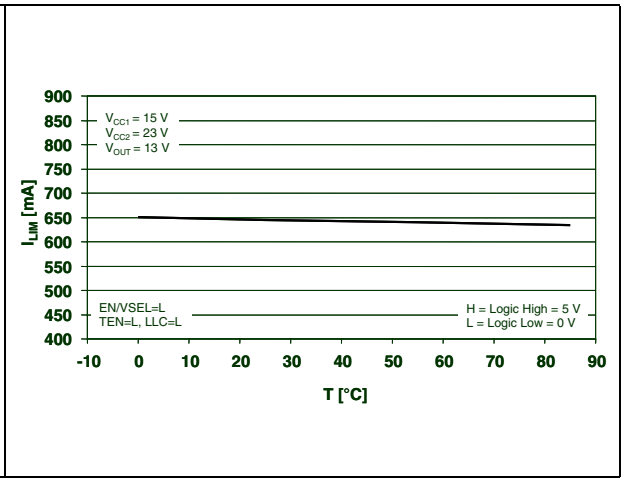


Figure 17. Output current limiting vs. temperature

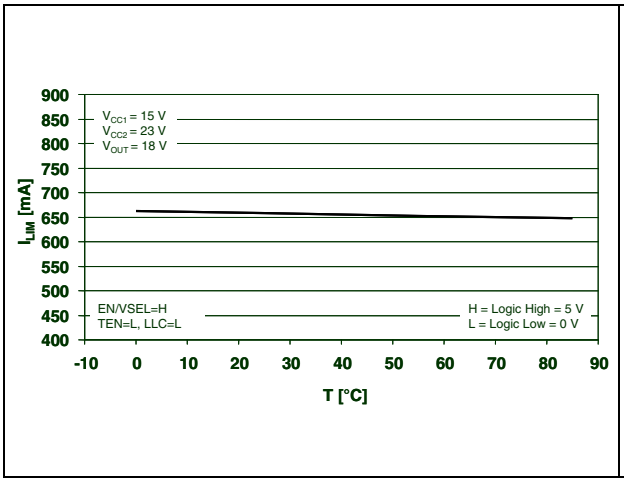


Figure 18. Dynamic overload protection ON time vs. temperature

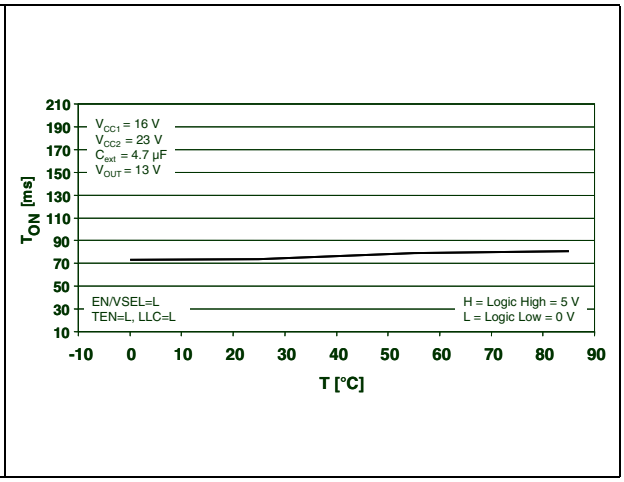


Figure 19. Dynamic overload protection OFF time vs. temperature

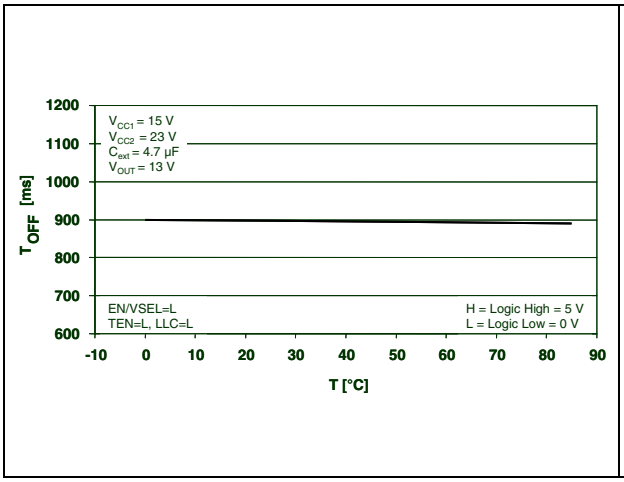


Figure 20. Tone enable

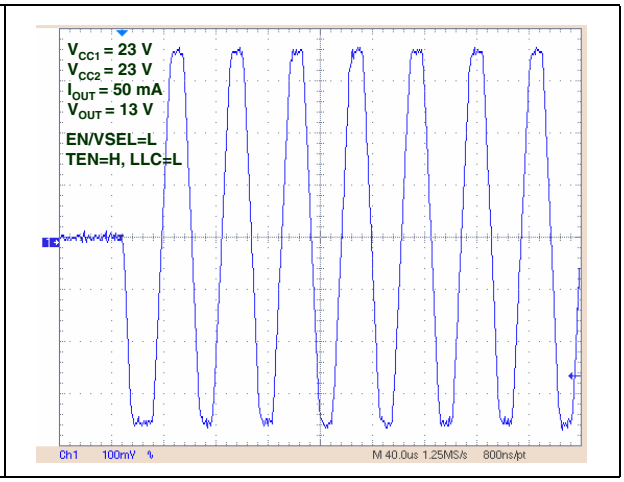


Figure 21. Tone disable

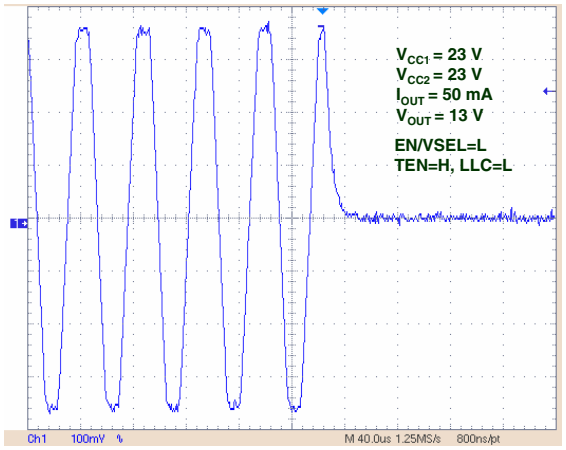


Figure 22. External modulation gain vs. temperature

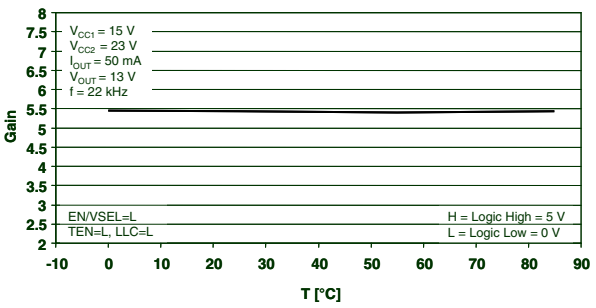


Figure 23. External modulation gain vs. frequency

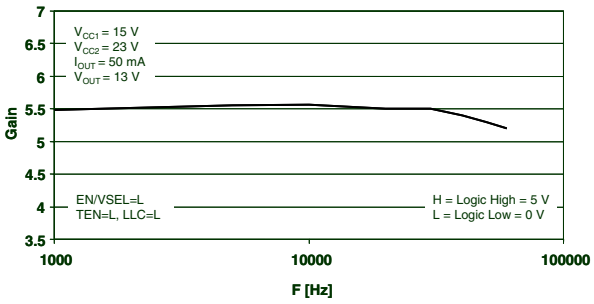


Figure 24. T_{ON} time vs. C_{EXT}

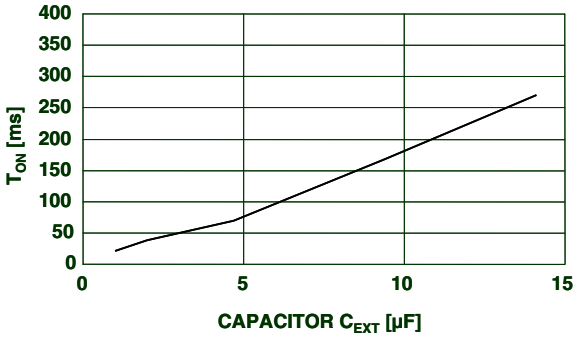
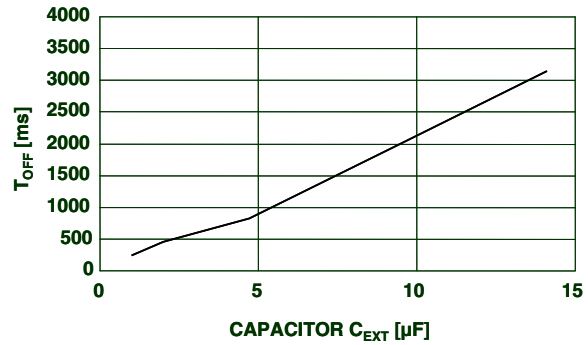


Figure 25. T_{OFF} time vs. C_{EXT}



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 26. IPPAK package dimensions

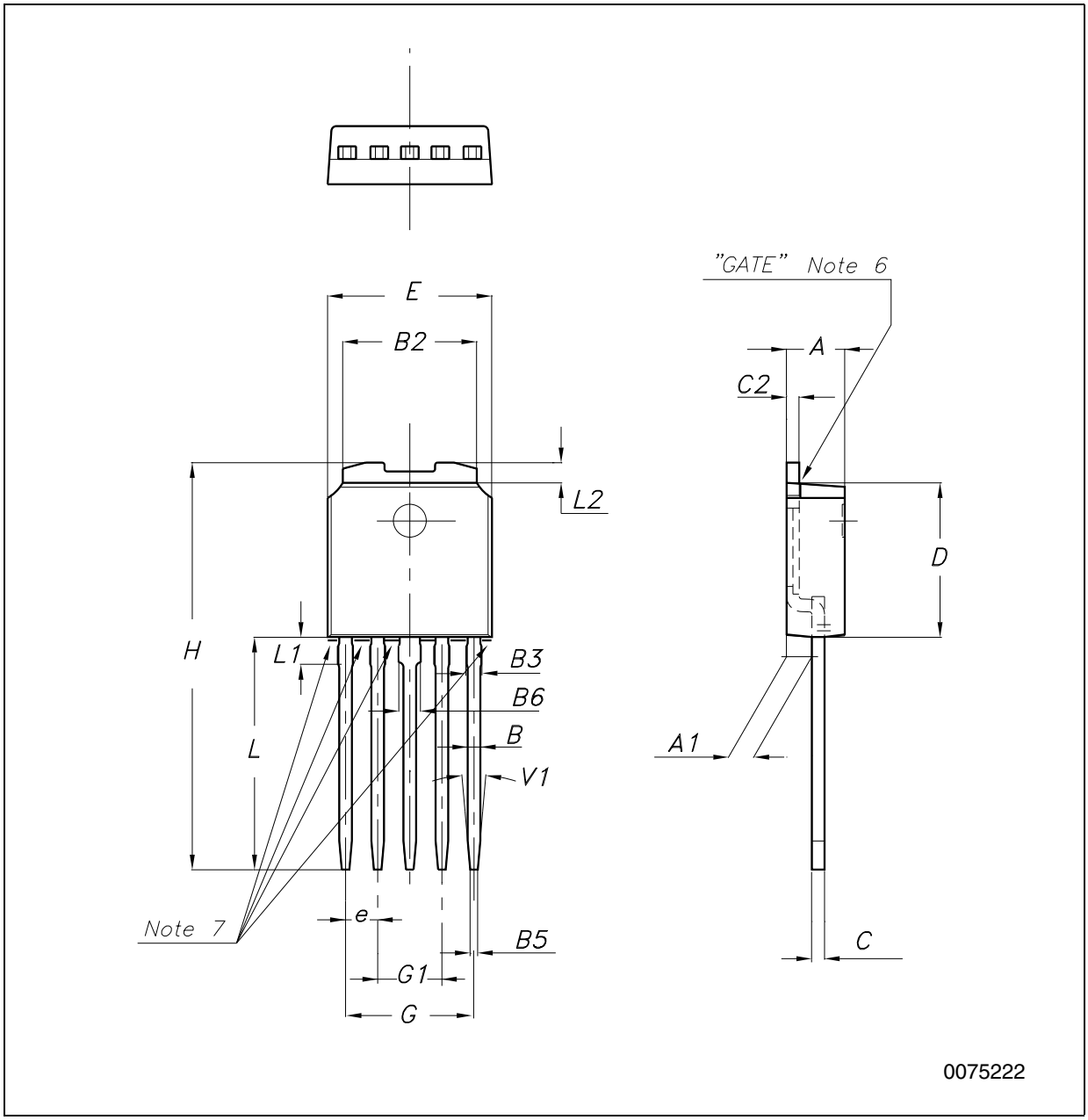


Table 6. IPPAK mechanical data

Dim.	(mm.)		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
B	0.40		0.60
B2	5.20		5.40
B3			0.70
B5		0.30	
B6			1
C	0.45		0.60
C2	0.48		0.60
D	6		6.20
E	6.40		6.60
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	15.90		16.30
L	9		9.40
L1	0.80		1.20
L2		0.80	1
V1		10°	

Note: 1 Controlling dimensions: millimeter.

2 Burrs larger than 0.25 mm are not allowed on the upper surface of the dissipater (FRONT) on the lower surface (REAR) the maximum allowed is: 0.05 mm.

3 The side of the dissipater to be connected to the external dissipater must be flat within 30 µ

4 The leads size is comprehensive of the thickness of the leads finishing material.

5 Package outline exclusive of any mold flashes dimensions and metal burrs.

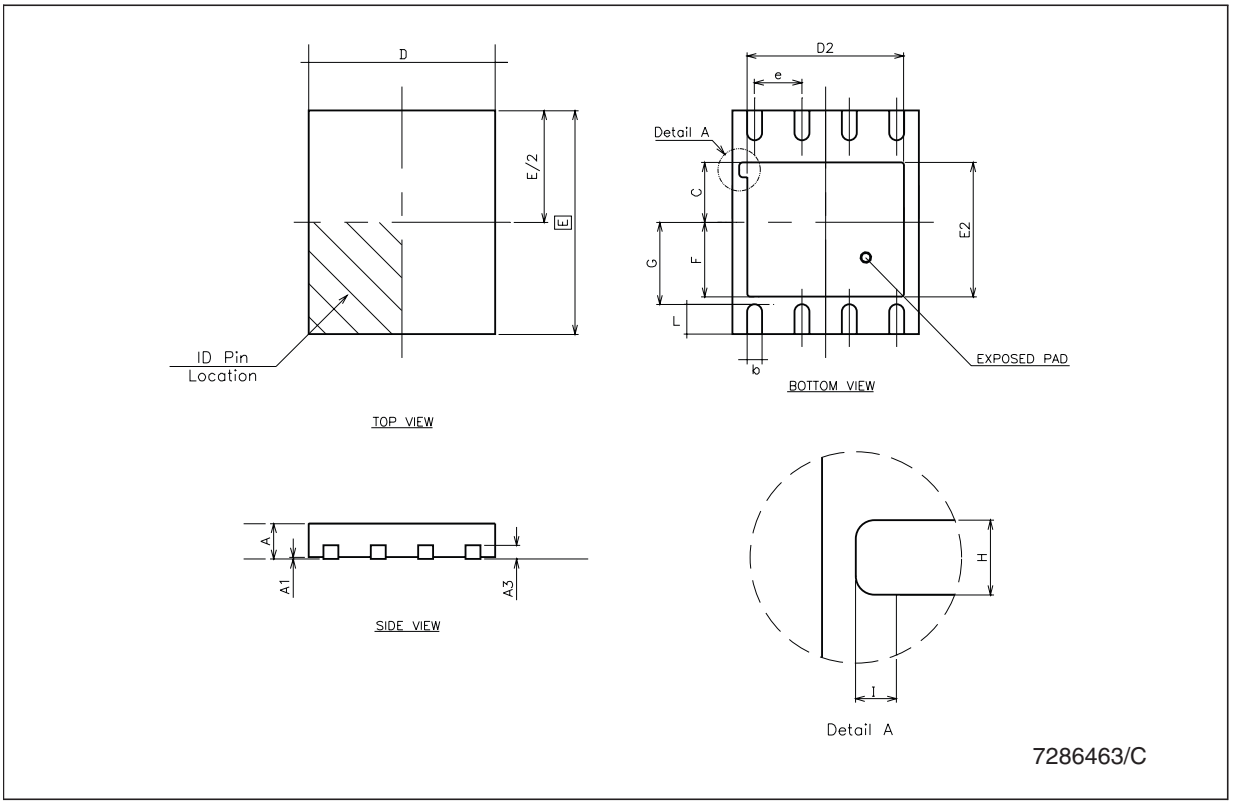
6 Max resin gate protrusion: 0.5 mm.

7 Max resin protrusion: 0.25 mm.

8 The maximum bent leads allowed, in any direction, is: # 2° if the devices are packed in tube.

DFN8 (5x6 mm) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.032	0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.20			0.008	
b	0.35	0.40	0.47	0.014	0.016	0.018
D		5.00			0.197	
D2	4.15	4.2	4.25	0.163	0.165	0.167
E		6.00			0.236	
E2	3.55	3.6	3.65	0.140	0.142	0.144
e		1.27			0.049	
F		1.99			0.078	
G		2.20			0.086	
H		0.40			0.015	
I		0.219			0.0086	
L	0.70		0.90	0.028		0.035



9 Ordering information

Table 7. Order codes

Part numbers	Order codes		Packing
	DFN8 (5 x 6 mm)	IPPAK	
LNBP8L		LNBP8LIT	Tape and reel
LNBP9L		LNBP9LIT	Tape and reel
LNBP10L	LNBP10LPUR		Tape and reel
LNBP11L	LNBP11LPUR		Tape and reel

10 Revision history

Table 8. Document revision history

Date	Revision	Changes
11-Nov-2008	1	Initial release.
25-Aug-2010	2	Document status promoted from preliminary data to datasheet.

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