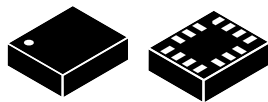


## iNEMO inertial module with embedded Machine Learning Core: always-on 3D accelerometer and 3D gyroscope



**LGA-14L**  
(2.5 x 3.0 x 0.83 mm) typ.

### Features

- Extended full-scale range for gyroscope up to 4000 dps
- High stability over temperature and time
- Smart FIFO up to 9 kbytes
- Android compliant
- Auxiliary SPI for OIS data output for gyroscope and accelerometer
- $\pm 2/\pm 4/\pm 8/\pm 16$  g full scale
- $\pm 125/\pm 250/\pm 500/\pm 1000/\pm 2000/\pm 4000$  dps full scale
- Analog supply voltage: 1.71 V to 3.6 V
- SPI / I<sup>2</sup>C & MIPI I3C<sup>SM</sup> serial interface with main processor data synchronization
- Supports sensor synchronization S4S for Qualcomm, full spec compliant (I<sup>2</sup>C, MIPI I3C<sup>SM</sup>, SPI)
- Advanced pedometer, step detector and step counter
- Significant Motion Detection, tilt detection
- Programmable Finite State Machine: accelerometer, gyroscope, and external sensors
- Machine Learning Core
- Standard interrupts: free-fall, wakeup, 6D/4D orientation, click and double-click
- Embedded temperature sensor
- ECOPACK, RoHS and “Green” compliant

### Applications

- Motion tracking and gesture detection
- Virtual and augmented reality
- OIS for camera applications
- Sensor hub
- Indoor navigation
- IoT and connected devices
- Sports applications
- Vibration monitoring and compensation
- Drones
- Robotics
- High-precision systems

### Description

The LSM6DSRX is a system-in-package featuring a 3D digital accelerometer and a 3D digital gyroscope with an extended full-scale range for the gyroscope, up to 4000 dps, and high stability over temperature and time.

The LSM6DSRX supports main OS requirements, offering real, virtual and batch sensors with 9 kbytes with FIFO compression up to three times for dynamic data batching.

| Product status link   |                                  |             |
|---|----------------------------------|-------------|
| <a href="#">LSM6DSRX</a>  |                                  |             |
| Product summary   |                                  |             |
| Order code  | LSM6DSRX                         | LSM6DSRXTR  |
| Temp. range [°C]  | -40 to +85                       |             |
| Package   | LGA-14L<br>(2.5 x 3.0 x 0.83 mm) |             |
| Packing   | Tray                             | Tape & Reel |
| Product label   |                                  |             |
|    |                                  |             |
| Product resources   |                                  |             |
| <a href="#">AN5382</a> (LSM6DSRX)<br><a href="#">AN5393</a> (Machine Learning Core)<br><a href="#">AN5389</a> (Finite State Machine)<br><a href="#">TN0018</a> (Design and soldering) |                                  |             |

ST's family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes.

The LSM6DSRX has a full-scale acceleration range of  $\pm 2/\pm 4/\pm 8/\pm 16$  g and an angular rate range of  $\pm 125/\pm 250/\pm 500/\pm 1000/\pm 2000/\pm 4000$  dps.

The LSM6DSRX embeds a broad range of advanced functions supporting Android wearable sensors and programmable sensors (suitable for activity recognition).

The LSM6DSRX embeds a Machine Learning Core able to identify if a data pattern matches an activity in a user-defined set of classes, reducing power consumption and increasing performance of the sensor.

The LSM6DSRX is available in a plastic land grid array (LGA) package.

## 1 Overview

The LSM6DSRX is a system-in-package featuring a high-performance 3-axis digital accelerometer and 3-axis digital gyroscope.

The LSM6DSRX delivers best-in-class motion sensing that can detect orientation and gestures in order to empower application developers and consumers with features and capabilities that are more sophisticated than simply orienting their devices to portrait and landscape mode.

This device is suitable for augmented reality and virtual reality applications as well as Optical Image Stabilization and motion-based gaming controllers as a result of its high stability over temperature and time, combined with superior sensing precision.

The LSM6DSRX fully supports OIS applications using both the gyroscope and accelerometer sensor. The device can output OIS data through a dedicated auxiliary SPI and includes a dedicated configurable signal processing path for OIS. For both the gyroscope and accelerometer, the UI signal processing path is completely independent from that of the OIS and is readable through FIFO. Moreover, self-test and full scale are available for both the UI and OIS chains.

The event-detection interrupts enable efficient and reliable motion tracking and contextual awareness, implementing hardware recognition of free-fall events, 6D orientation, click and double-click sensing, activity or inactivity, and wakeup events.

The LSM6DSRX supports main OS requirements, offering real, virtual and batch mode sensors. In addition, the LSM6DSRX can efficiently run the sensor-related features specified in Android. In particular, the LSM6DSRX has been designed to implement hardware features such as significant motion, tilt, pedometer functions, timestamping and to support the data acquisition of an external magnetometer.

The LSM6DSRX offers hardware flexibility to connect the pins with different mode connections to external sensors to expand functionalities such as adding a sensor hub.

Up to 9 kbytes of FIFO with compression and dynamic allocation of significant data (i.e. external sensors, timestamp, etc.) allows overall power saving of the system.

Like the entire portfolio of MEMS sensor modules, the LSM6DSRX leverages the robust and mature in-house manufacturing processes already used for the production of micromachined accelerometers and gyroscopes. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The LSM6DSRX is available in a small plastic land grid array (LGA) package of 2.5 x 3.0 x 0.83 mm to address ultra-compact solutions.

## 2 Embedded low-power features

The LSM6DSRX has been designed to be fully compliant with Android, featuring the following on-chip functions:

- 9 kbytes data buffering, data can be compressed two or three times
  - 100% efficiency with flexible configurations and partitioning
  - Possibility to store timestamp
- Event-detection interrupts (fully configurable):
  - Free-fall
  - Wakeup
  - 6D orientation
  - Click and double-click sensing
  - Activity/inactivity recognition
  - Stationary/Motion detection
- Specific IP blocks with negligible power consumption and high-performance:
  - Pedometer functions: step detector and step counters
  - Tilt
  - Significant Motion Detection
  - Finite State Machine (FSM) for accelerometer, gyroscope, and external sensors
  - Machine Learning Core (MLC)
- Sensor hub
  - Up to 6 total sensors: 2 internal (accelerometer and gyroscope) and 4 external sensors
- S4S data rate synchronization with external trigger for reduced sensor access and enhanced fusion

### 2.1 Tilt detection

The tilt function helps to detect activity change and has been implemented in hardware using only the accelerometer to achieve targets of both ultra-low power consumption and robustness during the short duration of dynamic accelerations.

The tilt function is based on a trigger of an event each time the device's tilt changes and can be used with different scenarios, for example:

- Triggers when phone is in a front pants pocket and the user goes from sitting to standing or standing to sitting;
- Doesn't trigger when phone is in a front pants pocket and the user is walking, running or going up stairs.

### 2.2 Significant Motion Detection

The Significant Motion Detection (SMD) function generates an interrupt when a 'significant motion', that could be due to a change in user location, is detected. In the LSM6DSRX device this function has been implemented in hardware using only the accelerometer.

SMD functionality can be used in location-based applications in order to receive a notification indicating when the user is changing location.

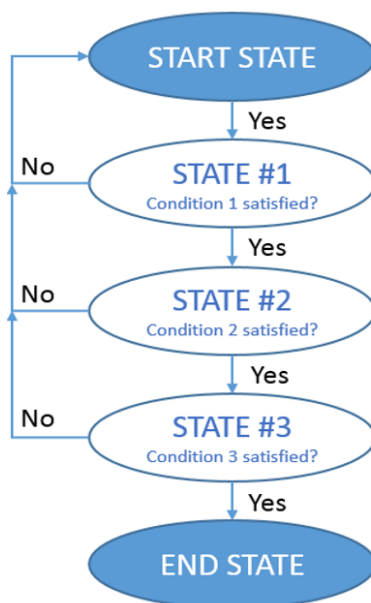
## 2.3 Finite State Machine

The LSM6DSRX can be configured to generate interrupt signals activated by user-defined motion patterns. To do this, up to 16 embedded finite state machines can be programmed independently for motion detection such as glance gestures, absolute wrist tilt, shake and double-shake detection.

### Definition of Finite State Machine

A state machine is a mathematical abstraction used to design logic connections. It is a behavioral model composed of a finite number of states and transitions between states, similar to a flow chart in which one can inspect the way logic runs when certain conditions are met. The state machine begins with a start state, goes to different states through transitions dependent on the inputs, and can finally end in a specific state (called stop state). The current state is determined by the past states of the system. The following figure shows a generic state machine.

Figure 1. Generic state machine



### Finite State Machine in the LSM6DSRX

The LSM6DSRX works as a combo accelerometer-gyroscope sensor, generating acceleration and angular rate output data. It is also possible to connect an external sensor (magnetometer) by using the Sensor Hub feature (Mode 2). These data can be used as input of up to 16 programs in the embedded Finite State Machine (Figure 2. State machine in the LSM6DSRX).

All 16 finite state machines are independent: each one has its dedicated memory area and it is independently executed. An interrupt is generated when the end state is reached or when some specific command is performed.

Figure 2. State machine in the LSM6DSRX



## 2.4 Machine Learning Core

The LSM6DSRX embeds a dedicated core for machine learning processing that provides system flexibility, allowing some algorithms run in the application processor to be moved to the MEMS sensor with the advantage of consistent reduction in power consumption.

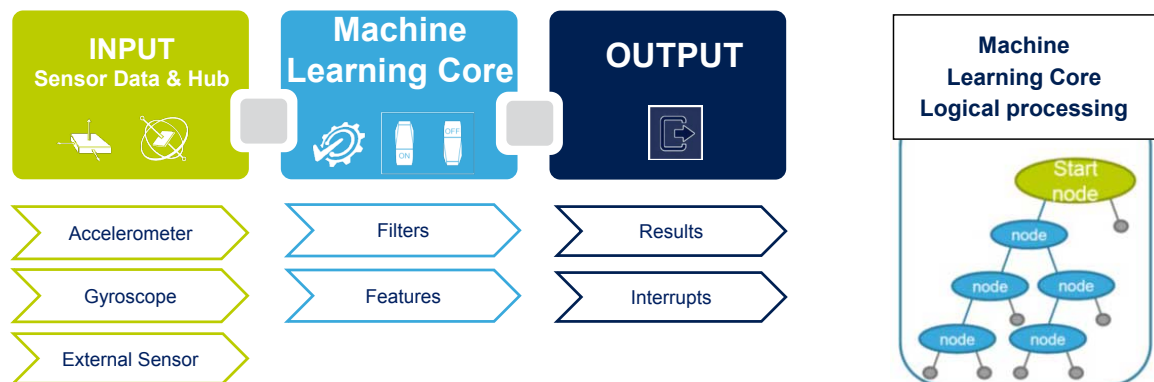
Machine Learning Core logic allows identifying if a data pattern (for example motion, pressure, temperature, magnetic data, etc.) matches a user-defined set of classes. Typical examples of applications could be activity detection like running, walking, driving, etc.

The LSM6DSRX Machine Learning Core works on data patterns coming from the accelerometer and gyro sensors, but it is also possible to connect and process external sensor data (like magnetometer) by using the Sensor Hub feature (Mode 2).

The input data can be filtered using a dedicated configurable computation block containing filters and features computed in a fixed time window defined by the user.

Machine learning processing is based on logical processing composed of a series of configurable nodes characterized by "if-then-else" conditions where the "feature" values are evaluated against defined thresholds.

Figure 3. Machine Learning Core in the LSM6DSRX



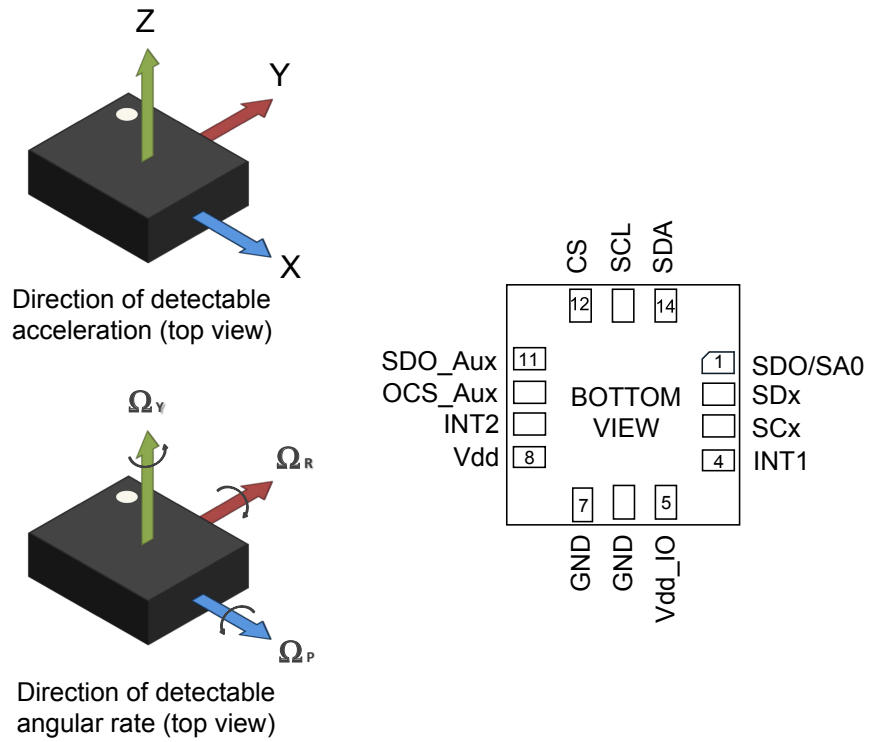
The LSM6DSRX can be configured to run up to 8 flows simultaneously and independently and every flow can generate up to 256 results. The total number of nodes can be up to 512.

The results of the machine learning processing are available in dedicated output registers readable from the application processor at any time.

The LSM6DSRX Machine Learning Core can be configured to generate an interrupt when a change in the result occurs.

### 3 Pin description

Figure 4. Pin connections

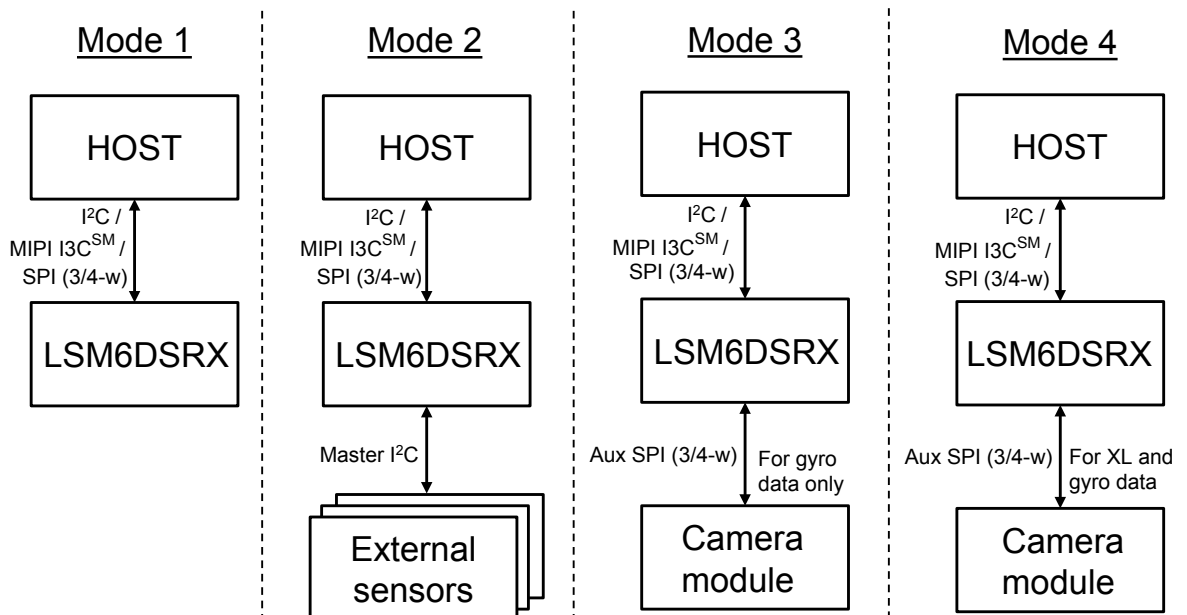


### 3.1 Pin connections

The LSM6DSRX offers flexibility to connect the pins in order to have four different mode connections and functionalities. In detail:

- **Mode 1:** I<sup>2</sup>C / MIPI I3C<sup>SM</sup> slave interface or SPI (3- and 4-wire) serial interface is available;
- **Mode 2:** I<sup>2</sup>C / MIPI I3C<sup>SM</sup> slave interface or SPI (3- and 4-wire) serial interface and I<sup>2</sup>C interface master for external sensor connections are available;
- **Mode 3:** I<sup>2</sup>C / MIPI I3C<sup>SM</sup> slave interface or SPI (3- and 4-wire) serial interface is available for the application processor interface while an auxiliary SPI (3- and 4-wire) serial interface for external sensor connections is available for the gyroscope ONLY;
- **Mode 4:** I<sup>2</sup>C / MIPI I3C<sup>SM</sup> slave interface or SPI (3- and 4-wire) serial interface is available for the application processor interface while an auxiliary SPI (3- and 4-wire) serial interface for external sensor connections is available for the accelerometer and gyroscope.

**Figure 5. LSM6DSRX connection modes**



In the following table each mode is described for the pin connections and function.



**Table 1. Pin description**

| Pin # | Name                  | Mode 1 function  | Mode 2 function  | Mode 3/4 function  |
|-------|-----------------------|--|--|--|
| 1     | SDO/SA0               | SPI 4-wire interface serial data output (SDO)<br>I <sup>2</sup> C least significant bit of the device address (SA0)  | SPI 4-wire interface serial data output (SDO)<br>I <sup>2</sup> C least significant bit of the device address (SA0)  | SPI 4-wire interface serial data output (SDO)<br>I <sup>2</sup> C least significant bit of the device address (SA0)  |
| 2     | SDx                   | Connect to Vdd_IO or GND   | I <sup>2</sup> C serial data master (MSDA)   | Auxiliary SPI 3/4-wire interface serial data input (SDI) and SPI 3-wire serial data output (SDO)   |
| 3     | SCx                   | Connect to Vdd_IO or GND   | I <sup>2</sup> C serial clock master (MSCL)  | Auxiliary SPI 3/4-wire interface serial port clock (SPC_Aux)   |
| 4     | INT1                  | Programmable interrupt in I <sup>2</sup> C and SPI   |  |  |
| 5     | Vdd_IO <sup>(1)</sup> | Power supply for I/O pins  |  |  |
| 6     | GND                   | 0 V supply   |  |  |
| 7     | GND                   | 0 V supply   |  |  |
| 8     | Vdd <sup>(1)</sup>    | Power supply   |  |  |
| 9     | INT2                  | Programmable interrupt 2 (INT2) / Data enabled (DEN)   | Programmable interrupt 2 (INT2) / Data enabled (DEN) / I <sup>2</sup> C master external synchronization signal (MDRDY)   | Programmable interrupt 2 (INT2) / Data enabled (DEN)   |
| 10    | OCS_Aux               | Leave unconnected <sup>(2)</sup>   | Leave unconnected <sup>(2)</sup>   | Auxiliary SPI 3/4-wire interface enable  |
| 11    | SDO_Aux               | Connect to Vdd_IO or leave unconnected <sup>(2)</sup>  | Connect to Vdd_IO or leave unconnected <sup>(2)</sup>  | Auxiliary SPI 3-wire interface: leave unconnected <sup>(2)</sup><br>Auxiliary SPI 4-wire interface: serial data output (SDO_Aux)   |
| 12    | CS                    | I <sup>2</sup> C and MIPI I3C <sup>SM</sup> /SPI mode selection (1: SPI idle mode / I <sup>2</sup> C and MIPI I3C <sup>SM</sup> communication enabled; 0: SPI communication mode / I <sup>2</sup> C and MIPI I3C <sup>SM</sup> disabled) | I <sup>2</sup> C and MIPI I3C <sup>SM</sup> /SPI mode selection (1: SPI idle mode / I <sup>2</sup> C and MIPI I3C <sup>SM</sup> communication enabled; 0: SPI communication mode / I <sup>2</sup> C and MIPI I3C <sup>SM</sup> disabled) | I <sup>2</sup> C and MIPI I3C <sup>SM</sup> /SPI mode selection (1: SPI idle mode / I <sup>2</sup> C and MIPI I3C <sup>SM</sup> communication enabled; 0: SPI communication mode / I <sup>2</sup> C and MIPI I3C <sup>SM</sup> disabled) |
| 13    | SCL                   | I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial clock (SCL) / SPI serial port clock (SPC)   | I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial clock (SCL) / SPI serial port clock (SPC)   | I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial clock (SCL) / SPI serial port clock (SPC)   |
| 14    | SDA                   | I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO)  | I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO)  | I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO)  |

1. Recommended 100 nF filter capacitor.

2. Leave pin electrically unconnected and soldered to PCB.

## 4 Module specifications

### 4.1 Mechanical characteristics

@ Vdd = 1.8 V, T = 25 °C, unless otherwise noted.

**Table 2. Mechanical characteristics**

| Symbol   | Parameter  | Test conditions       | Min. | Typ. <sup>(1)</sup> | Max. | Unit     |
|----------|--|-----------------------|------|---------------------|------|----------|
| LA_FS    | Linear acceleration measurement range                                      |                       |      | ±2                  |      | g        |
|          |  |                       |      | ±4                  |      |          |
|          |  |                       |      | ±8                  |      |          |
|          |  |                       |      | ±16                 |      |          |
| G_FS     | Angular rate measurement range   |                       |      | ±125                |      | dps      |
|          |  |                       |      | ±250                |      |          |
|          |  |                       |      | ±500                |      |          |
|          |  |                       |      | ±1000               |      |          |
|          |  |                       |      | ±2000               |      |          |
| LA_So    | Linear acceleration sensitivity <sup>(2)</sup>                             | FS = ±2 g             |      | 0.061               |      | mg/LSB   |
|          |  | FS = ±4 g             |      | 0.122               |      |          |
|          |  | FS = ±8 g             |      | 0.244               |      |          |
|          |  | FS = ±16 g            |      | 0.488               |      |          |
| G_So     | Angular rate sensitivity <sup>(2)</sup>                                    | FS = ±125 dps         |      | 4.375               |      | mdps/LSB |
|          |  | FS = ±250 dps         |      | 8.75                |      |          |
|          |  | FS = ±500 dps         |      | 17.50               |      |          |
|          |  | FS = ±1000 dps        |      | 35                  |      |          |
|          |  | FS = ±2000 dps        |      | 70                  |      |          |
|          |  | FS = ±4000 dps        |      | 140                 |      |          |
| G_So%    | Sensitivity tolerance <sup>(3)</sup>                                       | at component level    |      | ±1                  |      | %        |
| LA_SoDr  | Linear acceleration sensitivity change vs. temperature <sup>(4)</sup>      | from -40 °C to +85 °C |      | ±0.01               |      | %/°C     |
| G_SoDr   | Angular rate sensitivity change vs. temperature <sup>(4)</sup>             | from -40 °C to +85 °C |      | ±0.007              |      | %/°C     |
| LA_TyOff | Linear acceleration zero-g level offset accuracy <sup>(5)</sup>            |                       |      | ±10                 |      | mg       |
| G_TyOff  | Angular rate zero-rate level <sup>(5)</sup>                                |                       |      | ±1                  |      | dps      |
| LA_OffDr | Linear acceleration zero-g level change vs. temperature <sup>(4)</sup>     |                       |      | ±0.1                |      | mg/°C    |
| G_OffDr  | Angular rate typical zero-rate level change vs. temperature <sup>(4)</sup> |                       |      | ±0.005              |      | dps/°C   |
| Rn       | Rate noise density in high-performance mode <sup>(6)</sup>                 |                       |      | 5                   |      | mdps/√Hz |
| RnRMS    | Gyroscope RMS noise in low-power mode <sup>(7)</sup>                       |                       |      | 90                  |      | mdps     |
| An       | Acceleration noise density in high-performance mode <sup>(8)</sup>         |                       |      | 60                  |      | μg/√Hz   |
| RMS      | Acceleration RMS noise in low-power mode <sup>(9)(10)</sup>                |                       |      | 1.8                 |      | mg(RMS)  |

| Symbol | Parameter   | Test conditions | Min. | Typ. <sup>(1)</sup> | Max. | Unit |
|--------|---|-----------------|------|---------------------|------|------|
| LA_ODR | Linear acceleration output data rate                                  |                 |      | 1.6 <sup>(11)</sup> |      | Hz   |
|        |   |                 |      | 12.5                |      |      |
|        |   |                 |      | 26                  |      |      |
|        |   |                 |      | 52                  |      |      |
|        |   |                 |      | 104                 |      |      |
|        |   |                 |      | 208                 |      |      |
|        |   |                 |      | 416                 |      |      |
|        |   |                 |      | 833                 |      |      |
|        |   |                 |      | 1666                |      |      |
|        |   |                 |      | 3332                |      |      |
| G_ODR  | Angular rate output data rate   |                 |      | 12.5                |      | Hz   |
|        |   |                 |      | 26                  |      |      |
|        |   |                 |      | 52                  |      |      |
|        |   |                 |      | 104                 |      |      |
|        |   |                 |      | 208                 |      |      |
|        |   |                 |      | 416                 |      |      |
|        |   |                 |      | 833                 |      |      |
|        |   |                 |      | 1666                |      |      |
|        |   |                 |      | 3332                |      |      |
|        |   |                 |      | 6667                |      |      |
| Vst    | Linear acceleration self-test output change <sup>(12) (13) (14)</sup> |                 | 40   |                     | 1700 | mg   |
|        | Angular rate self-test output change <sup>(15)(16)</sup>              | FS = ±250 dps   | 20   |                     | 80   | dps  |
|        |   | FS = ±2000 dps  | 150  |                     | 700  | dps  |
| Top    | Operating temperature range   |                 | -40  |                     | +85  | °C   |

1. Typical specifications are not guaranteed.
2. Sensitivity values after factory calibration test and trimming.
3. Subject to change.
4. Measurements are performed in a uniform temperature setup and they are based on characterization data in a limited number of samples. Not measured during final test for production.
5. Values after factory calibration test and trimming.
6. Gyroscope rate noise density in high-performance mode is independent of the ODR and FS setting.
7. Gyroscope RMS noise in low-power mode is independent of the ODR and FS setting.
8. Accelerometer noise density in high-performance mode is independent of the ODR and full scale.
9. Accelerometer RMS noise in low-power mode is independent of the ODR.
10. Noise RMS related to  $BW = ODR/2$ .
11. This ODR is available when the accelerometer is in low-power mode.
12. The sign of the linear acceleration self-test output change is defined by the STx\_XL bits in a dedicated register for all axes.
13. The linear acceleration self-test output change is defined with the device in stationary condition as the absolute value of:  $OUTPUT[LSb] \text{ (self-test enabled)} - OUTPUT[LSb] \text{ (self-test disabled)}$ .  $1LSb = 0.061 \text{ mg}$  at  $\pm 2 \text{ g}$  full scale.
14. Accelerometer self-test limits are full-scale independent.
15. The sign of the angular rate self-test output change is defined by the STx\_G bits in a dedicated register for all axes.
16. The angular rate self-test output change is defined with the device in stationary condition as the absolute value of:  $OUTPUT[LSb] \text{ (self-test enabled)} - OUTPUT[LSb] \text{ (self-test disabled)}$ .  $1LSb = 70 \text{ mdps}$  at  $\pm 2000 \text{ dps}$  full scale

## 4.2 Electrical characteristics

@ Vdd = 1.8 V, T = 25 °C, unless otherwise noted.

**Table 3. Electrical characteristics**

| Symbol          | Parameter  | Test conditions                       | Min.         | Typ. <sup>(1)</sup> | Max.         | Unit |
|-----------------|--|---------------------------------------|--------------|---------------------|--------------|------|
| Vdd             | Supply voltage   |                                       | 1.71         | 1.8                 | 3.6          | V    |
| Vdd_IO          | Power supply for I/O   |                                       | 1.62         |                     | 3.6          | V    |
| IddHP           | Gyroscope and accelerometer current consumption in high-performance mode |                                       |              | 1.2                 |              | mA   |
| IddNM           | Gyroscope and accelerometer current consumption in normal mode           | ODR = 208 Hz                          |              | 0.7                 |              | mA   |
| LA_IddHP        | Accelerometer current consumption in high-performance mode               |                                       |              | 360                 |              | µA   |
| LA_IddLM        | Accelerometer current consumption in low-power mode                      | ODR = 52 Hz                           |              | 32                  |              | µA   |
|                 |  | ODR = 12.5 Hz                         |              | 11                  |              |      |
|                 |  | ODR = 1.6 Hz                          |              | 5.5                 |              |      |
| IddPD           | Gyroscope and accelerometer current consumption during power-down        |                                       |              | 3                   |              | µA   |
| Ton             | Turn-on time   |                                       |              | 35                  |              | ms   |
| V <sub>IH</sub> | Digital high-level input voltage   |                                       | 0.7 * Vdd_IO |                     |              | V    |
| V <sub>IL</sub> | Digital low-level input voltage  |                                       |              |                     | 0.3 * Vdd_IO | V    |
| V <sub>OH</sub> | Digital high-level output voltage  | I <sub>OH</sub> = 4 mA <sup>(2)</sup> | Vdd_IO - 0.2 |                     |              | V    |
| V <sub>OL</sub> | Digital low-level output voltage   | I <sub>OL</sub> = 4 mA <sup>(2)</sup> |              |                     | 0.2          | V    |
| Top             | Operating temperature range  |                                       | -40          |                     | +85          | °C   |

1. Typical specifications are not guaranteed.
2. 4 mA is the minimum driving capability, i.e. the minimum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V<sub>OH</sub> and V<sub>OL</sub>.

## 4.3 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

**Table 4. Temperature sensor characteristics**

| Symbol              | Parameter                                     | Test condition | Min. | Typ. <sup>(1)</sup> | Max. | Unit   |
|---------------------|---|----------------|------|---------------------|------|--------|
| TODR <sup>(2)</sup> | Temperature refresh rate                      |                |      | 52                  |      | Hz     |
| Toff                | Temperature offset <sup>(3)</sup>             |                | -15  |                     | +15  | °C     |
| TSen                | Temperature sensitivity                       |                |      | 256                 |      | LSB/°C |
| TST                 | Temperature stabilization time <sup>(4)</sup> |                |      |                     | 500  | µs     |
| T_ADC_res           | Temperature ADC resolution                    |                |      | 16                  |      | bit    |
| Top                 | Operating temperature range                   |                | -40  |                     | +85  | °C     |

1. Typical specifications are not guaranteed.
2. When the accelerometer is in low-power mode and the gyroscope part is turned off, the TODR value is equal to the accelerometer ODR.
3. The output of the temperature sensor is 0 LSB (typ.) at 25 °C.
4. Time from power ON to valid output data. Based on characterization data.

## 4.4 Communication interface characteristics

### 4.4.1 SPI - serial peripheral interface

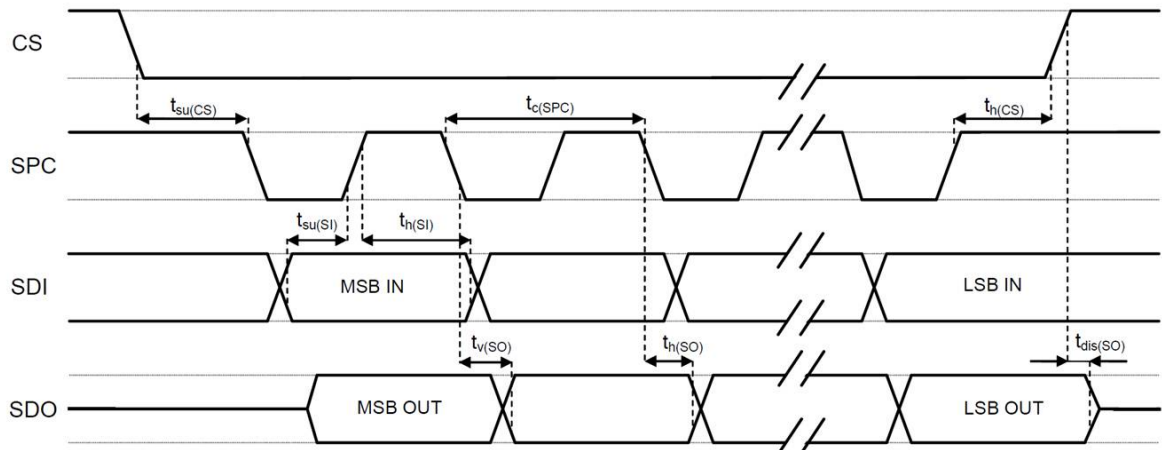
Subject to general operating conditions for Vdd and Top.

**Table 5. SPI slave timing values (in mode 3)**

| Symbol        | Parameter               | Value <sup>(1)</sup> |     | Unit |
|---------------|-------------------------|----------------------|-----|------|
|               |                         | Min                  | Max |      |
| $t_{c(SPC)}$  | SPI clock cycle         | 100                  |     | ns   |
| $f_{c(SPC)}$  | SPI clock frequency     |                      | 10  | MHz  |
| $t_{su(CS)}$  | CS setup time           | 5                    |     | ns   |
| $t_{h(CS)}$   | CS hold time            | 20                   |     |      |
| $t_{su(SI)}$  | SDI input setup time    | 5                    |     |      |
| $t_{h(SI)}$   | SDI input hold time     | 15                   |     |      |
| $t_{v(SO)}$   | SDO valid output time   |                      | 50  |      |
| $t_{h(SO)}$   | SDO output hold time    | 5                    |     |      |
| $t_{dis(SO)}$ | SDO output disable time |                      | 50  |      |

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

**Figure 6. SPI slave timing diagram (in mode 3)**



Note: Measurement points are done at 0.3·Vdd\_IO and 0.7·Vdd\_IO for both input and output ports.

#### 4.4.2 I<sup>2</sup>C - inter-IC control interface

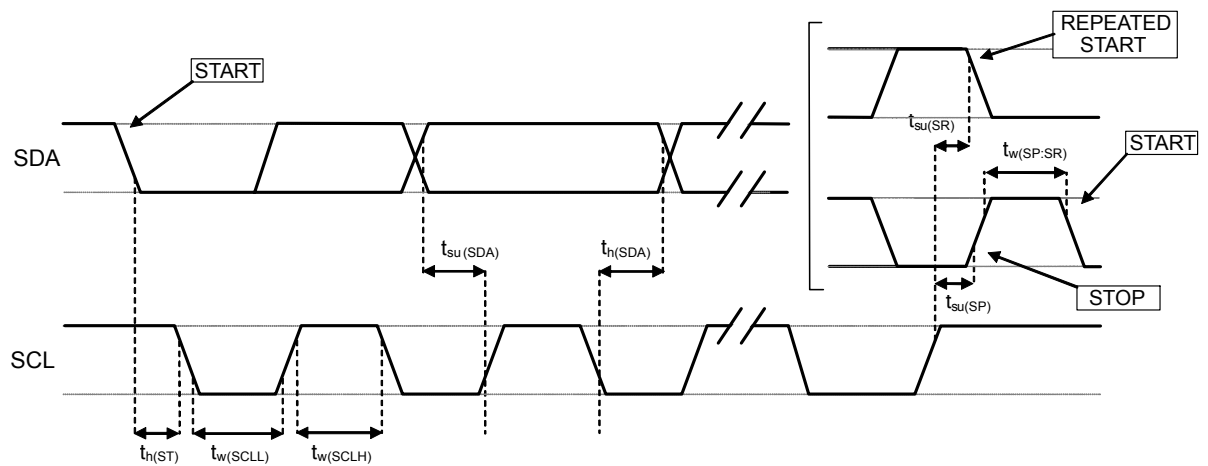
Subject to general operating conditions for V<sub>dd</sub> and Top.

**Table 6. I<sup>2</sup>C slave timing values**

| Symbol                | Parameter                                      | I <sup>2</sup> C fast mode <sup>(1)(2)</sup> |     | I <sup>2</sup> C fast mode + <sup>(1)(2)</sup> |      | Unit |
|-----------------------|--|--|-----|--|------|------|
|                       |  | Min  | Max | Min  | Max  |      |
| f <sub>(SCL)</sub>    | SCL clock frequency                            | 0  | 400 | 0  | 1000 | kHz  |
| t <sub>w(SCLL)</sub>  | SCL clock low time                             | 1.3  |     | 0.5  |      | μs   |
| t <sub>w(SCLH)</sub>  | SCL clock high time                            | 0.6  |     | 0.26   |      |      |
| t <sub>su(SDA)</sub>  | SDA setup time                                 | 100  |     | 50   |      | ns   |
| t <sub>h(SDA)</sub>   | SDA data hold time                             | 0  | 0.9 | 0  |      | μs   |
| t <sub>h(ST)</sub>    | START/REPEATED START condition hold time       | 0.6  |     | 0.26   |      |      |
| t <sub>su(SR)</sub>   | REPEATED START condition setup time            | 0.6  |     | 0.26   |      |      |
| t <sub>su(SP)</sub>   | STOP condition setup time                      | 0.6  |     | 0.26   |      |      |
| t <sub>w(SP:SR)</sub> | Bus free time between STOP and START condition | 1.3  |     | 0.5  |      |      |
|                       | Data valid time                                |  | 0.9 |  | 0.45 |      |
|                       | Data valid acknowledge time                    |  | 0.9 |  | 0.45 |      |
| C <sub>B</sub>        | Capacitive load for each bus line              |  | 400 |  | 550  | pF   |

1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.
2. Data for I<sup>2</sup>C fast mode and I<sup>2</sup>C fast mode + have been validated by characterization, not tested in production.

**Figure 7. I<sup>2</sup>C slave timing diagram**



Note: Measurement points are done at 0.3·V<sub>dd\_IO</sub> and 0.7·V<sub>dd\_IO</sub> for both ports.

## 4.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 7. Absolute maximum ratings**

| Symbol           | Ratings   | Maximum value                  | Unit     |
|------------------|---|--------------------------------|----------|
| Vdd              | Supply voltage  | -0.3 to 4.8                    | V        |
| T <sub>STG</sub> | Storage temperature range   | -40 to +125                    | °C       |
| Sg               | Acceleration <i>g</i> for 0.2 ms  | 20,000                         | <i>g</i> |
| ESD              | Electrostatic discharge protection (HBM)  | 2                              | kV       |
| V <sub>in</sub>  | Input voltage on any control pin<br>(including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0) | -0.3 to Vdd <sub>IO</sub> +0.3 | V        |

*Note: Supply voltage on any pin should never exceed 4.8 V.*



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

## 4.6 Terminology

### 4.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 g acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so,  $\pm 1$  g acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors (see [Table 2](#)).

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time (see [Table 2](#)).

### 4.6.2 Zero-g and zero-rate level

Linear acceleration zero-g level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 g on both the X-axis and Y-axis, whereas the Z-axis will measure 1 g. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called zero-g offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-g level change vs. temperature" in [Table 2](#). The zero-g level tolerance (TyOff) describes the standard deviation of the range of zero-g levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time (see [Table 2](#)).



## 5 Digital interfaces

### 5.1 I<sup>2</sup>C/SPI interface

The registers embedded inside the LSM6DSRX may be accessed through both the I<sup>2</sup>C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode. The device is compatible with SPI modes 0 and 3.

The serial interfaces are mapped onto the same pins. To select/exploit the I<sup>2</sup>C interface, the CS line must be tied high (i.e connected to Vdd\_IO).

**Table 8. Serial interface pin description**

| Pin name    | Pin description   |
|-------------|---|
| CS          | SPI enable<br>I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled;<br>0: SPI communication mode / I <sup>2</sup> C disabled) |
| SCL/SPC     | I <sup>2</sup> C Serial Clock (SCL)<br>SPI Serial Port Clock (SPC)  |
| SDA/SDI/SDO | I <sup>2</sup> C Serial Data (SDA)<br>SPI Serial Data Input (SDI)<br>3-wire Interface Serial Data Output (SDO)  |
| SDO/SA0     | SPI Serial Data Output (SDO)<br>I <sup>2</sup> C less significant bit of the device address   |

#### 5.1.1 I<sup>2</sup>C serial interface

The LSM6DSRX I<sup>2</sup>C is a bus slave. The I<sup>2</sup>C is employed to write the data to the registers, whose content can also be read back.

The relevant I<sup>2</sup>C terminology is provided in the table below.

**Table 9. I<sup>2</sup>C terminology**

| Term        | Description  |
|-------------|--|
| Transmitter | The device which sends data to the bus   |
| Receiver    | The device which receives data from the bus  |
| Master      | The device which initiates a transfer, generates clock signals and terminates a transfer |
| Slave       | The device addressed by the master   |

There are two signals associated with the I<sup>2</sup>C bus: the serial clock line (SCL) and the Serial DATA line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd\_IO through external pull-up resistors. When the bus is free, both the lines are high.

The I<sup>2</sup>C interface is implemented with fast mode (400 kHz) I<sup>2</sup>C standards as well as with fast mode plus (1000 kHz).

In order to disable the I<sup>2</sup>C block, (I2C\_disable) = 1 must be written in CTRL4\_C (13h).

### 5.1.1.1 I<sup>2</sup>C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave ADDRESS (SAD) associated to the LSM6DSRX is 110101xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the supply voltage, LSb is '1' (address 1101011b); else if the SDO/SA0 pin is connected to ground, the LSb value is '0' (address 1101010b). This solution permits to connect and address two different inertial modules to the same I<sup>2</sup>C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I<sup>2</sup>C embedded inside the LSM6DSRX behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The increment of the address is configured by the CTRL3\_C (12h) (IF\_INC).

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. Table 10 explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

**Table 10. SAD+Read/Write patterns**

| Command | SAD[6:1] | SAD[0] = SA0 | R/W | SAD+R/W        |
|---------|----------|--------------|-----|----------------|
| Read    | 110101   | 0            | 1   | 11010101 (D5h) |
| Write   | 110101   | 0            | 0   | 11010100 (D4h) |
| Read    | 110101   | 1            | 1   | 11010111 (D7h) |
| Write   | 110101   | 1            | 0   | 11010110 (D6h) |

**Table 11. Transfer when master is writing one byte to slave**

|        |    |         |     |     |     |      |     |    |
|--------|----|---------|-----|-----|-----|------|-----|----|
| Master | ST | SAD + W |     | SUB |     | DATA |     | SP |
| Slave  |    |         | SAK |     | SAK |      | SAK |    |

**Table 12. Transfer when master is writing multiple bytes to slave**

|        |    |         |     |     |     |      |     |      |     |    |
|--------|----|---------|-----|-----|-----|------|-----|------|-----|----|
| Master | ST | SAD + W |     | SUB |     | DATA |     | DATA |     | SP |
| Slave  |    |         | SAK |     | SAK |      | SAK |      | SAK |    |

**Table 13. Transfer when master is receiving (reading) one byte of data from slave**

|        |    |         |     |     |     |    |         |     |      |      |    |
|--------|----|---------|-----|-----|-----|----|---------|-----|------|------|----|
| Master | ST | SAD + W |     | SUB |     | SR | SAD + R |     |      | NMAK | SP |
| Slave  |    |         | SAK |     | SAK |    |         | SAK | DATA |      |    |

**Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave**

|        |    |       |     |     |     |    |       |     |      |     |      |     |      |      |    |
|--------|----|-------|-----|-----|-----|----|-------|-----|------|-----|------|-----|------|------|----|
| Master | ST | SAD+W |     | SUB |     | SR | SAD+R |     |      | MAK |      | MAK |      | NMAK | SP |
| Slave  |    |       | SAK |     | SAK |    |       | SAK | DATA |     | DATA |     | DATA |      |    |

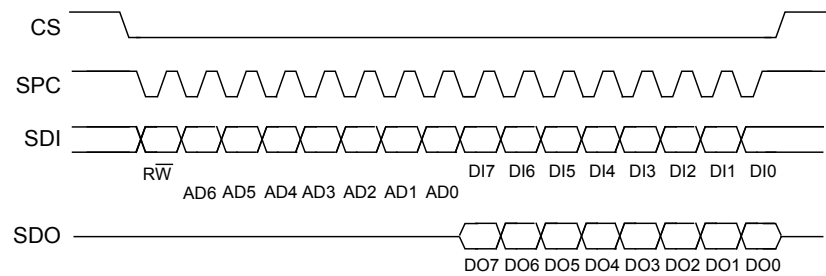
Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In the presented communication format MAK is master acknowledge and NMAK is no master acknowledge.

### 5.1.2 SPI bus interface

The LSM6DSRX SPI is a bus slave. The SPI allows writing and reading the registers of the device. The serial interface communicates with the application using 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

**Figure 8. Read and write protocol (in mode 3)**



**CS** is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

**bit 0**:  $\overline{RW}$  bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

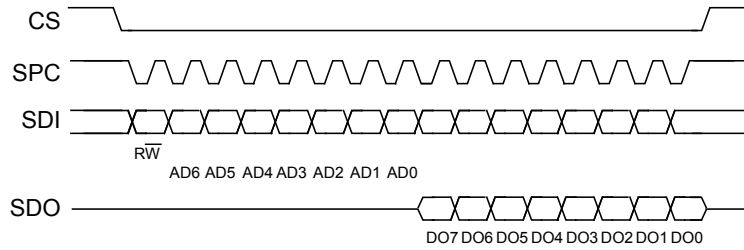
**bit 1-7**: address AD(6:0). This is the address field of the indexed register.

**bit 8-15**: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

**bit 8-15**: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the **CTRL3\_C** (12h) (IF\_INC) bit is '0', the address used to read/write data remains the same for every block. When the **CTRL3\_C** (12h) (IF\_INC) bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

**5.1.2.1 SPI read**
**Figure 9. SPI read protocol (in mode 3)**


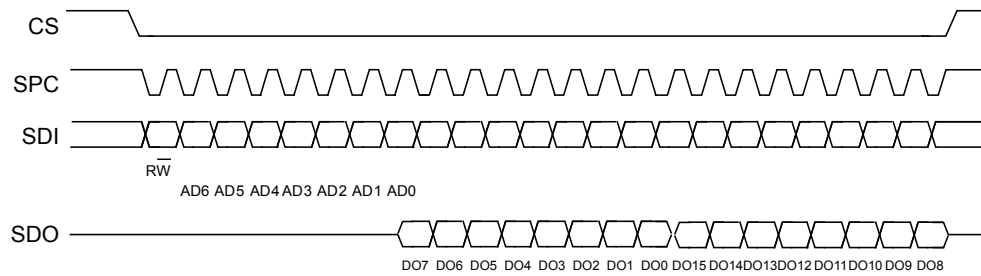
The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

**bit 0:** READ bit. The value is 1.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

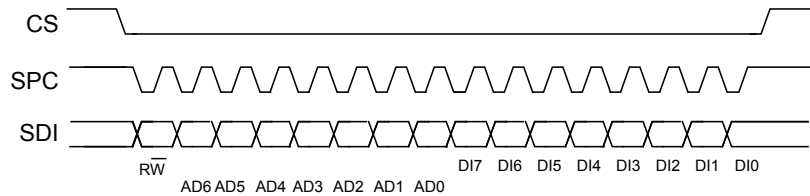
**bit 8-15:** data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

**bit 16-....:** data DO(...-8). Further data in multiple byte reads.

**Figure 10. Multiple byte SPI read protocol (2-byte example) (in mode 3)**


5.1.2.2 SPI write

Figure 11. SPI write protocol (in mode 3)



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

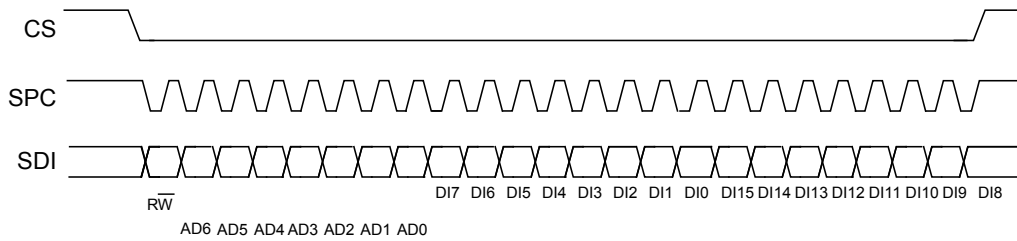
**bit 0:** WRITE bit. The value is 0.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

**bit 16-...** : data DI(...-8). Further data in multiple byte writes.

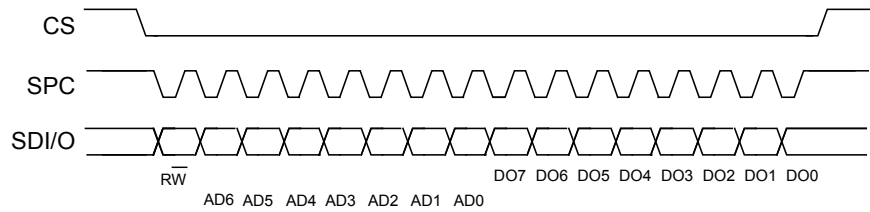
Figure 12. Multiple byte SPI write protocol (2-byte example) (in mode 3)



### 5.1.2.3 SPI read in 3-wire mode

A 3-wire mode is entered by setting the CTRL3\_C (12h) (SIM) bit equal to '1' (SPI serial interface mode selection).

**Figure 13. SPI read protocol in 3-wire mode (in mode 3)**



The SPI read command is performed with 16 clock pulses:

**bit 0:** READ bit. The value is 1.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

## 5.2 MIPI I3C<sup>SM</sup> interface

### 5.2.1 MIPI I3C<sup>SM</sup> slave interface

The LSM6DSRX interface includes a MIPI I3C<sup>SM</sup> SDR only slave interface (compliant with release 1.0 of the specification) with MIPI I3C<sup>SM</sup> SDR embedded features:

- CCC command
- Direct CCC communication (SET and GET)
- Broadcast CCC communication
- Private communications
- Private read and write for single byte
- Multiple read and write
- In-Band Interrupt request
- Error Detection and Recovery Methods (S0-S6)

*Note: Refer to Section 5.3 I<sup>2</sup>C/I3C coexistence in LSM6DSRX for details concerning the choice of the interface when powering up the device.*

### 5.2.2 MIPI I3C<sup>SM</sup> CCC supported commands

The list of MIPI I3C<sup>SM</sup> CCC commands supported by the device is detailed in the following table.

**Table 15. MIPI I3C<sup>SM</sup> CCC commands**

| Command  | Command code | Default                      | Description  |
|----------|--------------|------------------------------|--|
| ENTDAA   | 0x07         |                              | DAA procedure  |
| SETDASA  | 0x87         |                              | Assign Dynamic Address using Static Address 0x6B/0x6A depending on SDO pin |
| ENEC     | 0x80 / 0x00  |                              | Slave activity control (direct and broadcast)                              |
| DISEC    | 0x81 / 0x01  |                              | Slave activity control (direct and broadcast)                              |
| ENTAS0   | 0x82 / 0x02  |                              | Enter activity state (direct and broadcast)                                |
| ENTAS1   | 0x83 / 0x03  |                              | Enter activity state (direct and broadcast)                                |
| ENTAS2   | 0x84 / 0x04  |                              | Enter activity state (direct and broadcast)                                |
| ENTAS3   | 0x85 / 0x05  |                              | Enter activity state (direct and broadcast)                                |
| SETXTIME | 0x98 / 0x28  |                              | Timing information exchange  |
| GETXTIME | 0x99         | 0x07<br>0x00<br>0x05<br>0x92 | Timing information exchange  |
| RSTDAA   | 0x86 / 0x06  |                              | Reset the assigned dynamic address (direct and broadcast)                  |
| SETMWL   | 0x89 / 0x08  |                              | Define maximum write length during private write (direct and broadcast)    |
| SETMRL   | 0x8A / 0x09  |                              | Define maximum read length during private read (direct and broadcast)      |
| SETNEWDA | 0x88         |                              | Change dynamic address   |
| GETMWL   | 0x8B         | 0x00<br>0x08<br>(2 byte)     | Get maximum write length during private write                              |
| GETMRL   | 0x8C         | 0x00<br>0x10<br>0x09         | Get maximum read length during private read                                |



| Command   | Command code | Default                                      | Description  |
|-----------|--------------|--|--|
|           |              | (3 byte)                                     |  |
| GETPID    | 0x8D         | 0x02<br>0x08<br>0x00<br>0x6B<br>0x10<br>0x0B | Device ID register                                     |
| GETBCR    | 0x8E         | 0x07<br>(1 byte)                             | Bus characteristics register                           |
| GETDCR    | 0x8F         | 0x00   | MIPI I3C <sup>SM</sup> device characteristics register |
| GETSTATUS | 0x90         | 0x00<br>0x00<br>(2 byte)                     | Status register  |
| GETMXDS   | 0x94         | 0x00<br>0x38<br>(2 byte)                     | Return max data speed                                  |

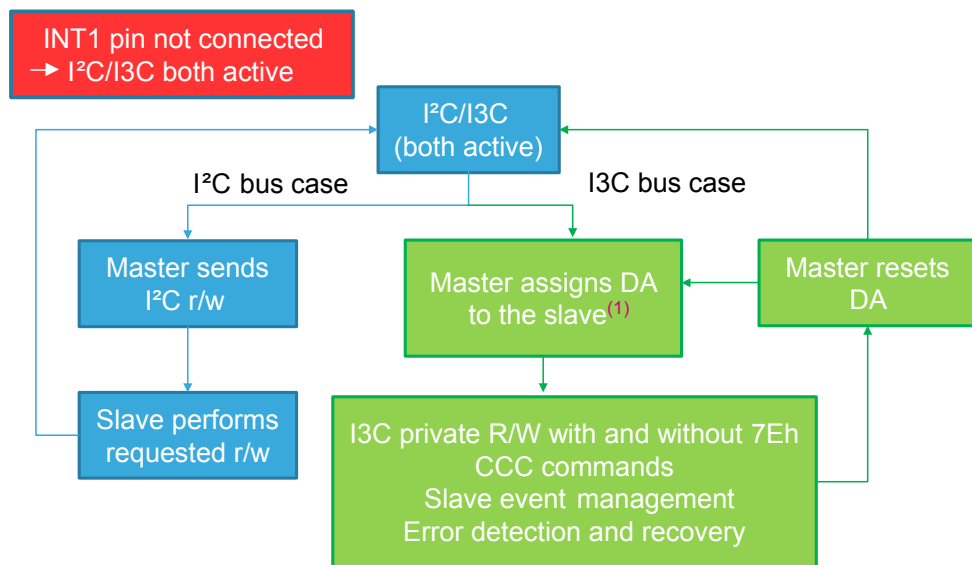
### 5.3 I<sup>2</sup>C/I<sup>3</sup>C coexistence in LSM6DSRX

In the LSM6DSRX, the SDA and SCL lines are common to both I<sup>2</sup>C and I<sup>3</sup>C. The I<sup>2</sup>C bus requires anti-spike filters on the SDA and SCL pins that are not compatible with I<sup>3</sup>C timing.

The device can be connected to both I<sup>2</sup>C and I<sup>3</sup>C or only to the I<sup>3</sup>C bus depending on the connection of the INT1 pin when the device is powered up:

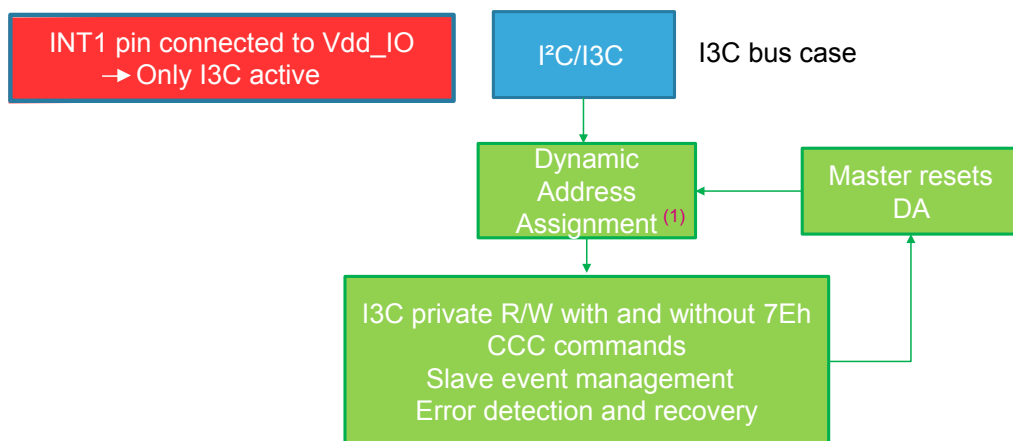
- INT1 pin floating (internal pull-down): I<sup>2</sup>C/I<sup>3</sup>C both active, see Figure 14
- INT1 pin connected to Vdd\_IO: only I<sup>3</sup>C active, see Figure 15

Figure 14. I<sup>2</sup>C and I<sup>3</sup>C both active (INT1 pin not connected)



1. Address assignment (DAA or ENTDA) must be performed with I<sup>2</sup>C Fast Mode Plus Timing. When the slave is addressed, the I<sup>2</sup>C slave is disabled and the timing is compatible with I<sup>3</sup>C specifications.

Figure 15. Only I<sup>3</sup>C active (INT1 pin connected to Vdd\_IO)



1. When the slave is I<sup>3</sup>C only, the I<sup>2</sup>C slave is always disabled. The address can be assigned using I<sup>3</sup>C SDR timing.

## 5.4 Master I<sup>2</sup>C interface

If the LSM6DSRX is configured in Mode 2, a master I<sup>2</sup>C line is available. The master serial interface is mapped in the following dedicated pins.

**Table 16. Master I<sup>2</sup>C pin details**

| Pin name | Pin description   |
|----------|---|
| MSCL     | I <sup>2</sup> C serial clock master                    |
| MSDA     | I <sup>2</sup> C serial data master                     |
| MDRDY    | I <sup>2</sup> C master external synchronization signal |

## 5.5 Auxiliary SPI interface

If the LSM6DSRX is configured in Mode 3 or Mode 4, the auxiliary SPI is available. The auxiliary SPI interface is mapped to the following dedicated pins.

**Table 17. Auxiliary SPI pin details**

| Pin name | Pin description  |
|----------|--|
| OCS_Aux  | Auxiliary SPI 3/4-wire enable  |
| SDx      | Auxiliary SPI 3/4-wire data input (SDI_Aux) and SPI 3-wire data output (SDO_Aux) |
| SCx      | Auxiliary SPI 3/4-wire interface serial port clock                               |
| SDO_Aux  | Auxiliary SPI 4-wire data output (SDO_Aux)                                       |

When the LSM6DSRX is configured in Mode 3 or Mode 4, the auxiliary SPI can be connected to a camera module for OIS/EIS support. In this configuration, the auxiliary SPI can write only to the dedicated registers [INT\\_OIS \(6Fh\)](#), [CTRL1\\_OIS \(70h\)](#), [CTRL2\\_OIS \(71h\)](#), [CTRL3\\_OIS \(72h\)](#). All the registers are accessible in Read mode from both the primary interface and auxiliary SPI.

Mode 3 is enabled when the OIS\_EN\_SPI2 bit in [CTRL1\\_OIS \(70h\)](#) register is set to 1.

Mode 4 is enabled when both the OIS\_EN\_SPI2 bit and the Mode4\_EN bit in [CTRL1\\_OIS \(70h\)](#) register are set to 1.

## 6 Functionality

### 6.1 Operating modes

In the LSM6DSRX, the accelerometer and the gyroscope can be turned on/off independently of each other and are allowed to have different ODRs and power modes.

The LSM6DSRX has three operating modes available:

- only accelerometer active and gyroscope in power-down or sleep mode
- only gyroscope active and accelerometer in power-down
- both accelerometer and gyroscope sensors active with independent ODR

The accelerometer is activated from power-down by writing ODR\_XL[3:0] in **CTRL1\_XL (10h)** while the gyroscope is activated from power-down by writing ODR\_G[3:0] in **CTRL2\_G (11h)**. For combo-mode the ODRs are totally independent.

### 6.2 Gyroscope power modes

In the LSM6DSRX, the gyroscope can be configured in four different operating modes: power-down, low-power, normal mode and high-performance mode. The operating mode selected depends on the value of the G\_HM\_MODE bit in **CTRL7\_G (16h)**. If G\_HM\_MODE is set to '0', high-performance mode is valid for all ODRs (from 12.5 Hz up to 6.66 kHz).

To enable the low-power and normal mode, the G\_HM\_MODE bit has to be set to '1'. Low-power mode is available for lower ODRs (12.5, 26, 52 Hz) while normal mode is available for ODRs equal to 104 and 208 Hz.

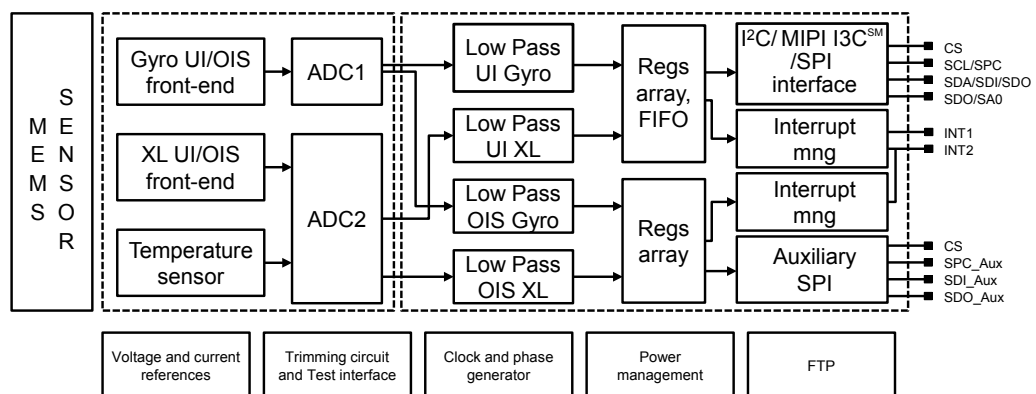
### 6.3 Accelerometer power modes

In the LSM6DSRX, the accelerometer can be configured in four different operating modes: power-down, low-power, normal mode and high-performance mode. The operating mode selected depends on the value of the XL\_HM\_MODE bit in **CTRL6\_C (15h)**. If XL\_HM\_MODE is set to '0', high-performance mode is valid for all ODRs (from 12.5 Hz up to 6.66 kHz).

To enable the low-power and normal mode, the XL\_HM\_MODE bit has to be set to '1'. Low-power mode is available for lower ODRs (1.6, 12.5, 26, 52 Hz) while normal mode is available for ODRs equal to 104 and 208 Hz.

### 6.4 Block diagram of filters

**Figure 16. Block diagram of filters**



### 6.4.1 Block diagrams of the accelerometer filters

In the LSM6DSRX, the filtering chain for the accelerometer part is composed of the following:

- Digital filter (LPF1)
- Composite filter

Details of the block diagram appear in the following figure.

Figure 17. Accelerometer UI chain

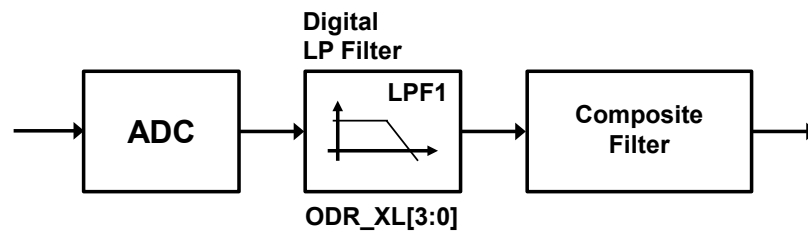
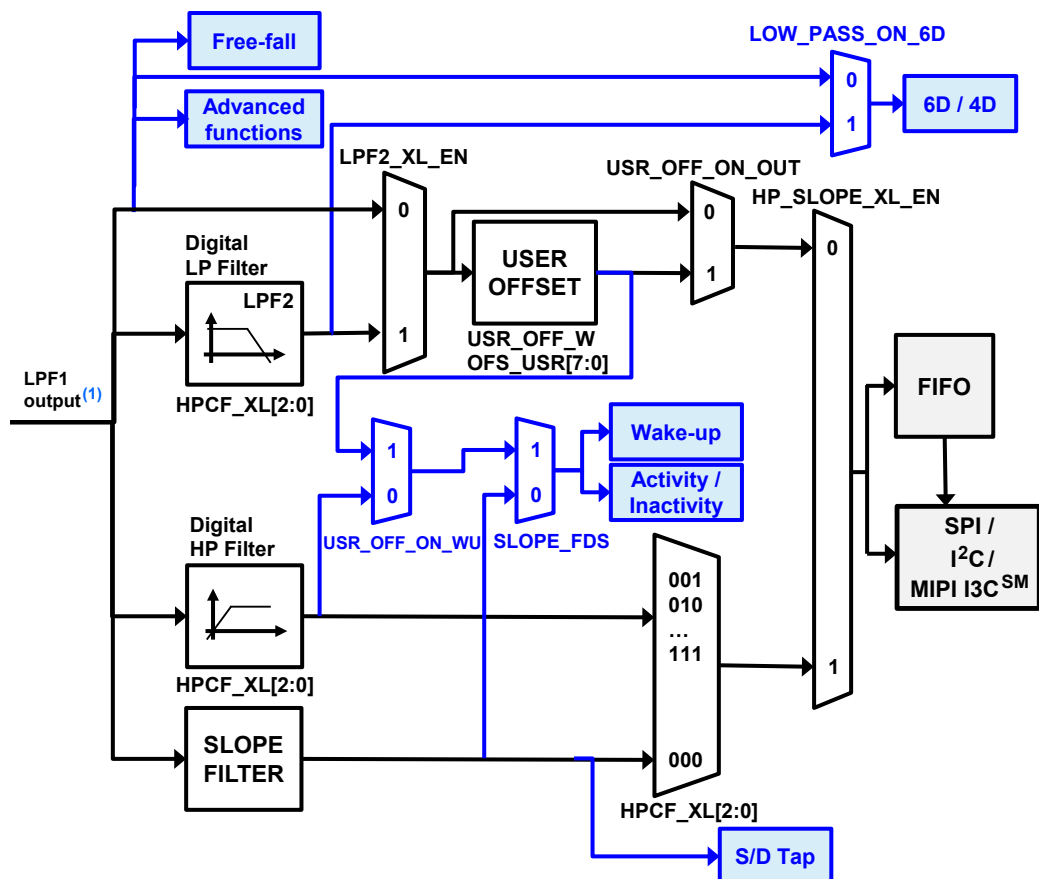


Figure 18. Accelerometer composite filter

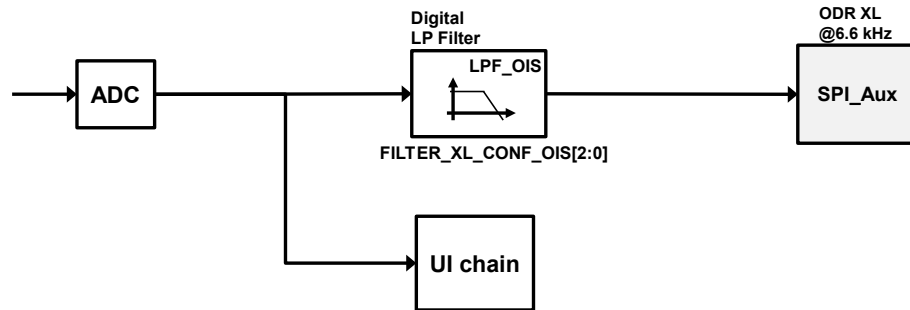


1. The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode and ODR up to 833 Hz. This value is equal to 780 Hz when the accelerometer is in low-power or normal mode.

*Note: Advanced functions include pedometer, step detector and step counter, significant motion detection, tilt function, Finite State Machine and Machine Learning Core.*

The accelerometer filtering chain when Mode 4 is enabled is illustrated in the following figure.

Figure 19. Accelerometer chain with Mode 4 enabled



Note: Mode 4 is enabled when  $Mode4\_EN = 1$  and  $OIS\_EN\_SPI2 = 1$  in  $CTRL1\_OIS$  (70h).

The configuration of the accelerometer UI chain is not affected by enabling Mode 4.

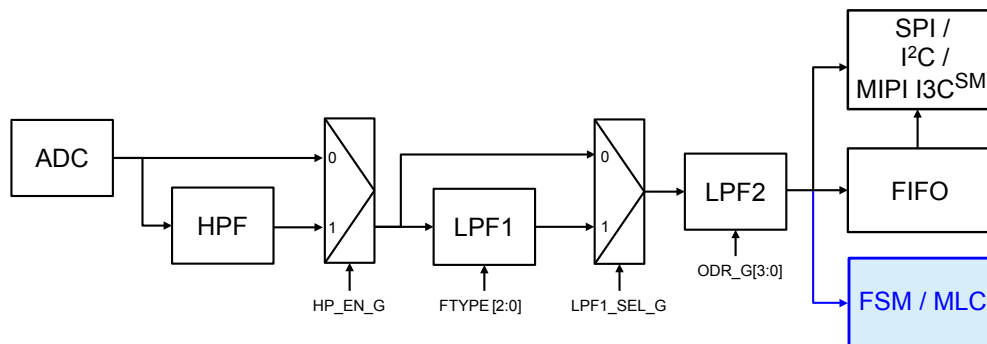
Accelerometer output values are in registers  $OUTX\_L\_A$  (28h) and  $OUTX\_H\_A$  (29h) through  $OUTZ\_L\_A$  (2Ch) and  $OUTZ\_H\_A$  (2Dh) and ODR at 6.66 kHz.

#### 6.4.2 Block diagrams of the gyroscope filters

In the LSM6DSRX, the gyroscope filtering chain depends on the mode configuration:

- Mode 1 (for User Interface (UI) and Electronic Image Stabilization (EIS) functionality through primary interface) and Mode 2

Figure 20. Gyroscope digital chain - Mode 1 (UI/EIS) and Mode 2



In this configuration, the gyroscope ODR is selectable from 12.5 Hz up to 6.66 kHz. A low-pass filter (LPF1) is available if the auxiliary SPI is disabled, for more details about the filter characteristics see [Table 65. Gyroscope LPF1 bandwidth selection](#).

The digital LPF2 filter cannot be configured by the user and its cutoff frequency depends on the selected gyroscope ODR, as indicated in the following table.

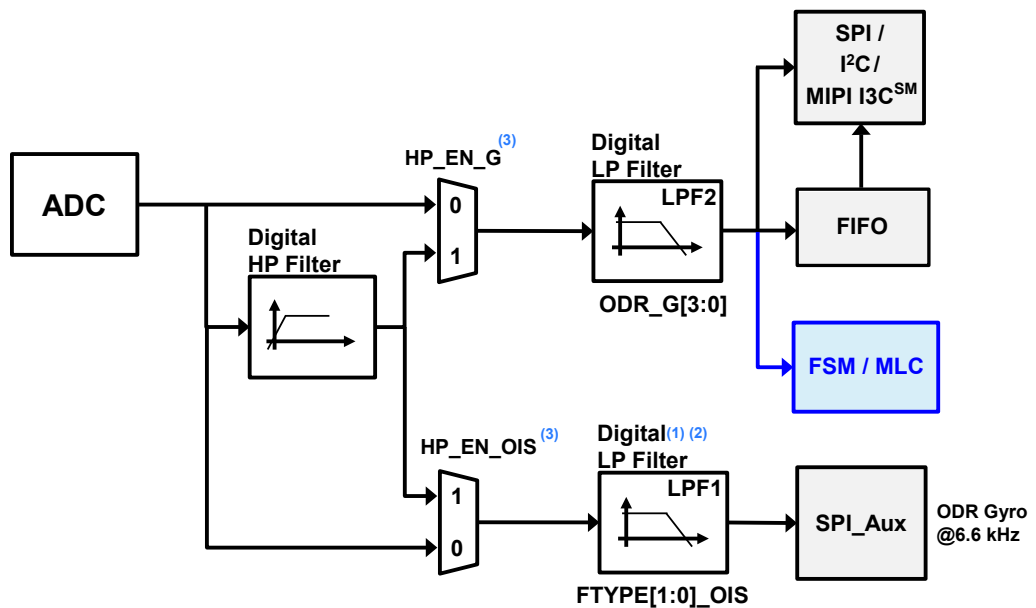
Table 18. Gyroscope LPF2 bandwidth selection

| Gyroscope ODR [Hz] | LPF2 cutoff [Hz] |
|--------------------|------------------|
| 12.5               | 4.3              |
| 26                 | 8.3              |
| 52                 | 16.7             |
| 104                | 33               |
| 208                | 67               |
| 417                | 133              |
| 833                | 267              |
| 1667               | 539              |
| 3333               | 1137             |
| 6667               | 3333             |

Data can be acquired from the output registers and FIFO over the primary I<sup>2</sup>C/I<sup>3</sup>C/SPI interface.

- Mode 3 / Mode 4 (for OIS and EIS functionality)

Figure 21. Gyroscope digital chain - Mode 3 / Mode 4 (OIS/EIS)



1. When Mode3/4 is enabled, the LPF1 filter is not available in the gyroscope UI chain.
2. It is recommended to avoid using the LPF1 filter in Mode1/2 when Mode3/4 is intended to be used.
3. HP\_EN\_OIS can be used to select the HPF on the OIS path only if the HPF is not used in the UI chain. If both the HP\_EN\_G bit and HP\_EN\_OIS bit are set to 1, the HP filter is applied to the UI chain only.

*Note: When S4S is enabled in the UI chain, the HPF is not available in the OIS chain.*

The auxiliary interface needs to be enabled in CTRL1\_OIS (70h).

In Mode 3/4 configuration, there are two paths:

- the chain for User Interface (UI) where the ODR is selectable from 12.5 Hz up to 6.66 kHz

- the chain for OIS/EIS where the ODR is at 6.66 kHz and the LPF1 is available. The LPF1 configuration depends on the setting of the FTYPE\_[1:0]\_OIS bit in register CTRL2\_OIS (71h); for more details about the filter characteristics see Table 160. Gyroscope OIS chain digital LPF1 filter bandwidth selection. Gyroscope output values are in registers 22h to 27h with the selected full scale (FS[1:0]\_G\_OIS bit in CTRL1\_OIS (70h)).

## 6.5 OIS

This paragraph describes OIS functionality and the dedicated accelerometer-gyroscope DSP chain.

There is a dedicated gyroscope and accelerometer DSP for OIS.

Other features can be configured:

- Self-test on OIS side
- DEN on OIS side

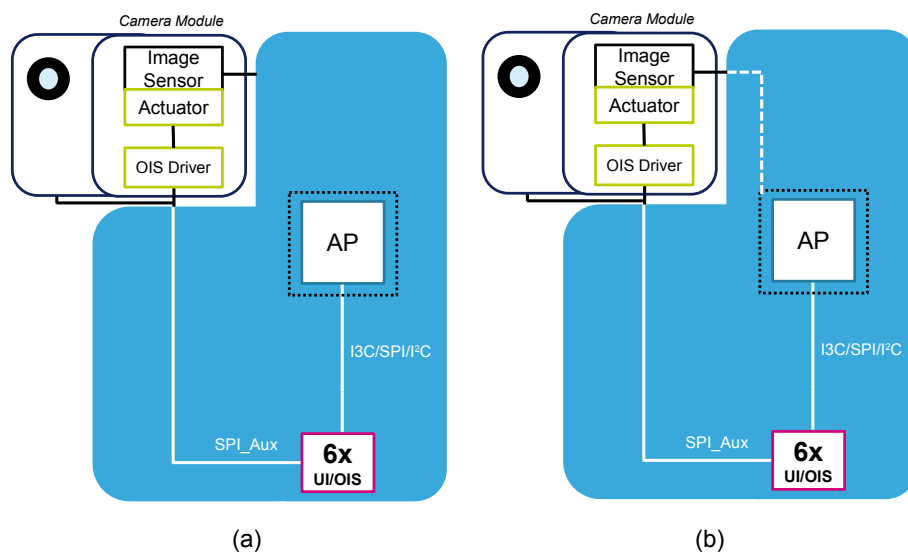
The camera module is completely independent from the application processor as shown in Figure 22.

The Auxiliary SPI can configure OIS functionality through INT\_OIS (6Fh), CTRL1\_OIS (70h), CTRL2\_OIS (71h), CTRL3\_OIS (72h).

Reading from the Auxiliary SPI is enabled only when the OIS\_EN\_SPI2 bit in the CTRL1\_OIS (70h) register is set to '1'. This bit also turns on the gyroscope OIS chain.

The Primary Interface can access the OIS control registers (INT\_OIS (6Fh), CTRL1\_OIS (70h), CTRL2\_OIS (71h), CTRL3\_OIS (72h)) in read mode.

**Figure 22. Auxiliary SPI full control (a) and enabling primary interface (b)**





## 6.6 FIFO

The presence of a FIFO allows consistent power saving for the system since the host processor does not need continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

The LSM6DSRX embeds 3 kbytes of data (up to 9 kbytes with the compression feature enabled) in FIFO to store the following data:

- Gyroscope
- Accelerometer
- External sensors (up to 4)
- Step counter
- Timestamp
- Temperature

Writing data in the FIFO can be configured to be triggered by the:

- Accelerometer / gyroscope data-ready signal
- Sensor hub data-ready signal
- Step detection signal

The applications have maximum flexibility in choosing the rate of batching for physical sensors with FIFO-dedicated configurations: accelerometer, gyroscope and temperature sensor batch rates can be selected by the user. External sensor writing in FIFO can be triggered by the accelerometer data-ready signal or by an external sensor interrupt. The step counter can be stored in FIFO with associated timestamp each time a step is detected. It is possible to select decimation for timestamp batching in FIFO with a factor of 1, 8, or 32.

The reconstruction of a FIFO stream is a simple task thanks to the FIFO\_DATA\_OUT\_TAG byte that allows recognizing the meaning of a word in FIFO.

FIFO allows correct reconstruction of the timestamp information for each sensor stored in FIFO. If a change in the ODR or BDR (Batch Data Rate) configuration is performed, the application can correctly reconstruct the timestamp and know exactly when the change was applied without disabling FIFO batching. FIFO stores information of the new configuration and timestamp in which the change was applied in the device.

Finally, FIFO embeds a compression algorithm that the user can enable in order to have up to 9 kbyte data stored in FIFO and take advantage of interface communication length for FIFO flushing and communication power consumption.

The programmable FIFO watermark threshold can be set in FIFO\_CTRL1 (07h) and FIFO\_CTRL2 (08h) using the WTM[8:0] bits. To monitor the FIFO status, dedicated registers (FIFO\_STATUS1 (3Ah), FIFO\_STATUS2 (3Bh)) can be read to detect FIFO overrun events, FIFO full status, FIFO empty status, FIFO watermark status and the number of unread samples stored in the FIFO. To generate dedicated interrupts on the INT1 and INT2 pins of these status events, the configuration can be set in INT1\_CTRL (0Dh) and INT2\_CTRL (0Eh).

The FIFO buffer can be configured according to six different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- Bypass-to-continuous mode
- Bypass-to-FIFO mode

Each mode is selected by the FIFO\_MODE\_[2:0] bits in the FIFO\_CTRL4 (0Ah) register.

### 6.6.1 Bypass mode

In Bypass mode (**FIFO\_CTRL4 (0Ah)**(**FIFO\_MODE\_[2:0]** = 000), the FIFO is not operational and it remains empty. Bypass mode is also used to reset the FIFO when in FIFO mode.

### 6.6.2 FIFO mode

In FIFO mode (**FIFO\_CTRL4 (0Ah)**(**FIFO\_MODE\_[2:0]** = 001) data from the output channels are stored in the FIFO until it is full.

To reset FIFO content, Bypass mode should be selected by writing **FIFO\_CTRL4 (0Ah)**(**FIFO\_MODE\_[2:0]**) to '000'. After this reset command, it is possible to restart FIFO mode by writing **FIFO\_CTRL4 (0Ah)** (**FIFO\_MODE\_[2:0]**) to '001'.

The FIFO buffer memorizes up to 9 kbytes of data (with compression enabled) but the depth of the FIFO can be resized by setting the WTM [8:0] bits in **FIFO\_CTRL1 (07h)** and **FIFO\_CTRL2 (08h)**. If the **STOP\_ON\_WTM** bit in **FIFO\_CTRL2 (08h)** is set to '1', FIFO depth is limited up to the WTM [8:0] bits in **FIFO\_CTRL1 (07h)** and **FIFO\_CTRL2 (08h)**.

### 6.6.3 Continuous mode

Continuous mode (**FIFO\_CTRL4 (0Ah)**(**FIFO\_MODE\_[2:0]** = 110) provides a continuous FIFO update: as new data arrives, the older data is discarded.

A FIFO threshold flag **FIFO\_STATUS2 (3Bh)**(**FIFO\_WTM\_IA**) is asserted when the number of unread samples in FIFO is greater than or equal to **FIFO\_CTRL1 (07h)** and **FIFO\_CTRL2 (08h)**(**WTM [8:0]**).

It is possible to route the **FIFO\_WTM\_IA** flag to the INT1 pin by writing in register **INT1\_CTRL (0Dh)** (**INT1\_FIFO\_TH**) = '1' or to the INT2 pin by writing in register **INT2\_CTRL (0Eh)**(**INT2\_FIFO\_TH**) = '1'.

A full-flag interrupt can be enabled, **INT1\_CTRL (0Dh)**(**INT1\_FIFO\_FULL**) = '1' or **INT2\_CTRL (0Eh)** (**INT2\_FIFO\_FULL**) = '1', in order to indicate FIFO saturation and eventually read its content all at once.

If an overrun occurs, at least one of the oldest samples in FIFO has been overwritten and the **FIFO\_OVR\_IA** flag in **FIFO\_STATUS2 (3Bh)** is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in **FIFO\_STATUS1 (3Ah)** and **FIFO\_STATUS2 (3Bh)**(**DIFF\_FIFO\_[9:0]**).

### 6.6.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode (**FIFO\_CTRL4 (0Ah)**(**FIFO\_MODE\_[2:0]** = 011), FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- Free-fall
- D6D

When the selected trigger bit is equal to '1', FIFO operates in FIFO mode.

When the selected trigger bit is equal to '0', FIFO operates in Continuous mode.

### 6.6.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (**FIFO\_CTRL4 (0Ah)**(**FIFO\_MODE\_[2:0]** = '100'), data measurement storage inside FIFO operates in Continuous mode when selected triggers are equal to '1', otherwise FIFO content is reset (Bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- Free-fall
- D6D

### 6.6.6 Bypass-to-FIFO mode

In Bypass-to-FIFO mode (`FIFO_CTRL4 (0Ah)`(`FIFO_MODE_[2:0] = '111'`), data measurement storage inside FIFO operates in FIFO mode when selected triggers are equal to '1', otherwise FIFO content is reset (Bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Single tap
- Double tap
- Wake-up
- Free-fall
- D6D

### 6.6.7 FIFO reading procedure

The data stored in FIFO are accessible from dedicated registers and each FIFO word is composed of 7 bytes: one tag byte (`FIFO_DATA_OUT_TAG (78h)`), in order to identify the sensor, and 6 bytes of fixed data (`FIFO_DATA_OUT` registers from `(79h)` to `(7Eh)`).

The `DIFF_FIFO_[9:0]` field in the `FIFO_STATUS1 (3Ah)` and `FIFO_STATUS2 (3Bh)` registers contains the number of words (1 byte TAG + 6 bytes DATA) collected in FIFO.

In addition, it is possible to configure a counter of the batch events of accelerometer or gyroscope sensors. The flag `COUNTER_BDR_IA` in `FIFO_STATUS2 (3Bh)` alerts that the counter reaches a selectable threshold (`CNT_BDR_TH_[10:0]` field in `COUNTER_BDR_REG1 (0Bh)` and `COUNTER_BDR_REG2 (0Ch)`). This allows triggering the reading of FIFO with the desired latency of one single sensor. The sensor is selectable using the `TRIG_COUNTER_BDR` bit in `COUNTER_BDR_REG1 (0Bh)`. As for the other FIFO status events, the flag `COUNTER_BDR_IA` can be routed on the INT1 or INT2 pins by asserting the corresponding bits (`INT1_CNT_BDR` of `INT1_CTRL (0Dh)`) and `INT2_CNT_BDR` of `INT2_CTRL (0Eh)`).

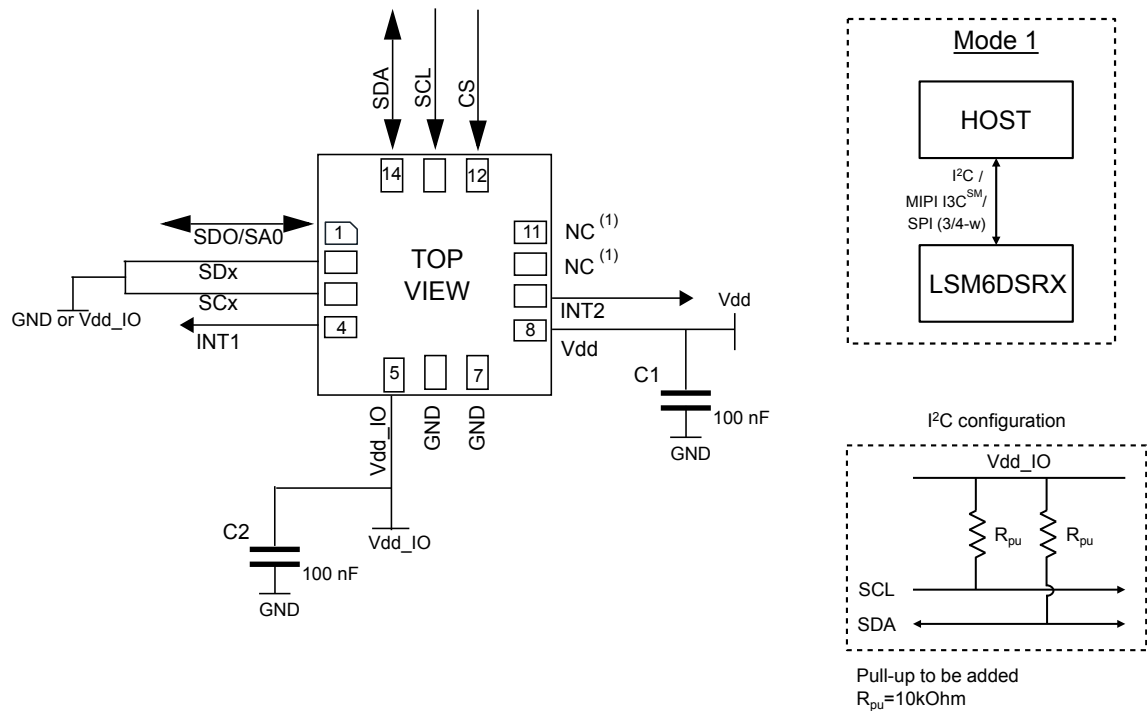
In order to maximize the amount of accelerometer and gyroscope data in FIFO, the user can enable the compression algorithm by setting to 1 both the `FIFO_COMPR_EN` bit in `EMB_FUNC_EN_B (05h)` (embedded functions registers bank) and the `FIFO_COMPR_RT_EN` bit in `FIFO_CTRL2 (08h)`. When compression is enabled, it is also possible to force writing non-compressed data at a selectable rate using the `UNCOPTR_RATE_[1:0]` field in `FIFO_CTRL2 (08h)`.

Meta information about accelerometer and gyroscope sensor configuration changes can be managed by enabling the `ODR_CHG_EN` bit in `FIFO_CTRL2 (08h)`.

## 7 Application hints

### 7.1 LSM6DSRX electrical connections in Mode 1

Figure 23. LSM6DSRX electrical connections in Mode 1



1. Leave pin electrically unconnected and soldered to PCB.

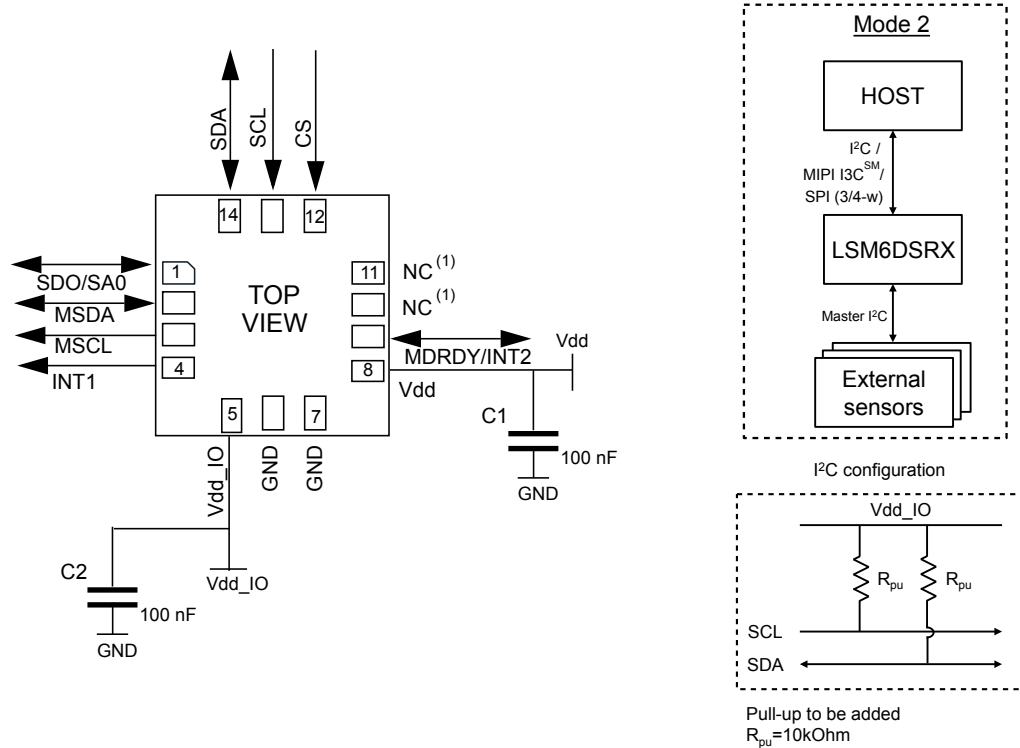
The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I<sup>2</sup>C/MIPI I3C<sup>SM</sup> interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I<sup>2</sup>C/MIPI I3C<sup>SM</sup> interface.

## 7.2 LSM6DSRX electrical connections in Mode 2

Figure 24. LSM6DSRX electrical connections in Mode 2



1. Leave pin electrically unconnected and soldered to PCB.

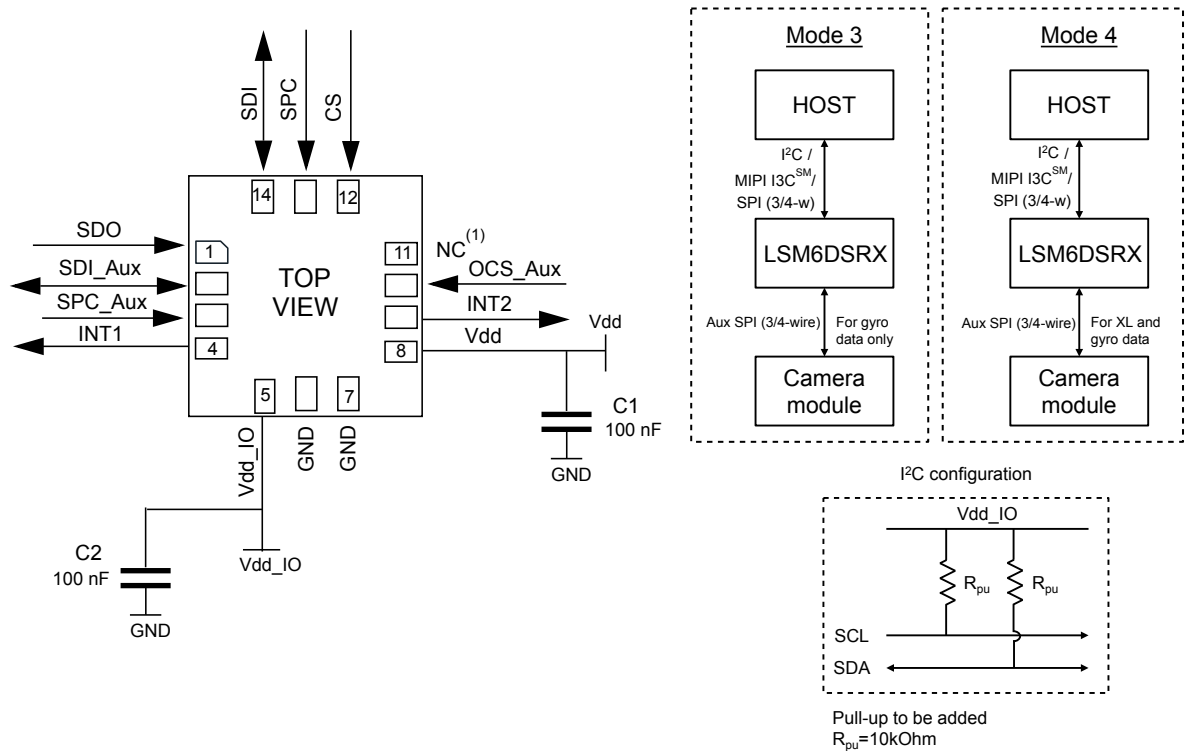
The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I<sup>2</sup>C/MIPI I3C<sup>SM</sup> primary interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I<sup>2</sup>C/MIPI I3C<sup>SM</sup> primary interface.

### 7.3 LSM6DSRX electrical connections in Mode 3 and Mode 4

Figure 25. LSM6DSRX electrical connections in Mode 3 and Mode 4 (auxiliary 3/4-wire SPI)



1. Leave pin electrically unconnected and soldered to PCB.

*Note: When Mode 3 and 4 are used, the pull-up on pins 10 and 11 can be disabled (refer to Table 19. Internal pin status). To avoid leakage current, it is recommended to add pull-up resistors on the SPI lines unless the SPI master can be left on while the OIS system is off.*

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device is selectable and accessible through the SPI/I<sup>2</sup>C/MIPI I3C<sup>SM</sup> primary interface.

Measured acceleration/angular rate data is selectable and accessible through the SPI/I<sup>2</sup>C/MIPI I3C<sup>SM</sup> primary interface and auxiliary SPI.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I<sup>2</sup>C/MIPI I3C<sup>SM</sup> interface.

Table 19. Internal pin status

| pin# | Name    | Mode 1 function  | Mode 2 function  | Mode 3 / Mode 4 function   | Pin status Mode 1  | Pin status Mode 2  |
|------|---------|--|--|--|--|--|
| 1    | SDO     | SPI 4-wire interface serial data output (SDO)  | SPI 4-wire interface serial data output (SDO)  | SPI 4-wire interface serial data output (SDO)  | Default: input without pull-up.<br>Pull-up is enabled if bit SDO_PU_EN = 1 in reg 02h.   | Default: input without pull-up.<br>Pull-up is enabled if bit SDO_PU_EN = 1 in reg 02h.   |
|      | SA0     | I <sup>2</sup> C least significant bit of the device address (SA0)<br>MIPI I3C <sup>SM</sup> least significant bit of the static address (SA0)         | I <sup>2</sup> C least significant bit of the device address (SA0)<br>MIPI I3C <sup>SM</sup> least significant bit of the static address (SA0)         | I <sup>2</sup> C least significant bit of the device address (SA0)<br>MIPI I3C <sup>SM</sup> least significant bit of the static address (SA0)         |  |  |
| 2    | SDx     | Connect to Vdd_IO or GND   | I <sup>2</sup> C serial data master (MSDA)   | Auxiliary SPI 3/4-wire interface serial data input (SDI) and SPI 3-wire serial data output (SDO)   | Default: input without pull-up.<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in reg 14h in sensor hub registers (see Note to enable pull-up). | Default: input without pull-up.<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in reg 14h in sensor hub registers (see Note to enable pull-up). |
| 3    | SCx     | Connect to Vdd_IO or GND   | I <sup>2</sup> C serial clock master (MSCL)  | Auxiliary SPI 3/4-wire interface serial port clock (SPC_Aux)   | Default: input without pull-up.<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in reg 14h in sensor hub registers (see Note to enable pull-up). | Default: input without pull-up.<br>Pull-up is enabled if bit SHUB_PU_EN = 1 in reg 14h in sensor hub registers (see Note to enable pull-up). |
| 4    | INT1    | Programmable interrupt 1 / If device is used as MIPI I3C <sup>SM</sup> pure slave, this pin must be set to '1'.  | Programmable interrupt 1 / If device is used as MIPI I3C <sup>SM</sup> pure slave, this pin must be set to '1'.  | Programmable interrupt 1 / If device is used as MIPI I3C <sup>SM</sup> pure slave, this pin must be set to '1'.  | Default: input with pull-down <sup>(2)</sup>   | Default: input with pull-down  |
| 5    | Vdd_IO  | Power supply for I/O pins  | Power supply for I/O pins  | Power supply for I/O pins  |  |  |
| 6    | GND     | 0 V supply   | 0 V supply   | 0 V supply   |  |  |
| 7    | GND     | 0 V supply   | 0 V supply   | 0 V supply   |  |  |
| 8    | Vdd     | Power supply   | Power supply   | Power supply   |  |  |
| 9    | INT2    | Programmable interrupt 2 (INT2) / Data enabled (DEN)   | Programmable interrupt 2 (INT2) / Data enabled (DEN) / I <sup>2</sup> C master external synchronization signal (MDRDY)                                 | Programmable interrupt 2 (INT2) / Data enabled (DEN)   | Default: output forced to ground   | Default: output forced to ground   |
| 10   | OCS_Aux | Leave unconnected  | Leave unconnected  | Auxiliary SPI 3/4-wire interface enabled   | Default: input with pull-up.<br>Pull-up is disabled if bit OIS_PU_DIS = 1 in reg 02h.  | Default: input with pull-up.<br>Pull-up is disabled if bit OIS_PU_DIS = 1 in reg 02h.  |
| 11   | SDO_Aux | Connect to Vdd_IO or leave unconnected   | Connect to Vdd_IO or leave unconnected   | Auxiliary SPI 3-wire interface: leave unconnected / Auxiliary SPI 4-wire interface: serial data output (SDO_Aux)                                       | Default: input with pull-up.<br>Pull-up is disabled if bit OIS_PU_DIS = 1 in reg 02h.  | Default: input with pull-up.<br>Pull-up is disabled if bit OIS_PU_DIS = 1 in reg 02h.  |
| 12   | CS      | I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled) | I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled) | I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled) | Default: input with pull-up.<br>Pull-up is disabled if bit I2C_disable = 1 in reg 13h and I3C_disable = 1 in reg 18h.                        | Default: input with pull-up.<br>Pull-up is disabled if bit I2C_disable = 1 in reg 13h and I3C_disable = 1 in reg 18h.                        |

| pin# | Name | Mode 1 function   | Mode 2 function   | Mode 3 / Mode 4 function  | Pin status Mode 1              | Pin status Mode 2              |
|------|------|---|---|---|--------------------------------|--------------------------------|
| 13   | SCL  | I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial clock (SCL) / SPI serial port clock (SPC)  | I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial clock (SCL) / SPI serial port clock (SPC)  | I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial clock (SCL) / SPI serial port clock (SPC)  | Default: input without pull-up | Default: input without pull-up |
| 14   | SDA  | I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO) | I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO) | I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO) | Default: input without pull-up | Default: input without pull-up |

1. Mode 3 is enabled when the *OIS\_EN\_SPI2* bit in the *CTRL1\_OIS (70h)* register is set to 1. Mode 4 is enabled when both the *OIS\_EN\_SPI2* bit and the *Mode4\_EN* bit in the *CTRL1\_OIS (70h)* register are set to 1.
2. *INT1* must be set to '0' or left unconnected during power-on if the I<sup>2</sup>C/SPI interfaces are used.

Internal pull-up value is from 30 kΩ to 50 kΩ, depending on Vdd\_IO.

*Note: The procedure to enable the pull-up on pins 2 and 3 is as follows:*

1. From the primary I<sup>2</sup>C/I3C/SPI interface : write 40h in register at address 01h (enable access to the sensor hub registers)
2. From the primary I<sup>2</sup>C/I3C/SPI interface : write 08h in register at address 14h (enable the pull-up on pins 2 and 3)
3. From the primary I<sup>2</sup>C/I3C/SPI interface : write 00h in register at address 01h (disable access to the sensor hub registers)



## 8 Register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

**Table 20. Registers address map**

| Name  | Type | Register address |          | Default  | Comment  |
|---|------|------------------|----------|----------|----------|
|   |      | Hex              | Binary   |          |          |
| FUNC_CFG_ACCESS   | RW   | 01               | 00000001 | 00000000 |          |
| PIN_CTRL  | RW   | 02               | 00000010 | 00111111 |          |
| RESERVED  | -    | 03               |          |          |          |
| S4S_TPH_L   | RW   | 04               | 00000100 | 00000000 |          |
| S4S_TPH_H   | RW   | 05               | 00000101 | 00000000 |          |
| S4S_RR  | RW   | 06               | 00000110 | 00000000 |          |
| FIFO_CTRL1  | RW   | 07               | 00000111 | 00000000 |          |
| FIFO_CTRL2  | RW   | 08               | 00001000 | 00000000 |          |
| FIFO_CTRL3  | RW   | 09               | 00001001 | 00000000 |          |
| FIFO_CTRL4  | RW   | 0A               | 00001010 | 00000000 |          |
| COUNTER_BDR_REG1  | RW   | 0B               | 00001011 | 00000000 |          |
| COUNTER_BDR_REG2  | RW   | 0C               | 00001100 | 00000000 |          |
| INT1_CTRL   | RW   | 0D               | 00001101 | 00000000 |          |
| INT2_CTRL   | RW   | 0E               | 00001110 | 00000000 |          |
| WHO_AM_I  | R    | 0F               | 00001111 | 01101011 | R (SPI2) |
| CTRL1_XL  | RW   | 10               | 00010000 | 00000000 | R (SPI2) |
| CTRL2_G   | RW   | 11               | 00010001 | 00000000 | R (SPI2) |
| CTRL3_C   | RW   | 12               | 00010010 | 00000100 | R (SPI2) |
| CTRL4_C   | RW   | 13               | 00010011 | 00000000 | R (SPI2) |
| CTRL5_C   | RW   | 14               | 00010100 | 00000000 | R (SPI2) |
| CTRL6_C   | RW   | 15               | 00010101 | 00000000 | R (SPI2) |
| CTRL7_G   | RW   | 16               | 00010110 | 00000000 | R (SPI2) |
| CTRL8_XL  | RW   | 17               | 00010111 | 00000000 | R (SPI2) |
| CTRL9_XL  | RW   | 18               | 00011000 | 11100000 | R (SPI2) |
| CTRL10_C  | RW   | 19               | 00011001 | 00000000 | R (SPI2) |
| ALL_INT_SRC   | R    | 1A               | 00011010 | output   |          |
| WAKE_UP_SRC   | R    | 1B               | 00011011 | output   |          |
| TAP_SRC   | R    | 1C               | 00011100 | output   |          |
| D6D_SRC   | R    | 1D               | 00011101 | output   |          |
| STATUS_REG <sup>(1)</sup> /STATUS_SPIAux <sup>(2)</sup> | R    | 1E               | 00011110 | output   |          |
| RESERVED  | -    | 1F               |          |          |          |
| OUT_TEMP_L  | R    | 20               | 00100000 | output   |          |
| OUT_TEMP_H  | R    | 21               | 00100001 | output   |          |

| Name                     | Type | Register address |          | Default  | Comment  |
|--------------------------|------|------------------|----------|----------|----------|
|                          |      | Hex              | Binary   |          |          |
| OUTX_L_G                 | R    | 22               | 00100010 | output   |          |
| OUTX_H_G                 | R    | 23               | 00100011 | output   |          |
| OUTY_L_G                 | R    | 24               | 00100100 | output   |          |
| OUTY_H_G                 | R    | 25               | 00100101 | output   |          |
| OUTZ_L_G                 | R    | 26               | 00100110 | output   |          |
| OUTZ_H_G                 | R    | 27               | 00100111 | output   |          |
| OUTX_L_A                 | R    | 28               | 00101000 | output   |          |
| OUTX_H_A                 | R    | 29               | 00101001 | output   |          |
| OUTY_L_A                 | R    | 2A               | 00101010 | output   |          |
| OUTY_H_A                 | R    | 2B               | 00101011 | output   |          |
| OUTZ_L_A                 | R    | 2C               | 00101100 | output   |          |
| OUTZ_H_A                 | R    | 2D               | 00101101 | output   |          |
| RESERVED                 | -    | 2E-34            |          |          |          |
| EMB_FUNC_STATUS_MAINPAGE | R    | 35               | 00110101 | output   |          |
| FSM_STATUS_A_MAINPAGE    | R    | 36               | 00110110 | output   |          |
| FSM_STATUS_B_MAINPAGE    | R    | 37               | 00110111 | output   |          |
| MLC_STATUS_MAINPAGE      | R    | 38               | 00111000 | output   |          |
| STATUS_MASTER_MAINPAGE   | R    | 39               | 00111001 | output   |          |
| FIFO_STATUS1             | R    | 3A               | 00111010 | output   |          |
| FIFO_STATUS2             | R    | 3B               | 00111011 | output   |          |
| RESERVED                 | -    | 3C-3F            |          |          |          |
| TIMESTAMP0               | R    | 40               | 01000000 | output   | R (SPI2) |
| TIMESTAMP1               | R    | 41               | 01000001 | output   | R (SPI2) |
| TIMESTAMP2               | R    | 42               | 01000010 | output   | R (SPI2) |
| TIMESTAMP3               | R    | 43               | 01000011 | output   | R (SPI2) |
| RESERVED                 | -    | 44-55            |          |          |          |
| TAP_CFG0                 | RW   | 56               | 01010110 | 00000000 |          |
| TAP_CFG1                 | RW   | 57               | 01010111 | 00000000 |          |
| TAP_CFG2                 | RW   | 58               | 01011000 | 00000000 |          |
| TAP_THS_6D               | RW   | 59               | 01011001 | 00000000 |          |
| INT_DUR2                 | RW   | 5A               | 01011010 | 00000000 |          |
| WAKE_UP_THS              | RW   | 5B               | 01011011 | 00000000 |          |
| WAKE_UP_DUR              | RW   | 5C               | 01011100 | 00000000 |          |
| FREE_FALL                | RW   | 5D               | 01011101 | 00000000 |          |
| MD1_CFG                  | RW   | 5E               | 01011110 | 00000000 |          |
| MD2_CFG                  | RW   | 5F               | 01011111 | 00000000 |          |
| S4S_ST_CMD_CODE          | RW   | 60               | 01100000 | 00000000 |          |
| S4S_DT_REG               | RW   | 61               | 01100001 | 00000000 |          |
| I3C_BUS_AVB              | RW   | 62               | 01100010 | 00000000 |          |

| Name               | Type | Register address |          | Default  | Comment   |
|--------------------|------|------------------|----------|----------|-----------|
|                    |      | Hex              | Binary   |          |           |
| INTERNAL_FREQ_FINE | R    | 63               | 01100011 | output   |           |
| RESERVED           | -    | 64-6E            |          |          |           |
| INT_OIS            | R    | 6F               | 01101111 | 00000000 | RW (SPI2) |
| CTRL1_OIS          | R    | 70               | 01110000 | 00000000 | RW (SPI2) |
| CTRL2_OIS          | R    | 71               | 01110001 | 00000000 | RW (SPI2) |
| CTRL3_OIS          | R    | 72               | 01110010 | 00000000 | RW (SPI2) |
| X_OFS_USR          | RW   | 73               | 01110011 | 00000000 |           |
| Y_OFS_USR          | RW   | 74               | 01110100 | 00000000 |           |
| Z_OFS_USR          | RW   | 75               | 01110101 | 00000000 |           |
| RESERVED           | -    | 76-77            |          |          |           |
| FIFO_DATA_OUT_TAG  | R    | 78               | 01111000 | output   |           |
| FIFO_DATA_OUT_X_L  | R    | 79               | 01111001 | output   |           |
| FIFO_DATA_OUT_X_H  | R    | 7A               | 01111010 | output   |           |
| FIFO_DATA_OUT_Y_L  | R    | 7B               | 01111011 | output   |           |
| FIFO_DATA_OUT_Y_H  | R    | 7C               | 01111100 | output   |           |
| FIFO_DATA_OUT_Z_L  | R    | 7D               | 01111101 | output   |           |
| FIFO_DATA_OUT_Z_H  | R    | 7E               | 01111110 | output   |           |

1. This register status is read using the primary interface for user interface data.
2. This register status is read using the auxiliary SPI for OIS data.

## 9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

### 9.1 FUNC\_CFG\_ACCESS (01h)

Enable embedded functions register (r/w)

**Table 21. FUNC\_CFG\_ACCESS register**

|                 |                 |                  |                  |                  |                  |                  |                  |
|-----------------|-----------------|------------------|------------------|------------------|------------------|------------------|------------------|
| FUNC_CFG_ACCESS | SHUB_REG_ACCESS | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|-----------------|-----------------|------------------|------------------|------------------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 22. FUNC\_CFG\_ACCESS register description**

|                 |   |
|-----------------|---|
| FUNC_CFG_ACCESS | Enable access to the embedded functions configuration registers.<br>Default value: 0 <sup>(1)</sup>     |
| SHUB_REG_ACCESS | Enable access to the sensor hub (I <sup>2</sup> C master) registers.<br>Default value: 0 <sup>(2)</sup> |

1. Details concerning the embedded functions configuration registers are available in [Section 10 Embedded functions register mapping](#) and [Section 11 Embedded functions register description](#).
2. Details concerning the sensor hub registers are available in [Section 14 Sensor hub register mapping](#) and [Section 15 Sensor hub register description](#).

### 9.2 PIN\_CTRL (02h)

SDO, OCS\_AUX, SDO\_AUX pins pull-up enable/disable register (r/w)

**Table 23. PIN\_CTRL register**

|            |           |                  |                  |                  |                  |                  |                  |
|------------|-----------|------------------|------------------|------------------|------------------|------------------|------------------|
| OIS_PU_DIS | SDO_PU_EN | 1 <sup>(1)</sup> | 1 <sup>(1)</sup> | 1 <sup>(1)</sup> | 1 <sup>(1)</sup> | 1 <sup>(1)</sup> | 1 <sup>(1)</sup> |
|------------|-----------|------------------|------------------|------------------|------------------|------------------|------------------|

1. This bit must be set to '1' for the correct operation of the device.

**Table 24. PIN\_CTRL register description**

|            |   |
|------------|---|
| OIS_PU_DIS | Disable pull-up on both OCS_Aux and SDO_Aux pins. Default value: 0<br>(0: OCS_Aux and SDO_Aux pins with pull-up;<br>1: OCS_Aux and SDO_Aux pins pull-up disconnected) |
| SDO_PU_EN  | Enable pull-up on SDO pin. Default value: 0<br>(0: SDO pin pull-up disconnected (default); 1: SDO pin with pull-up)   |

### 9.3 S4S\_TPH\_L (04h)

Sensor synchronization time frame register (r/w)

**Table 25. S4S\_TPH\_L register**

|           |         |         |         |         |         |         |         |
|-----------|---------|---------|---------|---------|---------|---------|---------|
| TPH_H_SEL | TPH_L_6 | TPH_L_5 | TPH_L_4 | TPH_L_3 | TPH_L_2 | TPH_L_1 | TPH_L_0 |
|-----------|---------|---------|---------|---------|---------|---------|---------|

**Table 26. S4S\_TPH\_L register description**

|             |   |
|-------------|---|
| TPH_H_SEL   | Chooses if the TPH formula must be taken into account (see equation below).   |
| TPH_L_[6:0] | S4S timeframe expressed in number of samples as described in the equation below.<br>If TPH_H_SEL=0 and TPH_L_[6:0] = d0, S4S is disabled. |

When TPH\_H\_SEL = 0:  $\text{TPH} [\#\text{Samples}] = 2 \times \text{TPHL}$

When TPH\_H\_SEL = 1:  $\text{TPH} [\#\text{Samples}] = 2 \times (\text{TPH\_L} + 256 \times \text{TPH\_H})$

### 9.4 S4S\_TPH\_H (05h)

Sensor synchronization time frame register (r/w)

**Table 27. S4S\_TPH\_H register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| TPH_H_7 | TPH_H_6 | TPH_H_5 | TPH_H_4 | TPH_H_3 | TPH_H_2 | TPH_H_1 | TPH_H_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 28. S4S\_TPH\_H register description**

|             |   |
|-------------|---|
| TPH_H_[7:0] | S4S time frame expressed in number of samples. Only if the TPH_H_SEL bit in S4S_TPH_L (04h) is high, is the value of this register taken into account as described in the equation in S4S_TPH_L (04h) |
|-------------|---|

### 9.5 S4S\_RR (06h)

Sensor synchronization resolution ratio register (r/w)

**Table 29. S4S\_RR register**

|                  |                  |                  |                  |                  |                  |      |      |
|------------------|------------------|------------------|------------------|------------------|------------------|------|------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | RR_1 | RR_0 |
|------------------|------------------|------------------|------------------|------------------|------------------|------|------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 30. S4S\_RR register description**

|          |   |
|----------|---|
| RR_[1:0] | (00: S4S, DT resolution $2^{11}$ ;<br>01: S4S, DT resolution $2^{12}$ ;<br>10: S4S, DT resolution $2^{13}$ ;<br>11: S4S, DT resolution $2^{14}$ ) |
|----------|---|

## 9.6 FIFO\_CTRL1 (07h)

FIFO control register 1 (r/w)

**Table 31. FIFO\_CTRL1 register**

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| WTM7 | WTM6 | WTM5 | WTM4 | WTM3 | WTM2 | WTM1 | WTM0 |
|------|------|------|------|------|------|------|------|

**Table 32. FIFO\_CTRL1 register description**

|          |  |
|----------|--|
| WTM[7:0] | FIFO watermark threshold, in conjunction with WTM8 in FIFO_CTRL2 (08h).<br>1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO<br>Watermark flag rises when the number of bytes written in the FIFO is greater than or equal to the threshold level. |
|----------|--|

## 9.7 FIFO\_CTRL2 (08h)

FIFO control register 2 (r/w)

**Table 33. FIFO\_CTRL2 register**

|             |                  |                  |           |                  |                |                |      |
|-------------|------------------|------------------|-----------|------------------|----------------|----------------|------|
| STOP_ON_WTM | FIFO_COMPR_RT_EN | 0 <sup>(1)</sup> | ODRCHG_EN | 0 <sup>(1)</sup> | UNCOPTR_RATE_1 | UNCOPTR_RATE_0 | WTM8 |
|-------------|------------------|------------------|-----------|------------------|----------------|----------------|------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 34. FIFO\_CTRL2 register**

|                                 |   |
|---------------------------------|---|
| STOP_ON_WTM                     | Sensing chain FIFO stop values memorization at threshold level<br>(0: FIFO depth is not limited (default);<br>1: FIFO depth is limited to the threshold level, defined in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h)   |
| FIFO_COMPR_RT_EN <sup>(1)</sup> | Enables/Disables compression algorithm runtime  |
| ODRCHG_EN                       | Enables ODR CHANGE virtual sensor to be batched in FIFO   |
| UNCOPTR_RATE_[1:0]              | This field configures the compression algorithm to write non-compressed data at each rate.<br>(0: Non-compressed data writing is not forced;<br>1: Non-compressed data every 8 batch data rate;<br>2: Non-compressed data every 16 batch data rate;<br>3: Non-compressed data every 32 batch data rate) |
| WTM8                            | FIFO watermark threshold, in conjunction with WTM[7:0] in FIFO_CTRL1 (07h).<br>1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO<br>Watermark flag rises when the number of bytes written in FIFO is greater than or equal to the threshold level.  |

1. This bit is effective if the FIFO\_COMPR\_EN bit of EMB\_FUNC\_EN\_B (05h) is set to 1.

## 9.8 FIFO\_CTRL3 (09h)

FIFO control register 3 (r/w)

**Table 35. FIFO\_CTRL3 register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| BDR_GY_3 | BDR_GY_2 | BDR_GY_1 | BDR_GY_0 | BDR_XL_3 | BDR_XL_2 | BDR_XL_1 | BDR_XL_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

**Table 36. FIFO\_CTRL3 register description**

|              |   |
|--------------|---|
| BDR_GY_[3:0] | <p>Selects Batch Data Rate (write frequency in FIFO) for gyroscope data.<br/>           (0000: Gyro not batched in FIFO (default);<br/>           0001: 12.5 Hz;<br/>           0010: 26 Hz;<br/>           0011: 52 Hz;<br/>           0100: 104 Hz;<br/>           0101: 208 Hz;<br/>           0110: 417 Hz;<br/>           0111: 833 Hz;<br/>           1000: 1667 Hz;<br/>           1001: 3333 Hz;<br/>           1010: 6667 Hz;<br/>           1011: 6.5 Hz;<br/>           1100-1111: not allowed)</p>              |
| BDR_XL_[3:0] | <p>Selects Batch Data Rate (write frequency in FIFO) for accelerometer data.<br/>           (0000: Accelerometer not batched in FIFO (default);<br/>           0001: 12.5 Hz;<br/>           0010: 26 Hz;<br/>           0011: 52 Hz;<br/>           0100: 104 Hz;<br/>           0101: 208 Hz;<br/>           0110: 417 Hz;<br/>           0111: 833 Hz;<br/>           1000: 1667 Hz;<br/>           1001: 3333 Hz;<br/>           1010: 6667 Hz;<br/>           1011: 1.6 Hz;<br/>           1100-1111: not allowed)</p> |

## 9.9 FIFO\_CTRL4 (0Ah)

FIFO control register 4 (r/w)

**Table 37. FIFO\_CTRL4 register**

|                |                |               |               |                  |            |            |            |
|----------------|----------------|---------------|---------------|------------------|------------|------------|------------|
| DEC_TS_BATCH_1 | DEC_TS_BATCH_0 | ODR_T_BATCH_1 | ODR_T_BATCH_0 | 0 <sup>(1)</sup> | FIFO_MODE2 | FIFO_MODE1 | FIFO_MODE0 |
|----------------|----------------|---------------|---------------|------------------|------------|------------|------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 38. FIFO\_CTRL4 register description**

|                    |   |
|--------------------|---|
| DEC_TS_BATCH_[1:0] | <p>Selects decimation for timestamp batching in FIFO. Write rate will be the maximum rate between XL and GYRO BDR divided by decimation decoder.</p> <p>(00: Timestamp not batched in FIFO (default);<br/>           01: Decimation 1: <math>\max(\text{BDR\_XL}[\text{Hz}], \text{BDR\_GY}[\text{Hz}])</math> [Hz];<br/>           10: Decimation 8: <math>\max(\text{BDR\_XL}[\text{Hz}], \text{BDR\_GY}[\text{Hz}])/8</math> [Hz];<br/>           11: Decimation 32: <math>\max(\text{BDR\_XL}[\text{Hz}], \text{BDR\_GY}[\text{Hz}])/32</math> [Hz])</p>  |
| ODR_T_BATCH_[1:0]  | <p>Selects batch data rate (write frequency in FIFO) for temperature data</p> <p>(00: Temperature not batched in FIFO (default);<br/>           01: 1.6 Hz;<br/>           10: 12.5 Hz;<br/>           11: 52 Hz)</p>   |
| FIFO_MODE[2:0]     | <p>FIFO mode selection</p> <p>(000: Bypass mode: FIFO disabled;<br/>           001: FIFO mode: stops collecting data when FIFO is full;<br/>           010: Reserved;<br/>           011: Continuous-to-FIFO mode: Continuous mode until trigger is deasserted, then FIFO mode;<br/>           100: Bypass-to-Continuous mode: Bypass mode until trigger is deasserted, then Continuous mode;<br/>           101: Reserved;<br/>           110: Continuous mode: if the FIFO is full, the new sample overwrites the older one;<br/>           111: Bypass-to-FIFO mode: Bypass mode until trigger is deasserted, then FIFO mode.)</p> |



## 9.10 COUNTER\_BDR\_REG1 (0Bh)

Counter batch data rate register 1 (r/w)

**Table 39. COUNTER\_BDR\_REG1 register**

|                  |                 |                  |                  |                  |               |              |              |
|------------------|-----------------|------------------|------------------|------------------|---------------|--------------|--------------|
| dataready_pulsed | RST_COUNTER_BDR | TRIG_COUNTER_BDR | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | CNT_BDR_TH_10 | CNT_BDR_TH_9 | CNT_BDR_TH_8 |
|------------------|-----------------|------------------|------------------|------------------|---------------|--------------|--------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 40. COUNTER\_BDR\_REG1 register description**

|                   |  |
|-------------------|--|
| dataready_pulsed  | Enables pulsed data-ready mode<br>(0: Data-ready latched mode (returns to 0 only after an interface reading) (default);<br>1: Data-ready pulsed mode (the data ready pulses are 75 µs long)  |
| RST_COUNTER_BDR   | Resets the internal counter of batch events for a single sensor.<br>This bit is automatically reset to zero if it was set to '1'.  |
| TRIG_COUNTER_BDR  | Selects the trigger for the internal counter of batch events between XL and gyro.<br>(0: XL batch event;<br>1: GYRO batch event)   |
| CNT_BDR_TH_[10:8] | In conjunction with CNT_BDR_TH_[7:0] in <a href="#">COUNTER_BDR_REG2 (0Ch)</a> , sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in <a href="#">FIFO_STATUS2 (3Bh)</a> is set to '1'. |

## 9.11 COUNTER\_BDR\_REG2 (0Ch)

Counter batch data rate register 2 (r/w)

**Table 41. COUNTER\_BDR\_REG2 register**

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| CNT_BDR_TH_7 | CNT_BDR_TH_6 | CNT_BDR_TH_5 | CNT_BDR_TH_4 | CNT_BDR_TH_3 | CNT_BDR_TH_2 | CNT_BDR_TH_1 | CNT_BDR_TH_0 |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

**Table 42. COUNTER\_BDR\_REG2 register description**

|                  |   |
|------------------|---|
| CNT_BDR_TH_[7:0] | In conjunction with CNT_BDR_TH_[10:8] in <a href="#">COUNTER_BDR_REG1 (0Bh)</a> , sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in <a href="#">FIFO_STATUS2 (3Bh)</a> is set to '1'. |
|------------------|---|

## 9.12 INT1\_CTRL (0Dh)

INT1 pin control register (r/w)

Each bit in this register enables a signal to be carried over INT1 when the MIPI I3C<sup>SM</sup> dynamic address is not assigned (I<sup>2</sup>C or SPI is used). Some bits can be also used to trigger an IBI (In-Band Interrupt) when the MIPI I3C<sup>SM</sup> interface is used.. The output of the pad will be the OR combination of the signals selected here and in register MD1\_CFG (5Eh).

**Table 43. INT1\_CTRL register**

|               |              |                |               |              |           |             |              |
|---------------|--------------|----------------|---------------|--------------|-----------|-------------|--------------|
| DEN_DRDY_flag | INT1_CNT_BDR | INT1_FIFO_FULL | INT1_FIFO_OVR | INT1_FIFO_TH | INT1_BOOT | INT1_DRDY_G | INT1_DRDY_XL |
|---------------|--------------|----------------|---------------|--------------|-----------|-------------|--------------|

**Table 44. INT1\_CTRL register description**

|                |   |
|----------------|---|
| DEN_DRDY_flag  | Sends DEN_DRDY (DEN stamped on Sensor Data flag) to INT1 pin.   |
| INT1_CNT_BDR   | Enables COUNTER_BDR_IA interrupt on INT1.   |
| INT1_FIFO_FULL | Enables FIFO full flag interrupt on INT1 pin.<br>It can be also used to trigger an IBI when the MIPI I3C <sup>SM</sup> interface is used.           |
| INT1_FIFO_OVR  | Enables FIFO overrun interrupt on INT1 pin.<br>It can be also used to trigger an IBI when the MIPI I3C <sup>SM</sup> interface is used.             |
| INT1_FIFO_TH   | Enables FIFO threshold interrupt on INT1 pin.<br>It can be also used to trigger an IBI when the MIPI I3C <sup>SM</sup> interface is used.           |
| INT1_BOOT      | Enables boot status on INT1 pin.  |
| INT1_DRDY_G    | Enables gyroscope data-ready interrupt on INT1 pin.<br>It can be also used to trigger an IBI when the MIPI I3C <sup>SM</sup> interface is used.     |
| INT1_DRDY_XL   | Enables accelerometer data-ready interrupt on INT1 pin.<br>It can be also used to trigger an IBI when the MIPI I3C <sup>SM</sup> interface is used. |

### 9.13 INT2\_CTRL (0Eh)

INT2 pin control register (r/w).

Each bit in this register enables a signal to be carried over INT2 when the MIPI I3C<sup>SM</sup> dynamic address is not assigned (I<sup>2</sup>C or SPI is used). Some bits can be also used to trigger an IBI when the MIPI I3C<sup>SM</sup> interface is used. The output of the pad will be the OR combination of the signals selected here and in register MD2\_CFG (5Fh).

**Table 45. INT2\_CTRL register**

|                  |              |                |               |              |                |             |              |
|------------------|--------------|----------------|---------------|--------------|----------------|-------------|--------------|
| 0 <sup>(1)</sup> | INT2_CNT_BDR | INT2_FIFO_FULL | INT2_FIFO_OVR | INT2_FIFO_TH | INT2_DRDY_TEMP | INT2_DRDY_G | INT2_DRDY_XL |
|------------------|--------------|----------------|---------------|--------------|----------------|-------------|--------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 46. INT2\_CTRL register description**

|                |  |
|----------------|--|
| INT2_CNT_BDR   | Enables COUNTER_BDR_IA interrupt on INT2 pin.  |
| INT2_FIFO_FULL | Enables FIFO full flag interrupt on INT2 pin.  |
| INT2_FIFO_OVR  | Enables FIFO overrun interrupt on INT2 pin.  |
| INT_FIFO_TH    | Enables FIFO threshold interrupt on INT2 pin.  |
| INT2_DRDY_TEMP | Enables temperature sensor data-ready interrupt on INT2 pin.<br>It can be also used to trigger an IBI when the MIPI I3C <sup>SM</sup> interface is used and INT2_ON_INT1 = '1' in CTRL4_C (13h). |
| INT2_DRDY_G    | Enables gyroscope data-ready interrupt on INT2 pin.  |
| INT2_DRDY_XL   | Enables accelerometer data-ready interrupt on INT2 pin.  |

### 9.14 WHO\_AM\_I (0Fh)

WHO\_AM\_I register (r). This is a read-only register. Its value is fixed at 6Bh.

**Table 47. WhoAml register**

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
|---|---|---|---|---|---|---|---|

## 9.15 CTRL1\_XL (10h)

Accelerometer control register 1 (r/w)

**Table 48. CTRL1\_XL register**

|         |         |         |         |        |        |            |                  |
|---------|---------|---------|---------|--------|--------|------------|------------------|
| ODR_XL3 | ODR_XL2 | ODR_XL1 | ODR_XL0 | FS1_XL | FS0_XL | LPF2_XL_EN | 0 <sup>(1)</sup> |
|---------|---------|---------|---------|--------|--------|------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 49. CTRL1\_XL register description**

|             |  |
|-------------|--|
| ODR_XL[3:0] | Accelerometer ODR selection (see Table 50).  |
| FS[1:0]_XL  | Accelerometer full-scale selection. Default value: 00<br>(00: $\pm 2$ g; 01: $\pm 16$ g; 10: $\pm 4$ g; 11: $\pm 8$ g)   |
| LPF2_XL_EN  | Accelerometer high-resolution selection<br>(0: output from first stage digital filtering selected (default);<br>1: output from LPF2 second filtering stage selected) |

**Table 50. Accelerometer ODR selection**

| ODR_XL3 | ODR_XL2 | ODR_XL1 | ODR_XL0 | ODR selection [Hz] when<br>XL_HM_MODE = 1 in CTRL6_C<br>(15h) | ODR selection [Hz] when<br>XL_HM_MODE = 0 in CTRL6_C<br>(15h) |
|---------|---------|---------|---------|---|---|
| 0       | 0       | 0       | 0       | Power-down  | Power-down  |
| 1       | 0       | 1       | 1       | 1.6 Hz (low power only)                                       | N.A.  |
| 0       | 0       | 0       | 1       | 12.5 Hz (low power)   | 12.5 Hz (high performance)                                    |
| 0       | 0       | 1       | 0       | 26 Hz (low power)   | 26 Hz (high performance)                                      |
| 0       | 0       | 1       | 1       | 52 Hz (low power)   | 52 Hz (high performance)                                      |
| 0       | 1       | 0       | 0       | 104 Hz (normal mode)  | 104 Hz (high performance)                                     |
| 0       | 1       | 0       | 1       | 208 Hz (normal mode)  | 208 Hz (high performance)                                     |
| 0       | 1       | 1       | 0       | 416 Hz (high performance)                                     | 416 Hz (high performance)                                     |
| 0       | 1       | 1       | 1       | 833 Hz (high performance)                                     | 833 Hz (high performance)                                     |
| 1       | 0       | 0       | 0       | 1.66 kHz (high performance)                                   | 1.66 kHz (high performance)                                   |
| 1       | 0       | 0       | 1       | 3.33 kHz (high performance)                                   | 3.33 kHz (high performance)                                   |
| 1       | 0       | 1       | 0       | 6.66 kHz (high performance)                                   | 6.66 kHz (high performance)                                   |
| 1       | 1       | x       | x       | Not allowed   | Not allowed   |

## 9.16 CTRL2\_G (11h)

Gyroscope control register 2 (r/w)

**Table 51. CTRL2\_G register**

|        |        |        |        |       |       |        |         |
|--------|--------|--------|--------|-------|-------|--------|---------|
| ODR_G3 | ODR_G2 | ODR_G1 | ODR_G0 | FS1_G | FS0_G | FS_125 | FS_4000 |
|--------|--------|--------|--------|-------|-------|--------|---------|

**Table 52. CTRL2\_G register description**

|                        |   |
|------------------------|---|
| ODR_G[3:0]             | Gyroscope output data rate selection. Default value: 0000<br>(Refer to Table 53)  |
| FS[1:0]_G              | Gyroscope chain full-scale selection<br>(00: ±250 dps;<br>01: ±500 dps;<br>10: ±1000 dps;<br>11: ±2000 dps)             |
| FS_125                 | Selects gyro chain full-scale ±125 dps<br>(0: FS selected through bits FS[1:0]_G;<br>1: FS set to ±125 dps)             |
| FS_4000 <sup>(1)</sup> | Selects gyro chain full-scale ±4000 dps<br>(0: FS selected through bits FS[1:0]_G or FS_125;<br>1: FS set to ±4000 dps) |

1. This bit has to be set to 0 when the OIS chain is ON (OIS\_EN\_SPI2 bit = 1 in CTRL1\_OIS (70h))

**Table 53. Gyroscope ODR configuration setting**

| ODR_G3 | ODR_G2 | ODR_G1 | ODR_G0 | ODR selection [Hz] when<br>G_HM_MODE = 1 in CTRL7_G (16h) | ODR selection [Hz] when<br>G_HM_MODE = 0 in CTRL7_G (16h) |
|--------|--------|--------|--------|---|---|
| 0      | 0      | 0      | 0      | Power-down  | Power-down  |
| 0      | 0      | 0      | 1      | 12.5 Hz (low power)                                       | 12.5 Hz (high performance)                                |
| 0      | 0      | 1      | 0      | 26 Hz (low power)   | 26 Hz (high performance)                                  |
| 0      | 0      | 1      | 1      | 52 Hz (low power)   | 52 Hz (high performance)                                  |
| 0      | 1      | 0      | 0      | 104 Hz (normal mode)                                      | 104 Hz (high performance)                                 |
| 0      | 1      | 0      | 1      | 208 Hz (normal mode)                                      | 208 Hz (high performance)                                 |
| 0      | 1      | 1      | 0      | 416 Hz (high performance)                                 | 416 Hz (high performance)                                 |
| 0      | 1      | 1      | 1      | 833 Hz (high performance)                                 | 833 Hz (high performance)                                 |
| 1      | 0      | 0      | 0      | 1.66 kHz (high performance)                               | 1.66 kHz (high performance)                               |
| 1      | 0      | 0      | 1      | 3.33 kHz (high performance)                               | 3.33 kHz (high performance)                               |
| 1      | 0      | 1      | 0      | 6.66 kHz (high performance)                               | 6.66 kHz (high performance)                               |
| 1      | 0      | 1      | 1      | Not available   | Not available   |

## 9.17 CTRL3\_C (12h)

Control register 3 (r/w)

**Table 54. CTRL3\_C register**

|      |     |           |       |     |        |                  |          |
|------|-----|-----------|-------|-----|--------|------------------|----------|
| BOOT | BDU | H_LACTIVE | PP_OD | SIM | IF_INC | 0 <sup>(1)</sup> | SW_RESET |
|------|-----|-----------|-------|-----|--------|------------------|----------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 55. CTRL3\_C register description**

|           |  |
|-----------|--|
| BOOT      | Reboots memory content. Default value: 0<br>(0: normal mode; 1: reboot memory content)<br>Note: the accelerometer must be ON. This bit is automatically cleared.               |
| BDU       | Block Data Update. Default value: 0<br>(0: continuous update;<br>1: output registers are not updated until MSB and LSB have been read)   |
| H_LACTIVE | Interrupt activation level. Default value: 0<br>(0: interrupt output pins active high; 1: interrupt output pins active low)  |
| PP_OD     | Push-pull/open-drain selection on INT1 and INT2 pins. This bit must be set to '0' when H_LACTIVE is set to '1'.<br>Default value: 0<br>(0: push-pull mode; 1: open-drain mode) |
| SIM       | SPI Serial Interface Mode selection. Default value: 0<br>(0: 4-wire interface; 1: 3-wire interface)  |
| IF_INC    | Register address automatically incremented during a multiple byte access with a serial interface (I <sup>2</sup> C or SPI).<br>Default value: 1<br>(0: disabled; 1: enabled)   |
| SW_RESET  | Software reset. Default value: 0<br>(0: normal mode; 1: reset device)<br>This bit is automatically cleared.  |

## 9.18 CTRL4\_C (13h)

Control register 4 (r/w)

**Table 56. CTRL4\_C register**

|                  |         |              |                  |           |             |            |                  |
|------------------|---------|--------------|------------------|-----------|-------------|------------|------------------|
| 0 <sup>(1)</sup> | SLEEP_G | INT2_on_INT1 | 0 <sup>(1)</sup> | DRDY_MASK | I2C_disable | LPF1_SEL_G | 0 <sup>(1)</sup> |
|------------------|---------|--------------|------------------|-----------|-------------|------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 57. CTRL4\_C register description**

|              |  |
|--------------|--|
| SLEEP_G      | Enables gyroscope Sleep mode. Default value:0<br>(0: disabled; 1: enabled)   |
| INT2_on_INT1 | All interrupt signals available on INT1 pin enable. Default value: 0<br>(0: interrupt signals divided between INT1 and INT2 pins;<br>1: all interrupt signals in logic or on INT1 pin) |
| DRDY_MASK    | Enables data available<br>(0: disabled;<br>1: mask DRDY on pin (both XL & Gyro) until filter settling ends (XL and Gyro independently masked).   |
| I2C_disable  | Disables I <sup>2</sup> C interface. Default value: 0<br>(0: SPI, I <sup>2</sup> C and MIPI I3C <sup>SM</sup> interfaces enabled (default); 1: I <sup>2</sup> C interface disabled)    |
| LPF1_SEL_G   | Enables gyroscope digital LPF1; the bandwidth can be selected through FTYPE[2:0] in CTRL6_C (15h).<br>(0: disabled; 1: enabled)  |

## 9.19 CTRL5\_C (14h)

Control register 5 (r/w)

**Table 58. CTRL5\_C register**

|                  |           |           |                  |       |       |        |        |
|------------------|-----------|-----------|------------------|-------|-------|--------|--------|
| 0 <sup>(1)</sup> | ROUNDING1 | ROUNDING0 | 0 <sup>(1)</sup> | ST1_G | ST0_G | ST1_XL | ST0_XL |
|------------------|-----------|-----------|------------------|-------|-------|--------|--------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 59. CTRL5\_C register description**

|               |   |
|---------------|---|
| ROUNDING[1:0] | Circular burst-mode (rounding) read of the output registers. Default value: 00<br>(00: no rounding;<br>01: accelerometer only;<br>10: gyroscope only;<br>11: gyroscope + accelerometer) |
| ST[1:0]_G     | Angular rate sensor self-test enable. Default value: 00<br>(00: Self-test disabled; Other: refer to <a href="#">Table 60</a> )  |
| ST[1:0]_XL    | Linear acceleration sensor self-test enable. Default value: 00<br>(00: Self-test disabled; Other: refer to <a href="#">Table 61</a> )   |

**Table 60. Angular rate sensor self-test mode selection**

| ST1_G | ST0_G | Self-test mode          |
|-------|-------|-------------------------|
| 0     | 0     | Normal mode             |
| 0     | 1     | Positive sign self-test |
| 1     | 0     | Not allowed             |
| 1     | 1     | Negative sign self-test |

**Table 61. Linear acceleration sensor self-test mode selection**

| ST1_XL | ST0_XL | Self-test mode          |
|--------|--------|-------------------------|
| 0      | 0      | Normal mode             |
| 0      | 1      | Positive sign self-test |
| 1      | 0      | Negative sign self-test |
| 1      | 1      | Not allowed             |



## 9.20 CTRL6\_C (15h)

Control register 6 (r/w)

**Table 62. CTRL6\_C register**

|         |         |         |            |           |         |         |         |
|---------|---------|---------|------------|-----------|---------|---------|---------|
| TRIG_EN | LVL1_EN | LVL2_EN | XL_HM_MODE | USR_OFF_W | FTYPE_2 | FTYPE_1 | FTYPE_0 |
|---------|---------|---------|------------|-----------|---------|---------|---------|

**Table 63. CTRL6\_C register description**

|            |  |
|------------|--|
| TRIG_EN    | Enables DEN data edge-sensitive trigger mode. Refer to Table 64.   |
| LVL1_EN    | Enables DEN data level-sensitive trigger mode. Refer to Table 64.  |
| LVL2_EN    | Enables DEN level-sensitive latched mode. Refer to Table 64.   |
| XL_HM_MODE | Disables high-performance operating mode for accelerometer. Default value: 0<br>(0: high-performance operating mode enabled;<br>1: high-performance operating mode disabled) |
| USR_OFF_W  | Weight of XL user offset bits of registers X_OFS_USR (73h), Y_OFS_USR (74h), Z_OFS_USR (75h)<br>(0 = 2 <sup>-10</sup> g/LSB;<br>1 = 2 <sup>-6</sup> g/LSB)                   |
| FTYPE[2:0] | Gyroscope low-pass filter (LPF1) bandwidth selection. Table 65 shows the selectable bandwidth values.  |

**Table 64. Trigger mode selection**

| TRIG_EN, LVL1_EN, LVL2_EN | Trigger mode                                 |
|---------------------------|--|
| 100                       | Edge-sensitive trigger mode is selected      |
| 010                       | Level-sensitive trigger mode is selected     |
| 011                       | Level-sensitive latched mode is selected     |
| 110                       | Level-sensitive FIFO enable mode is selected |

**Table 65. Gyroscope LPF1 bandwidth selection**

| FTYPE [2:0] | 12.5 Hz | 26 Hz | 52 Hz | 104 Hz | 208 Hz | 416 Hz | 833 Hz | 1.67 kHz | 3.33 kHz | 6.67 kHz |
|-------------|---------|-------|-------|--------|--------|--------|--------|----------|----------|----------|
| 000         | 4.3     | 8.3   | 16.7  | 33     | 67     | 133    | 222    | 274      | 292      | 297      |
| 001         | 4.3     | 8.3   | 16.7  | 33     | 67     | 128    | 186    | 212      | 220      | 223      |
| 010         | 4.3     | 8.3   | 16.7  | 33     | 67     | 112    | 140    | 150      | 153      | 154      |
| 011         | 4.3     | 8.3   | 16.7  | 33     | 67     | 134    | 260    | 390      | 451      | 470      |
| 100         | 4.3     | 8.3   | 16.7  | 34     | 62     | 86     | 96     | 90       | NA       |          |
| 101         | 4.3     | 8.3   | 16.9  | 31     | 43     | 48     | 49     | 50       | NA       |          |
| 110         | 4.3     | 8.3   | 13.4  | 19     | 23     | 24.6   | 25     | 25       | NA       |          |
| 111         | 4.3     | 8.3   | 9.8   | 11.6   | 12.2   | 12.4   | 12.6   | 12.6     | NA       |          |

## 9.21 CTRL7\_G (16h)

Control register 7 (r/w)

**Table 66. CTRL7\_G register**

|           |         |        |        |                  |           |                |        |
|-----------|---------|--------|--------|------------------|-----------|----------------|--------|
| G_HM_MODE | HP_EN_G | HPM1_G | HPM0_G | 0 <sup>(1)</sup> | OIS_ON_EN | USR_OFF_ON_OUT | OIS_ON |
|-----------|---------|--------|--------|------------------|-----------|----------------|--------|

1. This bit must be set to '0' for the correct operation of the device.

|                          |   |
|--------------------------|---|
| G_HM_MODE                | Disables high-performance operating mode for gyroscope. Default: 0<br>(0: high-performance operating mode enabled;<br>1: high-performance operating mode disabled)  |
| HP_EN_G                  | Enables gyroscope digital high-pass filter. The filter is enabled only if the gyro is in HP mode. Default value: 0<br>(0: HPF disabled; 1: HPF enabled)   |
| HPM_G[1:0]               | Gyroscope digital HP filter cutoff selection. Default: 00<br>(00 = 16 mHz;<br>01 = 65 mHz;<br>10 = 260 mHz;<br>11 = 1.04 Hz)  |
| OIS_ON_EN <sup>(1)</sup> | Selects how to enable and disable the OIS chain, after first configuration and enabling through SPI2.<br>(0: OIS chain is enabled/disabled with SPI2 interface;<br>1: OIS chain is enabled/disabled with primary interface)   |
| USR_OFF_ON_OUT           | Enables accelerometer user offset correction block; it's valid for the low-pass path - see <a href="#">Figure 18. Accelerometer composite filter</a> . Default value: 0<br>(0: accelerometer user offset correction block bypassed;<br>1: accelerometer user offset correction block enabled) |
| OIS_ON                   | Enables/disables the OIS chain from primary interface when the OIS_ON_EN bit is '1'.<br>(0: OIS disabled; 1: OIS enabled)   |

1. First, enabling OIS and OIS configurations must be done through SPI2, with OIS\_ON\_EN and OIS\_ON set to '0'.

## 9.22 CTRL8\_XL (17h)

Control register 8 (r/w)

**Table 67. CTRL8\_XL register**

|           |           |           |                |                   |                |                  |                |
|-----------|-----------|-----------|----------------|-------------------|----------------|------------------|----------------|
| HPCF_XL_2 | HPCF_XL_1 | HPCF_XL_0 | HP_REF_MODE_XL | FASTSETTL_MODE_XL | HP_SLOPE_XL_EN | 0 <sup>(1)</sup> | LOW_PASS_ON_6D |
|-----------|-----------|-----------|----------------|-------------------|----------------|------------------|----------------|

1. This bit must be set to '0' for the correct operation of the device.

|                   |  |
|-------------------|--|
| HPCF_XL[2:0]      | Accelerometer LPF2 and HP filter configuration and cutoff setting. Refer to <a href="#">Table 68</a> .   |
| HP_REF_MODE_XL    | Enables accelerometer high-pass filter reference mode (valid for high-pass path - HP_SLOPE_XL_EN bit must be '1'). Default value: 0<br>(0: disabled, 1: enabled <sup>(1)</sup> )                                     |
| FASTSETTL_MODE_XL | Enables accelerometer LPF2 and HPF fast-settling mode. The filter sets the second samples after writing this bit. Active only during device exit from power-down mode. Default value: 0<br>(0: disabled, 1: enabled) |
| HP_SLOPE_XL_EN    | Accelerometer slope filter / high-pass filter selection. Refer to <a href="#">Figure 26</a> .  |
| LOW_PASS_ON_6D    | LPF2 on 6D function selection. Refer to <a href="#">Figure 26</a> . Default value: 0<br>(0: ODR/2 low-pass filtered data sent to 6D interrupt function;<br>1: LPF2 output data sent to 6D interrupt function)        |

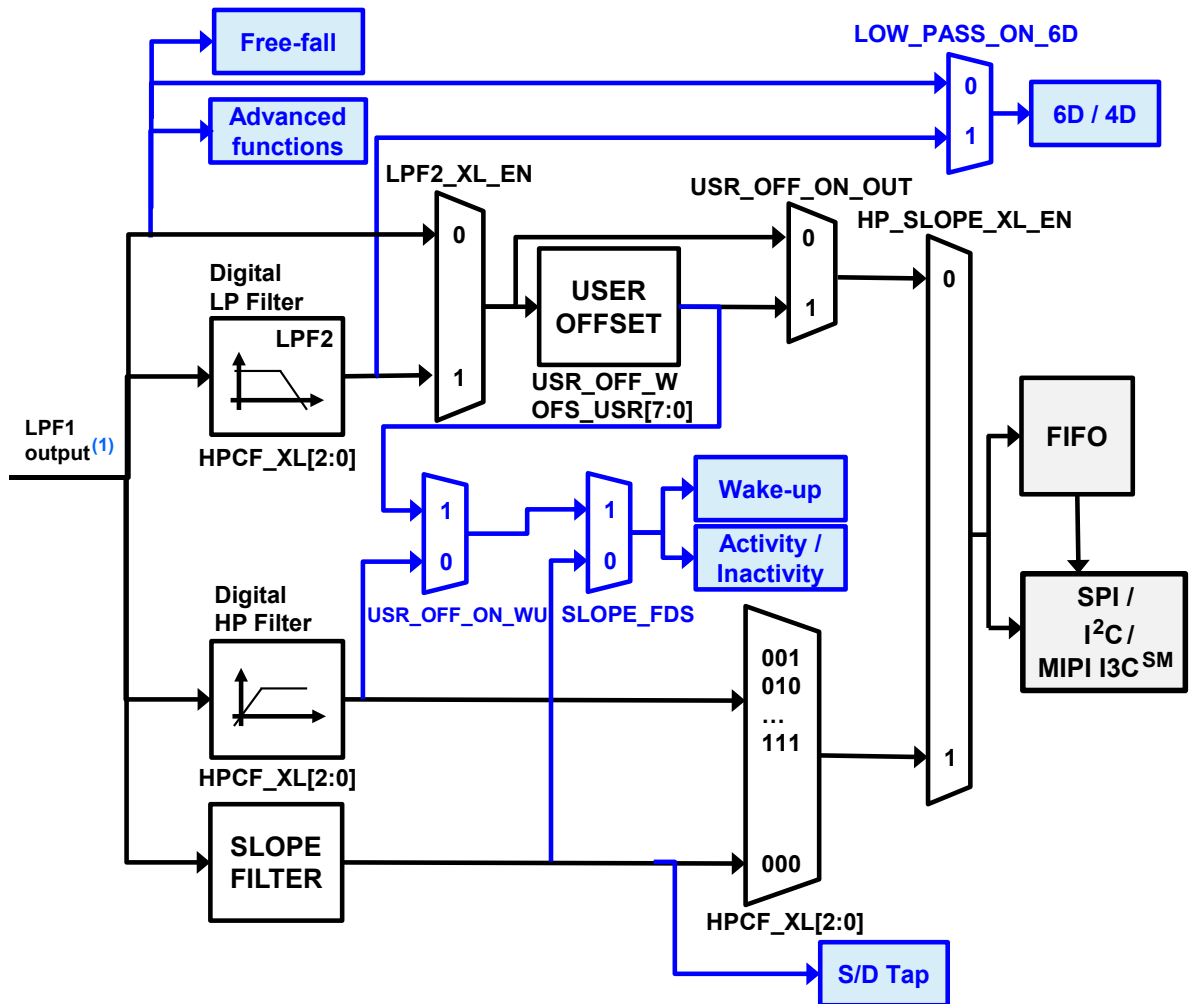
1. When enabled, the first output data have to be discarded.

**Table 68. Accelerometer bandwidth configurations**

| Filter type | HP_SLOPE_XL_EN | LPF2_XL_EN | HPCF_XL [2:0] | Bandwidth <sup>(1)</sup> |
|-------------|----------------|------------|---------------|--------------------------|
| Low pass    | 0              | 0          | -             | ODR/2                    |
|             |                |            | 000           | ODR/4                    |
|             |                | 1          | 001           | ODR/10                   |
|             |                |            | 010           | ODR/20                   |
|             |                |            | 011           | ODR/45                   |
|             |                |            | 100           | ODR/100                  |
|             |                |            | 101           | ODR/200                  |
|             |                |            | 110           | ODR/400                  |
| High pass   | 1              | -          | 111           | ODR/800                  |
|             |                |            | 000           | SLOPE (ODR/4)            |
|             |                |            | 001           | ODR/10                   |
|             |                |            | 010           | ODR/20                   |
|             |                |            | 011           | ODR/45                   |
|             |                |            | 100           | ODR/100                  |
|             |                |            | 101           | ODR/200                  |
|             |                |            | 110           | ODR/400                  |
| 111         | ODR/800        |            |               |                          |

1. Typical value for ODR up to 833 Hz.

Figure 26. Accelerometer block diagram



1. The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode and ODR up to 833 Hz. This value is equal to 780 Hz when the accelerometer is in low-power or normal mode.

## 9.23 CTRL9\_XL (18h)

Control register 9 (r/w)

**Table 69. CTRL9\_XL register**

|       |       |       |          |           |        |             |                  |
|-------|-------|-------|----------|-----------|--------|-------------|------------------|
| DEN_X | DEN_Y | DEN_Z | DEN_XL_G | DEN_XL_EN | DEN_LH | I3C_disable | 0 <sup>(1)</sup> |
|-------|-------|-------|----------|-----------|--------|-------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 70. CTRL9\_XL register description**

|             |   |
|-------------|---|
| DEN_X       | DEN value stored in LSB of X-axis. Default value: 1<br>(0: DEN not stored in X-axis LSB; 1: DEN stored in X-axis LSB)   |
| DEN_Y       | DEN value stored in LSB of Y-axis. Default value: 1<br>(0: DEN not stored in Y-axis LSB; 1: DEN stored in Y-axis LSB)   |
| DEN_Z       | DEN value stored in LSB of Z-axis. Default value: 1<br>(0: DEN not stored in Z-axis LSB; 1: DEN stored in Z-axis LSB)   |
| DEN_XL_G    | DEN stamping sensor selection. Default value: 0<br>(0: DEN pin info stamped in the gyroscope axis selected by bits [7:5];<br>1: DEN pin info stamped in the accelerometer axis selected by bits [7:5])    |
| DEN_XL_EN   | Extends DEN functionality to accelerometer sensor. Default value: 0<br>(0: disabled; 1: enabled)  |
| DEN_LH      | DEN active level configuration. Default value: 0<br>(0: active low; 1: active high)   |
| I3C_disable | Disables MIPI I3C <sup>SM</sup> communication protocol <sup>(1)</sup><br>(0: SPI, I <sup>2</sup> C, MIPI I3C <sup>SM</sup> interfaces enabled (default);<br>1: MIPI I3C <sup>SM</sup> interface disabled) |

1. It is recommended to set this bit to '1' during the initial device configuration phase, when the I3C interface is not used.

## 9.24 CTRL10\_C (19h)

Control register 10 (r/w)

**Table 71. CTRL10\_C register**

|                  |                  |              |                  |                  |                  |                  |                  |
|------------------|------------------|--------------|------------------|------------------|------------------|------------------|------------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | TIMESTAMP_EN | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|------------------|------------------|--------------|------------------|------------------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 72. CTRL10\_C register description**

|              |  |
|--------------|--|
| TIMESTAMP_EN | Enables timestamp counter. Default value: 0<br>(0: disabled; 1: enabled)<br><br>The counter is readable in TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h). |
|--------------|--|

## 9.25 ALL\_INT\_SRC (1A)

Source register for all interrupts (r)

**Table 73. ALL\_INT\_SRC register**

|                    |   |                 |        |            |            |       |       |
|--------------------|---|-----------------|--------|------------|------------|-------|-------|
| TIMESTAMP_ENDCOUNT | 0 | SLEEP_CHANGE_IA | D6D_IA | DOUBLE_TAP | SINGLE_TAP | WU_IA | FF_IA |
|--------------------|---|-----------------|--------|------------|------------|-------|-------|

**Table 74. ALL\_INT\_SRC register description**

|                    |  |
|--------------------|--|
| TIMESTAMP_ENDCOUNT | Alerts timestamp overflow within 6.4 ms  |
| SLEEP_CHANGE_IA    | Detects change event in activity/inactivity status. Default value: 0<br>(0: change status not detected; 1: change status detected)   |
| D6D_IA             | Interrupt active for change in position of portrait, landscape, face-up, face-down. Default value: 0<br>(0: change in position not detected; 1: change in position detected) |
| DOUBLE_TAP         | Double-tap event status. Default value: 0<br>(0: event not detected, 1: event detected)  |
| SINGLE_TAP         | Single-tap event status. Default value: 0<br>(0: event not detected, 1: event detected)  |
| WU_IA              | Wake-up event status. Default value: 0<br>(0: event not detected, 1: event detected)   |
| FF_IA              | Free-fall event status. Default value: 0<br>(0: event not detected, 1: event detected)   |

## 9.26 WAKE\_UP\_SRC (1Bh)

Wake-up interrupt source register (r)

**Table 75. WAKE\_UP\_SRC register**

|   |                 |       |             |       |      |      |      |
|---|-----------------|-------|-------------|-------|------|------|------|
| 0 | SLEEP_CHANGE_IA | FF_IA | SLEEP_STATE | WU_IA | X_WU | Y_WU | Z_WU |
|---|-----------------|-------|-------------|-------|------|------|------|

**Table 76. WAKE\_UP\_SRC register description**

|                 |   |
|-----------------|---|
| SLEEP_CHANGE_IA | Detects change event in activity/inactivity status. Default value: 0<br>(0: change status not detected; 1: change status detected)        |
| FF_IA           | Free-fall event detection status. Default: 0<br>(0: free-fall event not detected; 1: free-fall event detected)                            |
| SLEEP_STATE     | Sleep event status. Default value: 0<br>(0: sleep event not detected; 1: sleep event detected)  |
| WU_IA           | Wakeup event detection status. Default value: 0<br>(0: wakeup event not detected; 1: wakeup event detected.)                              |
| X_WU            | Wakeup event detection status on X-axis. Default value: 0<br>(0: wakeup event on X-axis not detected; 1: wakeup event on X-axis detected) |
| Y_WU            | Wakeup event detection status on Y-axis. Default value: 0<br>(0: wakeup event on Y-axis not detected; 1: wakeup event on Y-axis detected) |
| Z_WU            | Wakeup event detection status on Z-axis. Default value: 0<br>(0: wakeup event on Z-axis not detected; 1: wakeup event on Z-axis detected) |

## 9.27 TAP\_SRC (1Ch)

Tap source register (r)

**Table 77. TAP\_SRC register**

|   |        |            |            |          |       |       |       |
|---|--------|------------|------------|----------|-------|-------|-------|
| 0 | TAP_IA | SINGLE_TAP | DOUBLE_TAP | TAP_SIGN | X_TAP | Y_TAP | Z_TAP |
|---|--------|------------|------------|----------|-------|-------|-------|

**Table 78. TAP\_SRC register description**

|            |   |
|------------|---|
| TAP_IA     | Tap event detection status. Default: 0<br>(0: tap event not detected; 1: tap event detected)  |
| SINGLE_TAP | Single-tap event status. Default value: 0<br>(0: single tap event not detected; 1: single tap event detected)   |
| DOUBLE_TAP | Double-tap event detection status. Default value: 0<br>(0: double-tap event not detected; 1: double-tap event detected.)  |
| TAP_SIGN   | Sign of acceleration detected by tap event. Default: 0<br>(0: positive sign of acceleration detected by tap event;<br>1: negative sign of acceleration detected by tap event) |
| X_TAP      | Tap event detection status on X-axis. Default value: 0<br>(0: tap event on X-axis not detected; 1: tap event on X-axis detected)  |
| Y_TAP      | Tap event detection status on Y-axis. Default value: 0<br>(0: tap event on Y-axis not detected; 1: tap event on Y-axis detected)  |
| Z_TAP      | Tap event detection status on Z-axis. Default value: 0<br>(0: tap event on Z-axis not detected; 1: tap event on Z-axis detected)  |



## 9.28 DRD\_SRC (1Dh)

Portrait, landscape, face-up and face-down source register (r)

**Table 79. D6D\_SRC register**

|          |        |    |    |    |    |    |    |
|----------|--------|----|----|----|----|----|----|
| DEN_DRDY | D6D_IA | ZH | ZL | YH | YL | XH | XL |
|----------|--------|----|----|----|----|----|----|

**Table 80. D6D\_SRC register description**

|          |  |
|----------|--|
| DEN_DRDY | DEN data-ready signal. It is set high when data output is related to the data coming from a DEN active condition. <sup>(1)</sup>                                 |
| D6D_IA   | Interrupt active for change position portrait, landscape, face-up, face-down. Default value: 0<br>(0: change position not detected; 1: change position detected) |
| ZH       | Z-axis high event (over threshold). Default value: 0<br>(0: event not detected; 1: event (over threshold) detected)  |
| ZL       | Z-axis low event (under threshold). Default value: 0<br>(0: event not detected; 1: event (under threshold) detected)   |
| YH       | Y-axis high event (over threshold). Default value: 0<br>(0: event not detected; 1: event (over-threshold) detected)  |
| YL       | Y-axis low event (under threshold). Default value: 0<br>(0: event not detected; 1: event (under threshold) detected)   |
| XH       | X-axis high event (over threshold). Default value: 0<br>(0: event not detected; 1: event (over threshold) detected)  |
| XL       | X-axis low event (under threshold). Default value: 0<br>(0: event not detected; 1: event (under threshold) detected)   |

1. The DEN data-ready signal can be latched or pulsed depending on the value of the `dataready_pulsed` bit of the `COUNTER_BDR_REG1 (0Bh)` register.

## 9.29 STATUS\_REG (1Eh) / STATUS\_SPIAux (1Eh)

The STATUS\_REG register is read by the primary interface SPI/I<sup>2</sup>C & MIPI I3C<sup>SM</sup> (r)

**Table 81. STATUS\_REG register**

|   |   |   |   |   |     |     |      |
|---|---|---|---|---|-----|-----|------|
| 0 | 0 | 0 | 0 | 0 | TDA | GDA | XLDA |
|---|---|---|---|---|-----|-----|------|

**Table 82. STATUS\_REG register description**

|      |  |
|------|--|
| TDA  | Temperature new data available. Default: 0<br>(0: no set of data is available at temperature sensor output;<br>1: a new set of data is available at temperature sensor output) |
| GDA  | Gyroscope new data available. Default value: 0<br>(0: no set of data available at gyroscope output;<br>1: a new set of data is available at gyroscope output)                  |
| XLDA | Accelerometer new data available. Default value: 0<br>(0: no set of data available at accelerometer output;<br>1: a new set of data is available at accelerometer output)      |

The STATUS\_SPIAux register is read by the auxiliary SPI.

**Table 83. STATUS\_SPIAux register**

|   |   |   |   |   |                  |     |      |
|---|---|---|---|---|------------------|-----|------|
| 0 | 0 | 0 | 0 | 0 | GYRO<br>SETTLING | GDA | XLDA |
|---|---|---|---|---|------------------|-----|------|

**Table 84. STATUS\_SPIAux register description**

|               |  |
|---------------|--|
| GYRO_SETTLING | High when the gyroscope output is in the settling phase                                    |
| GDA           | Gyroscope data available (reset when one of the high parts of the output data is read)     |
| XLDA          | Accelerometer data available (reset when one of the high parts of the output data is read) |

### 9.30 OUT\_TEMP\_L (20h), OUT\_TEMP\_H (21h)

Temperature data output register (r). L and H registers together express a 16-bit word in two's complement.

**Table 85. OUT\_TEMP\_L register**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Temp7 | Temp6 | Temp5 | Temp4 | Temp3 | Temp2 | Temp1 | Temp0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

**Table 86. OUT\_TEMP\_H register**

|        |        |        |        |        |        |       |       |
|--------|--------|--------|--------|--------|--------|-------|-------|
| Temp15 | Temp14 | Temp13 | Temp12 | Temp11 | Temp10 | Temp9 | Temp8 |
|--------|--------|--------|--------|--------|--------|-------|-------|

**Table 87. OUT\_TEMP register description**

|            |  |
|------------|--|
| Temp[15:0] | Temperature sensor output data<br>The value is expressed as two's complement sign extended on the MSB. |
|------------|--|

### 9.31 OUTX\_L\_G (22h) and OUTX\_H\_G (23h)

Angular rate sensor pitch axis (X) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

If this register is read by the primary interface, data are according to the full scale and ODR settings ([CTRL2\\_G \(11h\)](#)) of gyro user interface.

If this register is read by the auxiliary interface, data are according to the full scale and ODR (6.66 kHz) settings of the OIS gyro.

**Table 88. OUTX\_L\_G register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 89. OUTX\_H\_G register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 90. OUTX\_H\_G register description**

|         |   |
|---------|---|
| D[15:0] | Pitch axis (X) angular rate value<br>D[15:0] expressed in two's complement and its value depends on the interface used:<br>SPI1/I <sup>2</sup> C/MIPI I3C <sup>SM</sup> : Gyro UI chain pitch axis output<br>SPI2: Gyro OIS chain pitch axis output |
|---------|---|

### 9.32 OUTY\_L\_G (24h) and OUTY\_H\_G (25h)

Angular rate sensor roll axis (Y) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

If this register is read by the primary interface, data are according to the full scale and ODR settings (CTRL2\_G (11h)) of the gyro user interface.

If this register is read by the auxiliary interface, data are according to the full scale and ODR (6.66 kHz) settings of the OIS gyro.

**Table 91. OUTY\_L\_G register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 92. OUTY\_H\_G register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 93. OUTY\_H\_G register description**

|         |  |
|---------|--|
| D[15:0] | Roll axis (Y) angular rate value<br>D[15:0] expressed in two's complement and its value depends on the interface used:<br>SPI1/I <sup>2</sup> C/MIPI I3C <sup>SM</sup> : Gyro UI chain roll axis output<br>SPI2: Gyro OIS chain roll axis output |
|---------|--|

### 9.33 OUTZ\_L\_G (26h) and OUTZ\_H\_G (27h)

Angular rate sensor yaw axis (Z) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

If this register is read by the primary interface, data are according to the full scale and ODR settings (CTRL2\_G (11h)) of the gyro user interface.

If this register is read by the auxiliary interface, data are according to the full scale and ODR (6.66 kHz) settings of the OIS gyro.

**Table 94. OUTZ\_L\_G register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 95. OUTZ\_H\_G register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 96. OUTZ\_H\_G register description**

|         |   |
|---------|---|
| D[15:0] | Yaw axis (Z) angular rate value<br>D[15:0] expressed in two's complement and its value depends on the interface used:<br>SPI1/I <sup>2</sup> C/MIPI I3C <sup>SM</sup> : Gyro UI chain yaw axis output<br>SPI2: Gyro OIS chain yaw axis output |
|---------|---|

### 9.34 OUTX\_L\_A (28h) and OUTX\_H\_A (29h)

Linear acceleration sensor X-axis output register (r). The value is expressed as a 16-bit word in two's complement.

If this register is read by the primary interface, data are according to the full-scale and ODR settings (CTRL1\_XL (10h)) of the accelerometer user interface.

If this register is read by the auxiliary interface, data are according to the full-scale and ODR (6.66 kHz) settings of the OIS (CTRL3\_OIS (72h)).

**Table 97. OUTX\_L\_A register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 98. OUTX\_H\_A register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 99. OUTX\_H\_A register description**

|         |   |
|---------|---|
| D[15:0] | X-axis linear acceleration value.<br>D[15:0] expressed in two's complement and its value depends on the interface used:<br>SPI1/I <sup>2</sup> C/MIPI I3C <sup>SM</sup> : Accelerometer UI chain X-axis output<br>SPI2: Accelerometer OIS chain X-axis output |
|---------|---|

### 9.35 OUTY\_L\_A (2Ah) and OUTY\_H\_A (2Bh)

Linear acceleration sensor Y-axis output register (r). The value is expressed as a 16-bit word in two's complement.

If this register is read by the primary interface, data are according to the full-scale and ODR settings (CTRL1\_XL (10h)) of the accelerometer user interface.

If this register is read by the auxiliary interface, data are according to the full-scale and ODR (6.66 kHz) settings of the OIS (CTRL3\_OIS (72h)).

**Table 100. OUTY\_L\_A register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 101. OUTY\_H\_A register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 102. OUTY\_H\_A register description**

|         |  |
|---------|--|
| D[15:0] | Y-axis linear acceleration value<br>D[15:0] expressed in two's complement and its value depends on the interface used:<br>SPI1/I <sup>2</sup> C/MIPI I3C <sup>SM</sup> : Accelerometer UI chain Y-axis output<br>SPI2: Accelerometer OIS chain Y-axis output |
|---------|--|

### 9.36 OUTZ\_L\_A (2Ch) and OUTZ\_H\_A (2Dh)

Linear acceleration sensor Z-axis output register (r). The value is expressed as a 16-bit word in two's complement.

If this register is read by the primary interface, data are according to the full-scale and ODR settings (CTRL1\_XL (10h)) of the accelerometer user interface.

If this register is read by the auxiliary interface, data are according to the full-scale and ODR (6.66 kHz) settings of the OIS (CTRL3\_OIS (72h)).

**Table 103. OUTZ\_L\_A register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

**Table 104. OUTZ\_H\_A register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 105. OUTZ\_H\_A register description**

|         |  |
|---------|--|
| D[15:0] | Z-axis linear acceleration value<br>D[15:0] expressed in two's complement and its value depends on the interface used:<br>SPI1/I <sup>2</sup> C/MIPI I3C <sup>SM</sup> : Accelerometer UI chain Z-axis output<br>SPI2: Accelerometer OIS chain Z-axis output |
|---------|--|

### 9.37 EMB\_FUNC\_STATUS\_MAINPAGE (35h)

Embedded function status register (r)

**Table 106. EMB\_FUNC\_STATUS\_MAINPAGE register**

|           |   |           |         |             |   |   |   |
|-----------|---|-----------|---------|-------------|---|---|---|
| IS_FSM_LC | 0 | IS_SIGMOT | IS_TILT | IS_STEP_DET | 0 | 0 | 0 |
|-----------|---|-----------|---------|-------------|---|---|---|

**Table 107. EMB\_FUNC\_STATUS\_MAINPAGE register description**

|             |  |
|-------------|--|
| IS_FSM_LC   | Interrupt status bit for FSM long counter timeout interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_SIGMOT   | Interrupt status bit for significant motion detection<br>(1: interrupt detected; 0: no interrupt)              |
| IS_TILT     | Interrupt status bit for tilt detection<br>(1: interrupt detected; 0: no interrupt)                            |
| IS_STEP_DET | Interrupt status bit for step detection<br>(1: interrupt detected; 0: no interrupt)                            |

### 9.38 FSM\_STATUS\_A\_MAINPAGE (36h)

Finite State Machine status register (r)

**Table 108. FSM\_STATUS\_A\_MAINPAGE register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| IS_FSM8 | IS_FSM7 | IS_FSM6 | IS_FSM5 | IS_FSM4 | IS_FSM3 | IS_FSM2 | IS_FSM1 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 109. FSM\_STATUS\_A\_MAINPAGE register description**

|         |   |
|---------|---|
| IS_FSM8 | Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM7 | Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM6 | Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM5 | Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM4 | Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM3 | Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM2 | Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM1 | Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt) |

### 9.39 FSM\_STATUS\_B\_MAINPAGE (37h)

Finite State Machine status register (r)

**Table 110. FSM\_STATUS\_B\_MAINPAGE register**

|          |          |          |          |          |          |          |         |
|----------|----------|----------|----------|----------|----------|----------|---------|
| IS_FSM16 | IS_FSM15 | IS_FSM14 | IS_FSM13 | IS_FSM12 | IS_FSM11 | IS_FSM10 | IS_FSM9 |
|----------|----------|----------|----------|----------|----------|----------|---------|

**Table 111. FSM\_STATUS\_B\_MAINPAGE register description**

|          |  |
|----------|--|
| IS_FSM16 | Interrupt status bit for FSM16 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM15 | Interrupt status bit for FSM15 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM14 | Interrupt status bit for FSM14 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM13 | Interrupt status bit for FSM13 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM12 | Interrupt status bit for FSM12 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM11 | Interrupt status bit for FSM11 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM10 | Interrupt status bit for FSM10 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM9  | Interrupt status bit for FSM9 interrupt event. (1: interrupt detected; 0: no interrupt)  |

## 9.40 MLC\_STATUS\_MAINPAGE (38h)

Machine Learning Core status register (r)

**Table 112. MLC\_STATUS\_MAINPAGE register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| IS_MLC8 | IS_MLC7 | IS_MLC6 | IS_MLC5 | IS_MLC4 | IS_MLC3 | IS_MLC2 | IS_MLC1 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 113. MLC\_STATUS\_MAINPAGE register description**

|         |   |
|---------|---|
| IS_MLC8 | Interrupt status bit for MLC8 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC7 | Interrupt status bit for MLC7 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC6 | Interrupt status bit for MLC6 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC5 | Interrupt status bit for MLC5 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC4 | Interrupt status bit for MLC4 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC3 | Interrupt status bit for MLC3 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC2 | Interrupt status bit for MLC2 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC1 | Interrupt status bit for MLC1 interrupt event. (1: interrupt detected; 0: no interrupt) |

## 9.41 STATUS\_MASTER\_MAINPAGE (39h)

Sensor hub source register (r)

**Table 114. STATUS\_MASTER\_MAINPAGE register**

|              |             |             |             |             |   |   |                |
|--------------|-------------|-------------|-------------|-------------|---|---|----------------|
| WR_ONCE_DONE | SLAVE3_NACK | SLAVE2_NACK | SLAVE1_NACK | SLAVE0_NACK | 0 | 0 | SENS_HUB_ENDOP |
|--------------|-------------|-------------|-------------|-------------|---|---|----------------|

**Table 115. STATUS\_MASTER\_MAINPAGE register description**

|                |   |
|----------------|---|
| WR_ONCE_DONE   | When the bit WRITE_ONCE in <b>MASTER_CONFIG (14h)</b> is configured as 1, this bit is set to 1 when the write operation on slave 0 has been performed and completed. Default value: 0 |
| SLAVE3_NACK    | This bit is set to 1 if Not acknowledge occurs on slave 3 communication. Default value: 0   |
| SLAVE2_NACK    | This bit is set to 1 if Not acknowledge occurs on slave 2 communication. Default value: 0   |
| SLAVE1_NACK    | This bit is set to 1 if Not acknowledge occurs on slave 1 communication. Default value: 0   |
| SLAVE0_NACK    | This bit is set to 1 if Not acknowledge occurs on slave 0 communication. Default value: 0   |
| SENS_HUB_ENDOP | Sensor hub communication status. Default value: 0<br>(0: sensor hub communication not concluded;<br>1: sensor hub communication concluded)  |



## 9.42 FIFO\_STATUS1 (3Ah)

FIFO status register 1 (r)

**Table 116. FIFO\_STATUS1 register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| DIFF_FIFO_7 | DIFF_FIFO_6 | DIFF_FIFO_5 | DIFF_FIFO_4 | DIFF_FIFO_3 | DIFF_FIFO_2 | DIFF_FIFO_1 | DIFF_FIFO_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 117. FIFO\_STATUS1 register description**

|                 |  |
|-----------------|--|
| DIFF_FIFO_[7:0] | Number of unread sensor data (TAG + 6 bytes) stored in FIFO<br>In conjunction with DIFF_FIFO[9:8] in FIFO_STATUS2 (3Bh). |
|-----------------|--|

## 9.43 FIFO\_STATUS2 (3Bh)

FIFO status register 2 (r)

**Table 118. FIFO\_STATUS2 register**

|             |             |              |                |                  |   |             |             |
|-------------|-------------|--------------|----------------|------------------|---|-------------|-------------|
| FIFO_WTM_IA | FIFO_OVR_IA | FIFO_FULL_IA | COUNTER_BDR_IA | FIFO_OVR_LATCHED | 0 | DIFF_FIFO_9 | DIFF_FIFO_8 |
|-------------|-------------|--------------|----------------|------------------|---|-------------|-------------|

**Table 119. FIFO\_STATUS2 register description**

|                  |  |
|------------------|--|
| FIFO_WTM_IA      | FIFO watermark status. Default value: 0<br>(0: FIFO filling is lower than WTM;<br>1: FIFO filling is equal to or greater than WTM)<br>Watermark is set through bits WTM[8:0] in FIFO_CTRL1 (07h) and FIFO_CTRL2 (08h). |
| FIFO_OVR_IA      | FIFO overrun status. Default value: 0<br>(0: FIFO is not completely filled; 1: FIFO is completely filled)  |
| FIFO_FULL_IA     | Smart FIFO full status. Default value: 0<br>(0: FIFO is not full; 1: FIFO will be full at the next ODR)  |
| COUNTER_BDR_IA   | Counter BDR reaches the CNT_BDR_TH_[10:0] threshold set in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch). Default value: 0<br>This bit is reset when these registers are read.                                     |
| FIFO_OVR_LATCHED | Latched FIFO overrun status. Default value: 0<br>This bit is reset when this register is read.   |
| DIFF_FIFO_[9:8]  | Number of unread sensor data (TAG + 6 bytes) stored in FIFO. Default value: 00<br>In conjunction with DIFF_FIFO[7:0] in FIFO_STATUS1 (3Ah).  |

## 9.44 **TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h)**

Timestamp first data output register (r). The value is expressed as a 32-bit word and the bit resolution is 25  $\mu$ s.

**Table 120. TIMESTAMP3 register**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 |
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 121. TIMESTAMP2 register**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 122. TIMESTAMP1 register**

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|

**Table 123. TIMESTAMP0 register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

|         |   |
|---------|---|
| D[31:0] | Timestamp output registers: 1LSB = 25 $\mu$ s |
|---------|---|

The formula below can be used to calculate a better estimation of the actual timestamp resolution:

$$TS\_Res = 1 / (40000 + (0.0015 * INTERNAL\_FREQ\_FINE * 40000))$$

where INTERNAL\_FREQ\_FINE is the content of [INTERNAL\\_FREQ\\_FINE \(63h\)](#).

## 9.45 TAP\_CFG0 (56h)

Activity/inactivity functions, configuration of filtering, and tap recognition functions (r/w)

**Table 124. TAP\_CFG0 register**

|                  |                 |                     |           |          |          |          |     |
|------------------|-----------------|---------------------|-----------|----------|----------|----------|-----|
| 0 <sup>(1)</sup> | INT_CLR_ON_READ | SLEEP_STATUS_ON_INT | SLOPE_FDS | TAP_X_EN | TAP_Y_EN | TAP_Z_EN | LIR |
|------------------|-----------------|---------------------|-----------|----------|----------|----------|-----|

1. This bit must be set to '0' for the correct operation of the device.

**Table 125. TAP\_CFG0 register description**

|                     |   |
|---------------------|---|
| INT_CLR_ON_READ     | This bit allows immediately clearing the latched interrupts of an event detection upon the read of the corresponding status register. It must be set to 1 together with LIR. Default value: 0<br>(0: latched interrupt signal cleared at the end of the ODR period;<br>1: latched interrupt signal immediately cleared) |
| SLEEP_STATUS_ON_INT | Activity/inactivity interrupt mode configuration.<br>If INT1_SLEEP_CHANGE or INT2_SLEEP_CHANGE bits are enabled, drives the sleep status or sleep change on the INT pins. Default value: 0<br>(0: sleep change notification on INT pins; 1: sleep status reported on INT pins)  |
| SLOPE_FDS           | HPF or SLOPE filter selection on wake-up and Activity/Inactivity functions. Default value: 0<br>(0: SLOPE filter applied; 1: HPF applied)   |
| TAP_X_EN            | Enable X direction in tap recognition. Default value: 0<br>(0: X direction disabled; 1: X direction enabled)  |
| TAP_Y_EN            | Enable Y direction in tap recognition. Default value: 0<br>(0: Y direction disabled; 1: Y direction enabled)  |
| TAP_Z_EN            | Enable Z direction in tap recognition. Default value: 0<br>(0: Z direction disabled; 1: Z direction enabled)  |
| LIR                 | Latched Interrupt. Default value: 0<br>(0: interrupt request not latched; 1: interrupt request latched)   |

## 9.46 TAP\_CFG1 (57h)

Tap configuration register (r/w)

**Table 126. TAP\_CFG1 register**

|                |                |                |             |             |             |             |             |
|----------------|----------------|----------------|-------------|-------------|-------------|-------------|-------------|
| TAP_PRIORITY_2 | TAP_PRIORITY_1 | TAP_PRIORITY_0 | TAP_THS_X_4 | TAP_THS_X_3 | TAP_THS_X_2 | TAP_THS_X_1 | TAP_THS_X_0 |
|----------------|----------------|----------------|-------------|-------------|-------------|-------------|-------------|

**Table 127. TAP\_CFG1 register description**

|                    |   |
|--------------------|---|
| TAP_PRIORITY_[2:0] | Selection of axis priority for TAP detection (see Table 128)                            |
| TAP_THS_X_[4:0]    | X-axis tap recognition threshold. Default value: 0<br>1 LSB = FS_XL / (2 <sup>5</sup> ) |

**Table 128. TAP priority decoding**

| TAP_PRIORITY_[2:0] | Max. priority | Mid. priority | Min. priority |
|--------------------|---------------|---------------|---------------|
| 000                | X             | Y             | Z             |
| 001                | Y             | X             | Z             |
| 010                | X             | Z             | Y             |
| 011                | Z             | Y             | X             |
| 100                | X             | Y             | Z             |
| 101                | Y             | Z             | X             |
| 110                | Z             | X             | Y             |
| 111                | Z             | Y             | X             |

## 9.47 TAP\_CFG2 (58h)

Enables interrupt and inactivity functions, and tap recognition functions (r/w)

**Table 129. TAP\_CFG2 register**

|                   |           |           |             |             |             |             |             |
|-------------------|-----------|-----------|-------------|-------------|-------------|-------------|-------------|
| INTERRUPTS_ENABLE | INACT_EN1 | INACT_EN0 | TAP_THS_Y_4 | TAP_THS_Y_3 | TAP_THS_Y_2 | TAP_THS_Y_1 | TAP_THS_Y_0 |
|-------------------|-----------|-----------|-------------|-------------|-------------|-------------|-------------|

**Table 130. TAP\_CFG2 register description**

|                   |  |
|-------------------|--|
| INTERRUPTS_ENABLE | Enable basic interrupts (6D/4D, free-fall, wake-up, tap, inactivity). Default value: 0<br>(0: interrupt disabled; 1: interrupt enabled)  |
| INACT_EN[1:0]     | Enable activity/inactivity (sleep) function. Default value: 00<br>(00: stationary/motion-only interrupts generated, XL and gyro do not change;<br>01: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro does not change;<br>10: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro to sleep mode;<br>11: sets accelerometer ODR to 12.5 Hz (low-power mode), gyro to power-down mode) |
| TAP_THS_Y_[4:0]   | Y-axis tap recognition threshold. Default value: 0<br>1 LSB = FS_XL / (2 <sup>5</sup> )  |

## 9.48 TAP\_THS\_6D (59h)

Portrait/landscape position and tap function threshold register (r/w)

**Table 131. TAP\_THS\_6D register**

|        |           |           |             |             |             |             |             |
|--------|-----------|-----------|-------------|-------------|-------------|-------------|-------------|
| D4D_EN | SIXD_THS1 | SIXD_THS0 | TAP_THS_Z_4 | TAP_THS_Z_3 | TAP_THS_Z_2 | TAP_THS_Z_1 | TAP_THS_Z_0 |
|--------|-----------|-----------|-------------|-------------|-------------|-------------|-------------|

**Table 132. TAP\_THS\_6D register description**

|                 |  |
|-----------------|--|
| D4D_EN          | Enables detection of 4D orientation. Z-axis position detection is disabled. Default value: 0 (0: disabled; 1: enabled) |
| SIXD_THS[1:0]   | Threshold for 4D/6D function:<br>(00: 80 degrees (default);<br>01: 70 degrees;<br>10: 60 degrees;<br>11: 50 degrees)   |
| TAP_THS_Z_[4:0] | Z-axis recognition threshold. Default value: 0<br>1 LSB = $FS_{XL} / (2^5)$  |

## 9.49 INT\_DUR2 (5Ah)

Tap recognition function setting register (r/w)

**Table 133. INT\_DUR2 register**

|      |      |      |      |        |        |        |        |
|------|------|------|------|--------|--------|--------|--------|
| DUR3 | DUR2 | DUR1 | DUR0 | QUIET1 | QUIET0 | SHOCK1 | SHOCK0 |
|------|------|------|------|--------|--------|--------|--------|

**Table 134. INT\_DUR2 register description**

|            |  |
|------------|--|
| DUR[3:0]   | Duration of maximum time gap for double-tap recognition. Default: 0000<br>When double-tap recognition is enabled, this register expresses the maximum time between two consecutive detected taps to determine a double-tap event. The default value of these bits is 0000b which corresponds to 16/ODR_XL time. If the DUR[3:0] bits are set to a different value, 1LSB corresponds to 32/ODR_XL time. |
| QUIET[1:0] | Expected quiet time after a tap detection. Default value: 00<br>Quiet time is the time after the first detected tap in which there must not be any overthreshold event. The default value of these bits is 00b which corresponds to 2/ODR_XL time. If the QUIET[1:0] bits are set to a different value, 1LSB corresponds to 4/ODR_XL time.   |
| SHOCK[1:0] | Maximum duration of overthreshold event. Default value: 00<br>Maximum duration is the maximum time of an overthreshold signal detection to be recognized as a tap event. The default value of these bits is 00b which corresponds to 4/ODR_XL time. If the SHOCK[1:0] bits are set to a different value, 1LSB corresponds to 8/ODR_XL time.  |

## 9.50 WAKE\_UP\_THS (5Bh)

Single/double-tap selection and wake-up configuration (r/w)

**Table 135. WAKE\_UP\_THS register**

|                    |                |         |         |         |         |         |         |
|--------------------|----------------|---------|---------|---------|---------|---------|---------|
| SINGLE_ DOUBLE_TAP | USR_OFF_ ON_WU | WK_THS5 | WK_THS4 | WK_THS3 | WK_THS2 | WK_THS1 | WK_THS0 |
|--------------------|----------------|---------|---------|---------|---------|---------|---------|

**Table 136. WAKE\_UP\_THS register description**

|                   |   |
|-------------------|---|
| SINGLE_DOUBLE_TAP | Single/double-tap event enable. Default: 0<br>(0: only single-tap event enabled;<br>1: both single and double-tap events enabled) |
| USR_OFF_ON_WU     | Sends the low-pass filtered data with user offset correction (instead of high-pass filtered data) to the wakeup function.         |
| WK_THS[5:0]       | Threshold for wakeup: 1 LSB weight depends on WAKE_THS_W in WAKE_UP_DUR (5Ch). Default value: 000000                              |

## 9.51 WAKE\_UP\_DUR (5Ch)

Free-fall, wakeup and sleep mode functions duration setting register (r/w)

**Table 137. WAKE\_UP\_DUR register**

|         |           |           |             |             |             |             |             |
|---------|-----------|-----------|-------------|-------------|-------------|-------------|-------------|
| FF_DUR5 | WAKE_DUR1 | WAKE_DUR0 | WAKE_ THS_W | SLEEP_ DUR3 | SLEEP_ DUR2 | SLEEP_ DUR1 | SLEEP_ DUR0 |
|---------|-----------|-----------|-------------|-------------|-------------|-------------|-------------|

**Table 138. WAKE\_UP\_DUR register description**

|                |  |
|----------------|--|
| FF_DUR5        | Free fall duration event. Default: 0<br>For the complete configuration of the free-fall duration, refer to FF_DUR[4:0] in FREE_FALL (5Dh) configuration.<br>1 LSB = 1 ODR_time |
| WAKE_DUR[1:0]  | Wake up duration event. Default: 00<br>1LSB = 1 ODR_time   |
| WAKE_THS_W     | Weight of 1 LSB of wakeup threshold. Default: 0<br>(0: 1 LSB = FS_XL / (2 <sup>6</sup> );<br>1: 1 LSB = FS_XL / (2 <sup>8</sup> ))   |
| SLEEP_DUR[3:0] | Duration to go in sleep mode. Default value: 0000 (this corresponds to 16 ODR)<br>1 LSB = 512 ODR  |

## 9.52 FREE\_FALL (5Dh)

Free-fall function duration setting register (r/w)

**Table 139. FREE\_FALL register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| FF_DUR4 | FF_DUR3 | FF_DUR2 | FF_DUR1 | FF_DUR0 | FF_THS2 | FF_THS1 | FF_THS0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 140. FREE\_FALL register description**

|             |   |
|-------------|---|
| FF_DUR[4:0] | Free-fall duration event. Default: 0<br>For the complete configuration of the free fall duration, refer to FF_DUR5 in WAKE_UP_DUR (5Ch) configuration.                  |
| FF_THS[2:0] | Free-fall threshold setting:<br>(000: 156 mg (default);<br>001: 219 mg;<br>010: 250 mg;<br>011: 312 mg;<br>100: 344 mg;<br>101: 406 mg;<br>110: 469 mg;<br>111: 500 mg) |

## 9.53 MD1\_CFG (5Eh)

Functions routing on INT1 register (r/w)

**Table 141. MD1\_CFG register**

|                   |                 |         |         |                 |         |               |           |
|-------------------|-----------------|---------|---------|-----------------|---------|---------------|-----------|
| INT1_SLEEP_CHANGE | INT1_SINGLE_TAP | INT1_WU | INT1_FF | INT1_DOUBLE_TAP | INT1_6D | INT1_EMB_FUNC | INT1_SHUB |
|-------------------|-----------------|---------|---------|-----------------|---------|---------------|-----------|

**Table 142. MD1\_CFG register description**

|                                  |   |
|----------------------------------|---|
| INT1_SLEEP_CHANGE <sup>(1)</sup> | Routing of activity/inactivity recognition event on INT1. Default: 0<br>(0: routing of activity/inactivity event on INT1 disabled;<br>1: routing of activity/inactivity event on INT1 enabled)  |
| INT1_SINGLE_TAP                  | Routing of single-tap recognition event on INT1. Default: 0<br>(0: routing of single-tap event on INT1 disabled;<br>1: routing of single-tap event on INT1 enabled)   |
| INT1_WU                          | Routing of wakeup event on INT1. Default value: 0<br>(0: routing of wakeup event on INT1 disabled;<br>1: routing of wakeup event on INT1 enabled)   |
| INT1_FF                          | Routing of free-fall event on INT1. Default value: 0<br>(0: routing of free-fall event on INT1 disabled;<br>1: routing of free-fall event on INT1 enabled)  |
| INT1_DOUBLE_TAP                  | Routing of tap event on INT1. Default value: 0<br>(0: routing of double-tap event on INT1 disabled;<br>1: routing of double-tap event on INT1 enabled)  |
| INT1_6D                          | Routing of 6D event on INT1. Default value: 0<br>(0: routing of 6D event on INT1 disabled;<br>1: routing of 6D event on INT1 enabled)   |
| INT1_EMB_FUNC                    | Routing of embedded functions event on INT1. Default value: 0<br>(0: routing of embedded functions event on INT1 disabled;<br>1: routing embedded functions event on INT1 enabled)  |
| INT1_SHUB                        | Routing of sensor hub communication concluded event on INT1. Default value: 0<br>(0: routing of sensor hub communication concluded event on INT1 disabled;<br>1: routing of sensor hub communication concluded event on INT1 enabled) |

1. Activity/Inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP\_STATUS\_ON\_INT bit in the TAP\_CFG0 (56h) register.



## 9.54 MD2\_CFG (5Fh)

Functions routing on INT2 register (r/w)

**Table 143. MD2\_CFG register**

| INT2_SLEEP_CHANGE | INT2_SINGLE_TAP | INT2_WU | INT2_FF | INT2_DOUBLE_TAP | INT2_6D | INT2_EMB_FUNC | INT2_TIMESTAMP |
|-------------------|-----------------|---------|---------|-----------------|---------|---------------|----------------|
|-------------------|-----------------|---------|---------|-----------------|---------|---------------|----------------|

**Table 144. MD2\_CFG register description**

|                                  |  |
|----------------------------------|--|
| INT2_SLEEP_CHANGE <sup>(1)</sup> | Routing of activity/inactivity recognition event on INT2. Default: 0<br>(0: routing of activity/inactivity event on INT2 disabled;<br>1: routing of activity/inactivity event on INT2 enabled) |
| INT2_SINGLE_TAP                  | Single-tap recognition routing on INT2. Default: 0<br>(0: routing of single-tap event on INT2 disabled;<br>1: routing of single-tap event on INT2 enabled)                                     |
| INT2_WU                          | Routing of wakeup event on INT2. Default value: 0<br>(0: routing of wakeup event on INT2 disabled;<br>1: routing of wake-up event on INT2 enabled)   |
| INT2_FF                          | Routing of free-fall event on INT2. Default value: 0<br>(0: routing of free-fall event on INT2 disabled;<br>1: routing of free-fall event on INT2 enabled)                                     |
| INT2_DOUBLE_TAP                  | Routing of tap event on INT2. Default value: 0<br>(0: routing of double-tap event on INT2 disabled;<br>1: routing of double-tap event on INT2 enabled)   |
| INT2_6D                          | Routing of 6D event on INT2. Default value: 0<br>(0: routing of 6D event on INT2 disabled;<br>1: routing of 6D event on INT2 enabled)  |
| INT2_EMB_FUNC                    | Routing of embedded functions event on INT2. Default value: 0<br>(0: routing of embedded functions event on INT2 disabled;<br>1: routing embedded functions event on INT2 enabled)             |
| INT2_TIMESTAMP                   | Enables routing on INT2 pin of the alert for timestamp overflow within 6.4 ms.   |

1. Activity/Inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP\_STATUS\_ON\_INT bit in the TAP\_CFG0 (56h) register.

## 9.55 S4S\_ST\_CMD\_CODE (60h)

S4S master command register (r/w)

**Table 145. S4S\_ST\_CMD\_CODE register**

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| ST_CMD_CODE7 | ST_CMD_CODE6 | ST_CMD_CODE5 | ST_CMD_CODE4 | ST_CMD_CODE3 | ST_CMD_CODE2 | ST_CMD_CODE1 | ST_CMD_CODE0 |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

**Table 146. S4S\_ST\_CMD\_CODE register description**

|                  |  |
|------------------|--|
| ST_CMD_CODE[7:0] | Master command code used for S4S. Default value: 0 |
|------------------|--|

## 9.56 S4S\_DT\_REG (61h)

S4S DT register (r/w)

**Table 147. S4S\_DT\_REG register**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| DT7 | DT6 | DT5 | DT4 | DT3 | DT2 | DT1 | DT0 |
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 148. S4S\_DT\_REG register description**

|         |                                   |
|---------|-----------------------------------|
| DT[7:0] | DT used for S4S. Default value: 0 |
|---------|-----------------------------------|

## 9.57 I3C\_BUS\_AVB (62h)

I3C\_BUS\_AVB register (r/w)

**Table 149. I3C\_BUS\_AVB register**

|                  |                  |                  |                  |                  |                  |                  |             |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | I3C_Bus_Avb_Sel1 | I3C_Bus_Avb_Sel0 | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | PD_DIS_INT1 |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 150. I3C\_BUS\_AVB register description**

|                      |   |
|----------------------|---|
| I3C_Bus_Avb_Sel[1:0] | <p>These bits are used to select the bus available time when I3C IBI is used.</p> <p>Default value: 00</p> <p>(00: bus available time equal to 50 µsec (default);</p> <p>01: bus available time equal to 2 µsec;</p> <p>10: bus available time equal to 1 msec;</p> <p>11: bus available time equal to 25 msec)</p> |
| PD_DIS_INT1          | <p>This bit allows disabling the INT1 pull-down.</p> <p>(0: Pull-down on INT1 enabled (pull-down is effectively connected only when no interrupts are routed to the INT1 pin or when the I3C dynamic address is assigned);</p> <p>1: Pull-down on INT1 disabled (pull-down not connected))</p>                      |

## 9.58 INTERNAL\_FREQ\_FINE (63h)

Internal frequency register (r)

**Table 151. INTERNAL\_FREQ\_FINE register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| FREQ_FINE7 | FREQ_FINE6 | FREQ_FINE5 | FREQ_FINE4 | FREQ_FINE3 | FREQ_FINE2 | FREQ_FINE1 | FREQ_FINE0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 152. INTERNAL\_FREQ\_FINE register description**

|                |  |
|----------------|--|
| FREQ_FINE[7:0] | Difference in percentage of the effective ODR (and timestamp rate) with respect to the typical. Step: 0.15%. 8-bit format, 2's complement. |
|----------------|--|

The formula below can be used to calculate a better estimation of the actual ODR:

$$\text{ODR\_Actual} = (6667 + ((0.0015 * \text{INTERNAL\_FREQ\_FINE}) * 6667)) / \text{ODR\_Coeff}$$

| Selected_ODR | ODR_Coeff |
|--------------|-----------|
| 12.5         | 512       |
| 26           | 256       |
| 52           | 128       |
| 104          | 64        |
| 208          | 32        |
| 416          | 16        |
| 833          | 8         |
| 1667         | 4         |
| 3333         | 2         |
| 6667         | 1         |

The Selected\_ODR parameter has to be derived from the ODR\_XL selection (Table 50. Accelerometer ODR selection) in order to estimate the accelerometer ODR and from the ODR\_G selection (Table 53. Gyroscope ODR configuration setting) in order to estimate the gyroscope ODR.

## 9.59 INT\_OIS (6Fh)

OIS interrupt configuration register and accelerometer self-test enable setting. Primary interface for read-only (r); only Aux SPI can write to this register (r/w).

**Table 153. INT\_OIS register**

|               |          |            |   |   |                  |            |            |
|---------------|----------|------------|---|---|------------------|------------|------------|
| INT2_DRDY_OIS | LVL2_OIS | DEN_LH_OIS | - | - | 0 <sup>(1)</sup> | ST1_XL_OIS | ST0_XL_OIS |
|---------------|----------|------------|---|---|------------------|------------|------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 154. INT\_OIS register description**

|                |   |
|----------------|---|
| INT2_DRDY_OIS  | Enables OIS chain DRDY on INT2 pin. This setting has priority over all other INT2 settings.   |
| LVL2_OIS       | Enables level-sensitive latched mode on the OIS chain. Default value: 0   |
| DEN_LH_OIS     | Indicates polarity of DEN signal on OIS chain<br>(0: DEN pin is active-low;<br>1: DEN pin is active-high)   |
| ST[1:0]_XL_OIS | Selects accelerometer self-test – effective only if XL OIS chain is enabled. Default value: 00<br>(00: Normal mode;<br>01: Positive sign self-test;<br>10: Negative sign self-test;<br>11: not allowed) |

## 9.60 CTRL1\_OIS (70h)

OIS configuration register. Primary interface for read-only (r); only Aux SPI can write to this register (r/w).

**Table 155. CTRL1\_OIS register**

|                  |          |         |          |           |           |            |             |
|------------------|----------|---------|----------|-----------|-----------|------------|-------------|
| 0 <sup>(1)</sup> | LVL1_OIS | SIM_OIS | Mode4_EN | FS1_G_OIS | FS0_G_OIS | FS_125_OIS | OIS_EN_SPI2 |
|------------------|----------|---------|----------|-----------|-----------|------------|-------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 156. CTRL1\_OIS register description**

|               |   |
|---------------|---|
| LVL1_OIS      | Enables level-sensitive trigger mode on OIS chain. Default value: 0   |
| SIM_OIS       | SPI2 3- or 4-wire interface. Default value: 0<br>(0: 4-wire SPI2;<br>1: 3-wire SPI2)  |
| Mode4_EN      | Enables accelerometer OIS chain. OIS outputs are available through SPI2 in registers <a href="#">OUTX_L_A (28h)</a> and <a href="#">OUTX_H_A (29h)</a> - <a href="#">OUTZ_L_A (2Ch)</a> and <a href="#">OUTZ_H_A (2Dh)</a> .<br>Note: OIS_EN_SPI2 must be enabled (i.e. set to '1') to enable also XL OIS chain.  |
| FS[1:0]_G_OIS | Selects gyroscope OIS chain full-scale<br>(00: ±250 dps;<br>01: ±500 dps;<br>10: ±1000 dps;<br>11: ±2000 dps)   |
| FS_125_OIS    | Selects gyroscope OIS chain full-scale ±125 dps<br>(0: FS selected through bits FS[1:0]_OIS_G;<br>1: ±125 dps)  |
| OIS_EN_SPI2   | Enables OIS chain data processing for gyro in Mode 3 and Mode 4 (mode4_en = 1) and accelerometer data in Mode 4 (mode4_en = 1).<br>When the OIS chain is enabled, the OIS outputs are available through the SPI2 in registers <a href="#">OUTX_L_G (22h)</a> and <a href="#">OUTX_H_G (23h)</a> through <a href="#">OUTZ_L_A (2Ch)</a> and <a href="#">OUTZ_H_A (2Dh)</a> and <a href="#">STATUS_REG (1Eh)</a> / <a href="#">STATUS_SPIAux (1Eh)</a> , and LPF1 is dedicated to this chain. |

DEN mode selection can be done using the LVL1\_OIS bit of register CTRL1\_OIS (70h) and the LVL2\_OIS bit of register INT\_OIS (6Fh).

DEN mode on the OIS path is active in the gyroscope only.

**Table 157. DEN mode selection**

| LVL1_OIS, LVL2_OIS | DEN mode                                 |
|--------------------|--|
| 10                 | Level-sensitive trigger mode is selected |
| 11                 | Level-sensitive latched mode is selected |

## 9.61 CTRL2\_OIS (71h)

OIS configuration register. Primary interface for read-only (r); only Aux SPI can write to this register (r/w).

**Table 158. CTRL2\_OIS register**

|   |   |          |          |                  |             |             |           |
|---|---|----------|----------|------------------|-------------|-------------|-----------|
| - | - | HPM1_OIS | HPM0_OIS | 0 <sup>(1)</sup> | FTYPE_1_OIS | FTYPE_0_OIS | HP_EN_OIS |
|---|---|----------|----------|------------------|-------------|-------------|-----------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 159. CTRL2\_OIS register description**

|                 |   |
|-----------------|---|
| HPM[1:0]_OIS    | Selects gyroscope OIS chain digital high-pass filter cutoff. Default value: 00<br>(00: 16 mHz;<br>01: 65 mHz;<br>10: 260 mHz;<br>11: 1.04 Hz) |
| FTYPE_[1:0]_OIS | Selects gyroscope digital LPF1 filter bandwidth. Table 160 shows cutoff and phase values obtained with all configurations.                    |
| HP_EN_OIS       | Enables gyroscope OIS chain digital high-pass filter.   |

**Table 160. Gyroscope OIS chain digital LPF1 filter bandwidth selection**

| ODR [Hz] | LPF1<br>FTYPE_[1:0]_OIS | Total BW [Hz]<br>(phase delay @20 Hz) |
|----------|-------------------------|---------------------------------------|
| 6.66 kHz | 00                      | 297 Hz (7°)                           |
|          | 01                      | 222 Hz (9°)                           |
|          | 10                      | 154 Hz (12°)                          |
|          | 11                      | 470 Hz (5°)                           |

## 9.62 CTRL3\_OIS (72h)

OIS configuration register. Primary interface for read-only (r); only Aux SPI can write to this register (r/w).

**Table 161. CTRL3\_OIS register**

|            |            |                      |                      |                      |         |         |                 |
|------------|------------|----------------------|----------------------|----------------------|---------|---------|-----------------|
| FS1_XL_OIS | FS0_XL_OIS | FILTER_XL_CONF_OIS_2 | FILTER_XL_CONF_OIS_1 | FILTER_XL_CONF_OIS_0 | ST1_OIS | ST0_OIS | ST_OIS_CLAMPDIS |
|------------|------------|----------------------|----------------------|----------------------|---------|---------|-----------------|

**Table 162. CTRL3\_OIS register description**

|                         |  |
|-------------------------|--|
| FS[1:0]_XL_OIS          | Selects accelerometer OIS channel full-scale. Default value: 00.<br>(00: $\pm 2$ g; 01: $\pm 16$ g; 10: $\pm 4$ g; 11: $\pm 8$ g)  |
| FILTER_XL_CONF_OIS[2:0] | Selects accelerometer OIS channel bandwidth. See <a href="#">Table 163</a> .   |
| ST[1:0]_OIS             | Selects gyroscope OIS chain self-test. Default value: 00<br><a href="#">Table 164</a> lists the output variation when the self-test is enabled and ST_OIS_CLAMPDIS='1'.<br>(00: Normal mode;<br>01: Positive sign self-test;<br>10: Normal mode;<br>11: Negative sign self-test) |
| ST_OIS_CLAMPDIS         | Disables OIS chain clamp<br>(0: All OIS chain outputs = 8000h during self-test;<br>1: OIS chain self-test outputs as shown in <a href="#">Table 164</a> .)   |

**Table 163. Accelerometer OIS channel bandwidth and phase**

| FILTER_XL_CONF_OIS[2:0] | Typ. overall bandwidth [Hz] | Typ. overall phase [°] |
|-------------------------|-----------------------------|------------------------|
| 000                     | 631                         | -4.20 @ 20 Hz          |
| 001                     | 295                         | -6.35 @ 20 Hz          |
| 010                     | 140                         | -10.6 @ 20 Hz          |
| 011                     | 68.2                        | -18.9 @ 20 Hz          |
| 100                     | 33.6                        | -17.8 @ 10 Hz          |
| 101                     | 16.7                        | -32.2 @ 10 Hz          |
| 110                     | 8.3                         | -26.2 @ 4 Hz           |
| 111                     | 4.14                        | -26.0 @ 2 Hz           |

**Table 164. Self-test nominal output variation**

| Full scale | Output variation [dps] |
|------------|------------------------|
| $\pm 2000$ | $\pm 400$              |
| $\pm 1000$ | $\pm 200$              |
| $\pm 500$  | $\pm 100$              |
| $\pm 250$  | $\pm 50$               |
| $\pm 125$  | $\pm 25$               |

### 9.63 X\_OFS\_USR (73h)

Accelerometer X-axis user offset correction (r/w). The offset value set in the X\_OFS\_USR offset register is internally subtracted from the acceleration value measured on the X-axis.

**Table 165. X\_OFS\_USR register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| X_OFS_USR_7 | X_OFS_USR_6 | X_OFS_USR_5 | X_OFS_USR_4 | X_OFS_USR_3 | X_OFS_USR_2 | X_OFS_USR_1 | X_OFS_USR_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 166. X\_OFS\_USR register description**

|                 |   |
|-----------------|---|
| X_OFS_USR_[7:0] | Accelerometer X-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127 127]. |
|-----------------|---|

### 9.64 Y\_OFS\_USR (74h)

Accelerometer Y-axis user offset correction (r/w). The offset value set in the Y\_OFS\_USR offset register is internally subtracted from the acceleration value measured on the Y-axis.

**Table 167. Y\_OFS\_USR register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Y_OFS_USR_7 | Y_OFS_USR_6 | Y_OFS_USR_5 | Y_OFS_USR_4 | Y_OFS_USR_3 | Y_OFS_USR_2 | Y_OFS_USR_1 | Y_OFS_USR_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

|                 |  |
|-----------------|--|
| Y_OFS_USR_[7:0] | Accelerometer Y-axis user offset calibration expressed in 2's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127, +127]. |
|-----------------|--|

### 9.65 Z\_OFS\_USR (75h)

Accelerometer Z-axis user offset correction (r/w). The offset value set in the Z\_OFS\_USR offset register is internally subtracted from the acceleration value measured on the Z-axis.

**Table 168. Z\_OFS\_USR register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Z_OFS_USR_7 | Z_OFS_USR_6 | Z_OFS_USR_5 | Z_OFS_USR_4 | Z_OFS_USR_3 | Z_OFS_USR_2 | Z_OFS_USR_1 | Z_OFS_USR_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 169. Z\_OFS\_USR register description**

|                 |  |
|-----------------|--|
| Z_OFS_USR_[7:0] | Accelerometer Z-axis user offset calibration expressed in 2's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127, +127]. |
|-----------------|--|



## 9.66 FIFO\_DATA\_OUT\_TAG (78h)

FIFO tag register (r)

**Table 170. FIFO\_DATA\_OUT\_TAG register**

|              |              |              |              |              |           |           |            |
|--------------|--------------|--------------|--------------|--------------|-----------|-----------|------------|
| TAG_SENSOR_4 | TAG_SENSOR_3 | TAG_SENSOR_2 | TAG_SENSOR_1 | TAG_SENSOR_0 | TAG_CNT_1 | TAG_CNT_0 | TAG_PARITY |
|--------------|--------------|--------------|--------------|--------------|-----------|-----------|------------|

**Table 171. FIFO\_DATA\_OUT\_TAG register description**

|                  |   |
|------------------|---|
| TAG_SENSOR_[4:0] | Identifies the sensor in:<br>FIFO_DATA_OUT_X_L (79h) and FIFO_DATA_OUT_X_H (7Ah), FIFO_DATA_OUT_Y_L (7Bh) and FIFO_DATA_OUT_Y_H (7Ch), and FIFO_DATA_OUT_Z_L (7Dh) and FIFO_DATA_OUT_Z_H (7Eh)<br>For details, refer to Table 172. FIFO tag |
| TAG_CNT_[1:0]    | 2-bit counter which identifies sensor time slot   |
| TAG_PARITY       | Parity check of TAG content   |

**Table 172. FIFO tag**

| TAG_SENSOR_[4:0] | Sensor name          |
|------------------|----------------------|
| 0x01             | Gyroscope NC         |
| 0x02             | Accelerometer NC     |
| 0x03             | Temperature          |
| 0x04             | Timestamp            |
| 0x05             | CFG_Change           |
| 0x06             | Accelerometer NC_T_2 |
| 0x07             | Accelerometer NC_T_1 |
| 0x08             | Accelerometer 2xC    |
| 0x09             | Accelerometer 3xC    |
| 0x0A             | Gyroscope NC_T_2     |
| 0x0B             | Gyroscope NC_T_1     |
| 0x0C             | Gyroscope 2xC        |
| 0x0D             | Gyroscope 3xC        |
| 0x0E             | Sensor Hub Slave 0   |
| 0x0F             | Sensor Hub Slave 1   |
| 0x10             | Sensor Hub Slave 2   |
| 0x11             | Sensor Hub Slave 3   |
| 0x12             | Step Counter         |
| 0x19             | Sensor Hub Nack      |

### 9.67 FIFO\_DATA\_OUT\_X\_L (79h) and FIFO\_DATA\_OUT\_X\_H (7Ah)

FIFO data output X (r)

**Table 173.** FIFO\_DATA\_OUT\_X\_H and FIFO\_DATA\_OUT\_X\_L registers

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| D7  | D6  | D5  | D4  | D3  | D2  | D1 | D0 |

**Table 174.** FIFO\_DATA\_OUT\_X\_H and FIFO\_DATA\_OUT\_X\_L register description

|         |                    |
|---------|--------------------|
| D[15:0] | FIFO X-axis output |
|---------|--------------------|

### 9.68 FIFO\_DATA\_OUT\_Y\_L (7Bh) and FIFO\_DATA\_OUT\_Y\_H (7Ch)

FIFO data output Y (r)

**Table 175.** FIFO\_DATA\_OUT\_Y\_H and FIFO\_DATA\_OUT\_Y\_L registers

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| D7  | D6  | D5  | D4  | D3  | D2  | D1 | D0 |

**Table 176.** FIFO\_DATA\_OUT\_Y\_H and FIFO\_DATA\_OUT\_Y\_L register description

|         |                    |
|---------|--------------------|
| D[15:0] | FIFO Y-axis output |
|---------|--------------------|

### 9.69 FIFO\_DATA\_OUT\_Z\_L (7Dh) and FIFO\_DATA\_OUT\_Z\_H (7Eh)

FIFO data output Z (r)

**Table 177.** FIFO\_DATA\_OUT\_Z\_H and FIFO\_DATA\_OUT\_Z\_L registers

|     |     |     |     |     |     |    |    |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| D7  | D6  | D5  | D4  | D3  | D2  | D1 | D0 |

**Table 178.** FIFO\_DATA\_OUT\_Z\_H and FIFO\_DATA\_OUT\_Z\_L register description

|         |                    |
|---------|--------------------|
| D[15:0] | FIFO Z-axis output |
|---------|--------------------|

## 10 Embedded functions register mapping

The table given below provides a list of the registers for the embedded functions available in the device and the corresponding addresses. Embedded functions registers are accessible when FUNC\_CFG\_EN is set to '1' in FUNC\_CFG\_ACCESS (01h).

**Table 179. Register address map - embedded functions**

| Name                   | Type | Register address |          | Default  | Comment |
|------------------------|------|------------------|----------|----------|---------|
|                        |      | Hex              | Binary   |          |         |
| PAGE_SEL               | RW   | 02               | 00000010 | 00000001 |         |
| RESERVED               | -    | 03               | 00000011 |          |         |
| EMB_FUNC_EN_A          | RW   | 04               | 00000100 | 00000000 |         |
| EMB_FUNC_EN_B          | RW   | 05               | 00000101 | 00000000 |         |
| PAGE_ADDRESS           | RW   | 08               | 00001000 | 00000000 |         |
| PAGE_VALUE             | RW   | 09               | 00001001 | 00000000 |         |
| EMB_FUNC_INT1          | RW   | 0A               | 00001010 | 00000000 |         |
| FSM_INT1_A             | RW   | 0B               | 00001011 | 00000000 |         |
| FSM_INT1_B             | RW   | 0C               | 00001100 | 00000000 |         |
| MLC_INT1               | RW   | 0D               | 00001101 | 00000000 |         |
| EMB_FUNC_INT2          | RW   | 0E               | 00001110 | 00000000 |         |
| FSM_INT2_A             | RW   | 0F               | 00001111 | 01101011 |         |
| FSM_INT2_B             | RW   | 10               | 00010000 | 00000000 |         |
| MLC_INT2               | RW   | 11               | 00010001 | 00000000 |         |
| EMB_FUNC_STATUS        | R    | 12               | 00010010 | output   |         |
| FSM_STATUS_A           | R    | 13               | 00010011 | output   |         |
| FSM_STATUS_B           | R    | 14               | 00010100 | output   |         |
| MLC_STATUS             | R    | 15               | 00010101 | output   |         |
| PAGE_RW                | RW   | 17               | 00010111 | 00000000 |         |
| RESERVED               | -    | 18-43            |          |          |         |
| EMB_FUNC_FIFO_CFG      | RW   | 44               | 01000100 | 00000000 |         |
| FSM_ENABLE_A           | RW   | 46               | 01000110 | 00000000 |         |
| FSM_ENABLE_B           | RW   | 47               | 01000111 | 00000000 |         |
| FSM_LONG_COUNTER_L     | RW   | 48               | 01001000 | 00000000 |         |
| FSM_LONG_COUNTER_H     | RW   | 49               | 01001001 | 00000000 |         |
| FSM_LONG_COUNTER_CLEAR | RW   | 4A               | 01001010 | 00000000 |         |
| FSM_OUTS1              | R    | 4C               | 01001100 | output   |         |
| FSM_OUTS2              | R    | 4D               | 01001101 | output   |         |
| FSM_OUTS3              | R    | 4E               | 01001110 | output   |         |
| FSM_OUTS4              | R    | 4F               | 01001111 | output   |         |
| FSM_OUTS5              | R    | 50               | 01010000 | output   |         |
| FSM_OUTS6              | R    | 51               | 01010001 | output   |         |

| Name               | Type | Register address |          | Default  | Comment |
|--------------------|------|------------------|----------|----------|---------|
|                    |      | Hex              | Binary   |          |         |
| FSM_OUTS7          | R    | 52               | 01010010 | output   |         |
| FSM_OUTS8          | R    | 53               | 01010011 | output   |         |
| FSM_OUTS9          | R    | 54               | 01010100 | output   |         |
| FSM_OUTS10         | R    | 55               | 01010101 | output   |         |
| FSM_OUTS11         | R    | 56               | 01010110 | output   |         |
| FSM_OUTS12         | R    | 57               | 01010111 | output   |         |
| FSM_OUTS13         | R    | 58               | 01011000 | output   |         |
| FSM_OUTS14         | R    | 59               | 01011001 | output   |         |
| FSM_OUTS15         | R    | 5A               | 01011010 | output   |         |
| FSM_OUTS16         | R    | 5B               | 01011011 | output   |         |
| RESERVED           | -    | 5C-5E            |          |          |         |
| EMB_FUNC_ODR_CFG_B | RW   | 5F               | 01011111 | 01001011 |         |
| EMB_FUNC_ODR_CFG_C | RW   | 60               | 01100000 | 00010101 |         |
| STEP_COUNTER_L     | R    | 62               | 01100010 | output   |         |
| STEP_COUNTER_H     | R    | 63               | 01100011 | output   |         |
| EMB_FUNC_SRC       | RW   | 64               | 01100100 | output   |         |
| EMB_FUNC_INIT_A    | RW   | 66               | 01100110 | 00000000 |         |
| EMB_FUNC_INIT_B    | RW   | 67               | 01100111 | 00000000 |         |
| MLC0_SRC           | R    | 70               | 01110000 | output   |         |
| MLC1_SRC           | R    | 71               | 01110001 | output   |         |
| MLC2_SRC           | R    | 72               | 01110010 | output   |         |
| MLC3_SRC           | R    | 73               | 01110011 | output   |         |
| MLC4_SRC           | R    | 74               | 01110100 | output   |         |
| MLC5_SRC           | R    | 75               | 01110101 | output   |         |
| MLC6_SRC           | R    | 76               | 01110110 | output   |         |
| MLC7_SRC           | R    | 77               | 01110111 | output   |         |

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

## 11 Embedded functions register description

### 11.1 PAGE\_SEL (02h)

Enable advanced features dedicated page (r/w)

**Table 180. PAGE\_SEL register**

|           |           |           |           |                  |                  |                  |                  |
|-----------|-----------|-----------|-----------|------------------|------------------|------------------|------------------|
| PAGE_SEL3 | PAGE_SEL2 | PAGE_SEL1 | PAGE_SEL0 | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 1 <sup>(2)</sup> |
|-----------|-----------|-----------|-----------|------------------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.
2. This bit must be set to '1' for the correct operation of the device.

**Table 181. PAGE\_SEL register description**

|               |  |
|---------------|--|
| PAGE_SEL[3:0] | Select the advanced features dedicated page<br>Default value: 0000 |
|---------------|--|

### 11.2 EMB\_FUNC\_EN\_A (04h)

Embedded functions enable register (r/w)

**Table 182. EMB\_FUNC\_EN\_A register**

|                  |                  |                |         |         |                  |                  |                  |
|------------------|------------------|----------------|---------|---------|------------------|------------------|------------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | SIGN_MOTION_EN | TILT_EN | PEDO_EN | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|------------------|------------------|----------------|---------|---------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 183. EMB\_FUNC\_EN\_A register description**

|                |  |
|----------------|--|
| SIGN_MOTION_EN | Enable significant motion detection function. Default value: 0<br>(0: significant motion detection function disabled;<br>1: significant motion detection function enabled) |
| TILT_EN        | Enable tilt calculation. Default value: 0<br>(0: tilt algorithm disabled;<br>1: tilt algorithm enabled)  |
| PEDO_EN        | Enable pedometer algorithm. Default value: 0<br>(0: pedometer algorithm disabled;<br>1: pedometer algorithm enabled)   |

### 11.3 EMB\_FUNC\_EN\_B (05h)

Embedded functions enable register (r/w)

**Table 184. EMB\_FUNC\_EN\_B register**

|                  |                  |                  |        |               |                  |                  |        |
|------------------|------------------|------------------|--------|---------------|------------------|------------------|--------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | MLC_EN | FIFO_COMPR_EN | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | FSM_EN |
|------------------|------------------|------------------|--------|---------------|------------------|------------------|--------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 185. EMB\_FUNC\_EN\_B register description**

|                              |  |
|------------------------------|--|
| MLC_EN                       | Enable Machine Learning Core feature. Default value: 0<br>(0: Machine Learning Core feature disabled;<br>1: Machine Learning Core feature enabled) |
| FIFO_COMPR_EN <sup>(1)</sup> | Enable FIFO compression feature. Default value: 0<br>(0: FIFO compression feature disabled;<br>1: FIFO compression feature enabled)                |
| FSM_EN                       | Enable Finite State Machine (FSM) feature. Default value: 0<br>(0: FSM feature disabled; 1: FSM feature enabled)                                   |

1. This bit is effective if the FIFO\_COMPR\_RT\_EN bit of FIFO\_CTRL2 (08h) is set to 1.

### 11.4 PAGE\_ADDRESS (08h)

Page address register (r/w)

**Table 186. PAGE\_ADDRESS register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| PAGE_ADDR7 | PAGE_ADDR6 | PAGE_ADDR5 | PAGE_ADDR4 | PAGE_ADDR3 | PAGE_ADDR2 | PAGE_ADDR1 | PAGE_ADDR0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 187. PAGE\_ADDRESS register description**

|                |   |
|----------------|---|
| PAGE_ADDR[7:0] | After setting the bit PAGE_WRITE / PAGE_READ in register PAGE_RW (17h), this register is used to set the address of the register to be written/read in the advanced features page selected through the bits PAGE_SEL[3:0] in register PAGE_SEL (02h). |
|----------------|---|

### 11.5 PAGE\_VALUE (09h)

Page value register (r/w)

**Table 188. PAGE\_VALUE register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| PAGE_VALUE7 | PAGE_VALUE6 | PAGE_VALUE5 | PAGE_VALUE4 | PAGE_VALUE3 | PAGE_VALUE2 | PAGE_VALUE1 | PAGE_VALUE0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 189. PAGE\_VALUE register description**

|                 |  |
|-----------------|--|
| PAGE_VALUE[7:0] | These bits are used to write (if the bit PAGE_WRITE = 1 in register PAGE_RW (17h)) or read (if the bit PAGE_READ = 1 in register PAGE_RW (17h)) the data at the address PAGE_ADDR[7:0] of the selected advanced features page. |
|-----------------|--|

## 11.6 EMB\_FUNC\_INT1 (0Ah)

INT1 pin control register (r/w)

Each bit in this register enables a signal to be carried over INT1. The pin's output will supply the OR combination of the selected signals.

**Table 190. EMB\_FUNC\_INT1 register**

|             |                  |              |           |                    |                  |                  |                  |
|-------------|------------------|--------------|-----------|--------------------|------------------|------------------|------------------|
| INT1_FSM_LC | 0 <sup>(1)</sup> | INT1_SIG_MOT | INT1_TILT | INT1_STEP_DETECTOR | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|-------------|------------------|--------------|-----------|--------------------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 191. EMB\_FUNC\_INT1 register description**

|                                   |  |
|-----------------------------------|--|
| INT1_FSM_LC <sup>(1)</sup>        | Routing of FSM long counter timeout interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_SIG_MOT <sup>(1)</sup>       | Routing of significant motion event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled)                 |
| INT1_TILT <sup>(1)</sup>          | Routing of tilt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled)                               |
| INT1_STEP_DETECTOR <sup>(1)</sup> | Routing of pedometer step recognition event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled)         |

1. This bit is effective if the INT1\_EMB\_FUNC bit of MD1\_CFG (5Eh) is set to 1.

## 11.7 FSM\_INT1\_A (0Bh)

INT1 pin control register (r/w).

Each bit in this register enables a signal to be carried over INT1. The pin's output will supply the OR combination of the selected signals.

**Table 192. FSM\_INT1\_A register**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| INT1_FSM8 | INT1_FSM7 | INT1_FSM6 | INT1_FSM5 | INT1_FSM4 | INT1_FSM3 | INT1_FSM2 | INT1_FSM1 |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|

**Table 193. FSM\_INT1\_A register description**

|                          |  |
|--------------------------|--|
| INT1_FSM8 <sup>(1)</sup> | Routing of FSM8 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM7 <sup>(1)</sup> | Routing of FSM7 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM6 <sup>(1)</sup> | Routing of FSM6 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM5 <sup>(1)</sup> | Routing of FSM5 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM4 <sup>(1)</sup> | Routing of FSM4 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM3 <sup>(1)</sup> | Routing of FSM3 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM2 <sup>(1)</sup> | Routing of FSM2 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM1 <sup>(1)</sup> | Routing of FSM1 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |

1. This bit is effective if the INT1\_EMB\_FUNC bit of MD1\_CFG (5Eh) is set to 1.



## 11.8 FSM\_INT1\_B (0Ch)

INT1 pin control register (r/w).

Each bit in this register enables a signal to be carried over INT1. The pin's output will supply the OR combination of the selected signals.

**Table 194. FSM\_INT1\_B register**

|            |            |            |            |            |            |            |           |
|------------|------------|------------|------------|------------|------------|------------|-----------|
| INT1_FSM16 | INT1_FSM15 | INT1_FSM14 | INT1_FSM13 | INT1_FSM12 | INT1_FSM11 | INT1_FSM10 | INT1_FSM9 |
|------------|------------|------------|------------|------------|------------|------------|-----------|

**Table 195. FSM\_INT1\_B register description**

|                           |   |
|---------------------------|---|
| INT1_FSM16 <sup>(1)</sup> | Routing of FSM16 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM15 <sup>(1)</sup> | Routing of FSM15 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM14 <sup>(1)</sup> | Routing of FSM14 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM13 <sup>(1)</sup> | Routing of FSM13 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM12 <sup>(1)</sup> | Routing of FSM12 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM11 <sup>(1)</sup> | Routing of FSM11 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM10 <sup>(1)</sup> | Routing of FSM10 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_FSM9 <sup>(1)</sup>  | Routing of FSM9 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled)  |

1. This bit is effective if the INT1\_EMB\_FUNC bit of MD1\_CFG (5Eh) is set to 1.

## 11.9 MLC\_INT1 (0Dh)

INT1 pin control register (r/w).

Each bit in this register enables a signal to be carried over INT1. The pin's output will supply the OR combination of the selected signals.

**Table 196. MLC\_INT1 register**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| INT1_MLC8 | INT1_MLC7 | INT1_MLC6 | INT1_MLC5 | INT1_MLC4 | INT1_MLC3 | INT1_MLC2 | INT1_MLC1 |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|

**Table 197. MLC\_INT1 register description**

|           |  |
|-----------|--|
| INT1_MLC8 | Routing of MLC8 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_MLC7 | Routing of MLC7 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_MLC6 | Routing of MLC6 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_MLC5 | Routing of MLC5 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_MLC4 | Routing of MLC4 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_MLC3 | Routing of MLC3 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_MLC2 | Routing of MLC2 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT1_MLC1 | Routing of MLC1 interrupt event on INT1. Default value: 0<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |

## 11.10 EMB\_FUNC\_INT2 (0Eh)

INT2 pin control register (r/w).

Each bit in this register enables a signal to be carried over INT2. The pin's output will supply the OR combination of the selected signals.

**Table 198. EMB\_FUNC\_INT2 register**

|             |                  |              |           |                    |                  |                  |                  |
|-------------|------------------|--------------|-----------|--------------------|------------------|------------------|------------------|
| INT2_FSM_LC | 0 <sup>(1)</sup> | INT2_SIG_MOT | INT2_TILT | INT2_STEP_DETECTOR | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|-------------|------------------|--------------|-----------|--------------------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 199. EMB\_FUNC\_INT2 register description**

|                                   |  |
|-----------------------------------|--|
| INT2_FSM_LC <sup>(1)</sup>        | Routing of FSM long counter timeout interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled) |
| INT2_SIG_MOT <sup>(1)</sup>       | Routing of significant motion event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)                 |
| INT2_TILT <sup>(1)</sup>          | Routing of tilt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)                               |
| INT2_STEP_DETECTOR <sup>(1)</sup> | Routing of pedometer step recognition event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)         |

1. This bit is effective if the INT2\_EMB\_FUNC bit of MD2\_CFG (5Fh) is set to 1.

## 11.11 FSM\_INT2\_A (0Fh)

INT2 pin control register (r/w).

Each bit in this register enables a signal to be carried over INT2. The pin's output will supply the OR combination of the selected signals.

**Table 200. FSM\_INT2\_A register**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| INT2_FSM8 | INT2_FSM7 | INT2_FSM6 | INT2_FSM5 | INT2_FSM4 | INT2_FSM3 | INT2_FSM2 | INT2_FSM1 |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|

**Table 201. FSM\_INT2\_A register description**

|                          |   |
|--------------------------|---|
| INT2_FSM8 <sup>(1)</sup> | Routing of FSM8 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)  |
| INT2_FSM7 <sup>(1)</sup> | Routing of FSM7 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)  |
| INT2_FSM6 <sup>(1)</sup> | Routing of FSM6 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)  |
| INT2_FSM5 <sup>(1)</sup> | Routing of FSM5 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)  |
| INT2_FSM4 <sup>(1)</sup> | Routing of FSM4 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)  |
| INT2_FSM3 <sup>(1)</sup> | Routing of FSM3 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT2_FSM2 <sup>(1)</sup> | Routing of FSM2 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)  |
| INT2_FSM1 <sup>(1)</sup> | Routing of FSM1 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)  |

1. This bit is effective if the INT2\_EMB\_FUNC bit of MD2\_CFG (5Fh) is set to 1.

## 11.12 FSM\_INT2\_B (10h)

INT2 pin control register (r/w).

Each bit in this register enables a signal to be carried over INT2. The pin's output will supply the OR combination of the selected signals.

**Table 202. FSM\_INT2\_B register**

|            |            |            |            |            |            |            |           |
|------------|------------|------------|------------|------------|------------|------------|-----------|
| INT2_FSM16 | INT2_FSM15 | INT2_FSM14 | INT2_FSM13 | INT2_FSM12 | INT2_FSM11 | INT2_FSM10 | INT2_FSM9 |
|------------|------------|------------|------------|------------|------------|------------|-----------|

**Table 203. FSM\_INT2\_B register description**

|                           |  |
|---------------------------|--|
| INT2_FSM16 <sup>(1)</sup> | Routing of FSM16 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)  |
| INT2_FSM15 <sup>(1)</sup> | Routing of FSM15 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)  |
| INT2_FSM14 <sup>(1)</sup> | Routing of FSM14 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)  |
| INT2_FSM13 <sup>(1)</sup> | Routing of FSM13 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)  |
| INT2_FSM12 <sup>(1)</sup> | Routing of FSM12 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)  |
| INT2_FSM11 <sup>(1)</sup> | Routing of FSM11 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)<br>(0: routing on INT1 disabled; 1: routing on INT1 enabled) |
| INT2_FSM10 <sup>(1)</sup> | Routing of FSM10 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)  |
| INT2_FSM9 <sup>(1)</sup>  | Routing of FSM9 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled)   |

1. This bit is effective if the INT2\_EMB\_FUNC bit of MD2\_CFG (5Fh) is set to 1.

### 11.13 MLC\_INT2 (11h)

INT2 pin control register (r/w).

Each bit in this register enables a signal to be carried over INT2. The pin's output will supply the OR combination of the selected signals.

**Table 204. MLC\_INT2 register**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| INT2_MLC8 | INT2_MLC7 | INT2_MLC6 | INT2_MLC5 | INT2_MLC4 | INT2_MLC3 | INT2_MLC2 | INT2_MLC1 |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|

**Table 205. MLC\_INT2 register description**

|           |  |
|-----------|--|
| INT2_MLC8 | Routing of MLC8 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled) |
| INT2_MLC7 | Routing of MLC7 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled) |
| INT2_MLC6 | Routing of MLC6 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled) |
| INT2_MLC5 | Routing of MLC5 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled) |
| INT2_MLC4 | Routing of MLC4 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled) |
| INT2_MLC3 | Routing of MLC3 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled) |
| INT2_MLC2 | Routing of MLC2 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled) |
| INT2_MLC1 | Routing of MLC1 interrupt event on INT2. Default value: 0<br>(0: routing on INT2 disabled; 1: routing on INT2 enabled) |

## 11.14 EMB\_FUNC\_STATUS (12h)

Embedded function status register (r)

**Table 206. EMB\_FUNC\_STATUS register**

|           |   |           |         |             |   |   |   |
|-----------|---|-----------|---------|-------------|---|---|---|
| IS_FSM_LC | 0 | IS_SIGMOT | IS_TILT | IS_STEP_DET | 0 | 0 | 0 |
|-----------|---|-----------|---------|-------------|---|---|---|

**Table 207. EMB\_FUNC\_STATUS register description**

|             |  |
|-------------|--|
| IS_FSM_LC   | Interrupt status bit for FSM long counter timeout interrupt event.<br>(1: interrupt detected; 0: no interrupt) |
| IS_SIGMOT   | Interrupt status bit for significant motion detection<br>(1: interrupt detected; 0: no interrupt)              |
| IS_TILT     | Interrupt status bit for tilt detection<br>(1: interrupt detected; 0: no interrupt)                            |
| IS_STEP_DET | Interrupt status bit for step detection<br>(1: interrupt detected; 0: no interrupt)                            |

## 11.15 FSM\_STATUS\_A (13h)

Finite State Machine status register (r)

**Table 208. FSM\_STATUS\_A register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| IS_FSM8 | IS_FSM7 | IS_FSM6 | IS_FSM5 | IS_FSM4 | IS_FSM3 | IS_FSM2 | IS_FSM1 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 209. FSM\_STATUS\_A register description**

|         |   |
|---------|---|
| IS_FSM8 | Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM7 | Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM6 | Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM5 | Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM4 | Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM3 | Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM2 | Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM1 | Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt) |

## 11.16 FSM\_STATUS\_B (14h)

Finite State Machine status register (r)

**Table 210. FSM\_STATUS\_B register**

|          |          |          |          |          |          |          |         |
|----------|----------|----------|----------|----------|----------|----------|---------|
| IS_FSM16 | IS_FSM15 | IS_FSM14 | IS_FSM13 | IS_FSM12 | IS_FSM11 | IS_FSM10 | IS_FSM9 |
|----------|----------|----------|----------|----------|----------|----------|---------|

**Table 211. FSM\_STATUS\_B register description**

|          |  |
|----------|--|
| IS_FSM16 | Interrupt status bit for FSM16 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM15 | Interrupt status bit for FSM15 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM14 | Interrupt status bit for FSM14 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM13 | Interrupt status bit for FSM13 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM12 | Interrupt status bit for FSM12 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM11 | Interrupt status bit for FSM11 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM10 | Interrupt status bit for FSM10 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_FSM9  | Interrupt status bit for FSM9 interrupt event. (1: interrupt detected; 0: no interrupt)  |

## 11.17 MLC\_STATUS (15h)

Machine Learning Core status register (r)

**Table 212. MLC\_STATUS register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| IS_MLC8 | IS_MLC7 | IS_MLC6 | IS_MLC5 | IS_MLC4 | IS_MLC3 | IS_MLC2 | IS_MLC1 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 213. MLC\_STATUS register description**

|         |   |
|---------|---|
| IS_MLC8 | Interrupt status bit for MLC8 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC7 | Interrupt status bit for MLC7 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC6 | Interrupt status bit for MLC6 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC5 | Interrupt status bit for MLC5 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC4 | Interrupt status bit for MLC4 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC3 | Interrupt status bit for MLC3 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC2 | Interrupt status bit for MLC2 interrupt event. (1: interrupt detected; 0: no interrupt) |
| IS_MLC1 | Interrupt status bit for MLC1 interrupt event. (1: interrupt detected; 0: no interrupt) |



## 11.18 PAGE\_RW (17h)

Enable read and write mode of advanced features dedicated page (r/w)

**Table 214. PAGE\_RW register**

|              |            |           |                  |                  |                  |                  |                  |
|--------------|------------|-----------|------------------|------------------|------------------|------------------|------------------|
| EMB_FUNC_LIR | PAGE_WRITE | PAGE_READ | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|--------------|------------|-----------|------------------|------------------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 215. PAGE\_RW register description**

|              |  |
|--------------|--|
| EMB_FUNC_LIR | Latched Interrupt mode for Embedded Functions. Default value: 0<br>(0: Embedded Functions interrupt request not latched;<br>1: Embedded Functions interrupt request latched) |
| PAGE_WRITE   | Enable writes to the selected advanced features dedicated page. <sup>(1)</sup><br>Default value: 0<br>(1: enable; 0: disable)  |
| PAGE_READ    | Enable reads from the selected advanced features dedicated page. <sup>(1)</sup><br>Default value: 0<br>(1: enable; 0: disable)   |

1. Page selected by PAGE\_SEL[3:0] in register PAGE\_SEL (02h).

## 11.19 EMB\_FUNC\_FIFO\_CFG (44h)

Embedded functions batching configuration register (r/w)

**Table 216. EMB\_FUNC\_FIFO\_CFG register**

|                  |              |                  |                  |                  |                  |                  |                  |
|------------------|--------------|------------------|------------------|------------------|------------------|------------------|------------------|
| 0 <sup>(1)</sup> | PEDO_FIFO_EN | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|------------------|--------------|------------------|------------------|------------------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 217. EMB\_FUNC\_FIFO\_CFG register description**

|              |   |
|--------------|---|
| PEDO_FIFO_EN | Enable FIFO batching of step counter values. Default value: 0 |
|--------------|---|

## 11.20 FSM\_ENABLE\_A (46h)

FSM enable register (r/w)

**Table 218. FSM\_ENABLE\_A register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| FSM8_EN | FSM7_EN | FSM6_EN | FSM5_EN | FSM4_EN | FSM3_EN | FSM2_EN | FSM1_EN |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 219. FSM\_ENABLE\_A register description**

|         |   |
|---------|---|
| FSM8_EN | FSM8 enable. Default value: 0 (0: FSM8 disabled; 1: FSM8 enabled) |
| FSM7_EN | FSM7 enable. Default value: 0 (0: FSM7 disabled; 1: FSM7 enabled) |
| FSM6_EN | FSM6 enable. Default value: 0 (0: FSM6 disabled; 1: FSM6 enabled) |
| FSM5_EN | FSM5 enable. Default value: 0 (0: FSM5 disabled; 1: FSM5 enabled) |
| FSM4_EN | FSM4 enable. Default value: 0 (0: FSM4 disabled; 1: FSM4 enabled) |
| FSM3_EN | FSM3 enable. Default value: 0 (0: FSM3 disabled; 1: FSM3 enabled) |
| FSM2_EN | FSM2 enable. Default value: 0 (0: FSM2 disabled; 1: FSM2 enabled) |
| FSM1_EN | FSM1 enable. Default value: 0 (0: FSM1 disabled; 1: FSM1 enabled) |

## 11.21 FSM\_ENABLE\_B (47h)

FSM enable register (r/w)

**Table 220. FSM\_ENABLE\_B register**

|          |          |          |          |          |          |          |         |
|----------|----------|----------|----------|----------|----------|----------|---------|
| FSM16_EN | FSM15_EN | FSM14_EN | FSM13_EN | FSM12_EN | FSM11_EN | FSM10_EN | FSM9_EN |
|----------|----------|----------|----------|----------|----------|----------|---------|

**Table 221. FSM\_ENABLE\_B register description**

|          |  |
|----------|--|
| FSM16_EN | FSM16 enable. Default value: 0 (0: FSM16 disabled; 1: FSM16 enabled) |
| FSM15_EN | FSM15 enable. Default value: 0 (0: FSM15 disabled; 1: FSM15 enabled) |
| FSM14_EN | FSM14 enable. Default value: 0 (0: FSM14 disabled; 1: FSM14 enabled) |
| FSM13_EN | FSM13 enable. Default value: 0 (0: FSM13 disabled; 1: FSM13 enabled) |
| FSM12_EN | FSM12 enable. Default value: 0 (0: FSM12 disabled; 1: FSM12 enabled) |
| FSM11_EN | FSM11 enable. Default value: 0 (0: FSM11 disabled; 1: FSM11 enabled) |
| FSM10_EN | FSM10 enable. Default value: 0 (0: FSM10 disabled; 1: FSM10 enabled) |
| FSM9_EN  | FSM9 enable. Default value: 0 (0: FSM9 disabled; 1: FSM9 enabled)    |

## 11.22 FSM\_LONG\_COUNTER\_L (48h) and FSM\_LONG\_COUNTER\_H (49h)

FSM long counter status register (r/w).

Long counter value is an unsigned integer value (16-bit format); this value can be reset using the LC\_CLEAR bit in FSM\_LONG\_COUNTER\_CLEAR (4Ah) register.

**Table 222. FSM\_LONG\_COUNTER\_L register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| FSM_LC_7 | FSM_LC_6 | FSM_LC_5 | FSM_LC_4 | FSM_LC_3 | FSM_LC_2 | FSM_LC_1 | FSM_LC_0 |
|----------|----------|----------|----------|----------|----------|----------|----------|

**Table 223. FSM\_LONG\_COUNTER\_L register description**

|              |  |
|--------------|--|
| FSM_LC_[7:0] | Long counter current value (LSbyte). Default value: 00000000 |
|--------------|--|

**Table 224. FSM\_LONG\_COUNTER\_H register**

|           |           |           |           |           |           |          |          |
|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|
| FSM_LC_15 | FSM_LC_14 | FSM_LC_13 | FSM_LC_12 | FSM_LC_11 | FSM_LC_10 | FSM_LC_9 | FSM_LC_8 |
|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|

**Table 225. FSM\_LONG\_COUNTER\_H register description**

|               |  |
|---------------|--|
| FSM_LC_[15:8] | Long counter current value (MSbyte). Default value: 00000000 |
|---------------|--|

## 11.23 FSM\_LONG\_COUNTER\_CLEAR (4Ah)

FSM long counter reset register (r/w)

**Table 226. FSM\_LONG\_COUNTER\_CLEAR register**

|                  |                  |                  |                  |                  |                  |                |              |
|------------------|------------------|------------------|------------------|------------------|------------------|----------------|--------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | FSM_LC_CLEARED | FSM_LC_CLEAR |
|------------------|------------------|------------------|------------------|------------------|------------------|----------------|--------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 227. FSM\_LONG\_COUNTER\_CLEAR register description**

|                |  |
|----------------|--|
| FSM_LC_CLEARED | This read-only bit is automatically set to 1 when the long counter reset is done. Default value: 0 |
| FSM_LC_CLEAR   | Clear FSM long counter value. Default value: 0   |

## 11.24 FSM\_OUTS1 (4Ch)

FSM1 output register (r)

**Table 228. FSM\_OUTS1 register**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 229. FSM\_OUTS1 register description**

|     |  |
|-----|--|
| P_X | FSM1 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM1 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM1 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM1 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM1 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM1 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM1 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM1 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 11.25 FSM\_OUTS2 (4Dh)

FSM2 output register (r)

**Table 230. FSM\_OUTS2 register**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 231. FSM\_OUTS2 register description**

|     |  |
|-----|--|
| P_X | FSM2 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM2 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM2 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM2 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM2 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM2 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM2 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM2 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 11.26 FSM\_OUTS3 (4Eh)

FSM3 output register (r)

**Table 232. FSM\_OUTS3 register**

| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 233. FSM\_OUTS3 register description**

|     |  |
|-----|--|
| P_X | FSM3 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM3 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM3 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM3 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM3 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM3 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM3 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM3 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 11.27 FSM\_OUTS4 (4Fh)

FSM4 output register (r)

**Table 234. FSM\_OUTS4 register**

| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 235. FSM\_OUTS4 register description**

|     |  |
|-----|--|
| P_X | FSM4 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM4 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM4 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM4 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM4 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM4 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM4 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM4 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 11.28 FSM\_OUTS5 (50h)

FSM5 output register (r)

**Table 236. FSM\_OUTS5 register**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 237. FSM\_OUTS5 register description**

|     |  |
|-----|--|
| P_X | FSM5 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM5 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM5 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM5 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM5 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM5 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM5 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM5 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 11.29 FSM\_OUTS6 (51h)

FSM6 output register (r)

**Table 238. FSM\_OUTS6 register**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 239. FSM\_OUTS6 register description**

|     |  |
|-----|--|
| P_X | FSM6 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM6 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM6 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM6 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM6 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM6 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM6 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM6 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

### 11.30 FSM\_OUTS7 (52h)

FSM7 output register (r)

**Table 240. FSM\_OUTS7 register**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 241. FSM\_OUTS7 register description**

|     |  |
|-----|--|
| P_X | FSM7 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM7 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM7 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM7 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM7 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM7 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM7 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM7 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

### 11.31 FSM\_OUTS8 (53h)

FSM8 output register (r)

**Table 242. FSM\_OUTS8 register**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 243. FSM\_OUTS8 register description**

|     |  |
|-----|--|
| P_X | FSM8 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM8 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM8 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM8 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM8 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM8 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM8 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM8 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

### 11.32 FSM\_OUTS9 (54h)

FSM9 output register (r)

**Table 244. FSM\_OUTS9 register**

| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 245. FSM\_OUTS9 register description**

|     |  |
|-----|--|
| P_X | FSM9 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM9 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM9 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM9 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM9 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM9 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM9 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM9 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

### 11.33 FSM\_OUTS10 (55h)

FSM10 output register (r)

**Table 246. FSM\_OUTS10 register**

| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 247. FSM\_OUTS10 register description**

|     |   |
|-----|---|
| P_X | FSM10 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM10 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM10 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM10 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM10 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM10 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM10 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM10 output: negative event detected on the vector. (0: event not detected; 1: event detected) |



### 11.34 FSM\_OUTS11 (56h)

FSM11 output register (r)

**Table 248. FSM\_OUTS11 register**

| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 249. FSM\_OUTS11 register description**

|     |   |
|-----|---|
| P_X | FSM11 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM11 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM11 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM11 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM11 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM11 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM11 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM11 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

### 11.35 FSM\_OUTS12 (57h)

FSM12 output register (r)

**Table 250. FSM\_OUTS12 register**

| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 251. FSM\_OUTS12 register description**

|     |   |
|-----|---|
| P_X | FSM12 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM12 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM12 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM12 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM12 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM12 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM12 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM12 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 11.36 FSM\_OUTS13 (58h)

FSM13 output register (r)

**Table 252. FSM\_OUTS13 register**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 253. FSM\_OUTS13 register description**

|     |   |
|-----|---|
| P_X | FSM13 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM13 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM13 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM13 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM13 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM13 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM13 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM13 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 11.37 FSM\_OUTS14 (59h)

FSM14 output register (r)

**Table 254. FSM\_OUTS14 register**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 255. FSM\_OUTS14 register description**

|     |   |
|-----|---|
| P_X | FSM14 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM14 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM14 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM14 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM14 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM14 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM14 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM14 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

### 11.38 FSM\_OUTS15 (5Ah)

FSM15 output register (r)

**Table 256. FSM\_OUTS15 register**

| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 257. FSM\_OUTS15 register description**

|     |   |
|-----|---|
| P_X | FSM15 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM15 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM15 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM15 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM15 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM15 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM15 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM15 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

### 11.39 FSM\_OUTS16 (5Bh)

FSM16 output register (r)

**Table 258. FSM\_OUTS16 register**

| P_X | N_X | P_Y | N_Y | P_Z | N_Z | P_V | N_V |
|-----|-----|-----|-----|-----|-----|-----|-----|
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 259. FSM\_OUTS16 register description**

|     |   |
|-----|---|
| P_X | FSM16 output: positive event detected on the X-axis. (0: event not detected; 1: event detected) |
| N_X | FSM16 output: negative event detected on the X-axis. (0: event not detected; 1: event detected) |
| P_Y | FSM16 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected) |
| N_Y | FSM16 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected) |
| P_Z | FSM16 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected) |
| N_Z | FSM16 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected) |
| P_V | FSM16 output: positive event detected on the vector. (0: event not detected; 1: event detected) |
| N_V | FSM16 output: negative event detected on the vector. (0: event not detected; 1: event detected) |

## 11.40 EMB\_FUNC\_ODR\_CFG\_B (5Fh)

Finite State Machine output data rate configuration register (r/w)

**Table 260. EMB\_FUNC\_ODR\_CFG\_B register**

|                  |                  |                  |          |          |                  |                  |                  |
|------------------|------------------|------------------|----------|----------|------------------|------------------|------------------|
| 0 <sup>(1)</sup> | 1 <sup>(2)</sup> | 0 <sup>(1)</sup> | FSM_ODR1 | FSM_ODR0 | 0 <sup>(1)</sup> | 1 <sup>(2)</sup> | 1 <sup>(2)</sup> |
|------------------|------------------|------------------|----------|----------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.
2. This bit must be set to '1' for the correct operation of the device

**Table 261. EMB\_FUNC\_ODR\_CFG\_B register description**

|              |   |
|--------------|---|
| FSM_ODR[1:0] | Finite State Machine ODR configuration:<br>(00: 12.5 Hz;<br>01: 26 Hz (default);<br>10: 52 Hz;<br>11: 104 Hz) |
|--------------|---|

## 11.41 EMB\_FUNC\_ODR\_CFG\_C (60h)

Machine Learning Core output data rate configuration register (r/w)

**Table 262. EMB\_FUNC\_ODR\_CFG\_C register**

|                  |                  |          |          |                  |                  |                  |                  |
|------------------|------------------|----------|----------|------------------|------------------|------------------|------------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | MLC_ODR1 | MLC_ODR0 | 0 <sup>(1)</sup> | 1 <sup>(2)</sup> | 0 <sup>(1)</sup> | 1 <sup>(2)</sup> |
|------------------|------------------|----------|----------|------------------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.
2. This bit must be set to '1' for the correct operation of the device.

**Table 263. EMB\_FUNC\_ODR\_CFG\_C register description**

|              |  |
|--------------|--|
| MLC_ODR[1:0] | Machine Learning Core ODR configuration:<br>(00: 12.5 Hz;<br>01: 26 Hz (default);<br>10: 52 Hz;<br>11: 104 Hz) |
|--------------|--|

## 11.42 STEP\_COUNTER\_L (62h) and STEP\_COUNTER\_H (63h)

Step counter output register (r)

**Table 264. STEP\_COUNTER\_L register**

|        |        |        |        |        |        |        |        |
|--------|--------|--------|--------|--------|--------|--------|--------|
| STEP_7 | STEP_6 | STEP_5 | STEP_4 | STEP_3 | STEP_2 | STEP_1 | STEP_0 |
|--------|--------|--------|--------|--------|--------|--------|--------|

**Table 265. STEP\_COUNTER\_L register description**

|            |                              |
|------------|------------------------------|
| STEP_[7:0] | Step counter output (LSbyte) |
|------------|------------------------------|

**Table 266. STEP\_COUNTER\_H register**

|         |         |         |         |         |         |        |        |
|---------|---------|---------|---------|---------|---------|--------|--------|
| STEP_15 | STEP_14 | STEP_13 | STEP_12 | STEP_11 | STEP_10 | STEP_9 | STEP_8 |
|---------|---------|---------|---------|---------|---------|--------|--------|

**Table 267. STEP\_COUNTER\_H register description**

|             |                              |
|-------------|------------------------------|
| STEP_[15:8] | Step counter output (MSbyte) |
|-------------|------------------------------|

## 11.43 EMB\_FUNC\_SRC (64h)

Embedded function source register (r/w)

**Table 268. EMB\_FUNC\_SRC register**

|               |                  |               |                     |               |                      |                  |                  |
|---------------|------------------|---------------|---------------------|---------------|----------------------|------------------|------------------|
| PEDO_RST_STEP | 0 <sup>(1)</sup> | STEP_DETECTED | STEP_COUNT_DELTA_IA | STEP_OVERFLOW | STEP_COUNTER_BIT_SET | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|---------------|------------------|---------------|---------------------|---------------|----------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 269. EMB\_FUNC\_SRC register description**

|                      |  |
|----------------------|--|
| PEDO_RST_STEP        | Reset pedometer step counter. Read/write bit.<br>(0: disabled; 1: enabled)   |
| STEP_DETECTED        | Step detector event detection status. Read-only bit.<br>(0: step detection event not detected; 1: step detection event detected)                                   |
| STEP_COUNT_DELTA_IA  | Pedometer step recognition on delta time status. Read-only bit.<br>(0: no step recognized during delta time;<br>1: at least one step recognized during delta time) |
| STEP_OVERFLOW        | Step counter overflow status. Read-only bit.<br>(0: step counter value < 2 <sup>16</sup> ; 1: step counter value reached 2 <sup>16</sup> )                         |
| STEP_COUNTER_BIT_SET | This bit is equal to 1 when the step count is increased. Read-only bit.  |

## 11.44 EMB\_FUNC\_INIT\_A (66h)

Embedded functions initialization register (r/w)

**Table 270. EMB\_FUNC\_INIT\_A register**

|                  |                  |              |           |               |                  |                  |                  |
|------------------|------------------|--------------|-----------|---------------|------------------|------------------|------------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | SIG_MOT_INIT | TILT_INIT | STEP_DET_INIT | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|------------------|------------------|--------------|-----------|---------------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 271. EMB\_FUNC\_INIT\_A register description**

|               |  |
|---------------|--|
| SIG_MOT_INIT  | Significant Motion Detection algorithm initialization request. Default value: 0    |
| TILT_INIT     | Tilt algorithm initialization request. Default value: 0                            |
| STEP_DET_INIT | Pedometer Step Counter/Detector algorithm initialization request. Default value: 0 |

## 11.45 EMB\_FUNC\_INIT\_B (67h)

Embedded functions initialization register (r/w)

**Table 272. EMB\_FUNC\_INIT\_B register**

|                  |                  |                  |          |                 |                  |                  |          |
|------------------|------------------|------------------|----------|-----------------|------------------|------------------|----------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | MLC_INIT | FIFO_COMPR_INIT | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | FSM_INIT |
|------------------|------------------|------------------|----------|-----------------|------------------|------------------|----------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 273. EMB\_FUNC\_INIT\_B register description**

|                 |   |
|-----------------|---|
| MLC_INIT        | Machine Learning Core initialization request. Default value: 0    |
| FIFO_COMPR_INIT | FIFO compression feature initialization request. Default value: 0 |
| FSM_INIT        | FSM initialization request. Default value: 0                      |

## 11.46 MLC0\_SRC (70h)

Machine Learning Core source register (r)

**Table 274. MLC0\_SRC register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| MLC0_SRC_7 | MLC0_SRC_6 | MLC0_SRC_5 | MLC0_SRC_4 | MLC0_SRC_3 | MLC0_SRC_2 | MLC0_SRC_1 | MLC0_SRC_0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 275. MLC0\_SRC register description**

|                |                                    |
|----------------|------------------------------------|
| MLC0_SRC_[7:0] | Output value of MLC0 decision tree |
|----------------|------------------------------------|

## 11.47 MLC1\_SRC (71h)

Machine Learning Core source register (r)

**Table 276. MLC1\_SRC register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| MLC1_SRC_7 | MLC1_SRC_6 | MLC1_SRC_5 | MLC1_SRC_4 | MLC1_SRC_3 | MLC1_SRC_2 | MLC1_SRC_1 | MLC1_SRC_0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 277. MLC1\_SRC register description**

|                |                                    |
|----------------|------------------------------------|
| MLC1_SRC_[7:0] | Output value of MLC1 decision tree |
|----------------|------------------------------------|

## 11.48 MLC2\_SRC (72h)

Machine Learning Core source register (r)

**Table 278. MLC2\_SRC register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| MLC2_SRC_7 | MLC2_SRC_6 | MLC2_SRC_5 | MLC2_SRC_4 | MLC2_SRC_3 | MLC2_SRC_2 | MLC2_SRC_1 | MLC2_SRC_0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 279. MLC2\_SRC register description**

|                |                                    |
|----------------|------------------------------------|
| MLC2_SRC_[7:0] | Output value of MLC2 decision tree |
|----------------|------------------------------------|

## 11.49 MLC3\_SRC (73h)

Machine Learning Core source register (r)

**Table 280. MLC3\_SRC register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| MLC3_SRC_7 | MLC3_SRC_6 | MLC3_SRC_5 | MLC3_SRC_4 | MLC3_SRC_3 | MLC3_SRC_2 | MLC3_SRC_1 | MLC3_SRC_0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 281. MLC3\_SRC register description**

|                |                                    |
|----------------|------------------------------------|
| MLC3_SRC_[7:0] | Output value of MLC3 decision tree |
|----------------|------------------------------------|

## 11.50 MLC4\_SRC (74h)

Machine Learning Core source register (r)

**Table 282. MLC4\_SRC register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| MLC4_SRC_7 | MLC4_SRC_6 | MLC4_SRC_5 | MLC4_SRC_4 | MLC4_SRC_3 | MLC4_SRC_2 | MLC4_SRC_1 | MLC4_SRC_0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 283. MLC4\_SRC register description**

|                |                                    |
|----------------|------------------------------------|
| MLC4_SRC_[7:0] | Output value of MLC4 decision tree |
|----------------|------------------------------------|

## 11.51 MLC5\_SRC (75h)

Machine Learning Core source register (r)

**Table 284. MLC5\_SRC register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| MLC5_SRC_7 | MLC5_SRC_6 | MLC5_SRC_5 | MLC5_SRC_4 | MLC5_SRC_3 | MLC5_SRC_2 | MLC5_SRC_1 | MLC5_SRC_0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 285. MLC5\_SRC register description**

|                |                                    |
|----------------|------------------------------------|
| MLC5_SRC_[7:0] | Output value of MLC5 decision tree |
|----------------|------------------------------------|



## 11.52 MLC6\_SRC (76h)

Machine Learning Core source register (r)

**Table 286. MLC6\_SRC register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| MLC6_SRC_7 | MLC6_SRC_6 | MLC6_SRC_5 | MLC6_SRC_4 | MLC6_SRC_3 | MLC6_SRC_2 | MLC6_SRC_1 | MLC6_SRC_0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 287. MLC6\_SRC register description**

|                |                                    |
|----------------|------------------------------------|
| MLC6_SRC_[7:0] | Output value of MLC6 decision tree |
|----------------|------------------------------------|

## 11.53 MLC7\_SRC (77h)

Machine Learning Core source register (r)

**Table 288. MLC7\_SRC register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| MLC7_SRC_7 | MLC7_SRC_6 | MLC7_SRC_5 | MLC7_SRC_4 | MLC7_SRC_3 | MLC7_SRC_2 | MLC7_SRC_1 | MLC7_SRC_0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 289. MLC7\_SRC register description**

|                |                                    |
|----------------|------------------------------------|
| MLC7_SRC_[7:0] | Output value of MLC7 decision tree |
|----------------|------------------------------------|

## 12 Embedded advanced features pages

The table given below provides a list of the registers for the embedded advanced features page 0. These registers are accessible when PAGE\_SEL[3:0] are set to 0000 in [PAGE\\_SEL \(02h\)](#).

**Table 290. Register address map - embedded advanced features page 0**

| Name              | Type | Register address |          | Default  | Comment |
|-------------------|------|------------------|----------|----------|---------|
|                   |      | Hex              | Binary   |          |         |
| MAG_SENSITIVITY_L | RW   | BA               | 10111010 | 00100100 |         |
| MAG_SENSITIVITY_H | RW   | BB               | 10111011 | 00010110 |         |
| MAG_OFFX_L        | RW   | C0               | 11000000 | 00000000 |         |
| MAG_OFFX_H        | RW   | C1               | 11000001 | 00000000 |         |
| MAG_OFFY_L        | RW   | C2               | 11000010 | 00000000 |         |
| MAG_OFFY_H        | RW   | C3               | 11000011 | 00000000 |         |
| MAG_OFFZ_L        | RW   | C4               | 11000100 | 00000000 |         |
| MAG_OFFZ_H        | RW   | C5               | 11000101 | 00000000 |         |
| MAG_SI_XX_L       | RW   | C6               | 11000110 | 00000000 |         |
| MAG_SI_XX_H       | RW   | C7               | 11000111 | 00111100 |         |
| MAG_SI_XY_L       | RW   | C8               | 11001000 | 00000000 |         |
| MAG_SI_XY_H       | RW   | C9               | 11001001 | 00000000 |         |
| MAG_SI_XZ_L       | RW   | CA               | 11001010 | 00000000 |         |
| MAG_SI_XZ_H       | RW   | CB               | 11001011 | 00000000 |         |
| MAG_SI_YY_L       | RW   | CC               | 11001100 | 00000000 |         |
| MAG_SI_YY_H       | RW   | CD               | 11001101 | 00111100 |         |
| MAG_SI_YZ_L       | RW   | CE               | 11001110 | 00000000 |         |
| MAG_SI_YZ_H       | RW   | CF               | 11001111 | 00000000 |         |
| MAG_SI_ZZ_L       | RW   | D0               | 11010000 | 00000000 |         |
| MAG_SI_ZZ_H       | RW   | D1               | 11010001 | 00111100 |         |
| MAG_CFG_A         | RW   | D4               | 11010100 | 00000101 |         |
| MAG_CFG_B         | RW   | D5               | 11010101 | 00000010 |         |

The following table provides a list of the registers for the embedded advanced features page 1. These registers are accessible when PAGE\_SEL[3:0] are set to 0001 in [PAGE\\_SEL \(02h\)](#).

**Table 291. Register address map - embedded advanced features page 1**

| Name                  | Type | Register address |          | Default  | Comment |
|-----------------------|------|------------------|----------|----------|---------|
|                       |      | Hex              | Binary   |          |         |
| FSM_LC_TIMEOUT_L      | RW   | 7A               | 01111010 | 00000000 |         |
| FSM_LC_TIMEOUT_H      | RW   | 7B               | 01111011 | 00000000 |         |
| FSM_PROGRAMS          | RW   | 7C               | 01111100 | 00000000 |         |
| FSM_START_ADD_L       | RW   | 7E               | 01111110 | 00000000 |         |
| FSM_START_ADD_H       | RW   | 7F               | 01111111 | 00000000 |         |
| PEDO_CMD_REG          | RW   | 83               | 10000011 | 00000000 |         |
| PEDO_DEB_STEPS_CONF   | RW   | 84               | 10000100 | 00001010 |         |
| PEDO_SC_DELTAT_L      | RW   | D0               | 11010000 | 00000000 |         |
| PEDO_SC_DELTAT_H      | RW   | D1               | 11010001 | 00000000 |         |
| MLC_MAG_SENSITIVITY_L | RW   | E8               | 11101000 | 00000000 |         |
| MLC_MAG_SENSITIVITY_H | RW   | E9               | 11101001 | 00111100 |         |

Registers marked as Reserved must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

**Write procedure example:**

Example: write value 06h register at address 84h (PEDO\_DEB\_STEPS\_CONF) in Page 1

1. Write bit FUNC\_CFG\_EN = 1 // Enable access to embedded functions registers  
in FUNC\_CFG\_ACCESS (01h)
2. Write bit PAGE\_WRITE = 1 // Select write operation mode  
in PAGE\_RW (17h) register
3. Write 0001 in PAGE\_SEL[3:0] field // Select page 1  
of register PAGE\_SEL (02h)
4. Write 84h in PAGE\_ADDR register (08h) // Set address
5. Write 06h in PAGE\_DATA register (09h) // Set value to be written
6. Write bit PAGE\_WRITE = 0 // Write operation disabled  
in PAGE\_RW (17h) register
7. Write bit FUNC\_CFG\_EN = 0 // Disable access to embedded functions registers  
in FUNC\_CFG\_ACCESS (01h)

**Read procedure example:**

Example: read value of register at address 84h (PEDO\_DEB\_STEPS\_CONF) in Page 1

1. Write bit FUNC\_CFG\_EN = 1 // Enable access to embedded functions registers  
in FUNC\_CFG\_ACCESS (01h)
2. Write bit PAGE\_READ = 1 // Select read operation mode  
in PAGE\_RW (17h) register
3. Write 0001 in PAGE\_SEL[3:0] field // Select page 1

of register PAGE\_SEL (02h)

- |    |   |   |
|----|---|---|
| 4. | Write 84h in PAGE_ADDR register (08h)                 | // Set address                                    |
| 5. | Read value of PAGE_DATA register (09h)                | // Get register value                             |
| 6. | Write bit PAGE_READ = 0<br>in PAGE_RW (17h) register  | // Read operation disabled                        |
| 7. | Write bit FUNC_CFG_EN = 0<br>in FUNC_CFG_ACCESS (01h) | // Disable access to embedded functions registers |

*Note: Steps 1 and 2 of both procedures are intended to be performed at the beginning of the procedure. Steps 6 and 7 of both procedures are intended to be performed at the end of the procedure. If the procedure involves multiple operations, only steps 3, 4 and 5 must be repeated for each operation. If, in particular, multiple operations involve consecutive registers, only step 5 can be performed.*

## 13 Embedded advanced features register description

### 13.1 Page 0 - Embedded advanced features registers

#### 13.1.1 **MAG\_SENSITIVITY\_L (BAh) and MAG\_SENSITIVITY\_H (BBh)**

External magnetometer sensitivity value register for the Finite State Machine (r/w).

This register corresponds to the LSB-to-gauss conversion value of the external magnetometer sensor. The register value is expressed as half-precision floating-point format: SEEEEEEEEEEEEEE

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

Default value of MAG\_SENS[15:0] is 0x1624, corresponding to 0.0015 gauss/LSB.

**Table 292. MAG\_SENSITIVITY\_L register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| MAG_SENS_7 | MAG_SENS_6 | MAG_SENS_5 | MAG_SENS_4 | MAG_SENS_3 | MAG_SENS_2 | MAG_SENS_1 | MAG_SENS_0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 293. MAG\_SENSITIVITY\_L register description**

|                |   |
|----------------|---|
| MAG_SENS_[7:0] | External magnetometer sensitivity (LSbyte). Default value: 00100100 |
|----------------|---|

**Table 294. MAG\_SENSITIVITY\_H register**

|             |             |             |             |             |             |            |            |
|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|
| MAG_SENS_15 | MAG_SENS_14 | MAG_SENS_13 | MAG_SENS_12 | MAG_SENS_11 | MAG_SENS_10 | MAG_SENS_9 | MAG_SENS_8 |
|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|

**Table 295. MAG\_SENSITIVITY\_H register description**

|                 |   |
|-----------------|---|
| MAG_SENS_[15:8] | External magnetometer sensitivity (MSbyte). Default value: 00010110 |
|-----------------|---|

**13.1.2 MAG\_OFFX\_L (C0h) and MAG\_OFFX\_H (C1h)**

Offset for X-axis hard-iron compensation register (r/w).

The value is expressed as half-precision floating-point format: SEEEEEEEEEEEEFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 296. MAG\_OFFX\_L register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| MAG_OFFX_7 | MAG_OFFX_6 | MAG_OFFX_5 | MAG_OFFX_4 | MAG_OFFX_3 | MAG_OFFX_2 | MAG_OFFX_1 | MAG_OFFX_0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 297. MAG\_OFFX\_L register description**

|                |  |
|----------------|--|
| MAG_OFFX_[7:0] | Offset for X-axis hard-iron compensation (LSbyte). Default value: 00000000 |
|----------------|--|

**Table 298. MAG\_OFFX\_H register**

|             |             |             |             |             |             |            |            |
|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|
| MAG_OFFX_15 | MAG_OFFX_14 | MAG_OFFX_13 | MAG_OFFX_12 | MAG_OFFX_11 | MAG_OFFX_10 | MAG_OFFX_9 | MAG_OFFX_8 |
|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|

**Table 299. MAG\_OFFX\_H register description**

|                 |  |
|-----------------|--|
| MAG_OFFX_[15:8] | Offset for X-axis hard-iron compensation (MSbyte). Default value: 00000000 |
|-----------------|--|

**13.1.3 MAG\_OFFY\_L (C2h) and MAG\_OFFY\_H (C3h)**

Offset for Y-axis hard-iron compensation register (r/w).

The value is expressed as half-precision floating-point format: SEEEEEEEEEEEEFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 300. MAG\_OFFY\_L register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| MAG_OFFY_7 | MAG_OFFY_6 | MAG_OFFY_5 | MAG_OFFY_4 | MAG_OFFY_3 | MAG_OFFY_2 | MAG_OFFY_1 | MAG_OFFY_0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 301. MAG\_OFFY\_L register description**

|                |  |
|----------------|--|
| MAG_OFFY_[7:0] | Offset for Y-axis hard-iron compensation (LSbyte). Default value: 00000000 |
|----------------|--|

**Table 302. MAG\_OFFY\_H register**

|             |             |             |             |             |             |            |            |
|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|
| MAG_OFFY_15 | MAG_OFFY_14 | MAG_OFFY_13 | MAG_OFFY_12 | MAG_OFFY_11 | MAG_OFFY_10 | MAG_OFFY_9 | MAG_OFFY_8 |
|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|

**Table 303. MAG\_OFFY\_H register description**

|                 |  |
|-----------------|--|
| MAG_OFFY_[15:8] | Offset for Y-axis hard-iron compensation (MSbyte). Default value: 00000000 |
|-----------------|--|

**13.1.4 MAG\_OFFZ\_L (C4h) and MAG\_OFFZ\_H (C5h)**

Offset for Z-axis hard-iron compensation register (r/w).

The value is expressed as half-precision floating-point format: SEEEEEEEEEEEEEE

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 304. MAG\_OFFZ\_L register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| MAG_OFFZ_7 | MAG_OFFZ_6 | MAG_OFFZ_5 | MAG_OFFZ_4 | MAG_OFFZ_3 | MAG_OFFZ_2 | MAG_OFFZ_1 | MAG_OFFZ_0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 305. MAG\_OFFZ\_L register description**

|                |  |
|----------------|--|
| MAG_OFFZ_[7:0] | Offset for Z-axis hard-iron compensation (LSbyte). Default value: 00000000 |
|----------------|--|

**Table 306. MAG\_OFFZ\_H register**

|             |             |             |             |             |             |            |            |
|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|
| MAG_OFFZ_15 | MAG_OFFZ_14 | MAG_OFFZ_13 | MAG_OFFZ_12 | MAG_OFFZ_11 | MAG_OFFZ_10 | MAG_OFFZ_9 | MAG_OFFZ_8 |
|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|

**Table 307. MAG\_OFFZ\_H register description**

|                 |  |
|-----------------|--|
| MAG_OFFZ_[15:8] | Offset for Z-axis hard-iron compensation (MSbyte). Default value: 00000000 |
|-----------------|--|

**13.1.5 MAG\_SI\_XX\_L (C6h) and MAG\_SI\_XX\_H (C7h)**

Soft-iron (3x3 symmetric) matrix correction register (r/w).

The value is expressed as half-precision floating-point format: SEEEEEEEEEEEEEE

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 308. MAG\_SI\_XX\_L register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_XX_7 | MAG_SI_XX_6 | MAG_SI_XX_5 | MAG_SI_XX_4 | MAG_SI_XX_3 | MAG_SI_XX_2 | MAG_SI_XX_1 | MAG_SI_XX_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 309. MAG\_SI\_XX\_L register description**

|                 |  |
|-----------------|--|
| MAG_SI_XX_[7:0] | Soft-iron correction row1 col1 coefficient (LSbyte). Default value: 00000000 |
|-----------------|--|

**Table 310. MAG\_SI\_XX\_H register**

|              |              |              |              |              |              |             |             |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|
| MAG_SI_XX_15 | MAG_SI_XX_14 | MAG_SI_XX_13 | MAG_SI_XX_12 | MAG_SI_XX_11 | MAG_SI_XX_10 | MAG_SI_XX_9 | MAG_SI_XX_8 |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|

**Table 311. MAG\_SI\_XX\_H register description**

|                  |  |
|------------------|--|
| MAG_SI_XX_[15:8] | Soft-iron correction row1 col1 coefficient (MSbyte). Default value: 00111100 |
|------------------|--|

**13.1.6 MAG\_SI\_XY\_L (C8h) and MAG\_SI\_XY\_H (C9h)**

Soft-iron (3x3 symmetric) matrix correction register (r/w).

The value is expressed as half-precision floating-point format: SEEEEEEEEEEEEEE

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 312. MAG\_SI\_XY\_L register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_XY_7 | MAG_SI_XY_6 | MAG_SI_XY_5 | MAG_SI_XY_4 | MAG_SI_XY_3 | MAG_SI_XY_2 | MAG_SI_XY_1 | MAG_SI_XY_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 313. MAG\_SI\_XY\_L register description**

|                 |  |
|-----------------|--|
| MAG_SI_XY_[7:0] | Soft-iron correction row1 col2 (and row2 col1) coefficient (LSbyte). Default value: 00000000 |
|-----------------|--|

**Table 314. MAG\_SI\_XY\_H register**

|              |              |              |              |              |              |             |             |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|
| MAG_SI_XY_15 | MAG_SI_XY_14 | MAG_SI_XY_13 | MAG_SI_XY_12 | MAG_SI_XY_11 | MAG_SI_XY_10 | MAG_SI_XY_9 | MAG_SI_XY_8 |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|

**Table 315. MAG\_SI\_XY\_H register description**

|                  |  |
|------------------|--|
| MAG_SI_XY_[15:8] | Soft-iron correction row1 col2 (and row2 col1) coefficient (MSbyte). Default value: 00000000 |
|------------------|--|

**13.1.7 MAG\_SI\_XZ\_L (CAh) and MAG\_SI\_XZ\_H (CBh)**

Soft-iron (3x3 symmetric) matrix correction register (r/w).

The value is expressed as half-precision floating-point format: SEEEEEEEEEEEEEE

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 316. MAG\_SI\_XZ\_L register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_XZ_7 | MAG_SI_XZ_6 | MAG_SI_XZ_5 | MAG_SI_XZ_4 | MAG_SI_XZ_3 | MAG_SI_XZ_2 | MAG_SI_XZ_1 | MAG_SI_XZ_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 317. MAG\_SI\_XZ\_L register description**

|                 |  |
|-----------------|--|
| MAG_SI_XZ_[7:0] | Soft-iron correction row1 col3 (and row3 col1) coefficient (LSbyte). Default value: 00000000 |
|-----------------|--|

**Table 318. MAG\_SI\_XZ\_H register**

|              |              |              |              |              |              |             |             |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|
| MAG_SI_XZ_15 | MAG_SI_XZ_14 | MAG_SI_XZ_13 | MAG_SI_XZ_12 | MAG_SI_XZ_11 | MAG_SI_XZ_10 | MAG_SI_XZ_9 | MAG_SI_XZ_8 |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|

**Table 319. MAG\_SI\_XZ\_H register description**

|                  |  |
|------------------|--|
| MAG_SI_XZ_[15:8] | Soft-iron correction row1 col3 (and row3 col1) coefficient (MSbyte). Default value: 00000000 |
|------------------|--|



**13.1.8 MAG\_SI\_YY\_L (CCh) and MAG\_SI\_YY\_H (CDh)**

Soft-iron (3x3 symmetric) matrix correction register (r/w).

The value is expressed as half-precision floating-point format: SEEEEEEEEEEEEFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 320. MAG\_SI\_YY\_L register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_YY_7 | MAG_SI_YY_6 | MAG_SI_YY_5 | MAG_SI_YY_4 | MAG_SI_YY_3 | MAG_SI_YY_2 | MAG_SI_YY_1 | MAG_SI_YY_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 321. MAG\_SI\_YY\_L register description**

|                 |  |
|-----------------|--|
| MAG_SI_YY_[7:0] | Soft-iron correction row2 col2 coefficient (LSbyte). Default value: 00000000 |
|-----------------|--|

**Table 322. MAG\_SI\_YY\_H register**

|              |              |              |              |              |              |             |             |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|
| MAG_SI_YY_15 | MAG_SI_YY_14 | MAG_SI_YY_13 | MAG_SI_YY_12 | MAG_SI_YY_11 | MAG_SI_YY_10 | MAG_SI_YY_9 | MAG_SI_YY_8 |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|

**Table 323. MAG\_SI\_YY\_H register description**

|                  |  |
|------------------|--|
| MAG_SI_YY_[15:8] | Soft-iron correction row2 col2 coefficient (MSbyte). Default value: 00111100 |
|------------------|--|

**13.1.9 MAG\_SI\_YZ\_L (CEh) and MAG\_SI\_YZ\_H (CFh)**

Soft-iron (3x3 symmetric) matrix correction register (r/w).

The value is expressed as half-precision floating-point format: SEEEEEEEEEEEEFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 324. MAG\_SI\_YZ\_L register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_YZ_7 | MAG_SI_YZ_6 | MAG_SI_YZ_5 | MAG_SI_YZ_4 | MAG_SI_YZ_3 | MAG_SI_YZ_2 | MAG_SI_YZ_1 | MAG_SI_YZ_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 325. MAG\_SI\_YZ\_L register description**

|                 |  |
|-----------------|--|
| MAG_SI_YZ_[7:0] | Soft-iron correction row2 col3 (and row3 col2) coefficient (LSbyte). Default value: 00000000 |
|-----------------|--|

**Table 326. MAG\_SI\_YZ\_H register**

|              |              |              |              |              |              |             |             |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|
| MAG_SI_YZ_15 | MAG_SI_YZ_14 | MAG_SI_YZ_13 | MAG_SI_YZ_12 | MAG_SI_YZ_11 | MAG_SI_YZ_10 | MAG_SI_YZ_9 | MAG_SI_YZ_8 |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|

**Table 327. MAG\_SI\_YZ\_H register description**

|                  |  |
|------------------|--|
| MAG_SI_YZ_[15:8] | Soft-iron correction row2 col3 (and row3 col2) coefficient (MSbyte). Default value: 00000000 |
|------------------|--|

**13.1.10 MAG\_SI\_ZZ\_L (D0h) and MAG\_SI\_ZZ\_H (D1h)**

Soft-iron (3x3 symmetric) matrix correction register (r/w).

The value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFFFF

(S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

**Table 328. MAG\_SI\_ZZ\_L register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MAG_SI_ZZ_7 | MAG_SI_ZZ_6 | MAG_SI_ZZ_5 | MAG_SI_ZZ_4 | MAG_SI_ZZ_3 | MAG_SI_ZZ_2 | MAG_SI_ZZ_1 | MAG_SI_ZZ_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 329. MAG\_SI\_ZZ\_L register description**

|                 |  |
|-----------------|--|
| MAG_SI_ZZ_[7:0] | Soft-iron correction row3 col3 coefficient (LSbyte). Default value: 00000000 |
|-----------------|--|

**Table 330. MAG\_SI\_ZZ\_H register**

|              |              |              |              |              |              |             |             |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|
| MAG_SI_ZZ_15 | MAG_SI_ZZ_14 | MAG_SI_ZZ_13 | MAG_SI_ZZ_12 | MAG_SI_ZZ_11 | MAG_SI_ZZ_10 | MAG_SI_ZZ_9 | MAG_SI_ZZ_8 |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|

**Table 331. MAG\_SI\_ZZ\_H register description**

|                  |  |
|------------------|--|
| MAG_SI_ZZ_[15:8] | Soft-iron correction row3 col3 coefficient (MSbyte). Default value: 00111100 |
|------------------|--|

**13.1.11 MAG\_CFG\_A (D4h)**

External magnetometer coordinates (Z and Y axes) rotation register (r/w)

**Table 332. MAG\_CFG\_A register**

|                  |                 |                 |                 |                  |                 |                 |                 |
|------------------|-----------------|-----------------|-----------------|------------------|-----------------|-----------------|-----------------|
| 0 <sup>(1)</sup> | MAG_Y_<br>AXIS2 | MAG_Y_<br>AXIS1 | MAG_Y_<br>AXIS0 | 0 <sup>(1)</sup> | MAG_Z_<br>AXIS2 | MAG_Z_<br>AXIS1 | MAG_Z_<br>AXIS0 |
|------------------|-----------------|-----------------|-----------------|------------------|-----------------|-----------------|-----------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 333. MAG\_CFG\_A register description**

|                 |  |
|-----------------|--|
| MAG_Y_AXIS[2:0] | Magnetometer Y-axis coordinates rotation (to be aligned to accelerometer/gyroscope axes orientation)<br>(000: Y = Y; (default)<br>001: Y = -Y;<br>010: Y = X;<br>011: Y = -X;<br>100: Y = -Z;<br>101: Y = Z;<br>Others: Y = Y) |
| MAG_Z_AXIS[2:0] | Magnetometer Z-axis coordinates rotation (to be aligned to accelerometer/gyroscope axes orientation)<br>(000: Z = Y;<br>001: Z = -Y;<br>010: Z = X;<br>011: Z = -X;<br>100: Z = -Z;<br>101: Z = Z; (default)<br>Others: Z = Y) |

**13.1.12 MAG\_CFG\_B (D5h)**

External magnetometer coordinates (X-axis) rotation register (r/w)

**Table 334. MAG\_CFG\_B register**

|                  |                  |                  |                  |                  |                 |                 |                 |
|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|-----------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | MAG_X_<br>AXIS2 | MAG_X_<br>AXIS1 | MAG_X_<br>AXIS0 |
|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|-----------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 335. MAG\_CFG\_B register description**

|                 |  |
|-----------------|--|
| MAG_X_AXIS[2:0] | Magnetometer X-axis coordinates rotation (to be aligned to accelerometer/gyroscope axes orientation)<br>(000: X = Y;<br>001: X = -Y;<br>010: X = X; (default)<br>011: X = -X;<br>100: X = -Z;<br>101: X = Z;<br>Others: X = Y) |
|-----------------|--|

## 13.2 Page 1 - Embedded advanced features registers

### 13.2.1 FSM\_LC\_TIMEOUT\_L (7Ah) and FSM\_LC\_TIMEOUT\_H (7Bh)

FSM long counter timeout register (r/w).

The long counter timeout value is an unsigned integer value (16-bit format). When the long counter value reaches this value, the FSM generates an interrupt.

**Table 336. FSM\_LC\_TIMEOUT\_L register**

|                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| FSM_LC_TIMEOUT7 | FSM_LC_TIMEOUT6 | FSM_LC_TIMEOUT5 | FSM_LC_TIMEOUT4 | FSM_LC_TIMEOUT3 | FSM_LC_TIMEOUT2 | FSM_LC_TIMEOUT1 | FSM_LC_TIMEOUT0 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|

**Table 337. FSM\_LC\_TIMEOUT\_L register description**

|                     |  |
|---------------------|--|
| FSM_LC_TIMEOUT[7:0] | FSM long counter timeout value (LSbyte). Default value: 00000000 |
|---------------------|--|

**Table 338. FSM\_LC\_TIMEOUT\_H register**

|                  |                  |                  |                  |                  |                  |                 |                 |
|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|
| FSM_LC_TIMEOUT15 | FSM_LC_TIMEOUT14 | FSM_LC_TIMEOUT13 | FSM_LC_TIMEOUT12 | FSM_LC_TIMEOUT11 | FSM_LC_TIMEOUT10 | FSM_LC_TIMEOUT9 | FSM_LC_TIMEOUT8 |
|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|

**Table 339. FSM\_LC\_TIMEOUT\_H register description**

|                      |  |
|----------------------|--|
| FSM_LC_TIMEOUT[15:8] | FSM long counter timeout value (MSbyte). Default value: 00000000 |
|----------------------|--|

### 13.2.2 FSM\_PROGRAMS (7Ch)

FSM number of programs register (r/w)

**Table 340. FSM\_PROGRAMS register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| FSM_N_PROG7 | FSM_N_PROG6 | FSM_N_PROG5 | FSM_N_PROG4 | FSM_N_PROG3 | FSM_N_PROG2 | FSM_N_PROG1 | FSM_N_PROG0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 341. FSM\_PROGRAMS register description**

|                 |   |
|-----------------|---|
| FSM_N_PROG[7:0] | Number of FSM programs; must be less than or equal to 16. Default value: 00000000 |
|-----------------|---|

**13.2.3 FSM\_START\_ADD\_L (7Eh) and FSM\_START\_ADD\_H (7Fh)**

FSM start address register (r/w). First available address is 0x033C.

**Table 342. FSM\_START\_ADD\_L register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| FSM_START7 | FSM_START6 | FSM_START5 | FSM_START4 | FSM_START3 | FSM_START2 | FSM_START1 | FSM_START0 |
|------------|------------|------------|------------|------------|------------|------------|------------|

**Table 343. FSM\_START\_ADD\_L register description**

|                |   |
|----------------|---|
| FSM_START[7:0] | FSM start address value (LSbyte). Default value: 00000000 |
|----------------|---|

**Table 344. FSM\_START\_ADD\_H register**

|             |             |             |             |             |             |            |            |
|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|
| FSM_START15 | FSM_START14 | FSM_START13 | FSM_START12 | FSM_START11 | FSM_START10 | FSM_START9 | FSM_START8 |
|-------------|-------------|-------------|-------------|-------------|-------------|------------|------------|

**Table 345. FSM\_START\_ADD\_H register description**

|                 |   |
|-----------------|---|
| FSM_START[15:8] | FSM start address value (MSbyte). Default value: 00000000 |
|-----------------|---|

**13.2.4 PEDO\_CMD\_REG (83h)**

Pedometer configuration register (r/w)

**Table 346. PEDO\_CMD\_REG register**

|                  |                  |                  |                  |                |                  |                  |                  |
|------------------|------------------|------------------|------------------|----------------|------------------|------------------|------------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | CARRY_COUNT_EN | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|------------------|------------------|------------------|------------------|----------------|------------------|------------------|------------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 347. PEDO\_CMD\_REG register description**

|                |   |
|----------------|---|
| CARRY_COUNT_EN | Set when user wants to generate interrupt only on count overflow event. |
|----------------|---|

**13.2.5 PEDO\_DEB\_CONF (84h)**

Pedometer debounce configuration register (r/w)

**Table 348. PEDO\_DEB\_STEPS\_CONF register**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| DEB_STEP7 | DEB_STEP6 | DEB_STEP5 | DEB_STEP4 | DEB_STEP3 | DEB_STEP2 | DEB_STEP1 | DEB_STEP0 |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|

**Table 349. PEDO\_DEB\_STEPS\_CONF register description**

|               |   |
|---------------|---|
| DEB_STEP[7:0] | Debounce threshold. Minimum number of steps to increment the step counter (debounce). Default value: 00001010 |
|---------------|---|

**13.2.6 PEDO\_SC\_DELTAT\_L (D0h) and PEDO\_SC\_DELTAT\_H (D1h)**

Time period register for step detection on delta time (r/w)

**Table 350. PEDO\_SC\_DELTAT\_L register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| PD_SC_7 | PD_SC_6 | PD_SC_5 | PD_SC_4 | PD_SC_3 | PD_SC_2 | PD_SC_1 | PD_SC_0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 351. PEDO\_SC\_DELTAT\_H register**

|          |          |          |          |          |          |         |         |
|----------|----------|----------|----------|----------|----------|---------|---------|
| PD_SC_15 | PD_SC_14 | PD_SC_13 | PD_SC_12 | PD_SC_11 | PD_SC_10 | PD_SC_9 | PD_SC_8 |
|----------|----------|----------|----------|----------|----------|---------|---------|

**Table 352. PEDO\_SC\_DELTAT\_H/L register description**

|              |                                   |
|--------------|-----------------------------------|
| PD_SC_[15:0] | Time period value (1LSB = 6.4 ms) |
|--------------|-----------------------------------|

**13.2.7 MLC\_MAG\_SENSITIVITY\_L (E8h) and MLC\_MAG\_SENSITIVITY\_H (E9h)**

External magnetometer sensitivity value register for the Machine Learning Core (r/w).

This register corresponds to the LSB-to-gauss conversion value of the external magnetometer sensor. The register value is expressed as half-precision floating-point format: S EEEEEEEEEEEEEEE (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits). Default value of MLC\_MAG\_S\_[15:0] is 0x3C00, corresponding to 1 gauss/LSB.

**Table 353. MLC\_MAG\_SENSITIVITY\_L register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| MLC_MAG_S_7 | MLC_MAG_S_6 | MLC_MAG_S_5 | MLC_MAG_S_4 | MLC_MAG_S_3 | MLC_MAG_S_2 | MLC_MAG_S_1 | MLC_MAG_S_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 354. MLC\_MAG\_SENSITIVITY\_L register description**

|                 |   |
|-----------------|---|
| MLC_MAG_S_[7:0] | External magnetometer sensitivity (LSbyte). Default value: 00000000 |
|-----------------|---|

**Table 355. MLC\_MAG\_SENSITIVITY\_H register**

|              |              |              |              |              |              |             |             |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|
| MLC_MAG_S_15 | MLC_MAG_S_14 | MLC_MAG_S_13 | MLC_MAG_S_12 | MLC_MAG_S_11 | MLC_MAG_S_10 | MLC_MAG_S_9 | MLC_MAG_S_8 |
|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|

**Table 356. MLC\_MAG\_SENSITIVITY\_H register description**

|                  |   |
|------------------|---|
| MLC_MAG_S_[15:8] | External magnetometer sensitivity (MSbyte). Default value: 00111100 |
|------------------|---|

## 14 Sensor hub register mapping

The table given below provides a list of the registers for the sensor hub functions available in the device and the corresponding addresses. The sensor hub registers are accessible when bit SHUB\_REG\_ACCESS is set to '1' in FUNC\_CFG\_ACCESS (01h).

**Table 357. Registers address map**

| Name           | Type | Register address |          | Default  | Comment |
|----------------|------|------------------|----------|----------|---------|
|                |      | Hex              | Binary   |          |         |
| SENSOR_HUB_1   | R    | 02               | 00000010 | output   |         |
| SENSOR_HUB_2   | R    | 03               | 00000011 | output   |         |
| SENSOR_HUB_3   | R    | 04               | 00000100 | output   |         |
| SENSOR_HUB_4   | R    | 05               | 00000101 | output   |         |
| SENSOR_HUB_5   | R    | 06               | 00000110 | output   |         |
| SENSOR_HUB_6   | R    | 07               | 00000111 | output   |         |
| SENSOR_HUB_7   | R    | 08               | 00001000 | output   |         |
| SENSOR_HUB_8   | R    | 09               | 00001001 | output   |         |
| SENSOR_HUB_9   | R    | 0A               | 00001010 | output   |         |
| SENSOR_HUB_10  | R    | 0B               | 00001011 | output   |         |
| SENSOR_HUB_11  | R    | 0C               | 00001100 | output   |         |
| SENSOR_HUB_12  | R    | 0D               | 00001101 | output   |         |
| SENSOR_HUB_13  | R    | 0E               | 00001110 | output   |         |
| SENSOR_HUB_14  | R    | 0F               | 00001111 | output   |         |
| SENSOR_HUB_15  | R    | 10               | 00010000 | output   |         |
| SENSOR_HUB_16  | R    | 11               | 00010001 | output   |         |
| SENSOR_HUB_17  | R    | 12               | 00010010 | output   |         |
| SENSOR_HUB_18  | R    | 13               | 00010011 | output   |         |
| MASTER_CONFIG  | RW   | 14               | 00010100 | 00000000 |         |
| SLV0_ADD       | RW   | 15               | 00010101 | 00000000 |         |
| SLV0_SUBADD    | RW   | 16               | 00010110 | 00000000 |         |
| SLV0_CONFIG    | RW   | 17               | 00010111 | 00000000 |         |
| SLV1_ADD       | RW   | 18               | 00011000 | 00000000 |         |
| SLV1_SUBADD    | RW   | 19               | 00011001 | 00000000 |         |
| SLV1_CONFIG    | RW   | 1A               | 00011010 | 00000000 |         |
| SLV2_ADD       | RW   | 1B               | 00011011 | 00000000 |         |
| SLV2_SUBADD    | RW   | 1C               | 00011100 | 00000000 |         |
| SLV2_CONFIG    | RW   | 1D               | 00011101 | 00000000 |         |
| SLV3_ADD       | RW   | 1E               | 00011110 | 00000000 |         |
| SLV3_SUBADD    | RW   | 1F               | 00011111 | 00000000 |         |
| SLV3_CONFIG    | RW   | 20               | 00100000 | 00000000 |         |
| DATAWRITE_SLV0 | RW   | 21               | 00100001 | 00000000 |         |
| STATUS_MASTER  | R    | 22               | 00100010 | output   |         |

Registers marked as Reserved must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.



## 15 Sensor hub register description

### 15.1 SENSOR\_HUB\_1 (02h)

Sensor hub output register (r)

First byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 358. SENSOR\_HUB\_1 register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Sensor Hub1_7 | Sensor Hub1_6 | Sensor Hub1_5 | Sensor Hub1_4 | Sensor Hub1_3 | Sensor Hub1_2 | Sensor Hub1_1 | Sensor Hub1_0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

**Table 359. SENSOR\_HUB\_1 register description**

|                 |   |
|-----------------|---|
| SensorHub1[7:0] | First byte associated to external sensors |
|-----------------|---|

### 15.2 SENSOR\_HUB\_2 (03h)

Sensor hub output register (r)

Second byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 360. SENSOR\_HUB\_2 register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Sensor Hub2_7 | Sensor Hub2_6 | Sensor Hub2_5 | Sensor Hub2_4 | Sensor Hub2_3 | Sensor Hub2_2 | Sensor Hub2_1 | Sensor Hub2_0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

**Table 361. SENSOR\_HUB\_2 register description**

|                 |  |
|-----------------|--|
| SensorHub2[7:0] | Second byte associated to external sensors |
|-----------------|--|

### 15.3 SENSOR\_HUB\_3 (04h)

Sensor hub output register (r)

Third byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 362. SENSOR\_HUB\_3 register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Sensor Hub3_7 | Sensor Hub3_6 | Sensor Hub3_5 | Sensor Hub3_4 | Sensor Hub3_3 | Sensor Hub3_2 | Sensor Hub3_1 | Sensor Hub3_0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

**Table 363. SENSOR\_HUB\_3 register description**

|                 |   |
|-----------------|---|
| SensorHub3[7:0] | Third byte associated to external sensors |
|-----------------|---|

## 15.4 SENSOR\_HUB\_4 (05h)

Sensor hub output register (r)

Fourth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 364. SENSOR\_HUB\_4 register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Sensor Hub4_7 | Sensor Hub4_6 | Sensor Hub4_5 | Sensor Hub4_4 | Sensor Hub4_3 | Sensor Hub4_2 | Sensor Hub4_1 | Sensor Hub4_0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

**Table 365. SENSOR\_HUB\_4 register description**

|                 |  |
|-----------------|--|
| SensorHub4[7:0] | Fourth byte associated to external sensors |
|-----------------|--|

## 15.5 SENSOR\_HUB\_5 (06h)

Sensor hub output register (r)

Fifth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 366. SENSOR\_HUB\_5 register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Sensor Hub5_7 | Sensor Hub5_6 | Sensor Hub5_5 | Sensor Hub5_4 | Sensor Hub5_3 | Sensor Hub5_2 | Sensor Hub5_1 | Sensor Hub5_0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

**Table 367. SENSOR\_HUB\_5 register description**

|                 |   |
|-----------------|---|
| SensorHub5[7:0] | Fifth byte associated to external sensors |
|-----------------|---|

## 15.6 SENSOR\_HUB\_6 (07h)

Sensor hub output register (r)

Sixth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 368. SENSOR\_HUB\_6 register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Sensor Hub6_7 | Sensor Hub6_6 | Sensor Hub6_5 | Sensor Hub6_4 | Sensor Hub6_3 | Sensor Hub6_2 | Sensor Hub6_1 | Sensor Hub6_0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

**Table 369. SENSOR\_HUB\_6 register description**

|                 |   |
|-----------------|---|
| SensorHub6[7:0] | Sixth byte associated to external sensors |
|-----------------|---|

## 15.7 SENSOR\_HUB\_7 (08h)

Sensor hub output register (r)

Seventh byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 370. SENSOR\_HUB\_7 register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Sensor Hub7_7 | Sensor Hub7_6 | Sensor Hub7_5 | Sensor Hub7_4 | Sensor Hub7_3 | Sensor Hub7_2 | Sensor Hub7_1 | Sensor Hub7_0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

**Table 371. SENSOR\_HUB\_7 register description**

|                 |   |
|-----------------|---|
| SensorHub7[7:0] | Seventh byte associated to external sensors |
|-----------------|---|

## 15.8 SENSOR\_HUB\_8 (09h)

Sensor hub output register (r)

Eighth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 372. SENSOR\_HUB\_8 register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Sensor Hub8_7 | Sensor Hub8_6 | Sensor Hub8_5 | Sensor Hub8_4 | Sensor Hub8_3 | Sensor Hub8_2 | Sensor Hub8_1 | Sensor Hub8_0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

**Table 373. SENSOR\_HUB\_8 register description**

|                 |  |
|-----------------|--|
| SensorHub8[7:0] | Eighth byte associated to external sensors |
|-----------------|--|

## 15.9 SENSOR\_HUB\_9 (0Ah)

Sensor hub output register (r)

Ninth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 374. SENSOR\_HUB\_9 register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Sensor Hub9_7 | Sensor Hub9_6 | Sensor Hub9_5 | Sensor Hub9_4 | Sensor Hub9_3 | Sensor Hub9_2 | Sensor Hub9_1 | Sensor Hub9_0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

**Table 375. SENSOR\_HUB\_9 register description**

|                 |   |
|-----------------|---|
| SensorHub9[7:0] | Ninth byte associated to external sensors |
|-----------------|---|

## 15.10 SENSOR\_HUB\_10 (0Bh)

Sensor hub output register (r)

Tenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 376. SENSOR\_HUB\_10 register**

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Sensor Hub10_7 | Sensor Hub10_6 | Sensor Hub10_5 | Sensor Hub10_4 | Sensor Hub10_3 | Sensor Hub10_2 | Sensor Hub10_1 | Sensor Hub10_0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**Table 377. SENSOR\_HUB\_10 register description**

|                  |   |
|------------------|---|
| SensorHub10[7:0] | Tenth byte associated to external sensors |
|------------------|---|

## 15.11 SENSOR\_HUB\_11 (0Ch)

Sensor hub output register (r)

Eleventh byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 378. SENSOR\_HUB\_11 register**

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Sensor Hub11_7 | Sensor Hub11_6 | Sensor Hub11_5 | Sensor Hub11_4 | Sensor Hub11_3 | Sensor Hub11_2 | Sensor Hub11_1 | Sensor Hub11_0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**Table 379. SENSOR\_HUB\_11 register description**

|                  |  |
|------------------|--|
| SensorHub11[7:0] | Eleventh byte associated to external sensors |
|------------------|--|

## 15.12 SENSOR\_HUB\_12 (0Dh)

Sensor hub output register (r)

Twelfth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 380. SENSOR\_HUB\_12 register**

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Sensor Hub12_7 | Sensor Hub12_6 | Sensor Hub12_5 | Sensor Hub12_4 | Sensor Hub12_3 | Sensor Hub12_2 | Sensor Hub12_1 | Sensor Hub12_0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**Table 381. SENSOR\_HUB\_12 register description**

|                  |   |
|------------------|---|
| SensorHub12[7:0] | Twelfth byte associated to external sensors |
|------------------|---|

### 15.13 SENSOR\_HUB\_13 (0Eh)

Sensor hub output register (r)

Thirteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 382. SENSOR\_HUB\_13 register**

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Sensor Hub13_7 | Sensor Hub13_6 | Sensor Hub13_5 | Sensor Hub13_4 | Sensor Hub13_3 | Sensor Hub13_2 | Sensor Hub13_1 | Sensor Hub13_0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**Table 383. SENSOR\_HUB\_13 register description**

|                  |  |
|------------------|--|
| SensorHub13[7:0] | Thirteenth byte associated to external sensors |
|------------------|--|

### 15.14 SENSOR\_HUB\_14 (0Fh)

Sensor hub output register (r)

Fourteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 384. SENSOR\_HUB\_14 register**

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Sensor Hub14_7 | Sensor Hub14_6 | Sensor Hub14_5 | Sensor Hub14_4 | Sensor Hub14_3 | Sensor Hub14_2 | Sensor Hub14_1 | Sensor Hub14_0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**Table 385. SENSOR\_HUB\_14 register description**

|                  |  |
|------------------|--|
| SensorHub14[7:0] | Fourteenth byte associated to external sensors |
|------------------|--|

### 15.15 SENSOR\_HUB\_15 (10h)

Sensor hub output register (r)

Fifteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 386. SENSOR\_HUB\_15 register**

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Sensor Hub15_7 | Sensor Hub15_6 | Sensor Hub15_5 | Sensor Hub15_4 | Sensor Hub15_3 | Sensor Hub15_2 | Sensor Hub15_1 | Sensor Hub15_0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**Table 387. SENSOR\_HUB\_15 register description**

|                  |   |
|------------------|---|
| SensorHub15[7:0] | Fifteenth byte associated to external sensors |
|------------------|---|

## 15.16 SENSOR\_HUB\_16 (11h)

Sensor hub output register (r)

Sixteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 388. SENSOR\_HUB\_16 register**

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Sensor Hub16_7 | Sensor Hub16_6 | Sensor Hub16_5 | Sensor Hub16_4 | Sensor Hub16_3 | Sensor Hub16_2 | Sensor Hub16_1 | Sensor Hub16_0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**Table 389. SENSOR\_HUB\_16 register description**

|                  |   |
|------------------|---|
| SensorHub16[7:0] | Sixteenth byte associated to external sensors |
|------------------|---|

## 15.17 SENSOR\_HUB\_17 (12h)

Sensor hub output register (r)

Seventeenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 390. SENSOR\_HUB\_17 register**

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Sensor Hub17_7 | Sensor Hub17_6 | Sensor Hub17_5 | Sensor Hub17_4 | Sensor Hub17_3 | Sensor Hub17_2 | Sensor Hub17_1 | Sensor Hub17_0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**Table 391. SENSOR\_HUB\_17 register description**

|                  |   |
|------------------|---|
| SensorHub17[7:0] | Seventeenth byte associated to external sensors |
|------------------|---|

## 15.18 SENSOR\_HUB\_18 (13h)

Sensor hub output register (r)

Eighteenth byte associated to external sensors. The content of the register is consistent with the SLAVEx\_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

**Table 392. SENSOR\_HUB\_18 register**

|                |                |                |                |                |                |                |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Sensor Hub18_7 | Sensor Hub18_6 | Sensor Hub18_5 | Sensor Hub18_4 | Sensor Hub18_3 | Sensor Hub18_2 | Sensor Hub18_1 | Sensor Hub18_0 |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|

**Table 393. SENSOR\_HUB\_18 register description**

|                  |  |
|------------------|--|
| SensorHub18[7:0] | Eighteenth byte associated to external sensors |
|------------------|--|

## 15.19 MASTER\_CONFIG (14h)

Master configuration register (r/w)

**Table 394. MASTER\_CONFIG register**

|                 |            |              |                   |            |           |              |              |
|-----------------|------------|--------------|-------------------|------------|-----------|--------------|--------------|
| RST_MASTER_REGS | WRITE_ONCE | START_CONFIG | PASS_THROUGH_MODE | SHUB_PU_EN | MASTER_ON | AUX_SENS_ON1 | AUX_SENS_ON0 |
|-----------------|------------|--------------|-------------------|------------|-----------|--------------|--------------|

**Table 395. MASTER\_CONFIG register description**

|                   |   |
|-------------------|---|
| RST_MASTER_REGS   | Reset Master logic and output registers. Must be set to '1' and then set it to '0'. Default value: 0  |
| WRITE_ONCE        | Slave 0 write operation is performed only at the first sensor hub cycle.<br>Default value: 0<br>(0: write operation for each sensor hub cycle;<br>1: write operation only for the first sensor hub cycle) |
| START_CONFIG      | Sensor hub trigger signal selection. Default value: 0<br>(0: sensor hub trigger signal is the accelerometer/gyro data-ready;<br>1: sensor hub trigger signal external from INT2 pin)                      |
| PASS_THROUGH_MODE | I <sup>2</sup> C interface pass-through. Default value: 0<br>(0: pass-through disabled;<br>1: pass-through enabled, main I <sup>2</sup> C line is short-circuited with the auxiliary line)                |
| SHUB_PU_EN        | Master I <sup>2</sup> C pull-up enable. Default value: 0<br>(0: internal pull-up on auxiliary I <sup>2</sup> C line disabled;<br>1: internal pull-up on auxiliary I <sup>2</sup> C line enabled)          |
| MASTER_ON         | Sensor hub I <sup>2</sup> C master enable. Default: 0<br>(0: master I <sup>2</sup> C of sensor hub disabled; 1: master I <sup>2</sup> C of sensor hub enabled)  |
| AUX_SENS_ON[1:0]  | Number of external sensors to be read by the sensor hub.<br>(00: one sensor (default);<br>01: two sensors;<br>10: three sensors;<br>11: four sensors)   |

## 15.20 SLV0\_ADD (15h)

I<sup>2</sup>C slave address of the first external sensor (Sensor 1) register (r/w)

**Table 396. SLV0\_ADD register**

|             |             |             |             |             |             |             |      |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------|
| slave0_add6 | slave0_add5 | slave0_add4 | slave0_add3 | slave0_add2 | slave0_add1 | slave0_add0 | rw_0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------|

**Table 397. SLV0\_ADD register description**

|                 |   |
|-----------------|---|
| slave0_add[6:0] | I <sup>2</sup> C slave address of Sensor1 that can be read by the sensor hub.<br>Default value: 0000000 |
| rw_0            | Read/write operation on Sensor 1. Default value: 0<br>(0: write operation; 1: read operation)           |

## 15.21 SLV0\_SUBADD (16h)

Address of register on the first external sensor (Sensor 1) register (r/w)

**Table 398. SLV0\_SUBADD register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| slave0_reg7 | slave0_reg6 | slave0_reg5 | slave0_reg4 | slave0_reg3 | slave0_reg2 | slave0_reg1 | slave0_reg0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 399. SLV0\_SUBADD register description**

|                 |   |
|-----------------|---|
| slave0_reg[7:0] | Address of register on Sensor1 that has to be read/written according to the rw_0 bit value in <b>SLV0_ADD (15h)</b> . Default value: 00000000 |
|-----------------|---|

## 15.22 SLAVE0\_CONFIG (17h)

First external sensor (Sensor1) configuration and sensor hub settings register (r/w)

**Table 400. SLAVE0\_CONFIG register**

|            |            |                  |                  |                     |               |               |               |
|------------|------------|------------------|------------------|---------------------|---------------|---------------|---------------|
| SHUB_ODR_1 | SHUB_ODR_0 | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | BATCH_EXT_SENS_0_EN | Slave0_numop2 | Slave0_numop1 | Slave0_numop0 |
|------------|------------|------------------|------------------|---------------------|---------------|---------------|---------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 401. SLAVE0\_CONFIG register description**

|                     |  |
|---------------------|--|
| SHUB_ODR_[1:0]      | Rate at which the master communicates. Default value: 00<br>(00: 104 Hz (or at the maximum ODR between the accelerometer and gyro if it is less than 104 Hz);<br>01: 52 Hz (or at the maximum ODR between the accelerometer and gyro if it is less than 52 Hz);<br>10: 26 Hz (or at the maximum ODR between the accelerometer and gyro if it is less than 26 Hz);<br>11: 12.5 Hz (or at the maximum ODR between the accelerometer and gyro if it is less than 12.5 Hz) |
| BATCH_EXT_SENS_0_EN | Enable FIFO data batching of first slave. Default value: 0   |
| Slave0_numop[2:0]   | Number of read operations on Sensor 1. Default value: 000  |



### 15.23 SLV1\_ADD (18h)

I<sup>2</sup>C slave address of the second external sensor (Sensor 2) register (r/w)

**Table 402. SLV1\_ADD register**

|             |             |             |             |             |             |             |     |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|
| Slave1_add6 | Slave1_add5 | Slave1_add4 | Slave1_add3 | Slave1_add2 | Slave1_add1 | Slave1_add0 | r_1 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|

**Table 403. SLV1\_ADD register description**

|                 |  |
|-----------------|--|
| Slave1_add[6:0] | I <sup>2</sup> C slave address of Sensor 2 that can be read by the sensor hub.<br>Default value: 0000000       |
| r_1             | Read operation on Sensor 2 enable. Default value: 0<br>(0: read operation disabled; 1: read operation enabled) |

### 15.24 SLV1\_SUBADD (19h)

Address of register on the second external sensor (Sensor 2) register (r/w)

**Table 404. SLV1\_SUBADD register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Slave1_reg7 | Slave1_reg6 | Slave1_reg5 | Slave1_reg4 | Slave1_reg3 | Slave1_reg2 | Slave1_reg1 | Slave1_reg0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 405. SLV1\_SUBADD register description**

|                 |   |
|-----------------|---|
| Slave1_reg[7:0] | Address of register on Sensor 2 that has to be read/written according to the r_1 bit value in SLV1_ADD (18h). |
|-----------------|---|

### 15.25 SLAVE1\_CONFIG (1Ah)

Second external sensor (Sensor 2) configuration register (r/w)

**Table 406. SLAVE1\_CONFIG register**

|                  |                  |                  |                  |                     |               |               |               |
|------------------|------------------|------------------|------------------|---------------------|---------------|---------------|---------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | BATCH_EXT_SENS_1_EN | Slave1_numop2 | Slave1_numop1 | Slave1_numop0 |
|------------------|------------------|------------------|------------------|---------------------|---------------|---------------|---------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 407. SLAVE1\_CONFIG register description**

|                     |   |
|---------------------|---|
| BATCH_EXT_SENS_1_EN | Enable FIFO data batching of second slave. Default value: 0 |
| Slave1_numop[2:0]   | Number of read operations on Sensor 2. Default value: 000   |

## 15.26 SLV2\_ADD (1Bh)

I<sup>2</sup>C slave address of the third external sensor (Sensor 3) register (r/w)

**Table 408. SLV2\_ADD register**

|             |             |             |             |             |             |             |     |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|
| Slave2_add6 | Slave2_add5 | Slave2_add4 | Slave2_add3 | Slave2_add2 | Slave2_add1 | Slave2_add0 | r_2 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|

**Table 409. SLV2\_ADD register description**

|                 |  |
|-----------------|--|
| Slave2_add[6:0] | I <sup>2</sup> C slave address of Sensor 3 that can be read by the sensor hub.                                 |
| r_2             | Read operation on Sensor 3 enable. Default value: 0<br>(0: read operation disabled; 1: read operation enabled) |

## 15.27 SLV2\_SUBADD (1Ch)

Address of register on the third external sensor (Sensor 3) register (r/w)

**Table 410. SLV2\_SUBADD register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Slave2_reg7 | Slave2_reg6 | Slave2_reg5 | Slave2_reg4 | Slave2_reg3 | Slave2_reg2 | Slave2_reg1 | Slave2_reg0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 411. SLV2\_SUBADD register description**

|                 |   |
|-----------------|---|
| Slave2_reg[7:0] | Address of register on Sensor 3 that has to be read/written according to the r_2 bit value in SLV2_ADD (1Bh). |
|-----------------|---|

## 15.28 SLAVE2\_CONFIG (1Dh)

Third external sensor (Sensor 3) configuration register (r/w)

**Table 412. SLAVE2\_CONFIG register**

|                  |                  |                  |                  |                     |               |               |               |
|------------------|------------------|------------------|------------------|---------------------|---------------|---------------|---------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | BATCH_EXT_SENS_2_EN | Slave2_numop2 | Slave2_numop1 | Slave2_numop0 |
|------------------|------------------|------------------|------------------|---------------------|---------------|---------------|---------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 413. SLAVE2\_CONFIG register description**

|                     |  |
|---------------------|--|
| BATCH_EXT_SENS_2_EN | Enable FIFO data batching of third slave. Default value: 0 |
| Slave2_numop[2:0]   | Number of read operations on Sensor 3. Default value: 000  |

## 15.29 SLV3\_ADD (1Eh)

I<sup>2</sup>C slave address of the fourth external sensor (Sensor 4) register (r/w)

**Table 414. SLV3\_ADD register**

|             |             |             |             |             |             |             |     |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|
| Slave3_add6 | Slave3_add5 | Slave3_add4 | Slave3_add3 | Slave3_add2 | Slave3_add1 | Slave3_add0 | r_3 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|

**Table 415. SLV3\_ADD register description**

|                 |  |
|-----------------|--|
| Slave3_add[6:0] | I <sup>2</sup> C slave address of Sensor 4 that can be read by the sensor hub.                                 |
| r_3             | Read operation on Sensor 4 enable. Default value: 0<br>(0: read operation disabled; 1: read operation enabled) |

## 15.30 SLV3\_SUBADD (1Fh)

Address of register on the fourth external sensor (Sensor 4) register (r/w)

**Table 416. SLV3\_SUBADD register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Slave3_reg7 | Slave3_reg6 | Slave3_reg5 | Slave3_reg4 | Slave3_reg3 | Slave3_reg2 | Slave3_reg1 | Slave3_reg0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|

**Table 417. SLV3\_SUBADD register description**

|                 |  |
|-----------------|--|
| Slave3_reg[7:0] | Address of register on Sensor 4 that has to be read according to the r_3 bit value in <a href="#">SLV3_ADD (1Eh)</a> . |
|-----------------|--|

## 15.31 SLAVE3\_CONFIG (20h)

Fourth external sensor (Sensor 4) configuration register (r/w)

**Table 418. SLAVE3\_CONFIG register**

|                  |                  |                  |                  |                     |               |               |               |
|------------------|------------------|------------------|------------------|---------------------|---------------|---------------|---------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | BATCH_EXT_SENS_3_EN | Slave3_numop2 | Slave3_numop1 | Slave3_numop0 |
|------------------|------------------|------------------|------------------|---------------------|---------------|---------------|---------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 419. SLAVE3\_CONFIG register description**

|                     |   |
|---------------------|---|
| BATCH_EXT_SENS_3_EN | Enable FIFO data batching of fourth slave. Default value: 0 |
| Slave3_numop[2:0]   | Number of read operations on Sensor 4. Default value: 000   |

### 15.32 DATAWRITE\_SLV0 (21h)

Data to be written into the slave device register (r/w)

**Table 420. DATAWRITE\_SLV0 register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Slave0_dataw7 | Slave0_dataw6 | Slave0_dataw5 | Slave0_dataw4 | Slave0_dataw3 | Slave0_dataw2 | Slave0_dataw1 | Slave0_dataw0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

**Table 421. DATAWRITE\_SLV0 register description**

|                   |  |
|-------------------|--|
| Slave0_dataw[7:0] | Data to be written into the slave 0 device according to the rw_0 bit in register <a href="#">SLV0_ADD (15h)</a> .<br>Default value: 00000000 |
|-------------------|--|

### 15.33 STATUS\_MASTER (22h)

Sensor hub source register (r)

**Table 422. STATUS\_MASTER register**

|              |             |             |             |             |   |   |                |
|--------------|-------------|-------------|-------------|-------------|---|---|----------------|
| WR_ONCE_DONE | SLAVE3_NACK | SLAVE2_NACK | SLAVE1_NACK | SLAVE0_NACK | 0 | 0 | SENS_HUB_ENDOP |
|--------------|-------------|-------------|-------------|-------------|---|---|----------------|

**Table 423. STATUS\_MASTER register description**

|                |  |
|----------------|--|
| WR_ONCE_DONE   | When the bit WRITE_ONCE in <a href="#">MASTER_CONFIG (14h)</a> is configured as 1, this bit is set to 1 when the write operation on slave 0 has been performed and completed. Default value: 0 |
| SLAVE3_NACK    | This bit is set to 1 if Not acknowledge occurs on slave 3 communication. Default value: 0  |
| SLAVE2_NACK    | This bit is set to 1 if Not acknowledge occurs on slave 2 communication. Default value: 0  |
| SLAVE1_NACK    | This bit is set to 1 if Not acknowledge occurs on slave 1 communication. Default value: 0  |
| SLAVE0_NACK    | This bit is set to 1 if Not acknowledge occurs on slave 0 communication. Default value: 0  |
| SENS_HUB_ENDOP | Sensor hub communication status. Default value: 0<br>(0: sensor hub communication not concluded;<br>1: sensor hub communication concluded)   |

## 16 Soldering information

---

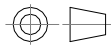
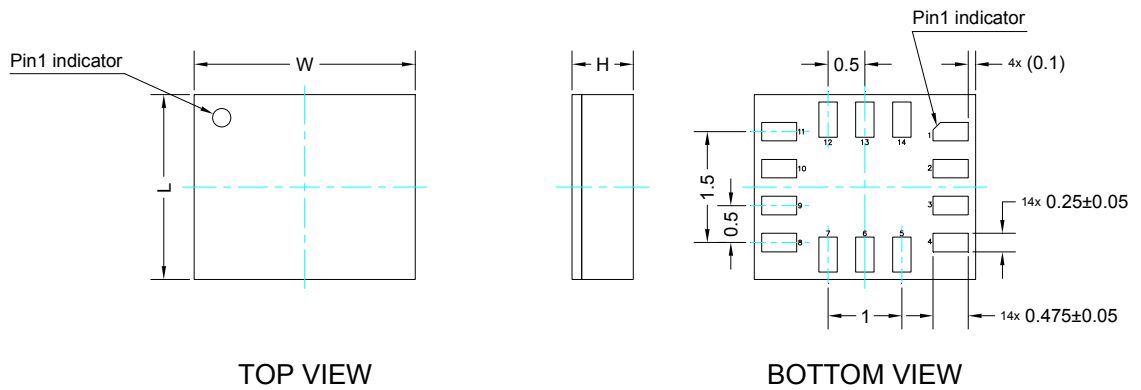
The LGA package is compliant with the [ECOPACK](#), RoHS and "Green" standard.  
It is qualified for soldering heat resistance according to JEDEC J-STD-020.  
Land pattern and soldering recommendations are available at [www.st.com/mems](http://www.st.com/mems).

## 17 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 17.1 LGA-14L package information

**Figure 27. LGA-14L 2.5 x 3.0 x 0.86 mm package outline and mechanical data**



Dimensions are in millimeter unless otherwise specified  
General tolerance is  $\pm 0.1$  mm unless otherwise specified

#### OUTER DIMENSIONS

| ITEM       | DIMENSION [mm] | TOLERANCE [mm] |
|------------|----------------|----------------|
| Length [L] | 2.50           | $\pm 0.1$      |
| Width [W]  | 3.00           | $\pm 0.1$      |
| Height [H] | 0.86           | MAX            |

DM00249496\_1

## 17.2 LGA-14 packing information

Figure 28. Carrier tape information for LGA-14 package

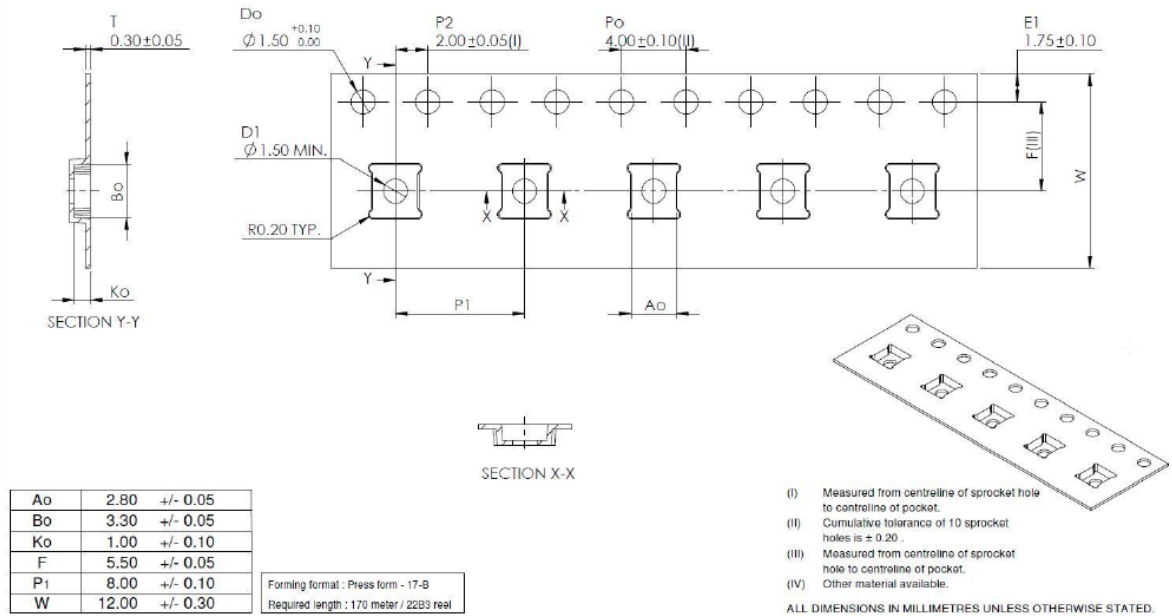


Figure 29. LGA-14 package orientation in carrier tape

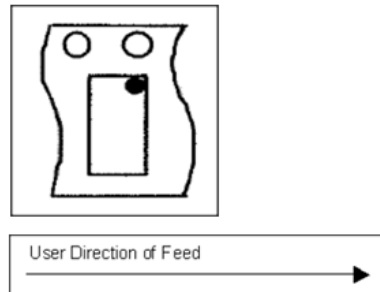


Figure 30. Reel information for carrier tape of LGA-14 package

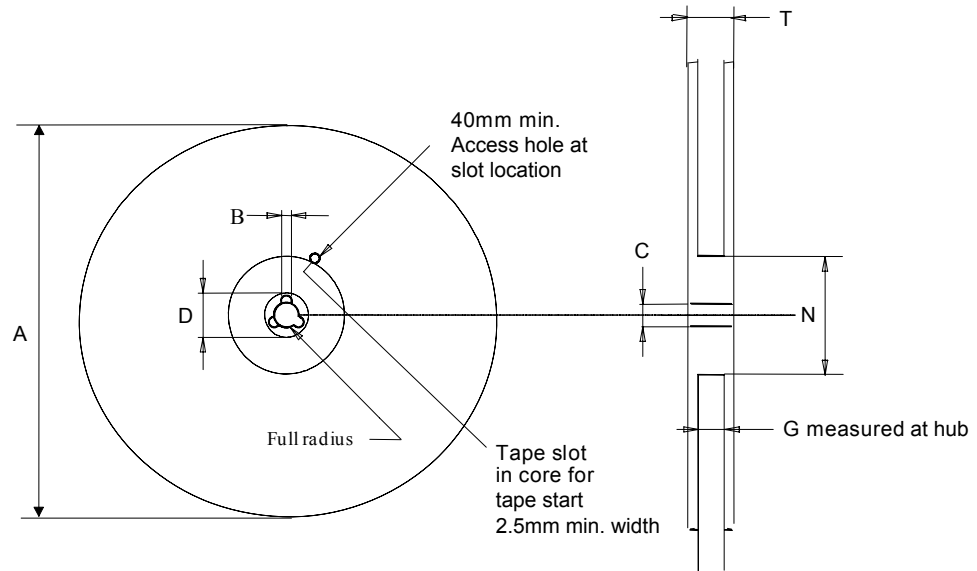


Table 424. Reel dimensions for carrier tape of LGA-14 package

| Reel dimensions (mm) |            |
|----------------------|------------|
| A (max)              | 330        |
| B (min)              | 1.5        |
| C                    | 13 ±0.25   |
| D (min)              | 20.2       |
| N (min)              | 60         |
| G                    | 12.4 +2/-0 |
| T (max)              | 18.4       |



## Revision history

**Table 425. Document revision history**

| Date        | Version | Changes  |
|-------------|---------|--|
| 19-Sep-2019 | 1       | Initial release  |
| 12-Mar-2020 | 2       | Updated title of datasheet, Descripton, added Product resources<br>Updated Table 6. I <sup>2</sup> C slave timing values<br>Updated description of bit 7 in TAP_THS_6D (59h)<br>Updated bit 0 in I3C_BUS_AVB (62h)<br>Updated PEDO_CMD_REG (83h)   |
| 18-Nov-2020 | 3       | Updated linear acceleration self-test output change in <a href="#">Table 2. Mechanical characteristics</a><br>Updated Note below <a href="#">Figure 6</a> and <a href="#">Figure 7</a><br>Updated <a href="#">Table 50. Accelerometer ODR selection</a><br>Updated description of bits in INT_DUR2 (5Ah) |

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