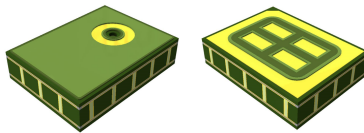


## MEMS audio sensor omnidirectional digital microphone



HCLGA - 4LD (3 x 4 x 1 mm)

### Features

- Single supply voltage
- Low power consumption
- AOP = 122.5 dB SPL
- 64 dB signal-to-noise ratio
- Omnidirectional sensitivity
- -26 dBFS  $\pm$  1 dB sensitivity
- PDM output
- HCLGA package
  - Top-port design
  - SMD-compliant
  - EMI-shielded
  - ECOPACK, RoHS, and "Green" compliant

### Applications

- Mobile terminals
- Laptop and notebook computers
- Portable media players
- VoIP
- Speech recognition
- A/V eLearning devices
- Gaming and virtual reality input devices
- Digital still and video cameras
- Antitheft systems

### Description

The **MP34DT06J** is an ultra-compact, low-power, omnidirectional, digital MEMS microphone built with a capacitive sensing element and an IC interface.

The sensing element, capable of detecting acoustic waves, is manufactured using a specialized silicon micromachining process dedicated to producing audio sensors.

The IC interface is manufactured using a CMOS process that allows designing a dedicated circuit able to provide a digital signal externally in PDM format.

The **MP34DT06J** is a low-distortion digital microphone with a 64 dB signal-to-noise ratio and -26 dBFS  $\pm$  1 dB sensitivity.

The **MP34DT06J** is available in a top-port, SMD-compliant, EMI-shielded package and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

| Product status link           |                              |
|-------------------------------|------------------------------|
| <a href="#">MP34DT06J</a>     |                              |
| Product summary               |                              |
| <b>Order code</b>             | MP34DT06JTR                  |
| <b>Temperature range [°C]</b> | -40 °C to +85                |
| <b>Package</b>                | HCLGA 4 LD<br>(3 x 4 x 1 mm) |
| <b>Packing</b>                | Tape and reel                |

# 1 Pin description

Figure 1. Pin connections

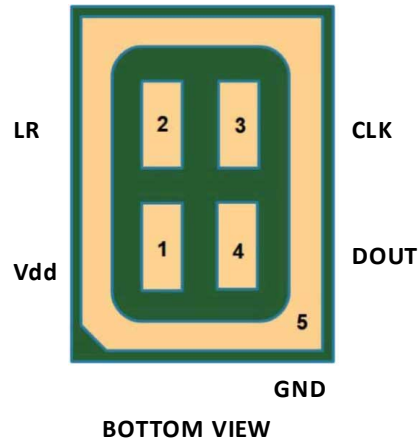


Table 1. Pin description

| Pin #              | Pin name | Function                     |
|--------------------|----------|------------------------------|
| 1                  | Vdd      | Power supply                 |
| 2                  | LR       | Left/Right channel selection |
| 3                  | CLK      | Synchronization input clock  |
| 4                  | DOUT     | Left/Right PDM data output   |
| 5<br>(ground ring) | GND      | Ground                       |

## 2 Acoustic and electrical specifications

### 2.1 Acoustic and electrical characteristics

The values listed in the table below are specified for Vdd = 1.8 V, Clock = 2.4 MHz, T = 25 °C, unless otherwise noted.

**Table 2. Acoustic and electrical characteristics**

| Symbol            | Parameter   | Test condition                                 | Min.     | Typ. <sup>(1)</sup> | Max.     | Unit   |
|-------------------|---|--|----------|---------------------|----------|--------|
| Vdd               | Supply voltage  |  | 1.6      | 1.8                 | 3.6      | V      |
| Idd               | Current consumption in normal mode                    | Mean value                                     |          | 650                 |          | μA     |
| IddPdn            | Current consumption in power-down mode <sup>(2)</sup> |  |          |                     | 5        | μA     |
| Sc                | Short-circuit current                                 |  | 1        |                     | 10       | mA     |
| AOP               | Acoustic overload point                               |  |          | 122.5               |          | dB SPL |
| So                | Sensitivity   |  | -27      | -26                 | -25      | dBFS   |
| SNR               | Signal-to-noise ratio                                 | A-weighted @1 kHz, 94 dB SPL                   |          | 64                  |          | dB(A)  |
| PSR               | Power supply rejection                                | 100 mVpp sine 1 kHz                            |          | -90                 |          | dBFS   |
| Clock             | Input clock frequency <sup>(3)</sup>                  |  | 1.2      | 2.4                 | 3.25     | MHz    |
| Ton               | Turn-on time <sup>(4)</sup>                           | Specified by design - not tested in production |          |                     | 10       | ms     |
| Top               | Operating temperature range                           |  | -40      |                     | +85      | °C     |
| V <sub>IOL</sub>  | Low-level logic input/output voltage                  | I <sub>out</sub> = 1 mA                        | -0.3     |                     | 0.35xVdd | V      |
| V <sub>IOH</sub>  | High-level logic input/output voltage                 | I <sub>out</sub> = 1 mA                        | 0.65xVdd |                     | Vdd+0.3  | V      |
| C <sub>LOAD</sub> | Capacitive load                                       |  |          |                     | 100      | pF     |

1. Typical specifications are not guaranteed.
2. Input clock in static mode.
3. Duty cycle: min = 40% max = 60%.
4. Time from the first clock edge to valid output data.

**Table 3. Distortion specifications @ 1 kHz**

| Parameter  | Test condition | Typical value <sup>(1)</sup> |
|------------|----------------|------------------------------|
| Distortion | 94 dB SPL      | 0.2% THD + N                 |
| Distortion | 110 dB SPL     | 0.7% THD + N                 |
| Distortion | 120 dB SPL     | 6% THD + N                   |

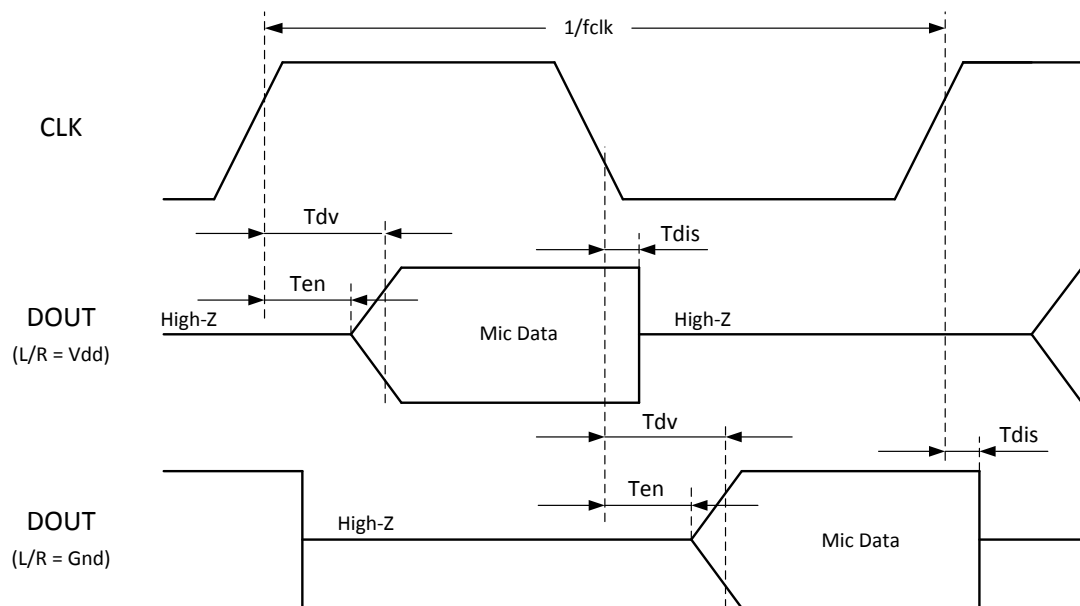
1. Typical specifications are not guaranteed.

## 2.2 Timing characteristics

**Table 4. Timing characteristics**

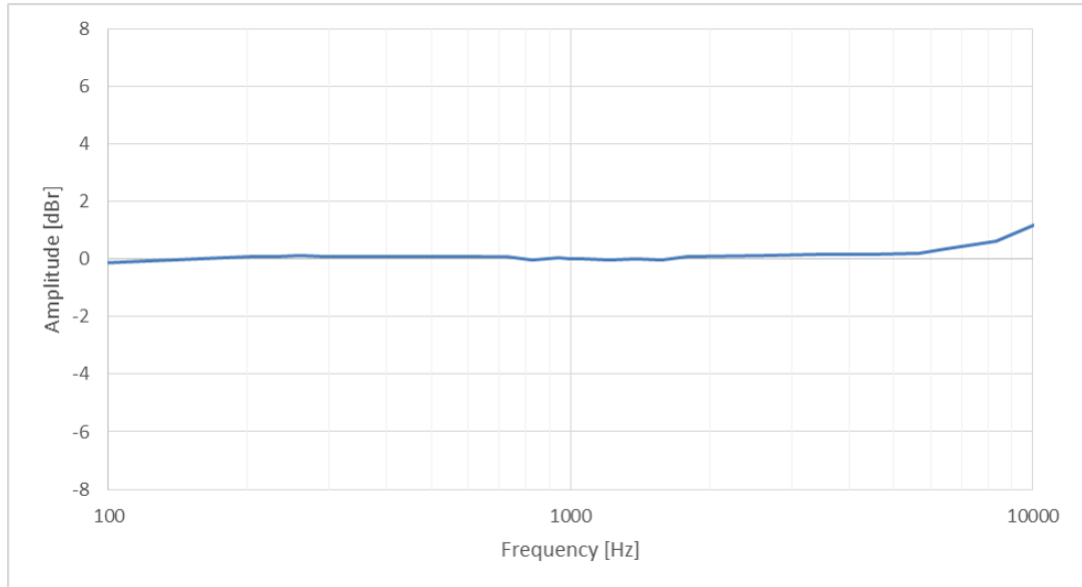
| Parameter | Description                                     | Min. | Max. | Unit |
|-----------|---|------|------|------|
| $f_{CLK}$ | Clock frequency for normal mode                 | 1.2  | 3.25 | MHz  |
| $f_{PD}$  | Clock frequency for power-down mode             |      | 0.23 | MHz  |
| $T_{CLK}$ | Clock period for normal mode                    | 308  | 1000 | ns   |
| $T_{dv}$  | Time delay to valid data ( $C_{LOAD} = 100$ pF) | -    | 105  |      |
| $T_{en}$  | Time delay to driven data                       | 18   | -    |      |
| $T_{dis}$ | Time delay to High-Z                            | 2    | 10   |      |

**Figure 2. Timing waveforms**



### 2.3 Frequency response

**Figure 3.** Typical frequency response normalized to 1 kHz



### 3 Application recommendations

Figure 4. MP34DT06J electrical connections (top view)

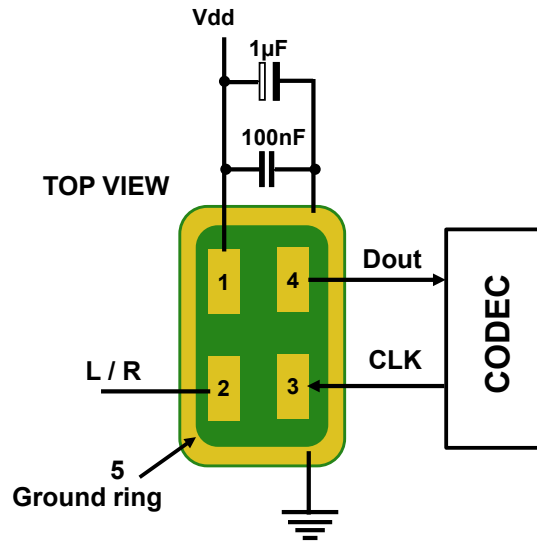
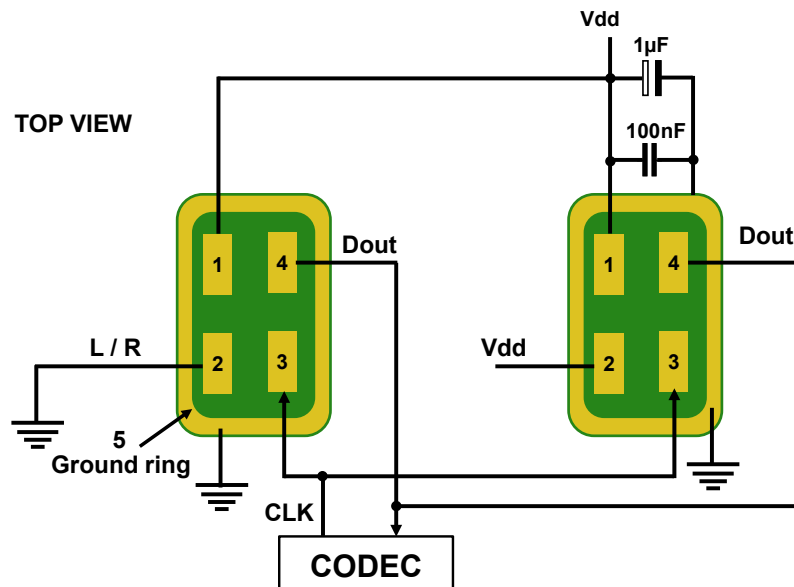


Figure 5. MP34DT06J electrical connections for stereo configuration (top view)



Power supply decoupling capacitors (100 nF ceramic, 1 µF ceramic) should be placed as near as possible to pin 1 of the device (common design practice).

The L/R pin must be connected to Vdd or GND (refer to [Table 6. L/R channel selection](#)).

## 4 Carrier tape mechanical specifications

Figure 6. Carrier tape without microphone (top view)

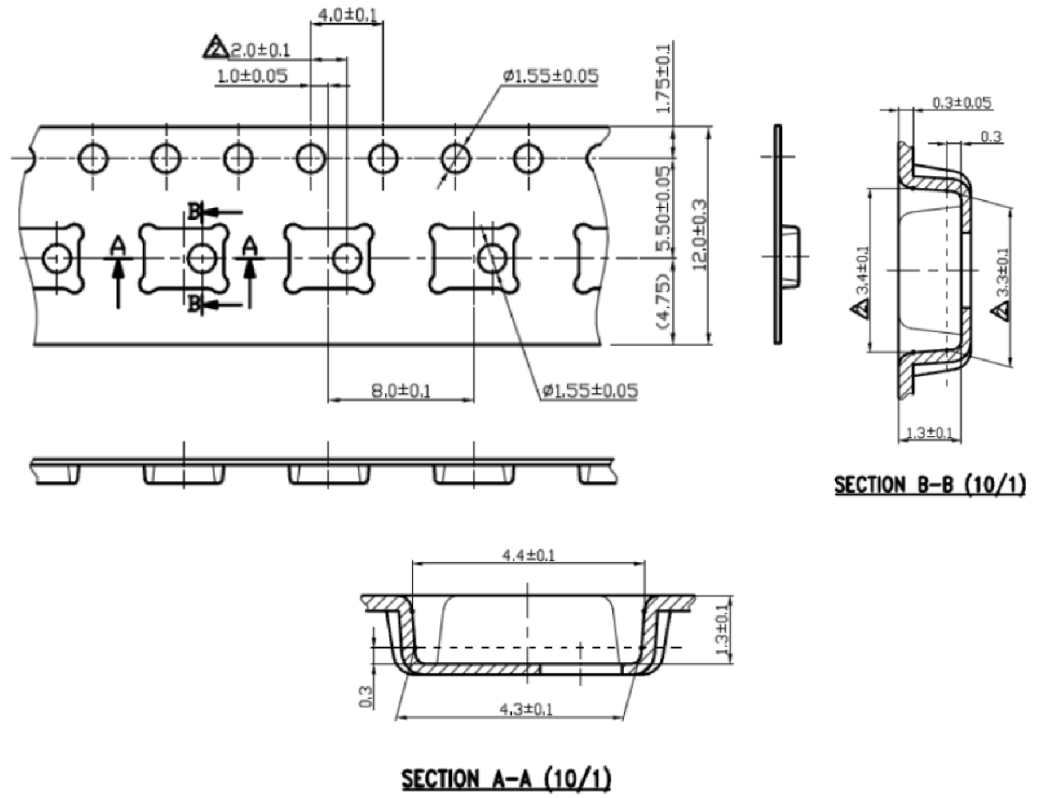
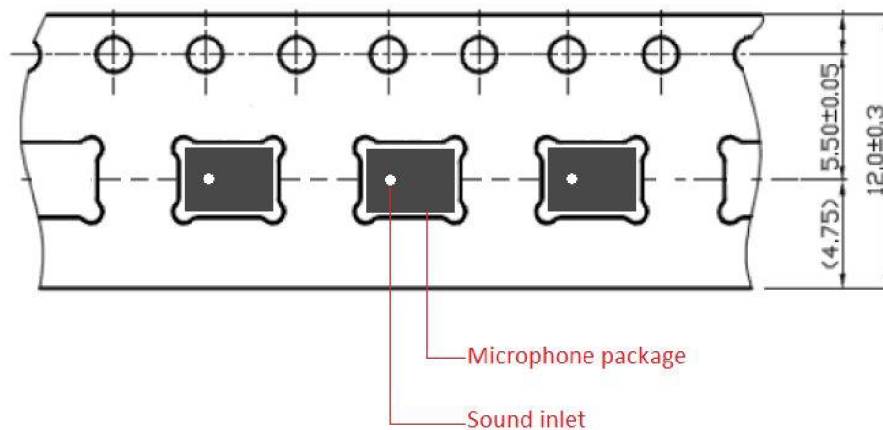


Figure 7. Carrier tape with microphone (top view)

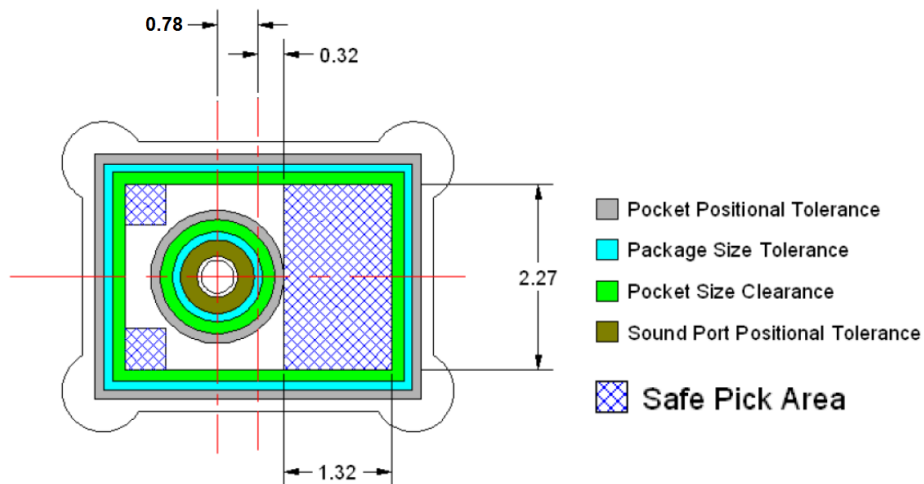


## 5 Process recommendations

To ensure a consistent manufacturing process it is strongly advised to comply with the following recommendations:

- The recommended pick-up area for the MP34DT06J package must be defined using the worst case (ie. no device alignment during picking process). This area has been defined considering all the tolerances of the components involved (reel, package, sound inlet). The picker tolerance shall be considered as well.
- To prevent damage to the MEMS membrane or incorrect pick-up and placement, do not pick up the component on the inlet area.
- For the package outline please refer to [Figure 7. Carrier tape with microphone \(top view\)](#). Nozzle shape, size, and placement accuracy are the other key factors to consider when deciding on the coordinates for picking.
- Device alignment before picking is highly recommended.
- A vacuum force greater than 7 psi must be avoided
- $1 \text{ kPa} = 0.145 \text{ psi (lb/in}^2\text{)} = 0.0102 \text{ kgf/cm}^2 = 0.0098 \text{ atm}$
- MSL (moisture sensitivity level) Class 3
- Maximum of 3 reflow cycles is recommended
- All recommended dimensions (device safe-picking area) do not include the pick-and-place equipment tolerances

Figure 8. Recommended picking area

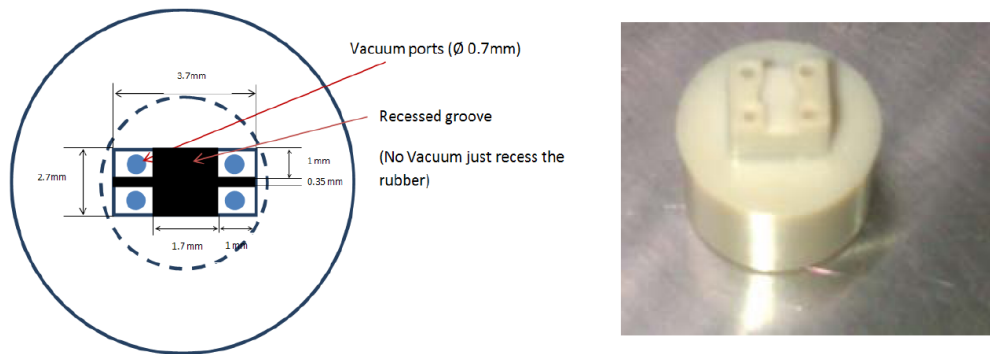


To have a safe pick-up “by design”, ST strongly advises an ad hoc nozzle.

The following picker ensures that the holes for the vacuum and the air stream are ALWAYS away from the porthole of the device (4 vacuum ports located at each corner of the device). The recommended nozzle also has a recess in the form of a cross which guarantees that the porthole is always left at atmospheric pressure. By using the recommended nozzle, the membrane will not suffer any sudden air disturbances during the picking or placing of the devices in the tape and reel.



Figure 9. Recommended picker design



## **6 Sensing element**

---

The sensing element shall mean the acoustic sensor consisting of a conductive movable plate and a fixed plate placed in a tiny silicon chip. This sensor transduces the sound pressure into the changes of coupled capacity between those two plates.

## 7 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 5. Absolute maximum ratings**

| Symbol           | Ratings   | Maximum value                | Unit |
|------------------|---|------------------------------|------|
| V <sub>dd</sub>  | Supply voltage                                    | -0.3 to 5                    | V    |
| V <sub>in</sub>  | Input voltage on any control pin                  | -0.3 to V <sub>dd</sub> +0.3 | V    |
| T <sub>STG</sub> | Storage temperature range                         | -40 to +125                  | °C   |
| ESD              | Electrostatic discharge protection                | ±2000 (HBM)                  | V    |
|                  |   | ±200 (MM)                    |      |
|                  |   | ±750 (CBM)                   |      |
| ESD              | Product standard EN 55024:2010 - 3 air discharges | ±15000                       | V    |



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

## 8 Functionality

### 8.1 L/R channel selection

The L/R digital pad lets the user select the DOUT signal pattern as shown in the following table. The L/R pin must be connected to Vdd or GND.

**Table 6. L/R channel selection**

| L/R | CLK low        | CLK high       |
|-----|----------------|----------------|
| GND | Data valid     | High impedance |
| Vdd | High impedance | Data valid     |

*Note: As the L/R pin is internally connected to GND via a 200 kohm pull-down resistor, it is not mandatory to connect the pin itself to GND for the respective channel selection.*

## 9 Package information

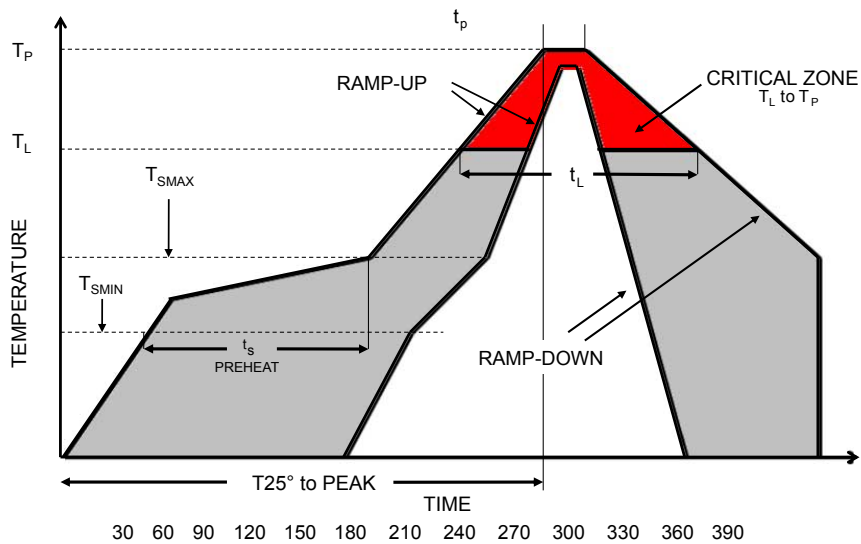
In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 9.1 Soldering information

The HCLGA (3 x 4) 4LD package is also compliant with the RoHS and “Green” standards and is qualified for soldering heat resistance according to JEDEC J-STD-020.

Landing pattern and soldering recommendations are available at [www.st.com](http://www.st.com).

**Figure 10. Recommended soldering profile limits**

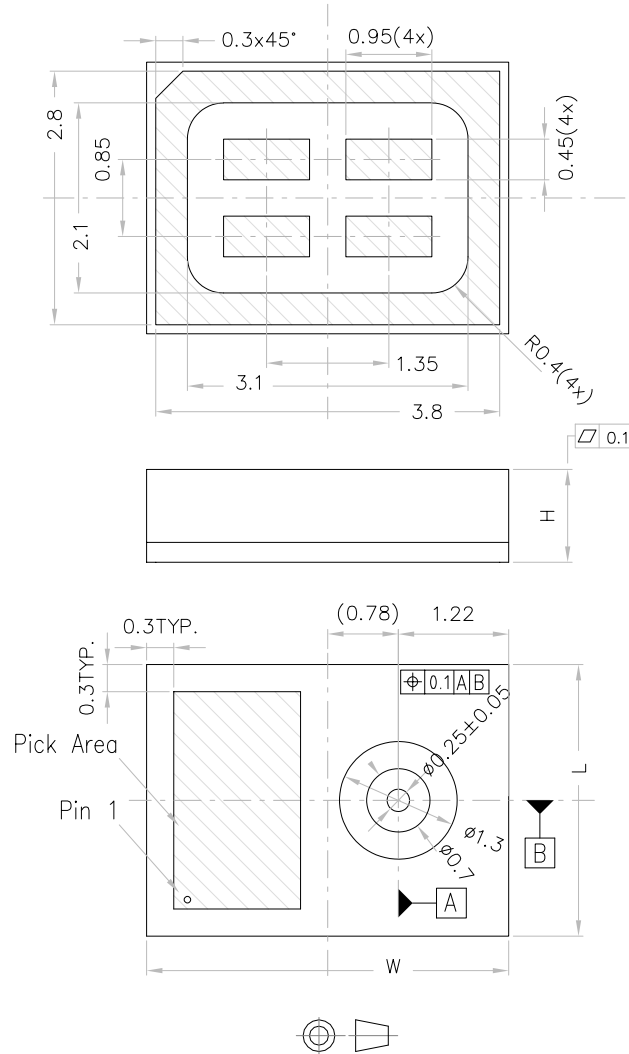


**Table 7. Recommended soldering profile limits**

| Description   | Parameter           | Pb free           |
|---|---------------------|-------------------|
| Average ramp rate                                     | $T_L$ to $T_P$      | 3 °C/sec max      |
| Preheat   |                     |                   |
| Minimum temperature                                   | $T_{SMIN}$          | 150 °C            |
| Maximum temperature                                   | $T_{SMAX}$          | 200 °C            |
| Time ( $T_{SMIN}$ to $T_{SMAX}$ )                     | $t_s$               | 60 sec to 120 sec |
| Ramp-up rate  | $T_{SMAX}$ to $T_L$ |                   |
| Time maintained above liquidus temperature            | $t_L$               | 60 sec to 150 sec |
| Liquidus temperature                                  | $T_L$               | 217 °C            |
| Peak temperature                                      | $T_P$               | 260 °C max        |
| Time within 5 °C of actual peak temperature           |                     | 20 sec to 40 sec  |
| Ramp-down rate  |                     | 6 °C/sec max      |
| Time 25 °C ( $t_{25\text{ °C}}$ ) to peak temperature |                     | 8 minutes max     |

## 9.2 HCLGA package information

**Figure 11. HCLGA (3 x 4 x 1 mm) 4-lead package outline and mechanical data**



Dimensions are in millimeter unless otherwise specified  
General Tolerance is  $\pm 0.15$  mm unless otherwise specified

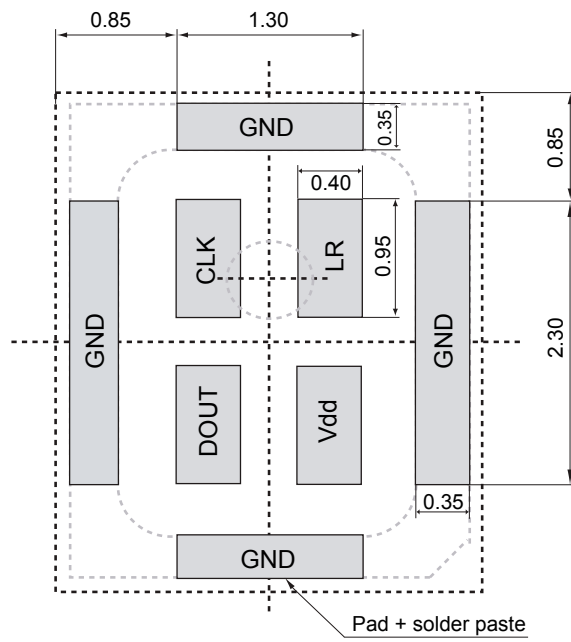
DM00231908\_5

**Table 8. Outer dimensions**

| Item       | Dimensions (mm)    | Tolerance (mm) |
|------------|--------------------|----------------|
| Length (L) | 3                  | $\pm 0.1$      |
| Width (W)  | 4                  | $\pm 0.1$      |
| Height (H) | 1.00               | $\pm 0.1$      |
| AP         | $\varnothing 0.25$ | $\pm 0.05$     |

1. The MEMS microphone plastic cap can exhibit some level of variation in color when the device is subjected to thermal processes. This variation does not affect acoustic or electrical performance.
2. Ring plating can be subject to change not affecting acoustic and electrical performance.

**Figure 12. Land pattern**



## Revision history

**Table 9. Document revision history**

| Date        | Version | Changes  |
|-------------|---------|--|
| 17-Jul-2018 | 1       | Initial release  |
| 29-Apr-2019 | 2       | Updated Table 4. Timing characteristics<br>Added Figure 12. Land pattern |
| 30-Jun-2021 | 3       | Updated <a href="#">Section 2.2</a> Timing characteristics               |



## Contents

|          |   |           |
|----------|---|-----------|
| <b>1</b> | <b>Pin description</b>                        | <b>2</b>  |
| <b>2</b> | <b>Acoustic and electrical specifications</b> | <b>3</b>  |
| 2.1      | Acoustic and electrical characteristics       | 3         |
| 2.2      | Timing characteristics                        | 4         |
| 2.3      | Frequency response                            | 5         |
| <b>3</b> | <b>Application recommendations</b>            | <b>6</b>  |
| <b>4</b> | <b>Carrier tape mechanical specifications</b> | <b>7</b>  |
| <b>5</b> | <b>Process recommendations</b>                | <b>8</b>  |
| <b>6</b> | <b>Sensing element</b>                        | <b>10</b> |
| <b>7</b> | <b>Absolute maximum ratings</b>               | <b>11</b> |
| <b>8</b> | <b>Functionality</b>                          | <b>12</b> |
| 8.1      | L/R channel selection                         | 12        |
| <b>9</b> | <b>Package information</b>                    | <b>13</b> |
| 9.1      | Soldering information                         | 13        |
| 9.2      | HCLGA package information                     | 14        |
|          | <b>Revision history</b>                       | <b>16</b> |

## List of tables

|                 |   |    |
|-----------------|---|----|
| <b>Table 1.</b> | Pin description . . . . .                         | 2  |
| <b>Table 2.</b> | Acoustic and electrical characteristics . . . . . | 3  |
| <b>Table 3.</b> | Distortion specifications @ 1 kHz . . . . .       | 3  |
| <b>Table 4.</b> | Timing characteristics . . . . .                  | 4  |
| <b>Table 5.</b> | Absolute maximum ratings . . . . .                | 11 |
| <b>Table 6.</b> | L/R channel selection . . . . .                   | 12 |
| <b>Table 7.</b> | Recommended soldering profile limits . . . . .    | 13 |
| <b>Table 8.</b> | Outer dimensions . . . . .                        | 14 |
| <b>Table 9.</b> | Document revision history . . . . .               | 16 |

## List of figures

|                   |  |    |
|-------------------|--|----|
| <b>Figure 1.</b>  | Pin connections . . . . .  | 2  |
| <b>Figure 2.</b>  | Timing waveforms . . . . .   | 4  |
| <b>Figure 3.</b>  | Typical frequency response normalized to 1 kHz . . . . .                       | 5  |
| <b>Figure 4.</b>  | MP34DT06J electrical connections (top view) . . . . .                          | 6  |
| <b>Figure 5.</b>  | MP34DT06J electrical connections for stereo configuration (top view) . . . . . | 6  |
| <b>Figure 6.</b>  | Carrier tape without microphone (top view) . . . . .                           | 7  |
| <b>Figure 7.</b>  | Carrier tape with microphone (top view) . . . . .                              | 7  |
| <b>Figure 8.</b>  | Recommended picking area . . . . .   | 8  |
| <b>Figure 9.</b>  | Recommended picker design . . . . .  | 9  |
| <b>Figure 10.</b> | Recommended soldering profile limits . . . . .                                 | 13 |
| <b>Figure 11.</b> | HCLGA (3 x 4 x 1 mm) 4-lead package outline and mechanical data . . . . .      | 14 |
| <b>Figure 12.</b> | Land pattern . . . . .   | 15 |

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