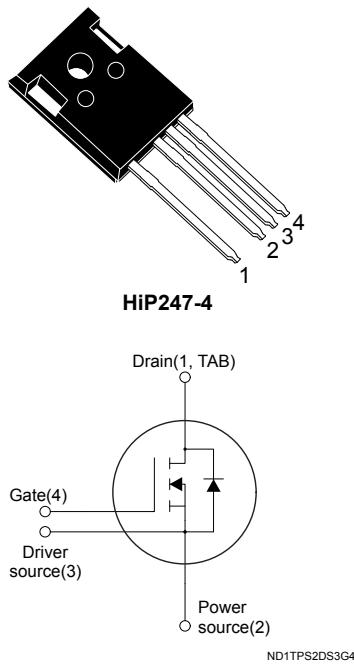


Silicon carbide Power MOSFET 650 V, 18 mΩ typ., 119 A in an HiP247-4 package



Features

Order code	V _{DS}	R _{D(on)} max.	I _D
SCTWA90N65G2V-4	650 V	24 mΩ	119 A

- High speed switching performance
- Very high operating junction temperature capability ($T_J = 200 \text{ }^{\circ}\text{C}$)
- Very fast and robust intrinsic body diode
- Extremely low gate charge and input capacitances
- Source sensing pin for increased efficiency

Applications

- Switching mode power supply
- DC-DC converters
- Industrial motor control

Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 2nd generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature.



Product status link

[SCTWA90N65G2V-4](#)

Product summary

Order code	SCTWA90N65G2V-4
Marking	SCT90N65G2V
Package	HiP247-4
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage (recommended operating values)	-5 to 18	
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	119	A
	Drain current (continuous) at $T_C = 100^\circ\text{C}$	90	
$I_{DM}^{(1)}$	Drain current (pulsed)	220	A
P_{TOT}	Total power dissipation at $T_C = 25^\circ\text{C}$	565	W
T_{stg}	Storage temperature range	-55 to 200	$^\circ\text{C}$
T_j	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.31	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	40	$^\circ\text{C}/\text{W}$

2 Electrical characteristics

($T_{CASE} = 25^\circ\text{C}$ unless otherwise specified).

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = -10 \text{ to } 22 \text{ V}$			± 100	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 1 \text{ mA}$	1.9	3.2	5.0	V
$R_{DS(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 18 \text{ V}, I_D = 50 \text{ A}$		18	24	$\text{m}\Omega$
		$V_{GS} = 18 \text{ V}, I_D = 50 \text{ A}, T_J = 200^\circ\text{C}$		30		

Table 4. Dynamic, based on HiP247 package option

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 400 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$	-	3380	-	pF
C_{oss}	Output capacitance		-	294	-	
C_{rss}	Reverse transfer capacitance		-	49	-	
Q_g	Total gate charge	$V_{DD} = 400 \text{ V}, I_D = 50 \text{ A}, V_{GS} = -5 \text{ V to } 18 \text{ V}$	-	157	-	nC
Q_{gs}	Gate-source charge		-	43	-	
Q_{gd}	Gate-drain charge		-	42	-	
R_g	Gate input resistance	$f = 1 \text{ MHz}, I_D = 0 \text{ A}$	-	1	-	Ω

Table 5. Switching energy (inductive load), based on HiP247 package option

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching energy	$V_{DD} = 400 \text{ V}, I_D = 50 \text{ A}, R_G = 2.2 \Omega, V_{GS} = -5 \text{ to } 18 \text{ V}$	-	130	-	μJ
E_{off}	Turn-off switching energy		-	210	-	
E_{on}	Turn-on switching energy	$V_{DD} = 400 \text{ V}, I_D = 50 \text{ A}, R_G = 2.2 \Omega, V_{GS} = -5 \text{ to } 18 \text{ V}, T_J = 200^\circ\text{C}$	-	135	-	μJ
E_{off}	Turn-off switching energy		-	200	-	

Table 6. Switching times, based on HiP247 package option

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400 \text{ V}$, $I_D = 50 \text{ A}$, $R_G = 2.2 \Omega$, $V_{GS} = -5 \text{ V}$ to 18 V ,	-	26	-	ns
t_f	Fall time		-	16	-	
$t_{d(off)}$	Turn-off delay time		-	58	-	
t_r	Rise time		-	38	-	

Table 7. Reverse SiC diode characteristics, based on HiP247 package option

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage	$I_F = 30 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	2.5	-	V
t_{rr}	Reverse recovery time	$I_F = 50 \text{ A}$, $dI/dt = 4000 \text{ A}/\mu\text{s}$, $V_{GS} = V_{DS} = -5 \text{ V}$ to 18 V , $V_{DD} = 400 \text{ V}$, $T_J = 25^\circ\text{C}$	-	17	-	ns
Q_{rr}	Reverse recovery charge		-	308	-	nC
I_{RRM}	Reverse recovery current		-	30	-	A

2.1

Electrical characteristics (curves), based on HiP247 package option

Figure 1. Safe operating area

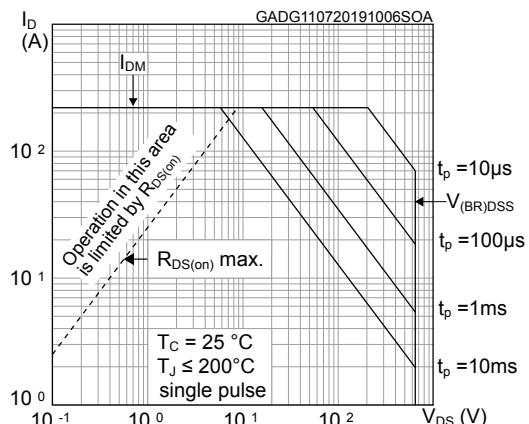


Figure 2. Maximum transient thermal impedance

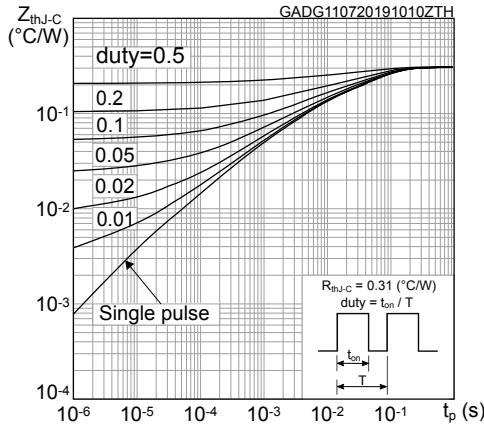


Figure 3. Typical output characteristics ($T_J = -50 \text{ }^\circ\text{C}$)

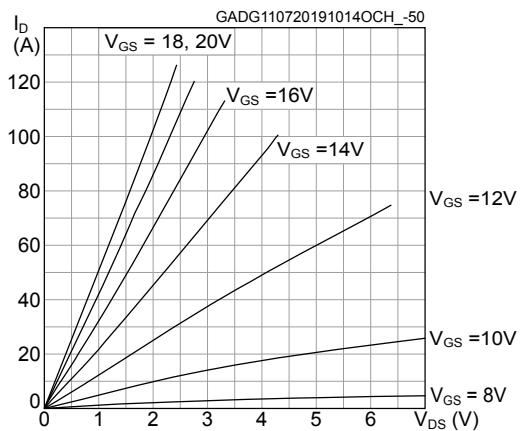


Figure 4. Typical output characteristics ($T_J = 25 \text{ }^\circ\text{C}$)

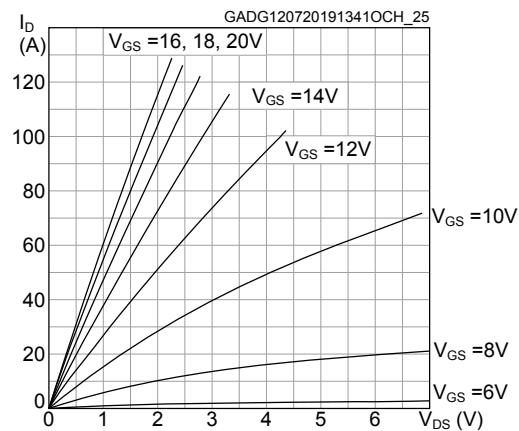


Figure 5. Typical output characteristics ($T_J = 200 \text{ }^\circ\text{C}$)

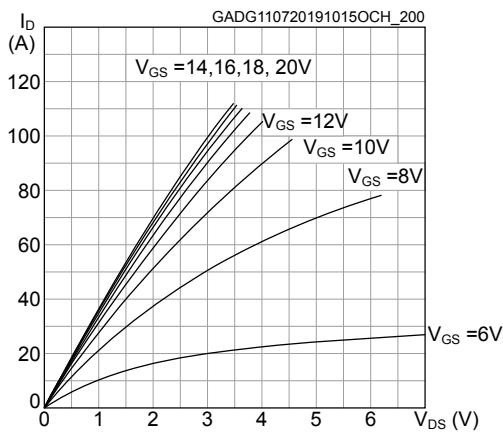


Figure 6. Typical transfer characteristics

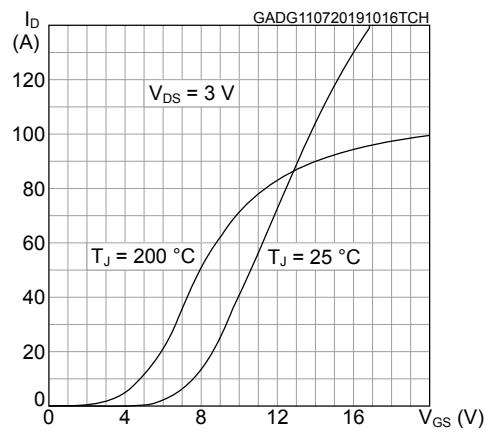


Figure 7. Typical capacitances

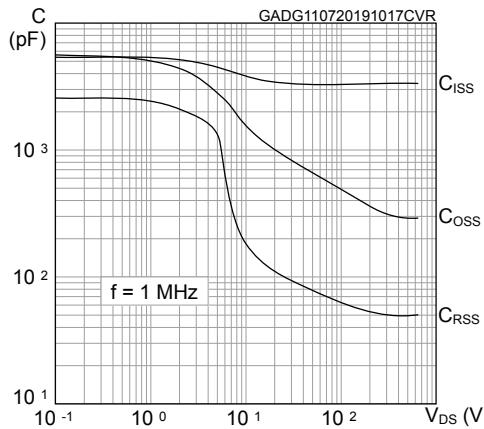


Figure 8. Typical gate charge

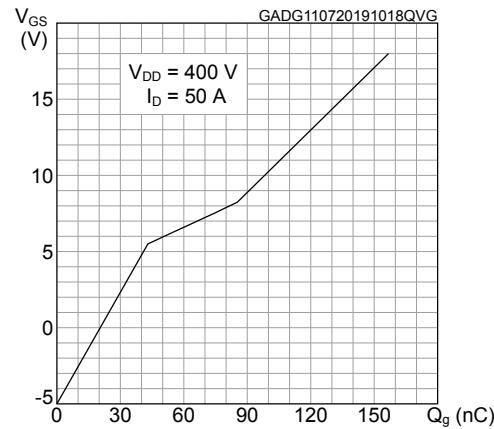


Figure 9. Maximum total power dissipation

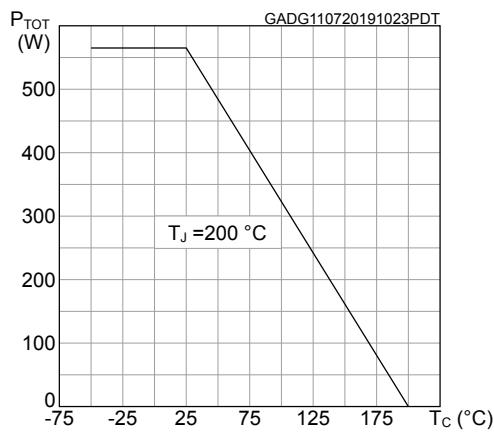


Figure 10. Typical drain-source on-resistance

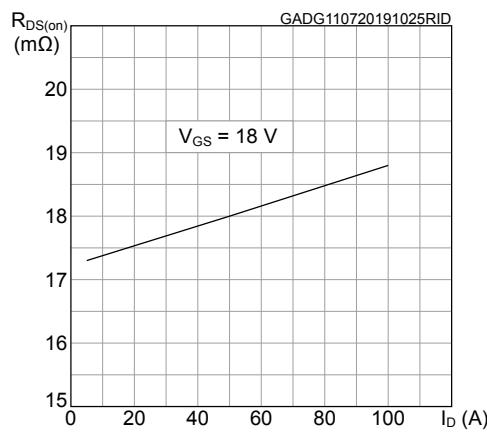


Figure 11. Normalized on-resistance vs temperature

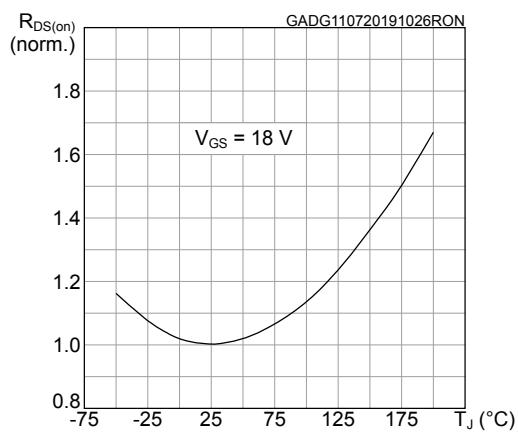


Figure 12. Normalized gate threshold voltage vs temperature

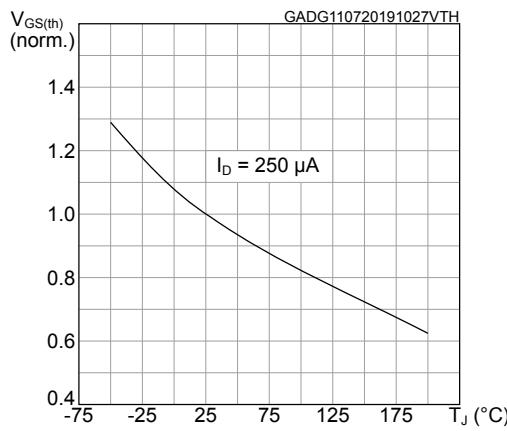


Figure 13. Normalized breakdown voltage vs temperature

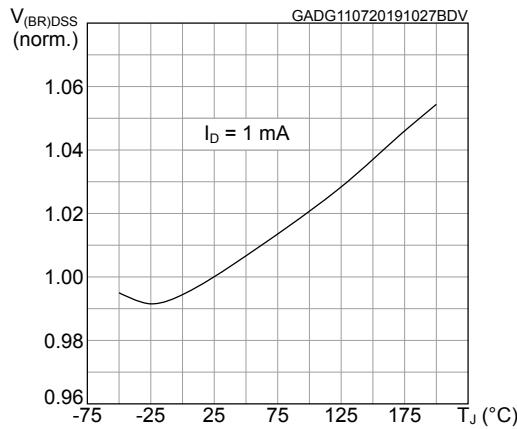


Figure 14. Typical switching energy vs drain current

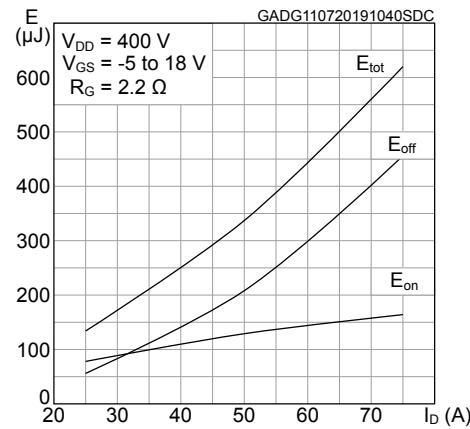


Figure 15. Typical switching energy vs temperature

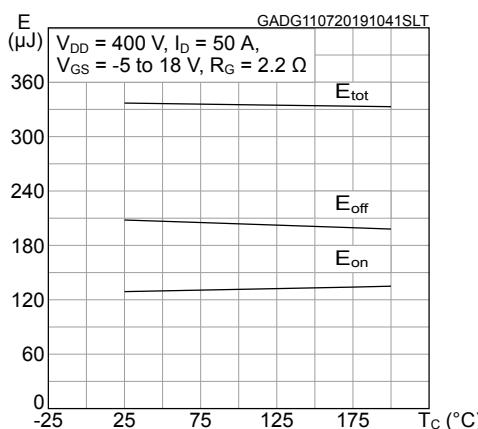


Figure 16. Typical reverse conduction characteristics ($T_J = -50 \text{ °C}$)

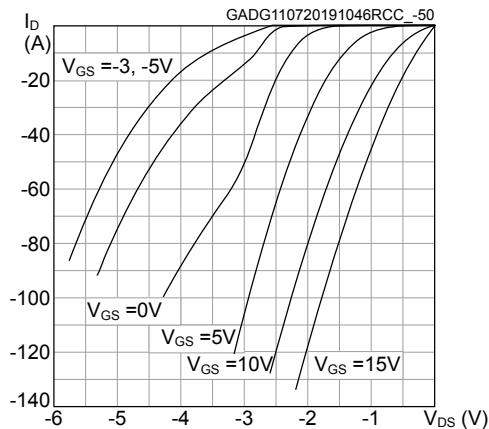


Figure 17. Typical reverse conduction characteristics ($T_J = 25 \text{ °C}$)

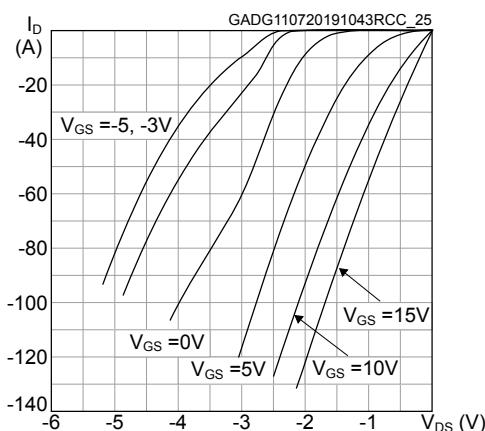
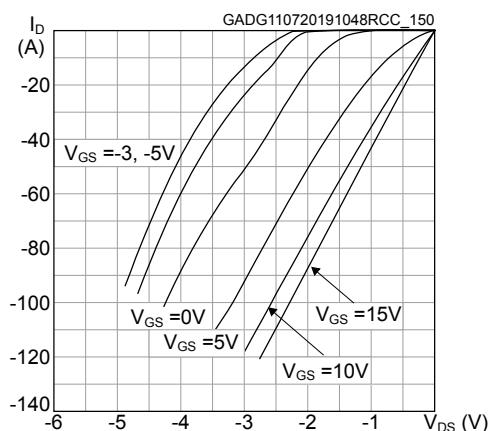


Figure 18. Typical reverse conduction characteristics ($T_J = 150 \text{ °C}$)



3 Test circuits

Figure 19. Switching times test circuit for resistive load

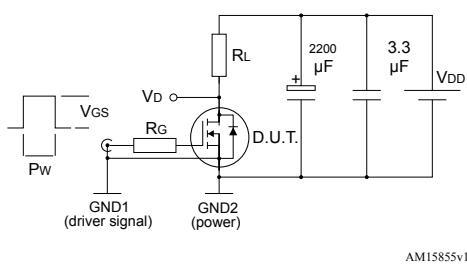


Figure 20. Test circuit for gate charge behavior

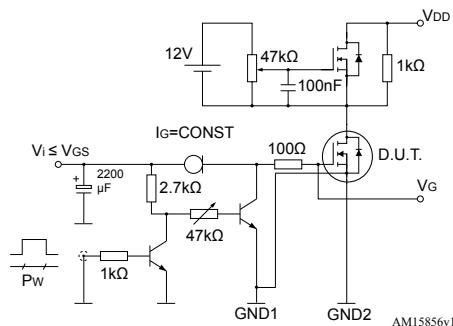


Figure 21. Test circuit for inductive load switching and diode recovery times

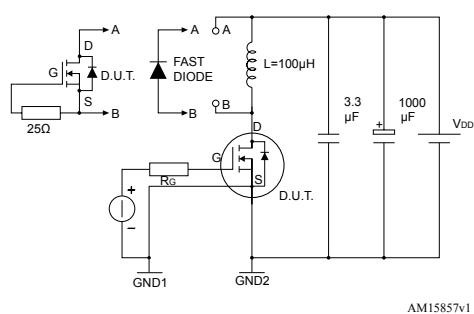


Figure 22. Unclamped inductive load test circuit

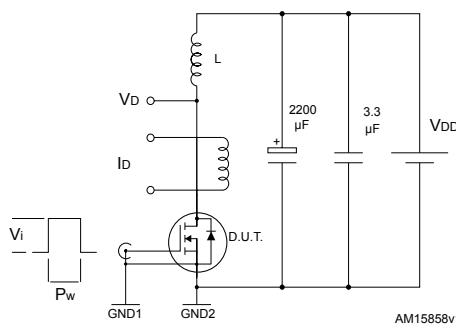


Figure 23. Unclamped inductive waveform

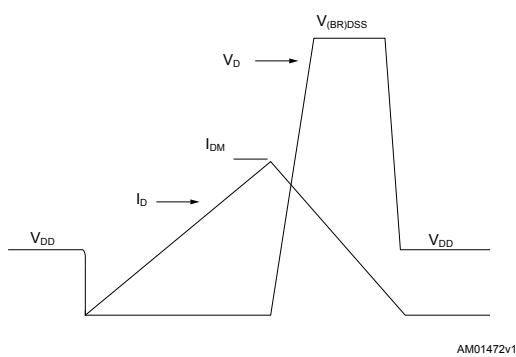
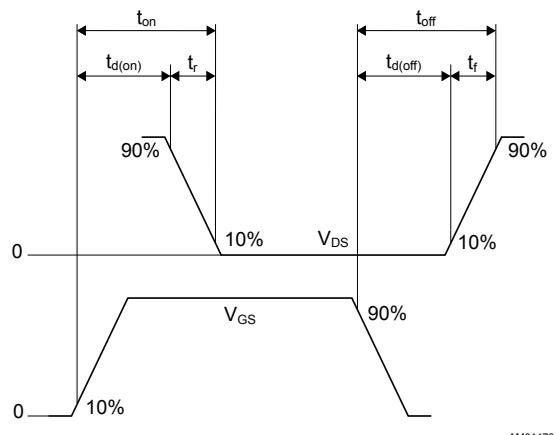


Figure 24. Switching time waveform

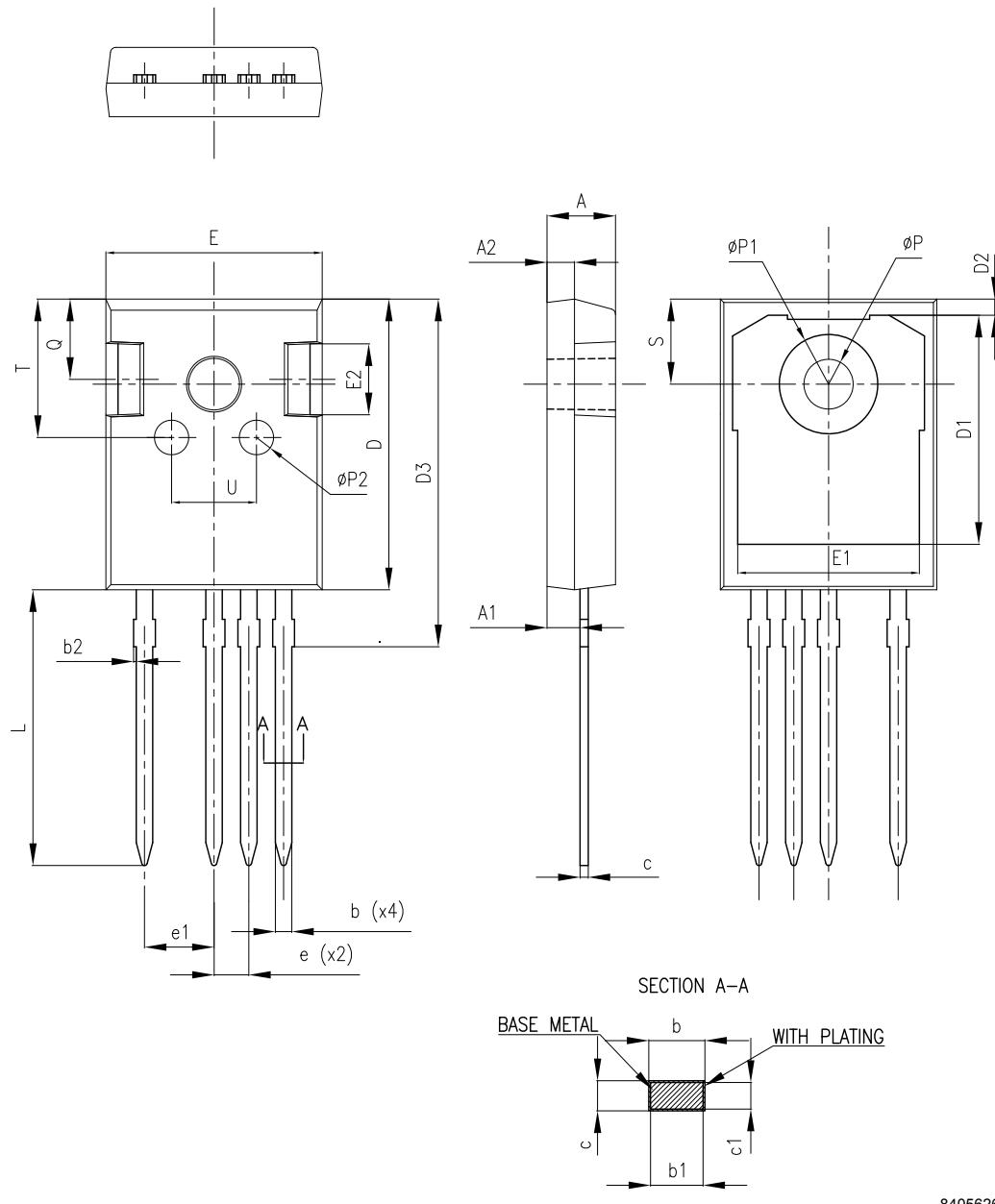


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 HiP247-4 package information

Figure 25. HiP247-4 package outline



8405626_2

Table 8. HiP247-4 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.29
b1	1.15	1.20	1.25
b2	0		0.20
c	0.59		0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
D3	24.97	25.12	25.27
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
L	19.80	19.92	20.10
P	3.50	3.60	3.70
P1			7.40
P2	2.40	2.50	2.60
Q	5.60		6.00
S		6.15	
T	9.80		10.20
U	6.00		6.40

Revision history

Table 9. Document revision history

Date	Revision	Changes
25-Nov-2020	1	First release.

Contents

1	Electrical ratings	2
2	Electrical characteristics.....	3
2.1	Electrical characteristics (curves), based on HiP247 package option	5
3	Test circuits	8
4	Package information.....	9
4.1	HiP247-4 package information	9
	Revision history	11

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