

Features

- Excellent thermal stability
- Common source configuration
- $P_{OUT} = 60W$ with 13dB gain @ 945MHz
- BeO free package
- In compliance with the 2002/95/EC european directive

Description

The SD57060 is a common source N-Channel enhancement-mode lateral Field-Effect RF power transistor designed for broadband commercial and industrial applications at frequencies up to 1.0 GHz. The SD57060 is designed for high gain and broadband performance operating in common source mode at 28V. It is ideal for base station applications requiring high linearity.

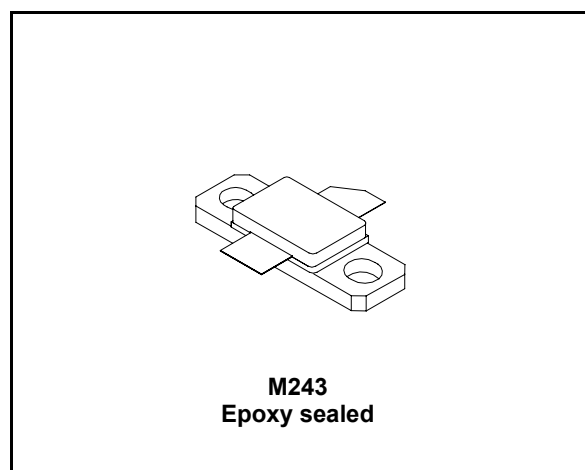


Figure 1. Pin connection

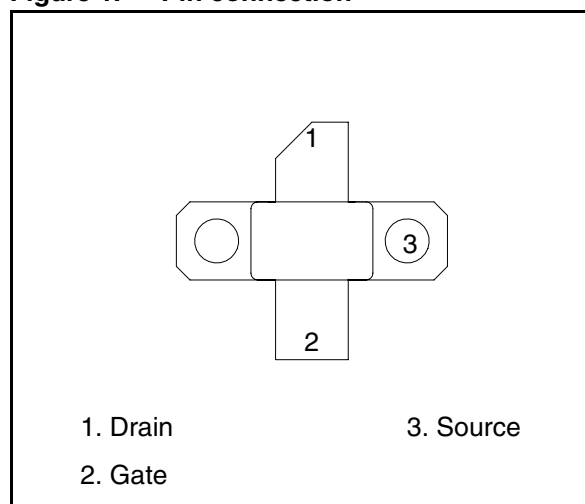


Table 1. Device summary

Order code	Package	Branding
SD57060	M243	SD57060

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1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings ($T_{CASE} = 25^{\circ}C$)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	65	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current	7	A
P_{DISS}	Power dissipation (@ $T_c = 70^{\circ}C$)	108	W
T_J	Max. operating junction temperature	200	$^{\circ}C$
T_{STG}	Storage temperature	-65 to + 150	$^{\circ}C$

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	1.2	$^{\circ}C/W$

2 Electrical characteristics

$$T_{CASE} = +25\text{ }^{\circ}\text{C}$$

2.1 Static

Table 4. Static

Symbol	Test conditions		Min	Typ	Max	Unit
$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$	$I_{DS} = 1\text{ mA}$	65			V
I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$			1	μA
I_{GSS}	$V_{GS} = 20\text{ V}$	$V_{DS} = 0\text{ V}$			1	μA
$V_{GS(Q)}$	$V_{DS} = 28\text{ V}$	$I_D = 250\text{ mA}$	2.0		5.0	V
$V_{DS(ON)}$	$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}$		0.7	0.8	V
G_{FS}	$V_{DS} = 10\text{ V}$	$I_D = 3\text{ A}$	2.5			S
$C_{ISS}^{(1)}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$		88		pF
C_{OSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$		44		pF
C_{RSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$		1.7		pF

1. Includes Internal Input Moscap.

2.2 Dynamic

Symbol	Test conditions		Min	Typ	Max	Unit
P_{OUT}	$V_{DD} = 28\text{ V}$	$I_{DQ} = 100\text{ mA}$	60			W
G_{PS}	$V_{DD} = 28\text{ V}$	$I_{DQ} = 100\text{ mA}$	13	15		dB
h_D	$V_{DD} = 28\text{ V}$	$I_{DQ} = 100\text{ mA}$	53	60		%
Load mismatch	$V_{DD} = 28\text{ V}$	$I_{DQ} = 100\text{ mA}$	5:1			VSW R

3 Impedance

Figure 2. Current conventions

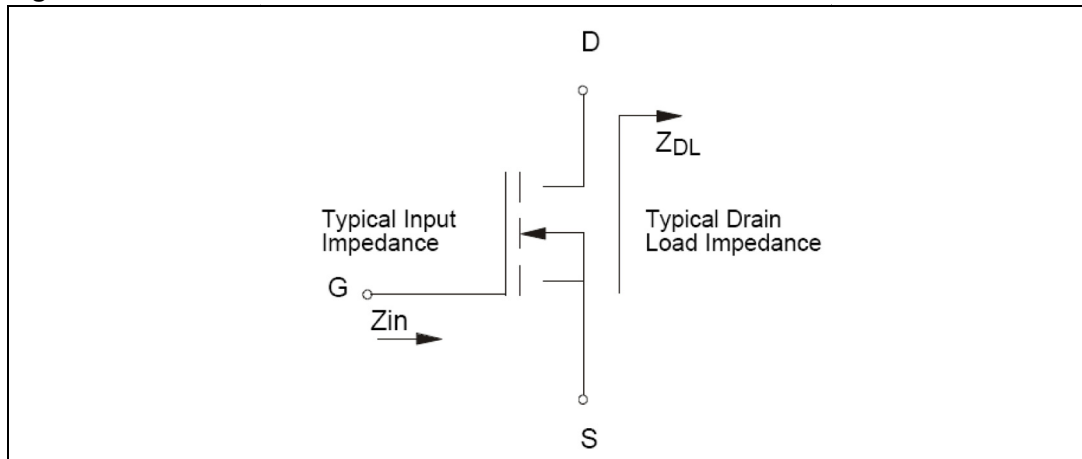


Table 5. Impedance data

Freq. (MHz)	Z_{IN} (Ω)	Z_{DL} (Ω)
925 MHz	$0.8 - j 0.095$	$1.5 + j 0.48$
945 MHz	$0.7 - j 0.05$	$1.6 + j 0.25$
960 MHz	$0.7 + j 0.1$	$1.7 + j 0.130$

4 Typical performance

Figure 3. Output power and power gain vs input power

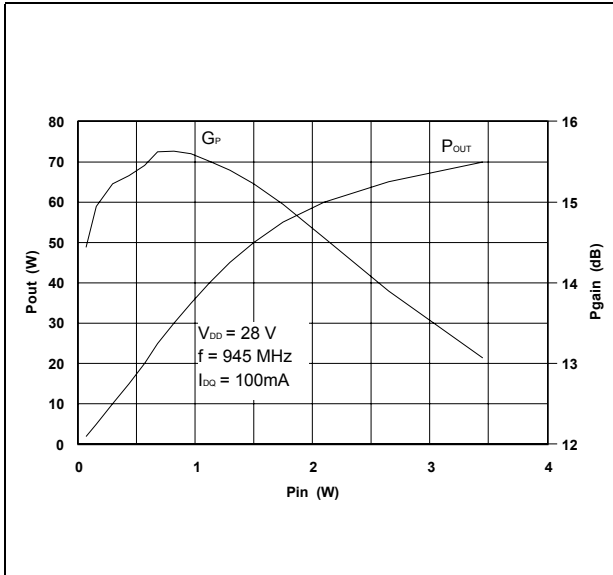


Figure 4. Output power and power gain vs input power

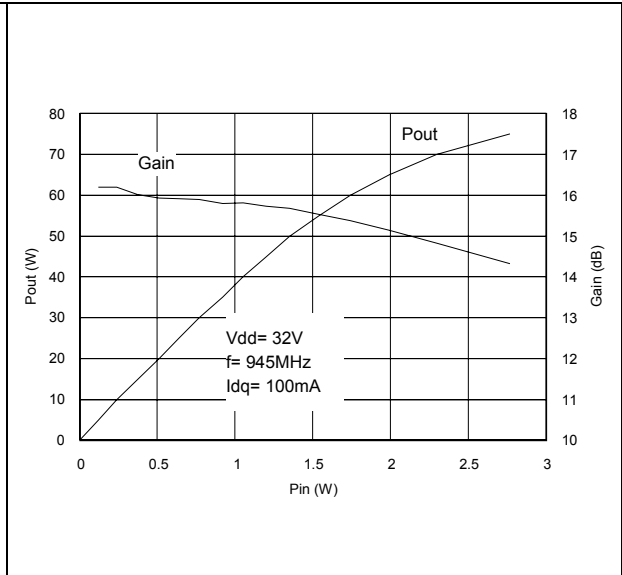


Figure 5. Efficiency vs output power

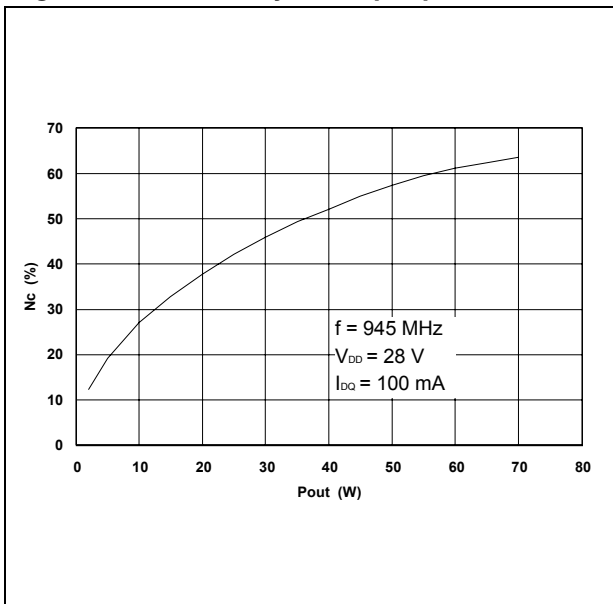


Figure 6. Efficiency vs output power

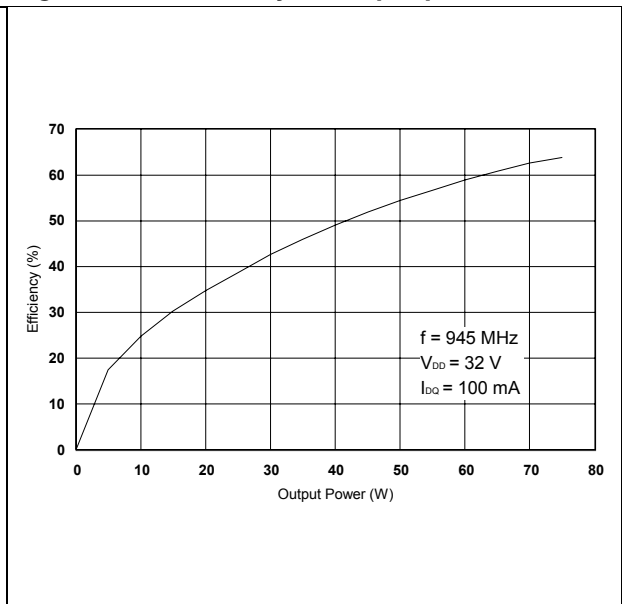


Figure 7. Output power vs drain-source voltage

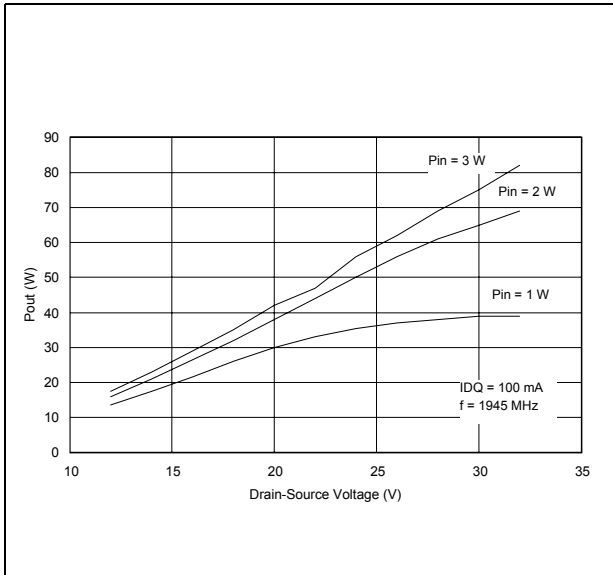


Figure 8. Intermodulation distortion vs output power

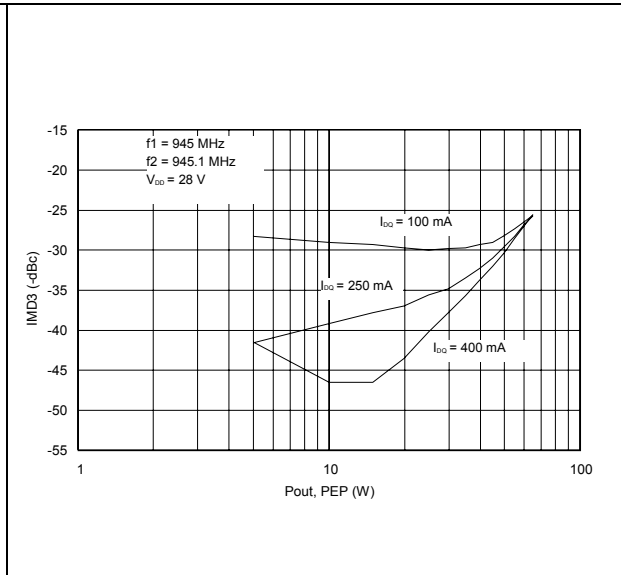


Figure 9. Power gain vs output power

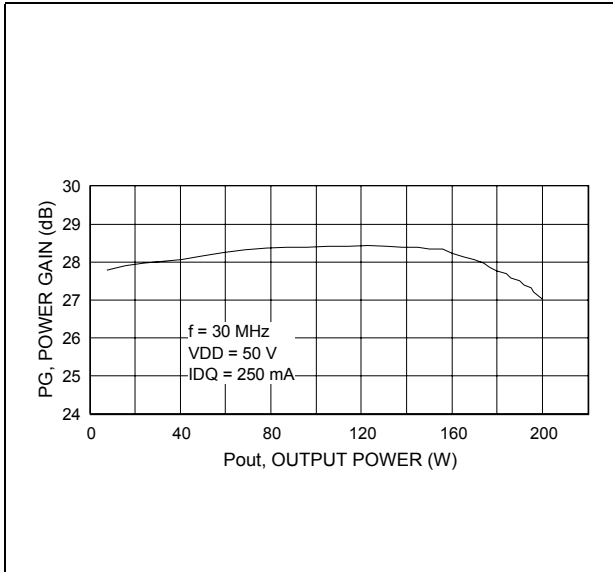


Figure 10. Safe operating area

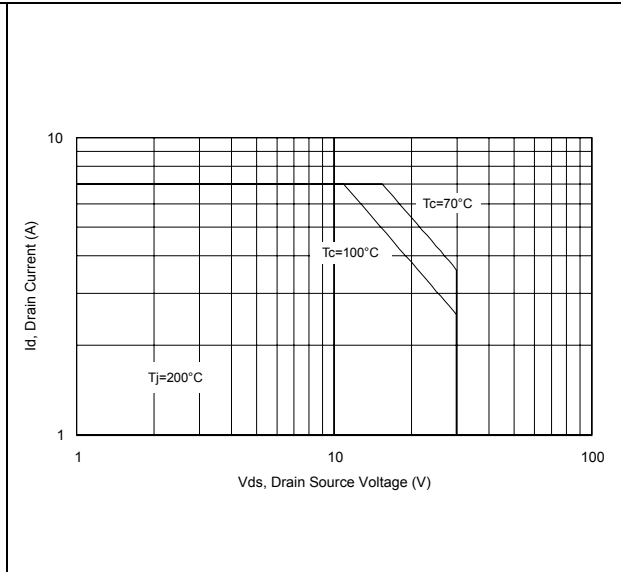
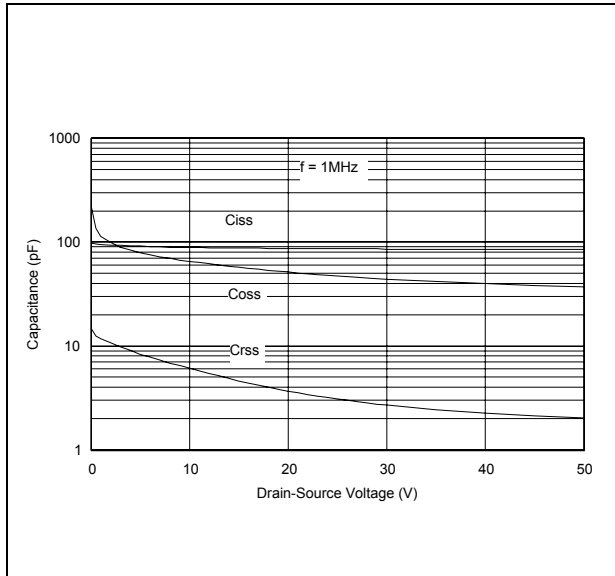


Figure 11. Capacitance vs drain-source voltage



5 Common source s-parameter

5.1 SD57060 ($V_{DS} = 13.5V$ $I_{DS} = 2A$)

Table 6. S-parameter

Freq (MHz)	s11 MAG	s11 ang	s21 MAG	s21 ang	s12 MAG	s12 ang	s22 MAG	s22 ang
50	0.896	-168.86	15.679	85.012	0.0116	-5.1128	0.796	-170.27
60	0.896	-169.3	14.859	84.592	0.0116	-5.4369	0.796	-170.49
70	0.869	-169.76	14.004	84.14	0.0116	-5.7912	0.797	-170.7
80	0.869	-170.23	13.122	83.644	0.0115	-6.0658	0.797	-170.9
90	0.897	-170.71	12.213	83.074	0.0115	-6.3789	0.798	-171.1
100	0.897	-171.19	11.285	82.404	0.0114	-6.8198	0.799	-171.29
150	0.9	-173.39	6.9575	76.841	0.0111	-9.6817	0.808	-171.96
200	0.905	-174.29	4.751	71.951	0.0103	-11.87	0.821	-171.79
250	0.912	-174.64	3.637	68.471	0.0097	-12.957	0.836	-171.36
300	0.92	-174.9	2.889	64.839	0.0089	-13.493	0.851	-171.03
350	0.927	-175.08	2.428	62.538	0.0083	-11.937	0.866	-170.76
400	0.934	-175.3	2.077	58.748	0.0077	-11.228	0.881	-170.6
450	0.941	-175.5	1.802	56.081	0.0071	-8.7753	0.894	-170.49
500	0.947	-175.73	1.592	51.84	0.0066	-7.5009	0.907	-170.47
550	0.952	-176.02	1.379	48.632	0.0059	-4.8834	0.917	-170.55
600	0.956	-176.29	1.221	45.777	0.0053	0.12909	0.927	-170.67
650	0.96	-176.6	1.049	42.778	0.0048	5.0249	0.936	-170.82
700	0.962	-176.9	0.924	42.212	0.0043	13.591	0.943	-170.94
750	0.965	-177.22	0.814	40.376	0.0039	22.729	0.95	-171.05
800	0.968	177.51	0.723	41.348	0.0036	37.954	0.956	-171.14
850	0.97	-177.83	0.662	40.788	0.0037	51.305	0.961	-171.16
900	0.972	-178.19	0.6	41.719	0.0041	63.188	0.966	-171.24
950	0.974	-178.56	0.566	41.469	0.0047	73.463	0.971	-171.24
1000	0.975	-178.96	0.523	41.747	0.0055	80.707	0.974	-171.25
1050	0.976	-179.28	0.504	41.439	0.0064	88.27	0.977	-171.26
1100	0.978	-179.62	0.477	40.692	0.0074	92.504	0.979	-171.36
1150	0.979	-179.85	0.466	39.239	0.0084	96.743	0.981	-171.43
1200	0.981	179.9	0.444	36.775	0.0097	98.282	0.982	171.5
1250	0.982	179.68	0.431	34.788	0.011	99.121	0.983	-171.58
1300	0.983	179.52	0.408	31.862	0.0125	98.773	0.983	-171.71
1350	0.984	179.35	0.395	30.219	0.0136	97.973	0.983	-171.86
1400	0.985	179.24	0.382	26.465	0.0148	97.464	0.984	-171.94
1450	0.987	179.13	0.365	23.869	0.0157	95.39	0.984	-171.98
1500	0.988	179.09	0.351	21.267	0.0165	93.871	0.985	-171.98

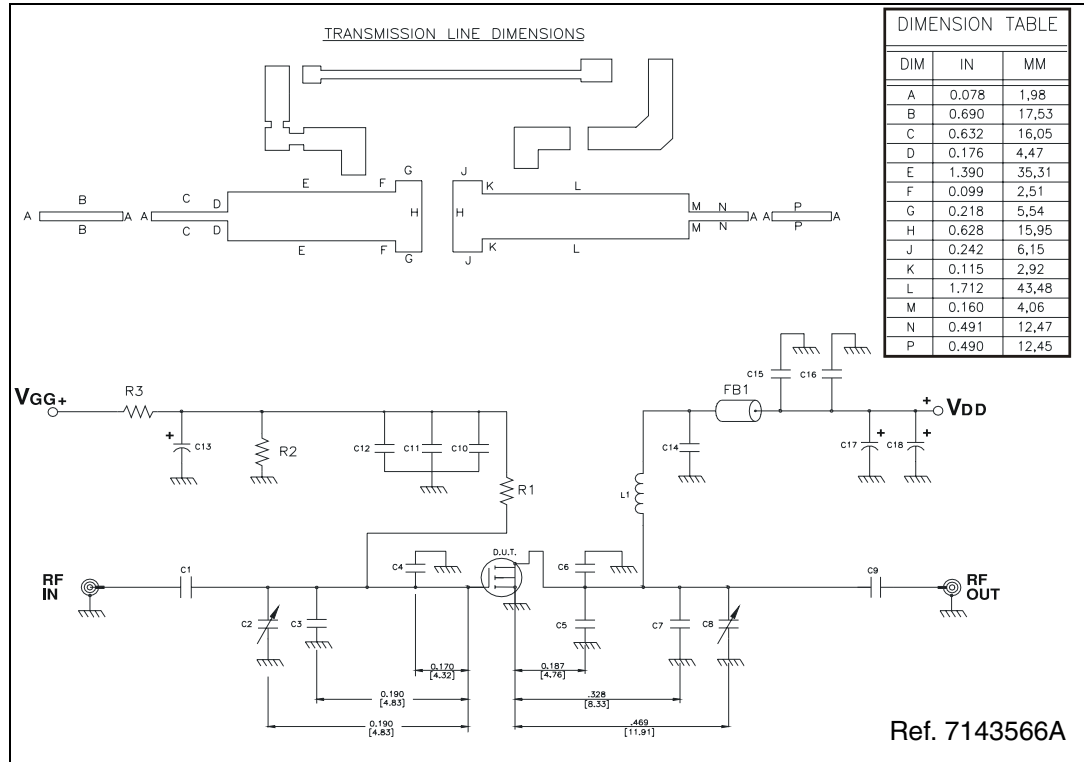
5.2 SD57060 ($V_{DS} = 28V$ $I_{DS} = 2A$)

Table 7. S-parameter

Freq (MHz)	s11 MAG	s11 ang	s21 MAG	s21 ang	s12 MAG	s12 ang	s22 MAG	s22 ang
50	0.857	-159.69	22.757	85.934	0.0114	-3.8342	0.67	-161.72
60	0.86	-160.69	21.547	85.328	0.0113	-4.4852	0.672	-162.07
70	0.862	-161.73	20.287	84.672	0.0112	-5.1512	0.674	-162.41
80	0.865	-162.8	18.987	83.933	0.0111	-5.8379	0.677	-162.74
90	0.869	-163.89	17.65	83.083	0.011	-6.5533	0.679	-163.07
100	0.872	-164.98	16.286	82.083	0.011	-7.4226	0.683	-163.39
150	0.891	-169.66	9.9447	74.03	0.0103	-12.13	0.708	-164.66
200	0.905	-171.43	6.719	67.256	0.0094	-15.548	0.74	-164.87
250	0.915	-172.29	5.074	62.268	0.0086	-17.236	0.774	-164.99
300	0.926	-172.84	3.978	57.533	0.0077	-18.625	0.806	-163.35
350	0.935	-173.34	3.297	54.035	0.0069	-17.313	0.834	-165.82
400	0.943	-173.79	2.775	49.488	0.0061	-16.81	0.86	-166.35
450	0.951	-174.24	2.376	46.121	0.0054	-13.006	0.881	-166.85
500	0.957	-174.67	2.061	41.541	0.0048	-9.175	0.898	-167.35
550	0.962	-175.11	1.766	38.23	0.0041	-2.5323	0.913	-167.83
600	0.966	-175.53	1.546	35.173	0.0035	-7.641	0.925	-168.25
650	0.969	-175.95	1.32	32.548	0.0031	19.501	0.937	-168.57
700	0.972	-176.34	1.162	31.674	0.0031	34.423	0.946	-168.81
750	0.974	-176.75	1.021	29.983	0.0032	48.345	0.954	-168.93
800	0.976	-177.15	0.91	30.341	0.0035	62.927	0.96	-168.98
850	0.977	-177.57	0.826	29.318	0.004	74.982	0.967	-168.95
900	0.978	-177.98	0.749	29.508	0.0047	81.962	0.973	-168.88
950	0.979	-178.41	0.696	28.477	0.0054	87.332	0.978	-168.77
1000	0.979	-178.85	0.639	27.949	0.0063	90.913	0.982	-168.72
1050	0.98	-179.24	0.601	26.768	0.0072	95.707	0.984	-168.75
1100	0.981	-179.61	0.561	25.598	0.0082	98.95	0.985	-168.87
1150	0.981	-179.95	0.533	23.746	0.0094	101.25	0.986	-169.13
1200	0.982	179.72	0.498	21.331	0.011	102.03	0.985	-169.64
1250	0.983	179.44	0.472	19.005	0.012	102.21	0.981	-170.42
1300	0.984	179.23	0.44	16.272	0.0131	101.78	0.976	-171.5
1350	0.985	179.02	0.417	14.424	0.0143	100.61	0.969	-172.89
1400	0.986	178.85	0.394	11.161	0.0156	99.505	0.96	-174.72
1450	0.986	178.7	0.372	8.789	0.0163	97.699	0.949	-176.87
1500	0.986	178.6	0.354	6.5533	0.0168	96.68	0.94	-178.58

6 Test circuit

Figure 12. Test circuit schematic



- 1 Dimensions at component symbols are reference for component placement.
- 2 Gap between ground & transmission line = 0.056 [1.42] +0.002 [0.05] -0.000 [0.00] typ.
- 3 Dimensions of input and output component from edge of transmission lines.

Table 8. Test circuit component part list

Component	Description
L1	INDUCTOR, 5 TURNS AIR WOUND #18 AWG, ID = 0.125 [3.18] NYLON COATED MAGNET WIRE
FB1	SHIELD BEAD SURFACE MOUNT EMI
R1	1 K Ohm, SURFACE MOUNT CHIP RESISTOR
R2	18 K Ohm, SURFACE MOUNT CHIP RESISTOR
R3	10 K Ohm, SURFACE MOUNT CHIP RESISTOR
C1	36 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C2,C8	0.8-8.0 pF GIGA TRIM VARIABLE CAPACITOR
C3	4.7 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C4	11 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C5	1.3 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C6	7.5 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C7	8.2 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C9	100 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C10,C14	47 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C11,C15	10000 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C12,C16	0.1 μ F / 500 V SURFACE MOUNT CERAMIC CHIP CAPACITOR
C13,C17	10 μ F / 50 V ALUMINIUM ELECTROLITIC RADIAL LEAD CAPACITOR
C18	220 μ F / 63 V V ALUMINIUM ELECTROLITIC RADIAL LEAD CAPACITOR
PCB	ULTRALAM 2000, WOVEN FIBERGLASS REINFORCED PTFE. 0.030" THK, $\epsilon_r= 2.55$, 2 OZ ED CU BOTH SIDES

7 Text circuit layout

Figure 13. Test fixture

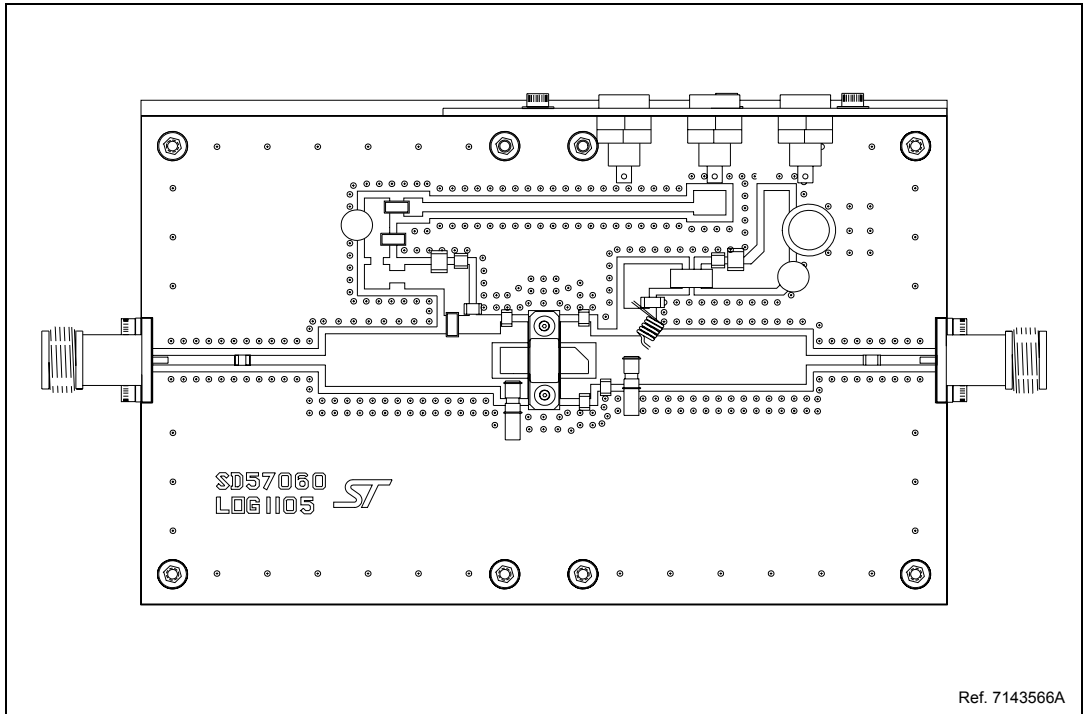
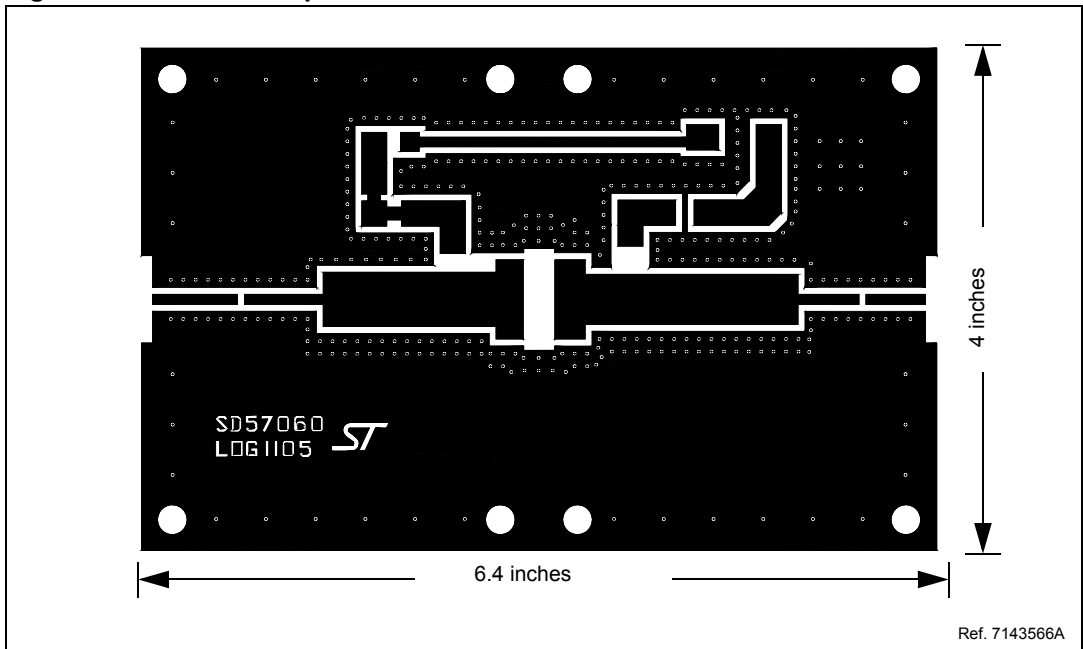


Figure 14. Test circuit photomaster

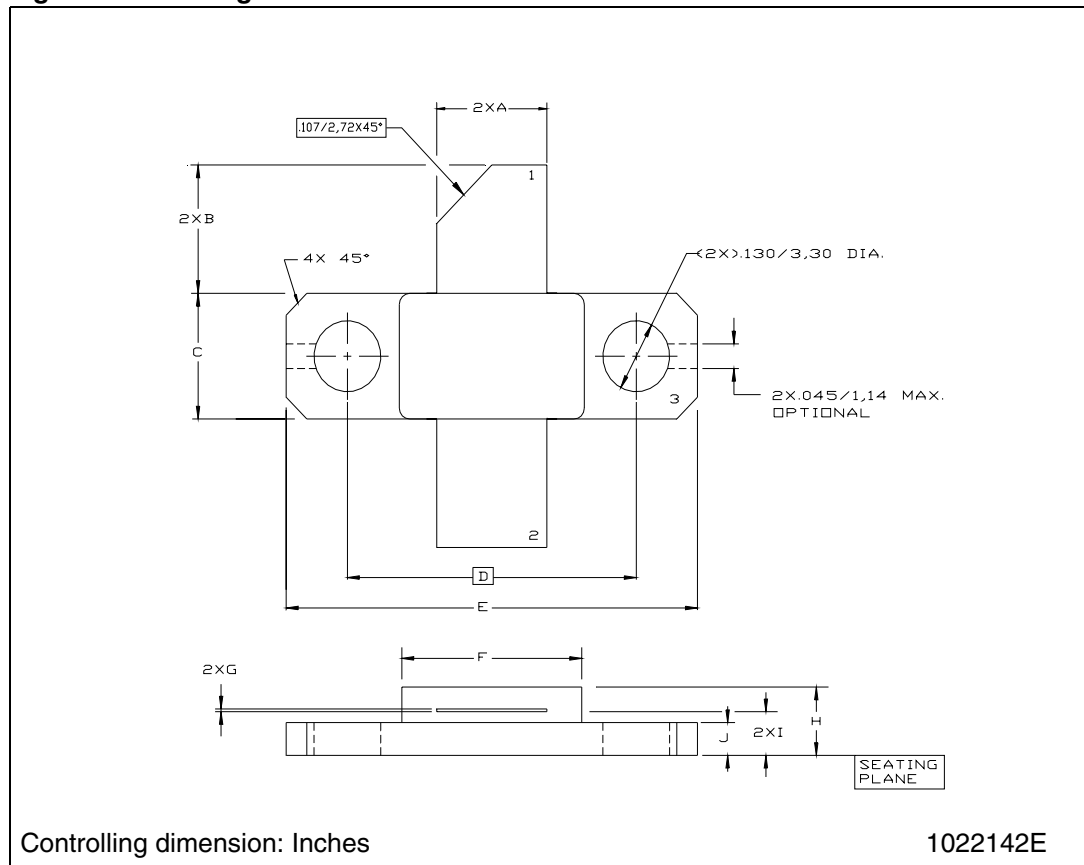


8 Package mechanical data

Table 9. M243 (.230 x .360 2L N/HERM W/FLG) mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	5.21		5.72	0.205		0.225
B	5.46		6.48	0.215		0.255
C	5.59		6.10	0.220		0.240
D		14.27			0.562	
E	20.07		20.57	0.790		0.810
F	8.89		9.40	0.350		0.370
G	0.10		0.15	0.004		0.006
H	3.18		4.45	0.125		0.175
I	1.83		2.24	0.072		0.088
J	1.27		1.78	0.050		0.070

Figure 15. Package dimensions



9 Revision history

Table 10. Document revision history

Date	Revision	Changes
24-Mar-2003	5	First Issue.
23-Jul-2007	6	Document reformatted, added lead free info
24-Aug-2007	7	Cover page title updated

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