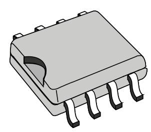
# Constant voltage and current controller with online digital trimming

**Datasheet - production data**



SO8

**Figure 1. Internal schematic**

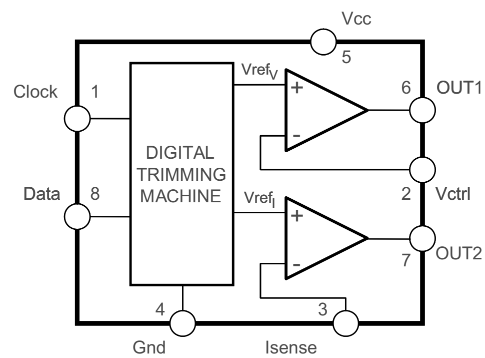
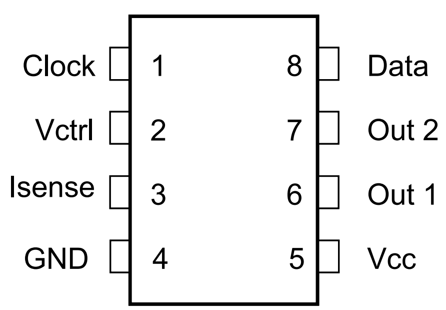



**Figure 2. Pin connections (top view)**




## Features

- Online digital trimming for the highest end-product accuracy in voltage and current control
- Automatic operation eliminates manual intervention in the production line
- Simple and robust trimming protocol and storage
- Redundant OTP (first and second trimming)
- Extended operating voltage range
- Very low quiescent current
- Offered in an SO8 package

## Applications

- SMPS requiring accurate voltage and current regulation
- AC-DC adapters
- Battery chargers

## Description

SEA01 is a highly integrated solution for SMPS applications requiring precise voltage and current regulation.

The device integrates two voltage references, two op-amps (with open-drain outputs), a low-side current sensing circuit and an online digital trimming machine.

The internal reference Vref$_V$, along with one op-amp, is the core of the voltage control loop.

The internal reference Vref$_I$ and the other op-amp make up the current control loop. The embedded digital trimming allows the user, through software, to adjust and permanently store both Vref$_V$ and Vref$_I$ internal references during the production test of the end product, compensating the tolerance of the external components and the error due to their discretized values. Redundant OTP gives the user a second chance to change the values stored in the non-volatile memory of the IC during the first trimming process.

This feature allows having the highest end-product accuracy of voltage and current control without the use of external discrete components or manual intervention.

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# 1 Absolute maximum ratings

**Table 1. Absolute maximum ratings**

| Symbol | Pin | Parameter | Value | Unit |
|---|---|---|---|---|
| $V_{cc}$ | 5 | Dc supply voltage | -0.3 to 38 | V |
| $V_{out}$1-2 | 6, 7 | Open-drain voltage | -0.3 to $V_{cc}$ | V |
| $I_{sense}$ | 3 | Analog input | -0.3 to $V_{cc}$ | V |
| $I_{out}$1-2 | 6, 7 | Max sink current | 20 (*) | mA |
| $V_{ctrl}$ | 2 | Analog input | -0.3 to $V_{cc}$ | V |
| Data | 8 | Digital input/output | -0.3 to $V_{cc}$ | V |
| Clock | 1 | Digital input | -0.3 to $V_{cc}$ | V |

*Note: Please note that, during steady state operation, the maximum power that the device can dissipate is limited by thermal constraints. For this reason is not possible to sink the maximum current in OUT1 and OUT2 while their voltages are close to their AMR. The junction operating temperature, which can be calculated as $T_{amb} + R_{th\ j\text{-}amb} \cdot Pdiss$, must always be lower than 150 °C. Pdiss is the total dissipated power in the device and it can be calculated with the formula $Pdiss = Vcc \cdot Icc + I_{OUT1} \cdot V_{OUT1} + I_{OUT2} \cdot V_{OUT2}$.*

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance, junction-to-ambient | 150 (SO8) | °C/W |
| $Tj_{op}$ | Junction temperature operating range | -40 to 150 | °C |
| Tstg | Storage temperature | -55 to 150 | |

**Table 3. Pin functions**

| N. | Name | Function |
|---|---|---|
| 1 | Clock | Clock logic input for $I^2C$ serial communication protocol.<br>This pin will be externally pulled up to 3.6 V max.<br>A small internal pull-up is present to prevent false signal detection (the pin is floating during normal operation). |
| 2 | Vctrl | Inverting input of the op-amp connected to $Vref_V$. The pin is typically tied to the midpoint of a resistor divider that senses the output voltage. |
| 3 | Isense | Inverting input of the op-amp connected to $Vref_I$. The pin will be typically tied to the positive end of the current sense resistor through a decoupling resistor. |
| 4 | GND | Ground. Return of the bias current of the device. 0 V reference for all voltages. The pin should be tied as close to the ground output terminal of the converter as possible to minimize load current effect on the voltage regulation setpoint. |

**Table 3. Pin functions (continued)**

| N. | Name | Function |
|---|---|---|
| 5 | $V_{cc}$ | Supply voltage of the device. A small bypass capacitor (0.1 µF typ.) to GND, located as close to the IC's pins as possible, might be useful to get a clean supply voltage. |
| 6 | OUT1 | Open-drain output of the internal op-amp, whose non-inverting input is connected to $Vref_V$. The pin, able to sink current only, is typically connected to the branch of the optocoupler's photodiode to transmit the error signal to the primary side for voltage control loop. |
| 7 | OUT2 | Open-drain output of the internal op-amp, whose non-inverting input is connected to $Vref_I$. The pin, able to sink current only, is typically connected to the branch of the optocoupler's photodiode to transmit the error signal to the primary side for current control loop. |
| 8 | Data | Data logic input/output for $I^2C$ serial communication protocol.<br>This pin will be externally pulled up to 3.6 V max<br>A small internal pull-up is present to prevent false signal detection (the pin is floating during normal operation). |

**Table 4. Electrical characteristics**
**( Tj = 25 °C, $V_{cc}$ = 12 V; unless otherwise specified )**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Device supply | | | | | | |
| Vcc | Voltage operating range | | 3.5 | | 36 | V |
| Icc | Quiescent current | | | 200 | | µA |
| | | (1) | | | 300 | |
| | | Vcc = 20 V (1) | | | 400 | |
| Voltage control loop op-amp | | | | | | |
| $Gm_V$ | Transconductance (sink current only) (2) | | | 19 | | S |
| | | (1) | | 6 | | |
| $Vref_V$ | Voltage reference default value(3) (0% trimming) | | 2.48 | 2.5 | 2.52 | V |
| | | (1) | 2.455 | | 2.545 | |
| Ibias | Inverting input bias current | | | 50 | | nA |
| | | (1) | | 100 | | |
| Current control loop | | | | | | |
| $Gm_I$ | Transconductance(4) (sink current only) | | | 22 | | S |
| | | (1) | | 19 | | |
| $Vref_I$ | Current loop reference (5) @ I(Iout) = 1 mA | | 27 | 30 | 33 | mV |
| | | (1) | 25 | | 35 | |
| Ibias | Non-inverting input source current | | | 10 | | µA |
| | | (1) | | 20 | | |

**Table 4. Electrical characteristics (continued)**
**( Tj = 25 °C, $V_{cc}$ = 12 V; unless otherwise specified )**

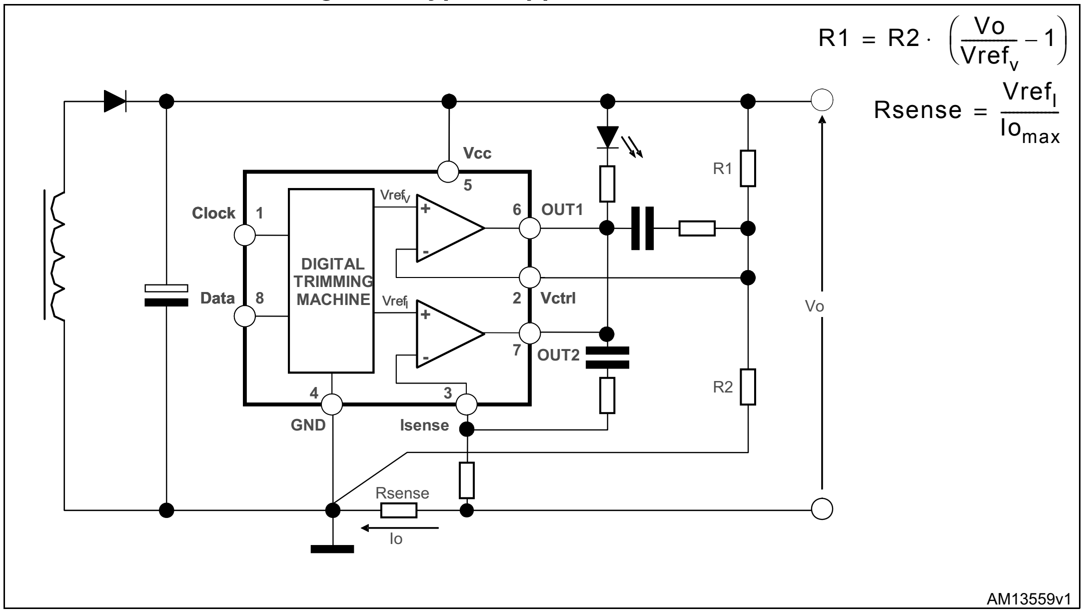
| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output stage | | | | | | |
| $V_{OUT1-2low}$ | Low output level @ 2 mA sink current | | | 200 | | mV |
| | | (1) | | | 400 | mV |
| Trimming functions | | | | | | |
| $V_{ClockLOW}$ | Clock input low level | | | | 0.8 | V |
| $V_{ClockHI}$(6) | Clock input high level | | 2 | | 3.45 | V |
| $C_{Clock}$ | Clock input capacitance | | | | 5 | pF |
| $f_{Clock}$ | Clock frequency | | | | 100 | KHz |
| $V_{DataLOW}$(6) | Data input low level | | | | 0.8 | V |
| $V_{DataHI}$ | Data input high level | | 2 | | 3.45 | V |
| $C_{Data}$ | Data input capacitance | | | | 5 | pF |
| $Vcc_{zap}$ | PROM zapping voltage | | 17 | | 20 | V |
| $I_{ZAP}$ | PROM zapping current | $V_{cc}$= 19 V | | 50 | 90 | mA |
| $t_{ZAP}$ | PROM zapping time | $V_{cc}$= 19 V | | 34 | 45 | ms |
| $Vref_V$ | Trimming range | Referred to 0% trimming | -3 | | 3 | % |
| $\Delta Vref_V$ | Trimming step | | | 0.2 | | % |
| $Vref_I$ | Trimming range | Referred to 0% trimming | -50 | | 50 | % |
| $\Delta Vref_I$ | Trimming step | | | 3.3 | | % |
| Temperature stability | | | | | | |
| $\Delta Vref_V$ $\Delta Vref_I$ | Voltage reference deviation over temperature range -25 °C < $T_{amb}$ < 105 °C | | | 0.3% | | |

1. Specification referred to -25 °C < Tamb < 105 °C.
2. With $V_{OUT1}$ > 3 V, If the voltage on Vctrl (the inverting input of the amplifier) is higher than the non-inverting input ($Vref_V$), and it is increased by 1 mV, the sink current at the output Out1 will be increased by 19 mA.
3. The internal voltage reference is set to $Vref_V$. The voltage control loop precision takes into account the cumulative effects of the internal voltage reference deviation as well as the input offset voltage of the transconductance operational amplifier.
4. When the inverting input at Isense is greater than 30 mV, and the voltage is increased by 1mV, the sinking current at the output Out2 will be increased by 22 mA (please take into account the internal current limit typ 28 mA).
5. The internal current sense threshold is triggered when the voltage on the Isense pin is $Vref_I$. The current control loop precision takes into account the cumulative effects of the internal voltage reference deviation as well as the input offset voltage of the transconductance operational amplifier. Please note that this value can be trimmed with a resolution of 1 mV.
6. The Data and Clock pins are connected to an internal bus at 3.3 V.

# 2 Application information

## 2.1 Constant voltage and current control and with online digital trimming

Figure 3. Typical application schematic




The online digital trimming allows the user to adjust the $Vref_V$ and $Vref_I$ internal references in order to have the highest accuracy of voltage and current of the application (SMPS requiring an accurate current limitation or regulation and/or very accurate voltage regulation).

This new way of trimming allows the user to have the highest accuracy simply using software without the use of external discrete components or manual intervention.

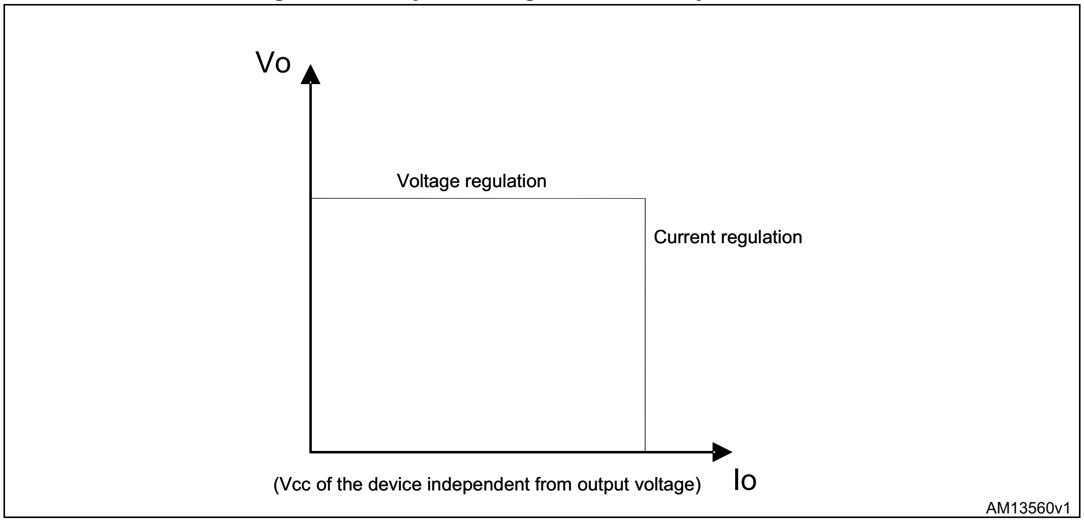
The parameters of the IC that the user can trim are $Vref_V$ and $Vref_I$.

$Vref_V$ is the parameter typically relevant to the voltage regulation and it has to be trimmed as the first step after measuring the output voltage of the application.

$Vref_I$ is typically the parameter relevant to the current regulation and it has to be trimmed to adjust the value of the measured current to the target current.

The relation between the controlled current and the controlled output voltage can be described as a square as shown in the following V/I output-power graph (with the power supply of the device independent from the output voltage).

**Figure 4. Output voltage versus output current**



# 3 Online digital trimming procedure

## 3.1 General features

The embedded digital trimming allows the user to adjust and permanently store using software, both the $Vref_V$ and $Vref_I$ internal references during the production test of the end-product, compensating the tolerance of the external components and the error due to their discretized values.

The device provides a non-volatile memory (NVM) based on a redundant OTP (two OTP, one-time-programmable memories) and a volatile memory.

The volatile memory is used to adjust the value of both $Vref_V$ and $Vref_I$ internal references. Once the optimal values have been found, the user can permanently store them in the OTP memory.

The presence of a second OTP allows the user to perform a second trimming of the device. It is possible to perform a new search of the optimal values of $Vref_V$ and $Vref_I$ and permanently store these values in the second OTP.

At device power-on the values of $Vref_V$ and $Vref_I$ depend on the OTP status:

– if the IC non-volatile memory has never been burned (i.e. no value has ever been permanently stored in OTP memories) $Vref_V$ and $Vref_I$ are initialized at the default values (see *Table 6* and *Table 7*)

– if the IC non-volatile memory has been burned a first time (i.e. values stored in the first OTP) $Vref_V$ and $Vref_I$ are the values selected and stored by the user during the first trimming process

– if the IC non-volatile memory has been burned a second time (i.e.values stored in the second OTP) $Vref_V$ and $Vref_I$ are the values selected and stored by the user during the second trimming process

The device is provided with an $I^2C$ slave-only interface that requires only two pins for the communication: DATA and CLOCK. The $I^2C$ interface allows the user to access the device in a simple way, using the $I^2C$-bus, also assuring robust data communication integrity thanks to an additional parity check control.

Two wires, serial data and serial clock, carry information between the devices connected to the $I^2C$ bus. SEA01 can operate only as an $I^2C$-slave, i.e. it needs to be addressed by a master (a microcontroller, industrial PC, ATE, etc.) that initiates a data transfer on the bus and generates the clock signal to permit that transfer. Generation of clock signals on the $I^2C$-bus is always the responsibility of the master. SEA01 can operate as either a receiver or transmitter (transmitter-slave) depending on the command received from the master. The serial data and serial clock are bidirectional lines connected to a positive supply voltage through a pull-up resistor: SEA01 has an internal pull-up on the DATA and CLOCK pins in order to pull HIGH the pins when they are floating, but the user has to implement an adequate pull-up of the lines using external pull-up resistors. When the bus is free, both lines are HIGH. The data on the serial data line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the serial clock line is LOW.

Within the procedure of the $I^2C$-bus, unique situations arise which are defined as START (S) and STOP (P) conditions. A HIGH-to-LOW transition on the serial data line while the serial clock is HIGH is one such unique case. This situation indicates a START condition. A LOW-to-HIGH transition on the serial data line while the serial clock line is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical

- every byte put on the serial data line is 8 bits long
- each byte is followed by an acknowledge bit
- data is transferred with the most significant bit (MSB) first
- data transfer with acknowledge is obligatory

The acknowledge-related clock pulse is generated by the master. The transmitter releases the serial data line (HIGH) during the acknowledge clock pulse. The receiver pulls down the serial data line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. Of course, setup and hold time must also be taken into account.

When SEA01 is addressed, it generates an acknowledge after each byte has been received. When SEA01 doesn't acknowledge its address, the data line is left HIGH by the device. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a SEA01-receiver does acknowledge its address but, sometime later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by SEA01 generating the not-acknowledge on the first byte to follow. SEA01 leaves the data line HIGH and the master generates a STOP or a repeated START condition. If a master-receiver is involved in a transfer, it must signal the end of data to the slave- transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

Data transfers have the following format: after the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address the slave without first generating a STOP condition.

## 3.2 Device address

The device is provided with the following fixed 7-bit address, while the $8^{th}$ bit is the data direction (R/W).

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| A1 | A2 | A3 | A4 | A5 | A6 | A7 | R/W |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1/0 |

This address corresponds to <52> Hex.

## 3.3 Device commands

The commands are implemented with a one-byte word including a bit for parity check (LSB).

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| C1 | C2 | C3 | C4 | C5 | C6 | C7 | C8 |

C8 = parity check bit.

The parity check has the following structure.

$C8 = C1 \oplus C2 \oplus C3 \oplus C4 \oplus C5 \oplus C6 \oplus C7$.

The possible commands are summarized in *Table 5*. If the device receives a command not specified in *Table 5* or in case of failure of parity check, no command is executed and a fail flag is internally activated.

**Table 5. Command mapping**

| | Command code | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **C1** | **C2** | **C3** | **C4** | **C5** | **C6** | **C7** | **C8** |
| Emulate/read $Vref_V$ | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Emulate/read $Vref_I$ | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| Write NVM | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| Reload NVM | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

C8 = parity check bit data.

The data are implemented with a one-byte word including a bit for parity check (LSB).

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 |

D8 = parity check bit.

The parity check has the following structure.

$D8 = D1 \oplus D2 \oplus D3 \oplus D4 \oplus D5 \oplus D6 \oplus D7$.

If the parity bit check is not correct, the data is not acquired, and the value on $Vref_V$ or $Vref_I$ (depending on the command) will be not updated. An internal parity fail flag is activated and it is not possible to execute any command before a read command.

## 3.4 Emulation commands

It is possible to change both $Vref_V$ and $Vref_I$ values by writing to the volatile memory ($Vref_V$ and $Vref_I$ register) before deciding to permanently store the values in the device.

Changing $Vref_V$ and $Vref_I$ is done independently.

### 3.4.1 Emulate $Vref_V$

The command “emulate $Vref_V$” writes data in the volatile $Vref_V$ register. It is a write command and corresponds to the code given in *Table 5*.

| | Start/stop | Byte 1 (address, write type) | | | | | | | | Ack | Byte 2: command | | | | | | | | Ack | Byte 3: write data | | | | | | | | Ack | Start/stop |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Emulate $Vref_V$ | S | A1 | A2 | A3 | A4 | A5 | A6 | A7 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | pck | 0 | P |

| x | Sent by slave (device) |
|---|---|

| x | x | Sent by master |
|---|---|---|

The value of $Vref_V$ is changed according to the data sent (see *Table 6*). The 8$^{th}$ bit D8 is the parity check bit.

**Table 6. $Vref_V$ values**

| Data bits | | | | | | | | Trim step [%] | $Vref_V$ value [V] |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | Default(1) | | |
| | | | | | | | | | |
| MSB | | | | | | | LSB | | |
| D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 (pck) | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2.500 default (1) (2) |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0.2 | 2.505 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0.4 | 2.510 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0.6 | 2.515 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0.8 | 2.520 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 2.525 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1.2 | 2.530 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1.4 | 2.535 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1.6 | 2.540 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1.8 | 2.545 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 2 | 2.550 |

**Table 6. $Vref_V$ values (continued)**

| Data bits | | | | | | | | Trim step [%] | $Vref_V$ value [V] |
|---|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Default**(1) | | |
| | | | | | | | | | |
| **MSB** | | | | | | | **LSB** | | |
| **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** | **D8 (pck)** | | |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 2.2 | 2.555 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 2.4 | 2.560 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 2.6 | 2.565 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 2.8 | 2.570 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 3 | 2.575 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | -0 | 2.500 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | -0.2 | 2.495 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | -0.4 | 2.490 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | -0.6 | 2.485 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | -0.8 | 2.480 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | -1 | 2.475 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | -1.2 | 2.470 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | -1.4 | 2.465 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | -1.6 | 2.460 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | -1.8 | 2.455 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | -2 | 2.450 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | -2.2 | 2.445 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | -2.4 | 2.440 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | -2.6 | 2.435 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | -2.8 | 2.430 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | -3 | 2.425 |

1. The device is initialized with the default value of 0000000 (i.e. the 0% trim value for $Vref_V$). If the device has already been burned once, the default value is the one stored in the first OTP memory.
2. The 0% trim value was assumed 2.5 V as an example, but this value can be in the range [2.48 V, 2.52 V]. The trimming range is proportional to the trimming value [-3% , + 3%] with a trimming step of 0.2% referenced to the 0% trim value.

If the parity check fails (command or data), the command is not executed ($Vref_V$ register doesn't change) and the internal parity fail flag is activated. If the parity fail flag was activated from the previous communication, the command is not executed even if the parity check is ok. To reset the parity fail flag the user has to perform a read command.

If the parity check is ok, $Vref_V$ is changed according to the content in the $Vref_V$ register resulting in a direct change from the old to the new value.

### 3.4.2 Emulate $Vref_I$

The command “emulate $Vref_I$” writes data in the volatile $Vref_I$ register. It is a write command and corresponds to the code given in *Table 5*.

| | Start/stop | Byte 1 (address, write type) | | | | | | | | Ack | Byte 2: command | | | | | | | | Ack | Byte 3: write data | | | | | | | | Ack | Start/stop |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Emulate $Vref_I$ | S | A1 | A2 | A3 | A4 | A5 | A6 | A7 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | pck | 0 | P |

| x | Sent by slave (device) |
|---|---|

| x | x | Sent by master |
|---|---|---|

The value of $Vref_I$ is changed according to the data sent (see *Table 7*).

The 8th bit D8 is the parity check bit.

**Table 7. $Vref_I$ values**

| Data bits | | | | | | | | Trim step [%] | $Vref_I$ value [mV] |
|---|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Default (1)** | | |
| | | | | | | | | | |
| **MSB** | | | | | | | **LSB** | | |
| **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** | **D8 (pck)** | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 30 default (1) (2) |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3.3 | 31 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 6.6 | 32 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 10 | 33 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 13.3 | 34 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 16.6 | 35 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 20 | 36 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 23.3 | 37 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 26.6 | 38 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 30 | 39 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 33.3 | 40 |

**Table 7. Vref$_I$ values (continued)**

| Data bits | | | | | | | | Trim step [%] | Vref$_I$ value [mV] |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | Default [(1)] | | |
| MSB | | | | | | | LSB | | |
| D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 (pck) | | |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 36.6 | 41 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 40 | 42 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 43.3 | 43 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 46.6 | 44 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 50 | 45 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 30 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | -3.3 | 29 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | -6.6 | 28 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | -10 | 27 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | -13.3 | 26 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | -16.6 | 25 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | -20 | 24 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | -23.3 | 23 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | -26.6 | 22 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | -30 | 21 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | -33.3 | 20 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | -36.6 | 19 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | -40 | 18 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | -43.3 | 17 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | -46.6 | 16 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | -50 | 15 |

1. The device is initialized with the default value of 0000000 (i.e. 0% trim value of Vrefl). If the device has already been burned once, the default value is the one stored in the first OTP memory.
2. The 0% trim value was assumed 30 mV as an example but this value can be in the range [27 mV, 33 mV]. The trimming range is proportional to the trimming value [-50% + 50%] with a trimming step of 3.3% referenced to the 0% trim value.

If the parity check fails (command or data), the command is not executed (Vref$_I$ register doesn't change) and the internal parity fail flag is activated. If the parity fail flag was activated from the previous communication, the command is not executed even if the parity check is ok. To reset the parity fail flag the user has to perform a read command.

If the parity check is ok, Vref$_I$ is changed according to the content in the Vref$_I$ register resulting in a direct change from the old to the new value.

## 3.5 Read commands and status register

It is possible to read the content of the volatile memory and also the status of the NVM memory (two OTP), that indicates how many times the NVM has been burned (zero, one or two) or if a an error occurred during the trimming process (Status register) (see *Table 8*).

**Table 8. Status register**

| Status register | | NVM write residual possibility | Parity fail flag |
|---|---|---|---|
| **M1** | **M2** | | |
| 0 | 0 | 2 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | X | 1 |

The read command of the volatile memory can be used to check the value written in the volatile memory before permanently storing it, increasing the robustness of the trimming process. As described in *Section 3.4: Emulation commands*, the read of the non-volatile memory is necessary to reset the internal parity fail flag eventually activated by a communication error during the trimming process.

### 3.5.1 Read $Vref_V$

The command “read $Vref_V$” reads data from the volatile $Vref_V$ register and the OTP status register. It is a write/read command and corresponds to the code given in *Table 5*

Once the device receives the Emulate/read $Vref_V$ command, in order to perform a read, it is necessary to send a repeated start (Sr) and address as a read, i.e. with the 8th bit (R/W) set to 'one'. The device will send to the data bus an 8-bit word where the first two bits are the status register bit M1 and M2 and the following 6 bits are the value of $Vref_V$ with the parity check as the last bit.

| | Start/stop | Byte 1 (address, write type) | | | | | | | | Ack | Byte 2 command | | | | | | | | Ack | Start/stop | Byte 3 (address, read type) | | | | | | | | Ack | Byte 4 read data | | | | | | | | Nack | Start/stop |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read $Vref_V$ | S | A1 | A2 | A3 | A4 | A5 | A6 | A7 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | S | A1 | A2 | A3 | A4 | A5 | A6 | A7 | 1 | 0 | M1 | M2 | D3 | D4 | D5 | D6 | D7 | pck | 1 | P |

| | | |
|---|---|---|
| x | x | Sent by slave (device) |
| x | x | Sent by master |

In case of a communication error, the content of status register is <11>, which means that the internal parity flag fail was activated. After a read command is executed, the parity flag fail is reset and a new command can be executed by the device.

### 3.5.2 Read $Vref_I$

The command "read $Vref_I$" reads data from the volatile $Vref_I$ register and the OTP status register. It is a write/read command and corresponds to the code given in *Table 5*.

Once the device receives the Emulate/read $Vref_I$ command, in order to perform a read, it is necessary to send a repeated start (Sr) and address as a read, i.e. with the $8^{th}$ bit (R/W) set to 'one'. The device will send to the data bus an 8-bit word where the first two bits are the status register bit M1 and M2 and the following 6 bits are the value of $Vref_I$ with parity check as last bit.

| | Start/stop | Byte 1 (address, write type) | | | | | | | | Ack | Byte 2 command | | | | | | | | Ack | Start/stop | Byte 3 (address, read type) | | | | | | | | Ack | Byte 4 read data | | | | | | | | Nack | Start/stop |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read $Vref_I$ | S | A1 | A2 | A3 | A4 | A5 | A6 | A7 | 0 | 0 | 1 | 0 | 0 | | 0 | 1 | 1 | 1 | 0 | Sr | A1 | A2 | A3 | A4 | A5 | A6 | A7 | 1 | 0 | M1 | M2 | D3 | D4 | D5 | D6 | D7 | pck | 1 | P |

| | | | | | |
|---|---|---|---|---|---|
| x | x | Sent by slave (device) | x | x | Sent by master |

In case of a communication error, the content of the status register is <11>, which means that the internal parity flag fail was activated. After a read command is executed, the parity flag fail is reset and a new command can be executed by the device.

## 3.6 Write NVM (OTP)

After $Vref_V$ and $Vref_I$ have been trimmed to the desired level, the user can confirm their values and store them permanently.

The presence of two OTP allows the user to repeat the trimming procedure a second time and change the value previously stored in the device. Please note that when the user starts from an IC already burned once, the default values of $Vref_V$ or $Vref_I$ are the ones stored in the first OTP.

This is virtually a real-time trim-and-test without switching off the supply. It is important that during the entire process the supply voltage of the IC never falls below its UVLO level, otherwise, the settings stored in the volatile memory will be lost and the IC will return to the default setting or the values stored in the first OTP. It is also necessary that the burn command is executed with Vcc = 19 V with a current capability of 90 mA.

If the search for the best value of $Vref_V$ and $Vref_I$ is done with a Vcc value lower than 19 V, the user has to pay attention that, during the step-up of Vcc before the burning of the NVM, a negative ringing on Vcc will cause a drop below the UVLO of the IC.

The user can eventually decide to perform the search for the best value of $Vref_V$ and $Vref_I$, storing these values in an external memory (ATE, industrial PC, etc.), then increasing Vcc to 19 V and waiting to have a stable Vcc level. The user can then resend the selected value of $Vref_V$ and $Vref_I$ stored in the external memory before sending the burn NVM command.

Both values written in the $Vref_V$ & $Vref_I$ register (volatile memory) are permanently stored in the NVM (OTP) in a single step.

It is possible to burn the NVM by sending the burn command (write) given in *Table 5* followed by a data byte with the same code as a burn command.

| | Start/stop | Byte 1 (address, write type) | | | | | | | | Ack | Byte 2: command | | | | | | | | Ack | Byte 3 (address, read type) | | | | | | | | Ack | Start/stop |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write NVM | S | A1 | A2 | A3 | A4 | A5 | A6 | A7 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | P |

| | |
|---|---|
| x | Sent by slave (device) |

| | | |
|---|---|---|
| x | x | Sent by master |

It is important to provide a zapping time of at least 45 msec and to have Vcc of the IC equal to 19 V with a current capability of 90 mA, in order to ensure correct blowing of the anti-fuse cells. After the stop (P) the device doesn't acknowledge any $I^2C$ communication for about 45 ms in order to perform the burning of the NVM.

To protect the NVM memory from an incorrect write, if the parity fail flag was activated, i.e. an error occurred during the trimming process, the burn command is not executed.

The NVM is written only if it was never written or written one time. If the NVM is written a second time, the previous content is lost.

Please note that after a Write NVM command the Status Register is not automatically updated. It must be updated by turning off and on again the IC or by sending a Reload NVM command to the device. Once the update is performed, the number of times the IC has been burned can be read from the status register.

## 3.7 Reload NVM (OTP)

During the trimming process if the user has changed the value of $Vref_V$ or $Vref_I$ with the emulation command and wants to reload the content stored in the NVM, he can use the “Reload NVM” command which is a write command that reloads the NVM into the $Vref_V$/$Vref_I$ registers (volatile memory).

| | Start/stop | Byte 1 (address, write type) | | | | | | | | Ack | Byte 2 command | | | | | | | | Ack | Start/stop |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reload NVM | S | A1 | A2 | A3 | A4 | A5 | A6 | A7 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | P |

| | |
|---|---|
| x | Sent by slave (device) |

| | | |
|---|---|---|
| x | x | Sent by master |

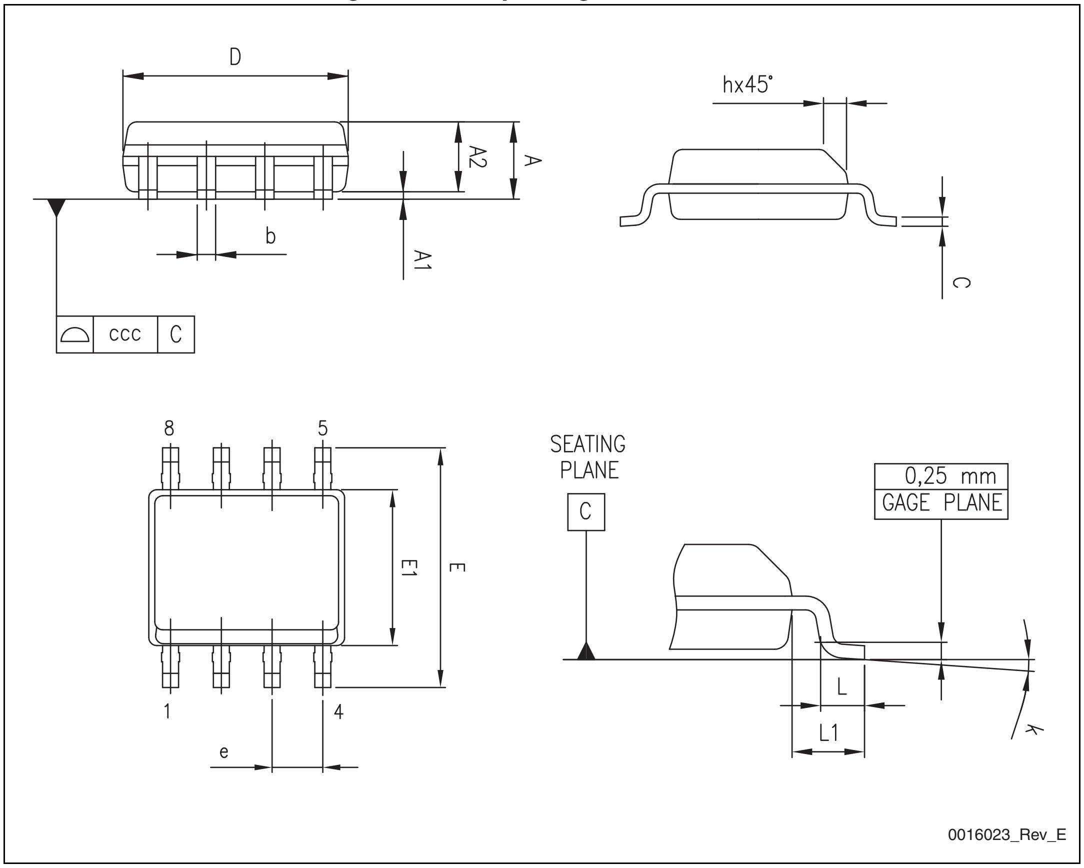
# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

**Table 9. SO8 mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | **Min.** | **Typ.** | **Max.** |
| A | | | 1.75 |
| A1 | 0.10 | | 0.25 |
| A2 | 1.25 | | |
| b | 0.28 | | 0.48 |
| c | 0.17 | | 0.23 |
| D | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | | 1.27 | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| L1 | | 1.04 | |
| k | 0° | | 8° |
| ccc | | | 0.10 |

**Figure 5. SO8 package dimensions**



# 5 Ordering information

**Table 10. Ordering information**

| Order code | Package | Packaging |
|---|---|---|
| SEA01 | SO8 | Tube |
| SEA01TR | | Tape and reel |

# 6 Revision history

**Table 11. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 07-May-2013 | 1 | Initial release. |