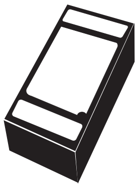
SPT02-236DDB

Automation sensor transient and overvoltage protection

**Datasheet − production data**



µQFN-2L
SPT02-236DDB

## Features

- Double diode array for switch protection and reverse blocking protection
- 6 V to 36 V supply voltage range
- Minimum breakdown voltage $V_{BR}$: 38 V
- 8/20 µs 2 A maximum clamping voltage: 46 V
- Blocking diode drop forward voltage $V_F$: 1.1 V at 300 mA
- Blocking diode maximum 10 ms square pulse current $I_{FSM}$: 3 A
- Ambient temperature: -40 °C to +100 °C
- µQFN 2L 0.8 mm flat package

### Complies with following standards

- Voltage surge: IEC 61000-4-5, $R_{CC}$ = 500 Ω, ±1 kV
- Electrostatic discharge, IEC 61000-4-2:
  – ±8 kV contact discharge
  – ±15 kV air discharge
- Electrical transient immunity: IEC 61000-4-4: ±2 kV

### Benefits

- Compliant for interface with logic input type 1, 2 and 3 IEC 61131-2 standard
- Highly compact with integrated power solution in SMD version

## Applications

- Factory automation sensor application
- Proximity sensor interface protection
- Transient and surge voltage protection
- Compliant with sensor standard, EN 60947-5-2

## Description

The SPT02 is specifically designed for the protection of 24 V proximity sensors. It implements the reverse polarity and the overvoltage protection of the sensor power supply and the power switch overvoltage protection.

It provides a very compact and flexible solution.

Thanks to high performance ST technology, the SPT02 protects the proximity sensor to the highest level compliant with IEC 61000-4-2, IEC 61000-4-4 and IEC 61000-4-5 standards.

**Figure 1. Functional diagram (top view)**

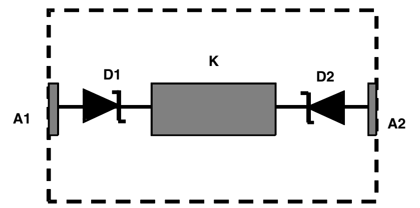
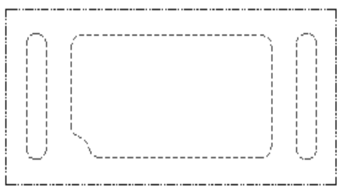
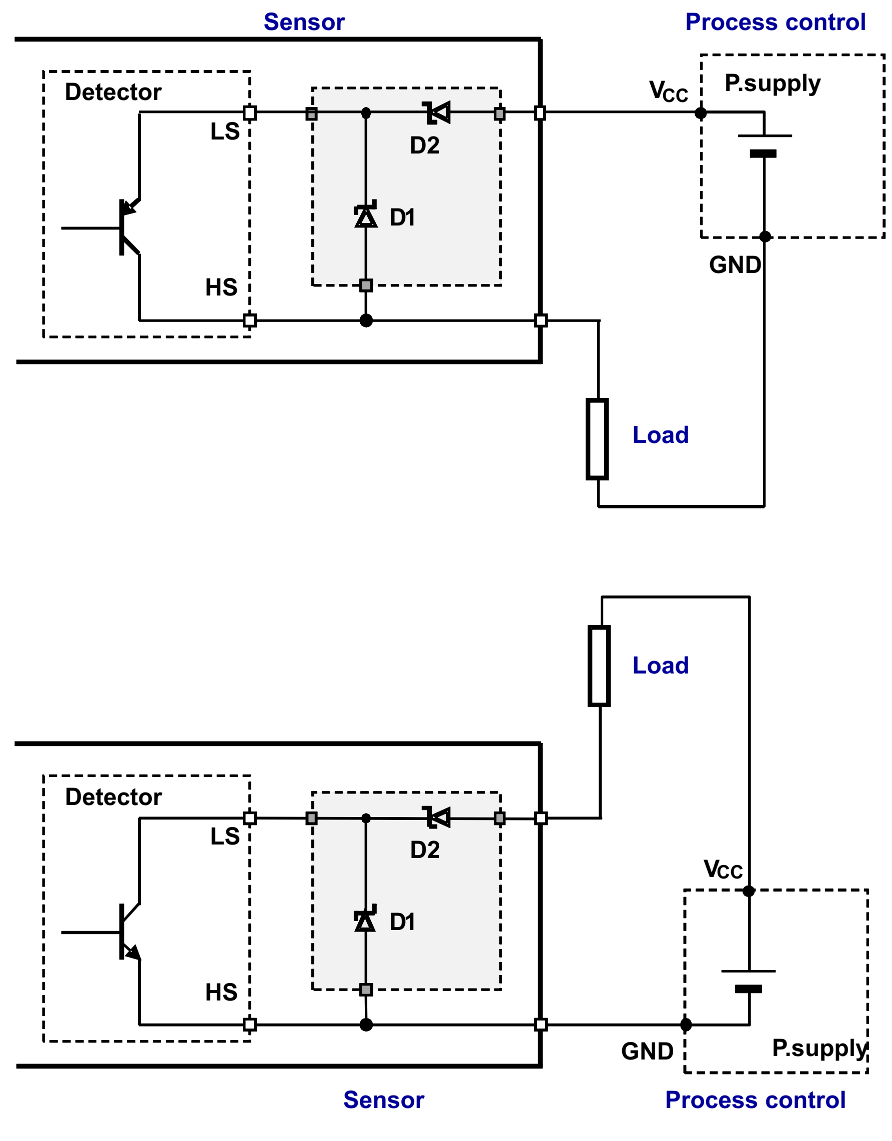



**Figure 2. Bottom view**



# 1 Basic application

**Figure 3. STP02 configuration**



# 2 Characteristics

**Table 1. Pinout connections(1)**

| Symbol | Description |
|---|---|
| K | D1 power bus protection diode cathode and D2 reverse blocking protection cathode |
| A1 | D1 power bus protection diode anode |
| A2 | D2 reverse blocking protection anode |

1. See *Figure 1*

**Table 2. Absolute ratings ($T_{amb}$ = 25 °C)**

| Symbol | Diode | Parameter | Value | Unit |
|---|---|---|---|---|
| $V_{PP}$ | All | ESD protection, IEC 61000-4-2, per diode, in air (1) | 30 | kV |
| | | ESD protection, IEC 61000-4-2, per diode, in contact (1) | 30 | kV |
| $V_{PP}$ | All | Peak Surge Voltage, IEC 61000-4-5, per diode, $R_{CC}$ = 500 Ω, (1) | 1 | kV |
| $P_{PP}$ | All | Peak pulse current, $T_J$ = $T_{amb}$ = 85 °C, $t_P$ = 8/20 µs | 1400 | W |
| $I_{PP}$ | All | Peak pulse power dissipation, $T_J$ = $T_{amb}$ = 85 °C, $t_P$ = 8/20 µs | 25 | A |
| $I_{FSM}$ | All | Maximum forward surge current, $t_P$ = 10 ms square | 3 | A |
| $E_{AR}$ | D1 | Maximum repetitive avalanche energy L= 1 H, $I_{RAS}$= 0.3A, $R_S$ = 100 Ω, $V_{CC}$ = 30 V, $T_{amb}$ = 85 °C, (1) | 66 | mJ |
| $T_J$ | All | Storage junction temperature range | - 40 to 150 | °C |

1. See system oriented test circuits in *Figure 5* (ESD) and *Figure 4* (Surge as also described in IEC 60947-5-2).

**Table 3. Recommended operating conditions**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Operating power bus supply voltage | -30 to 35 | V |
| | Pulse repetitive voltage $t_P$ = 0.5 s, $R_{CC}$ = 500 Ω | -30 to 37 | V |
| $I_F$ | D2 forward peak current $T_j$ = 150 °C duty cycle = 50% | 300 | mA |
| $T_{amb}$ | Operating ambient temperature range | -40 to 100 | °C |
| $T_J$ | Operating junction temperature range(1) | -40 to 150 | °C |

1. Extended from DC operating at 150 °C up to peak repetitive value during the inductive load demagnetization

**Table 4. Thermal resistance**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| Rth(j-a) | SMD thermal resistance junction to ambient, per diode<br>FR4 board, copper thickness = 35 µm, recommended footprint | 230 | °C/W |
| Zth(j-a) | SMD thermal transient impedance junction to ambient, per diode<br>$t_p$ = 15 ms, $T_{amb}$ = 85 °C, recommended footprint | 6.5 | °C/W |

**Table 5. Electrical characteristics ($T_J$ = 25 °C, unless otherwise specified)**

| Symbol | Diode | Name | Test conditions | | Value | Unit |
|---|---|---|---|---|---|---|
| $V_{RM}$ | ALL | Reverse stand off voltage | $I_R$ = 200 nA | MIN | 33 | V |
| | | | $I_R$ = 1 µA | MIN | 36 | |
| $I_{RM}$ | ALL | Leakage reverse current | $V_{RM}$ = 36 V(1) | MAX | 1 | µA |
| | | | $V_{RM}$ = 36 V,<br>$T_J$ = 150 °C | MAX | 5 | µA |
| $V_{BR}$ | ALL | Reverse breakdown voltage | $I_R$ = 1 mA | MIN | 38 | V |
| | | | | TYP | 41.4 | V |
| $V_{CL}$ | ALL | Peak clamping voltage | $I_{PP}$ = 2 A,<br>$t_P$ = 8 /20 µs | MAX | 46 | V |
| | | | | TYP | 44 | V |
| $R_D$ | ALL | 8/20µs dynamic resistance | | TYP | 0.5 | Ω |
| αT | ALL | $V_{BR}$ Temperature sensitivity(2) | | MAX | 17 | $10^{-4}$ /°C |
| $V_{CL}$ | D1 | Peak clamping voltage | $I_R$ = 0.3 A, L = 1 H,<br>$V_{CC}$ = 30 V | MAX | 46 | V |
| $V_F$ | D2 | Forward drop voltage | $I_F$ = 300 mA | MAX | 1.1 | V |

1. Voltage applied at the nodes of each diode
2. $V_{BR}$ @ $T_J$ = $V_{BR}$ @25 °C x (1+ αT x ($T_J$ - 25))

# 3 System related electromagnetic compatibility ratings

Figure 4. Surge Voltage test circuit according to IEC 61000-4-5 with 500 Ω serial resistor

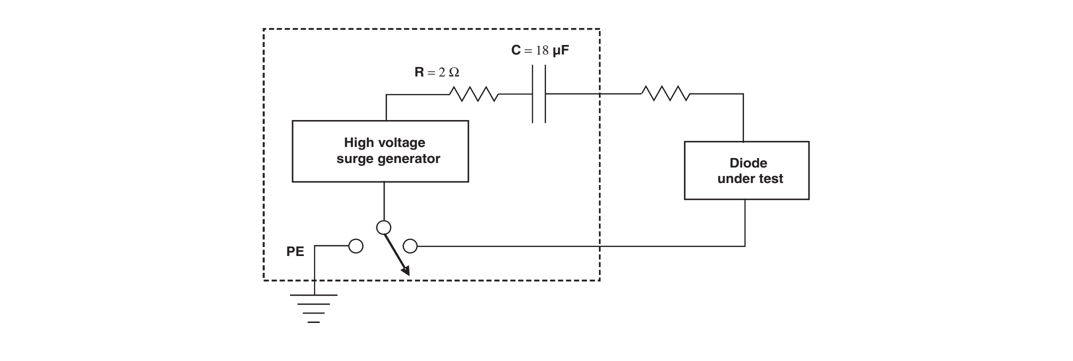



Figure 5. ESD test circuit according to IE 61000-4-2

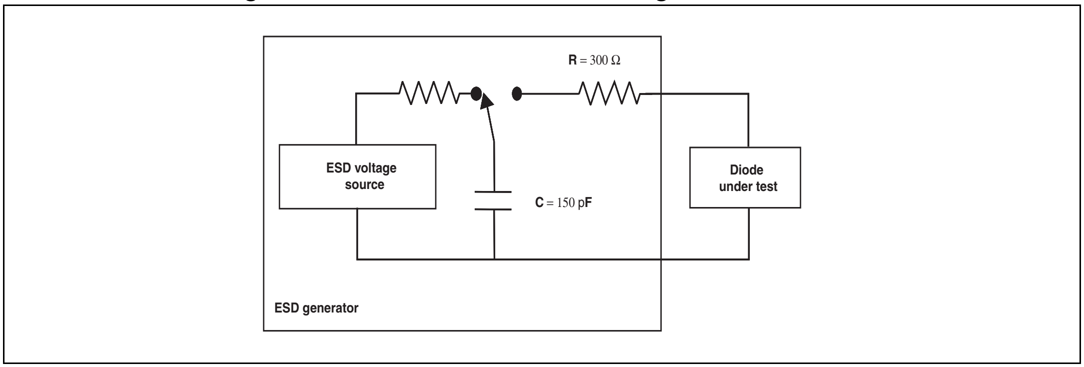
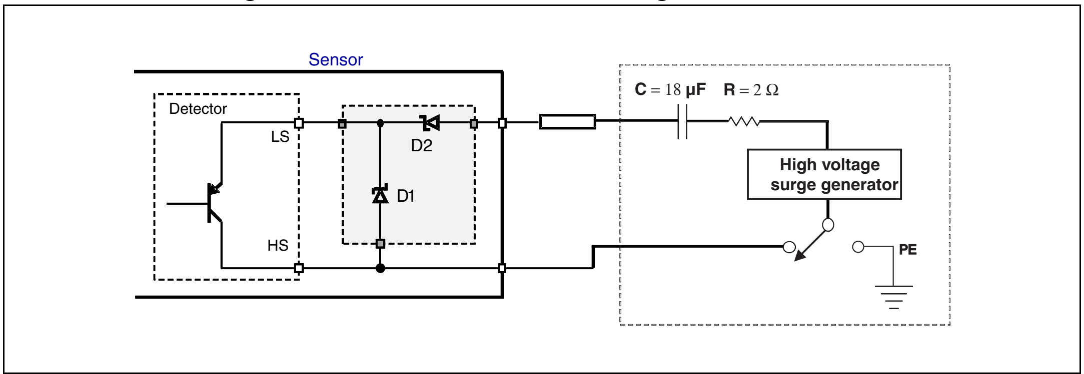



Figure 6. EOS test circuit according to IE 61000-4-5




# 4 Evaluation of the clamping voltage

$V_{BR} (T_J) = V_{BR} (25) \times (1+ \alpha T (T_J - 25))$

$V_{CL\ MAX} (8/20\ \mu s) = V_{BR\ MAX} + R_D \times I_{PP}$

# 5 Application considerations

## 5.1 Demagnetization of an inductive load driven by the switch protection diode.

The turn off energy EOFF that could be dissipated in the D1 diode is calculated as shown in AN587 and AN1351 application notes:

$E_{OFF} = V_{BR} \times L / / (R_S)^2 \times [V_{CC} + (V_{CC} - V_{BR}) \times \ln (V_{BR} / (V_{BR} - V_{CC}))]$

$t_{OFF} = L \times \ln (V_{BR} / (V_{BR} - V_{CC})) / R_S$

$P_{OFF} = E_{OFF} / t_{OFF}$

With L = 1 H; I = 0.3 A; $V_{BR}$ = 39 V; $V_{CC}$ = 30 V, $R_S$ = 100 Ω the stress withstood by $D_1$ becomes:

$E_{OFF}$ = 65 mJ; $t_{OFF}$ = 15 ms; $P_{OFF}$ = 4.3 W

In a single pulse mode operation, the junction temperature can be fairly estimated:

$T_J = T_{amb} + [Z_{TH} (t_{OFF}) \times P_{OFF}]$

In a repetitive operation with an F repetitive rate,

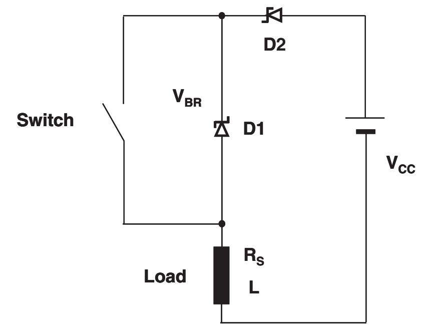
$P_{AV} = E_{OFF} \times F$

$T_{J\_AV} = T_{amb} + P_{AV} \times R_{TH\_JA}$

And during the demagnetization $t_{OFF}$, $T_{J\_PK} < T_{J\_AV} + P_{OFF} \times Z_{TH} (t_{OFF})$

$Z_{TH}$ is the transient thermal impedance of each diode for a pulse having a duration $t_{OFF}$.

**Figure 7. Electrical diagram for inductive load demagnetization**




## 5.2 Life time considerations

Life time of the product is calculated to exceed 10 years. The key parameters to consider are the ambient temperature ($T_{amb}$ < 100 °C), the power supply voltage ($V_{CC}$ < 30 V), and the current in the reverse blocking diode ($I_F$ = 0.1 A switching at 0.5 Hz with 50% duty cycle, the stand-by current being less than 1.5 mA).

For higher current or higher switching frequency operation, the life time should be calculated considering the peak and average junction temperature.

# 6 Package information

- Epoxy meets UL94,V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

**Figure 8. µQFN-2L dimensions (definitions)**

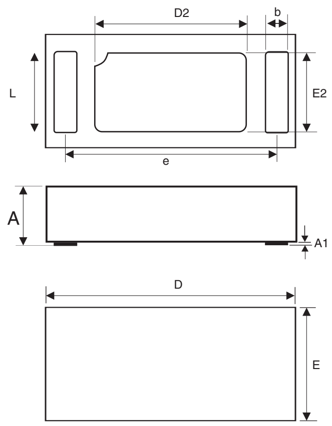
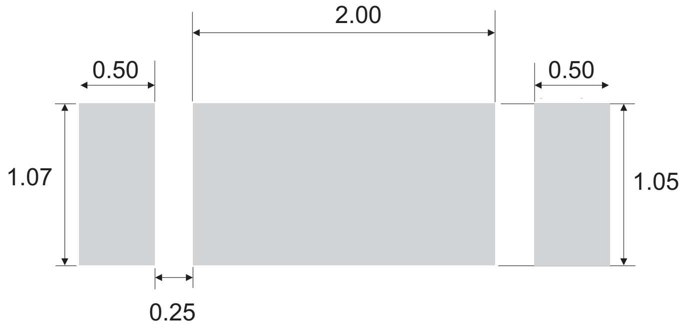



**Table 6. µQFN-2L dimensions (values)**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.70 | 0.75 | 0.80 | 0.027 | 0.029 | 0.031 |
| A1 | 0.00 | 0.02 | 0.05 | 0.00 | 0.001 | 0.002 |
| b | 0.25 | 0.30 | 0.35 | 0.010 | 0.011 | 0.014 |
| D | - | 3.30 | - | - | 0.13 | - |
| D2 | 1.85 | 2.00 | 2.10 | 0.073 | 0.079 | 0.082 |
| E | - | 1.50 | - | - | 0.06 | - |
| E2 | 0.90 | 1.05 | 1.16 | 0.035 | 0.041 | 0.046 |
| e | - | 2.8 | - | - | 0.110 | - |
| L | 0.97 | 1.07 | 1.18 | 0.038 | 0.042 | 0.046 |

Figure 9. Footprint (dimensions in mm)

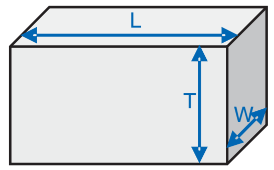


# 7 Recommendation on PCB assembly

## 7.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

**Figure 10. Stencil opening dimensions**




   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1,5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0,66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

## 7.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

## 7.3 Placement

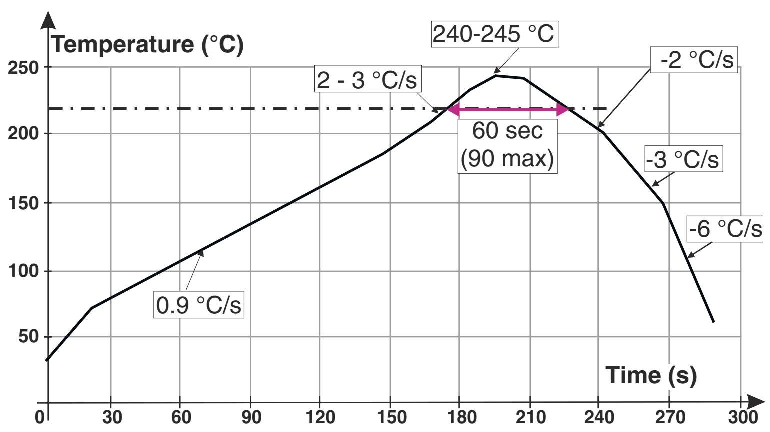
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

## 7.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

## 7.5 Reflow profile

**Figure 11. ST ECOPACK® recommended soldering reflow profile for PCB mounting**




*Note:* *Minimize air convection currents in the reflow oven to avoid component movement.*
*Compliant with J-STD-020D soldering profile*

# 8 Ordering information

**Figure 12. Ordering information scheme**

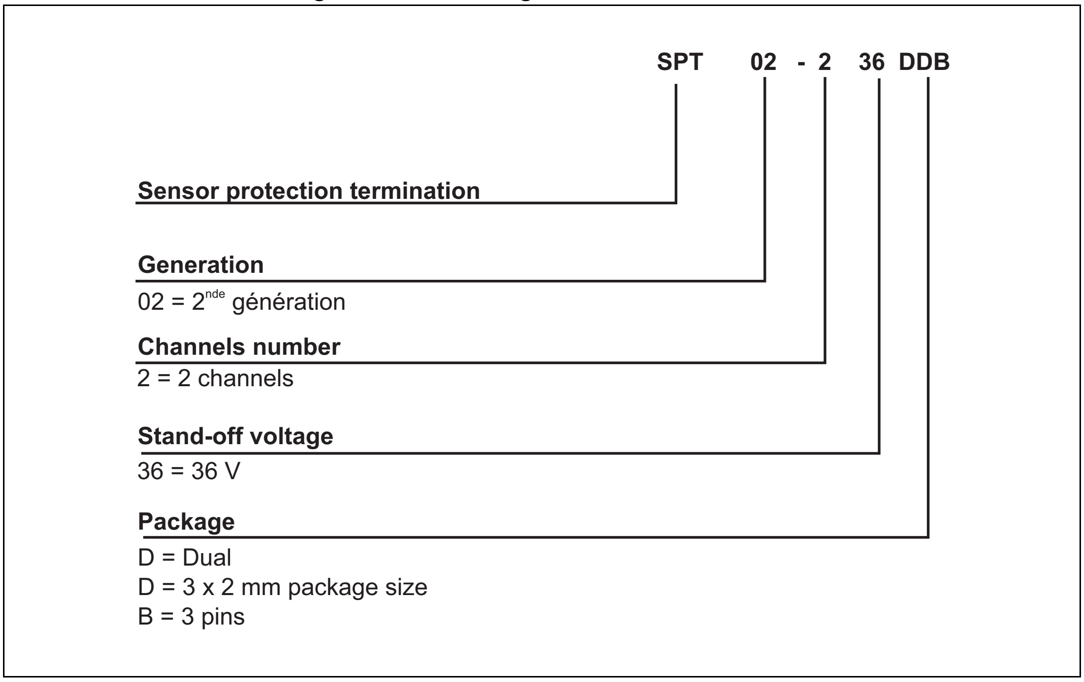



**Table 7. Ordering information**

| Order code | Marking | Package | Weight | Packing |
|---|---|---|---|---|
| SPT02-236DDB | S2 | µQFN-2L with exposed pad | 15.55 mg | Tape and reel |

# 9 Revision history

**Table 8. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 06-May-2013 | 1 | First issue |
| 21-Mar-2014 | 2 | Updated *Table 2*, *Table 6* and *Figure 9*. |