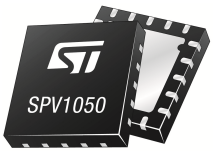
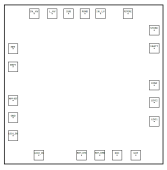
SPV1050

Datasheet

Ultralow power energy harvester and battery charger



VFQFPN 3 x 3 x 1 mm 20L



Die form

Features

- Transformerless thermoelectric generators and PV modules energy harvester
- High efficiency for any harvesting source
- Up to 70 mA output current
- Fully integrated MOSFETs for Boost or Buck-boost configurations
- Selectable enable/disable MPPT functionality
- Programmable MPPT by external resistors
- 2.6 V to 5.3 V trimmable output overvoltage level (± 1% accuracy)
- 2.2 V to 3.6 V trimmable output undervoltage level (± 1% accuracy)
- Two fully independent LDOs (1.8 V and 3.3 V output)
- Enable/disable LDO pins
- Load disconnect function (by-pass transistor open) prior the first start-up (Cold Start) to avoid battery lifetime shortening
- Battery Connected and DC-DC switching open drain indication pins

Application

- Internet of things
- Remote control
- Fleet and livestock tracking
- Agriculture sensors
- Toll-pay
- Electronic labels
- Smart watch and wearable.

Product status link

SPV1050

Product label

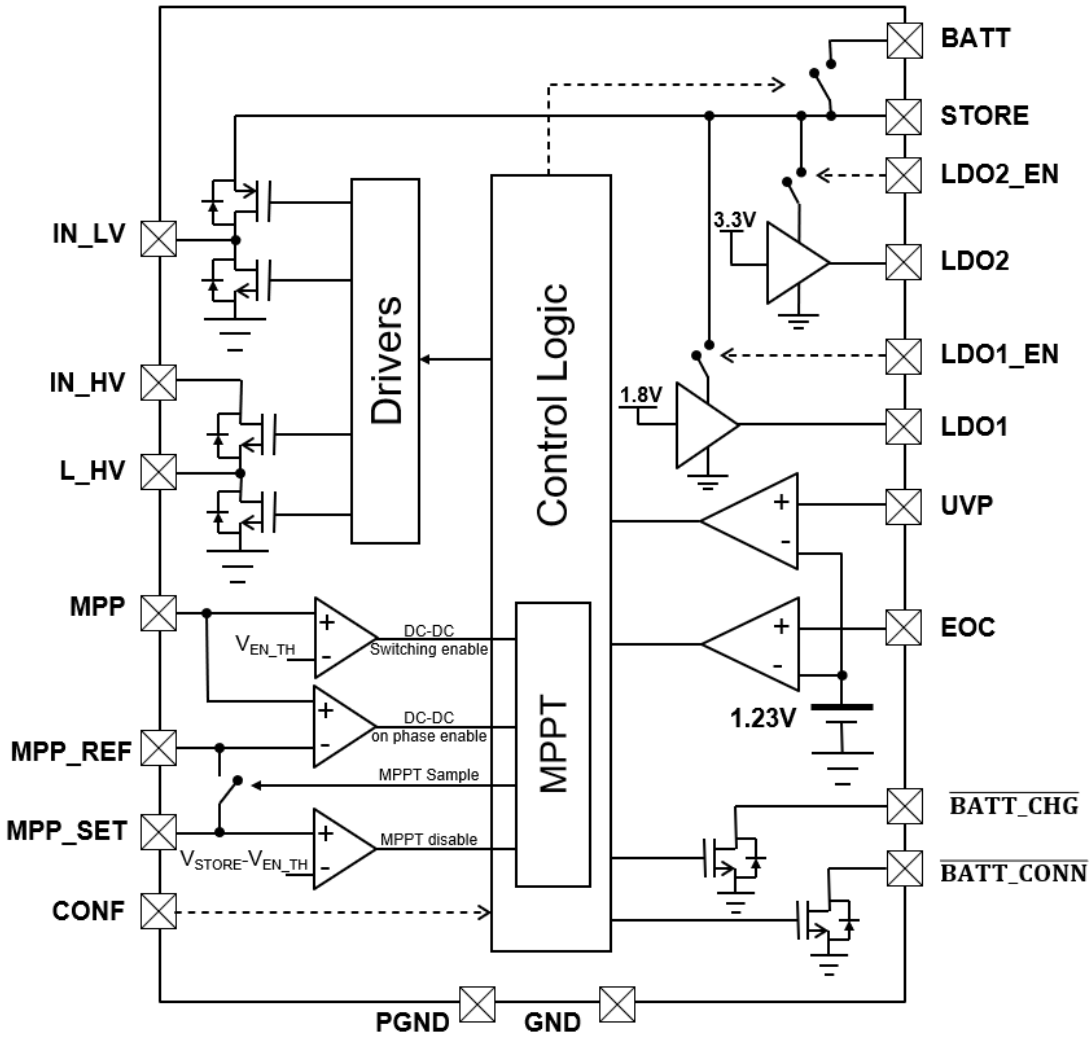
SUSTAINABLE TECHNOLOGY

Description

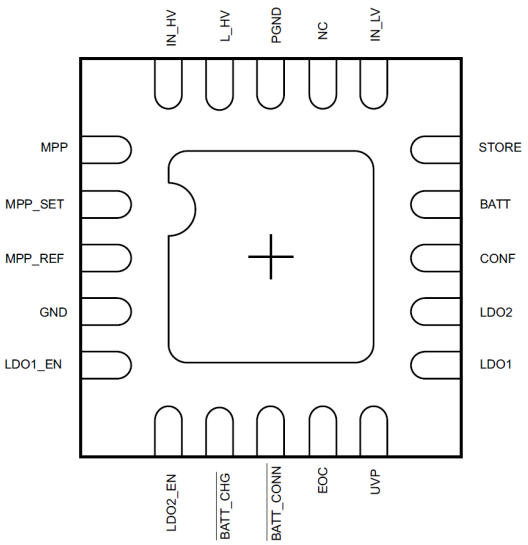
The SPV1050 is an ultra-low power and high-efficiency power manager embedding four MOSFETs for boost or buck-boost DC-DC converter and an additional transistor for the load connection/disconnection.
An internal high accuracy MPPT algorithm can be used to maximize the power extracted from PV panel or TEG.
The internal logic works to guarantee tight monitoring of both the end-of-charge voltage (V_{EOC}) and the minimum battery voltage (V_{UVP}) by opening the pass-transistor at triggering of the V_{EOC} threshold or at triggering of the V_{UVP} threshold to preserve the battery life. Both the V_{EOC} and V_{UVP} thresholds can be trimmed by external resistors connected between the STORE rail and the EOC and UVP pins, respectively.
In boost configuration (CONF pin connected to the supply source), the IC requires 550 mV and 30 µA to Cold start; while after the first start-up the input voltage can range between 150 mV and V_{EOC}. In buck-boost configuration (CONF pin connected to ground), the IC requires 2.6 V and 5 µA at Cold start; while after the first start-up input voltage can range between 150 mV up to 18 V.
The STORE pin is available as unregulated voltage output (e.g. to supply by external LDO a micro-controller), while two fully independent LDOs (1.8 V and 3.3 V) are embedded for powering other companion ICs like MCU, sensors or RF transceivers. Both LDOs can be independently enabled through the related pins.

1 Block Diagram

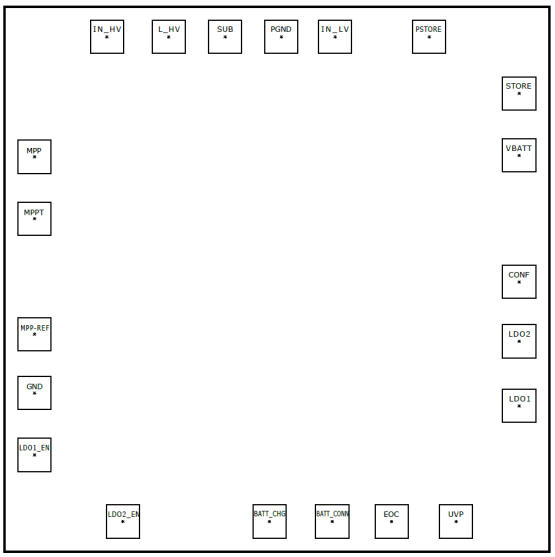
Figure 1. **Block diagram**



2 Pin configurations



VFQFPN 3 x 3 x 1 mm - 20L
(Top Through view)



DIE FORM (Bottom view)

3 Pin description

Pin no. (VFQFPN 20)	Name	Type	Description
1	MPP	I	Input voltage sense pin: to be connected to the voltage source. The connection can be direct or through a ladder resistor, depending on the maximum voltage of the source despite the AMR and operating range of the MPP pin. The switching of the DC-DC is disabled when $V_{MPP} < V_{EN\_TH}$.
2	MPP_SET	I	MPPT enable/disable and setting voltage pin. Connect this pin directly to STORE pin when MPPT function is not required: this configuration ($V_{MPP\_SET} > V_{STORE}$-V_{EN_TH}) inhibits the periodic deactivation of the embedded DC-DC. If MPPT function is required, then connect MPP_SET and MPP pins through a ladder resistor: the MPPT algorithm periodically deactivates the DC-DC for sampling of the open circuit voltage of the source. Typically, the DC-DC is stopped for ~400 ms every ~16 s.
3	MPP_REF	I	Voltage reference pin. The switching of the DC-DC is controlled by internal logic purposing high conversion efficiency, even with low power sources. The switching remains active until $V_{MPP} > V_{MPP\_REF}$. Connecting this pin to ground enables continuous switching of the DC-DC converter, provided that enough power can be supplied by the source. When MPPT function is required, connect this pin to a 10 nF capacitor: at every sampling period (~16 s) this capacitor stores the reference voltage (% of the open circuit voltage of the source) V_{MPP_REF}. When MPPT function is not required, connect this pin to an external voltage reference.
4	GND	GND	Signal ground pin.
5	LDO1_EN	I	If high, enables LDO1 (1.8V).
6	LDO2_EN	I	If high, enables LDO2 (3.3V).
7	$\overline{\text{BATT\_CHG}}$	O	DC-DC operation output flag pin (open drain): if low, it indicates that the DC-DC is switching; if high, it indicates that the DC-DC is not switching.
8	$\overline{\text{BATT\_CONN}}$	O	Embedded pass transistor connection status pin (open drain): if low, it indicates that the pass transistor between the STORE and BATT pins is closed (load connected); if high, it indicates that the pass transistor between the STORE and BATT pins is open (load disconnected).
9	EOC	I	Load overvoltage/battery end of charge protection pin. To be connected to the STORE pin through a resistor divider. Internal DC-DC stops/restarts switching when the voltage at EOC pin is higher/lower than the internal bandgap voltage (V_{BG} = 1.23 V, typical value). Also, at start-up (internal pass transistor between STORE and BATT is still open) and while V_{STORE} is increasing, the triggering of the internal bandgap voltage makes the internal pass transistor gets closed.
10	UVP	I	Load/battery undervoltage protection pin. To be connected to the STORE pin through a resistor divider. Internal pass transistor between STORE and BATT pins opens when the voltage at UVP pin goes below the internal bandgap voltage (V_{BG} = 1.23 V, typical value).
11	LDO1	O	1.8 V regulated output voltage pin.
12	LOD2	O	3.3 V regulated output voltage pin.
13	CONF	I	DC-DC converter configuration pin. Boost configuration: CONF pin connected to the input supply source. Buck-boost configuration: CONF pin connected to ground.
14	BATT	I/O	Load/battery connection pin.

Pin no. (VFQFPN 20)	Name	Type	Description
15	STORE	I/O	Tank capacitor connection pin.
16	IN_LV	I	Low voltage input source. It has to be connected to the inductor for both boost and buck-boost configuration.
17	NC	-	Not connected.
18	PGND	PGND	Power ground pin.
19	L_HV	I	Input pin for buck-boost configuration. Boost configuration: to be connected to ground. Buck-boost configuration: to be connected to the inductor.
20	IN_HV	I	High voltage input source. Boost configuration: to be connected to ground. Buck-boost configuration: to be connected to the input supply source.
EP	Exposed Pad	GND	Connect to ground layer of the application board. It's warmly recommended a direct connection (without any vias) between EP, GND, PGND and the ground net of the tank capacitor on STORE pin.

4 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
IN_LV	Analog input	V_{STORE} + 0.3	V
IN_HV	Analog input	20	V
L_HV	Analog input	IN_HV +0.3	V
CONF	Analog input	5.5	V
MPP	Analog input	5.5	V
MPP_SET	Analog input	5.5	V
MPP_REF	Analog input	5.5	V
BATT	Analog input/output	5.5	V
STORE	Analog input/output	5.5	V
UVP	Analog input	V_{STORE} + 0.3	V
EOC	Analog input	V_{STORE} + 0.3	V
$\overline{BATT\_CONN}$	Digital output	5.5	V
$\overline{BATT\_CHG}$	Digital output	5.5	V
LDO1_EN	Digital input	V_{STORE} + 0.3	V
LDO2_EN	Digital input	V_{STORE} + 0.3	V
LDO1	Analog output	V_{STORE} + 0.3	V
LDO2	Analog output	V_{STORE} + 0.3	V
PGND	Power ground	0	V
GND	Signal ground	-0.3 to 0.3	V
T_J	Junction temperature	-40 to 125	°C
$T_{STORAGE}$	Storage temperature	150	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case	7.5	°C/W
$R_{th(JA)}$ (1)	Thermal resistance junction-ambient	49	°C/W

1. *Measured on 2-layer application board FR4, Cu thickness = 17 um with total exposed pad area = 16 mm^2*

5 Electrical characteristics

V_{STORE} = 4 V; -40 °C < T_J < 85 °C, unless otherwise specified. Voltage with respect to GND, unless otherwise specified

Table 3. Electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
Load/battery operating range							
I_{BATT}	Output current to load/ battery	boost configuration		-	-	70	mA
		buck-boost configuration		30	-	-	
V_{BATT}	BATT pin voltage range			2.2	-	5.3	V
R_{BATT}	Pass transistor resistance	$\overline{BATT\_CONN}$ = low		6	7	8	Ω
Bandgap							
V_{BG}	Internal reference voltage			-	1.23	-	V
	Accuracy			-1	-	+1	%
UVP							
$V_{STORE(UVP)}$	V_{STORE} undervoltage protection range	$(V_{UVP} + UVP_{HYS}) < (V_{EOC} - EOC_{HYS})$		2.2	-	3.6	V
UVP_{HYS}	UVP hysteresis	V_{STORE} rising		-	5	-	%
EOC							
$V_{STORE(EOC)}$	V_{STORE} end-of-charge voltage range	$(V_{UVP} + UVP_{HYS}) < (V_{EOC} - EOC_{HYS})$		2.6	-	5.3	V
EOC_{HYS}	EOC hysteresis	V_{STORE} falling		-	-1	-	%
STORE							
V_{STORE}	STORE pin voltage operating range			$V_{STORE(UVP)}$	-	$V_{STORE(EOC)}$	V
Static current consumption							
I_{SD}	Shutdown current	Shutdown mode: before first start-up or $\overline{BATT\_CONN}$ high T_{AMB} < 60 °C		-	-	1	nA
I_{SB}	Standby current	Standby mode: $\overline{BATT\_CONN}$ low, $\overline{BATT\_CHG}$ high, V_{STORE} = 5.3 V, $V_{MPP} < V_{EN\_TH}$ and LDO1,2_EN low T_{AMB} = 25 °C		-	0.8	-	µA
I_{OP}	Operating current in open load	Operating mode (LDOs in open load), $\overline{BATT\_CONN}$ low, $\overline{BATT\_CHG}$ high, T_{AMB} = 25 °C	LDO1_EN = 1 or LDO2_EN = 1	-	1.7	-	µA
			LDO1_EN = 1 and LDO2_EN = 1	-	2.6	-	
DC-DC converter							
V_{IN-SU}	Cold start minimum input voltage	Boost configuration, $\overline{BATT\_CONN}$ high or at first start-up		-	0.55	0.58	V
		Buck-boost configuration $\overline{BATT\_CONN}$ high or at first start-up		-	2.6	2.8	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SU}	Cold start minimum input current	Boost configuration	-	30	-	µA
		Buck-boost configuration	-	5	-	
V_{EN_TH}	DC-DC switching enable threshold	Voltage checked during T_{SAMPLE}		0.1	0.15	V
V_{IN_LV}	Input voltage range	Boost configuration	V_{EN_TH}	-	V_{EOC}	V
V_{IN_HV}		Buck-boost configuration	V_{EN_TH}	-	18	
$R\text{-}ON_B$	Low-side MOS resistance	Boost configuration	0.5	1.0	1.5	Ω
$SR\text{-}ON_B$	Synchronous rectifier MOS resistance		0.5	1.0	1.5	
$R\text{-}ON_{BB}$	Low-side MOS resistance	Buck-boost configuration	1	1.5	2	Ω
$SR\text{-}ON_{BB}$	Synchronous rectifier MOS resistance		1	1.5	2	
f_{SW}	Maximum allowed switching frequency	Boost and buck-boost configurations	-	-	1	MHz
$UVLO_H$	Undervoltage lockout activation threshold	V_{STORE} increasing	-	2.6	2.8	V
$UVLO_L$	Undervoltage lockout deactivation threshold	V_{STORE} falling	2	2.1	-	V
$I_{L(PEAK)}$	DC-DC input current high peak threshold	DC-DC active and input current rising (T_{AMB} = 25°C)	85		190	mA
$I_{L(ZC)}$	DC-DC output current low threshold	DC-DC active and input current falling (T_{AMB} = 25°C)	0		82	mA
$T_{ON(MAX)}$	DC-DC ON Time	DC-DC maximum ON time			10	µs
$T_{OFF(MIN)}$	DC-DC OFF Time	DC-DC- minimum OFF time	0.2			µs
MPPT						
$T_{TRACKING}$	MPPT tracking period	$\overline{BATT\_CHG}$ low	12		20	s
T_{SAMPLE}	MPPT sampling time	$\overline{BATT\_CHG}$ high	0.3		0.5	s
V_{MPP}	MPP pin voltage range	MPPT enabled, $MPPT_{RATIO}$ = 50%, $V_{MPP(MAX)}$ = 150mV, DC-DC switching (see Section 6.4 MPPT setting)	0.075		V_{UVP} -0.1	V
MPP_{ACC}	MPP tracking accuracy	Boost and buck-boost configurations	95			%
LDO						
$V_{LDO1,2}$	LDO1,2 adjusted output voltage	LDO1_EN = 1		1.8		V
		LDO2_EN = 1		3.3		
$\Delta V_{LDO1,2}$	LDO1 dropout	V_{UVP} + 200 mV < V_{STORE} ≤ 5.3 V; I_{LDO1} = 100 mA			0.5	%
	LDO2 dropout	3.3 V < V_{UVP} + 200 mV < V_{STORE} ≤ 5.3 V; I_{LDO2} = 100 mA			0.5	
t_{LDO}	LDO1,2 START-up time	$\overline{BATT\_CONN}$ = low; $C_{LDO1,2}$ = 100 nF	-	-	1	ms
$I_{LDO1,2}$ (1)	I_{OUT} max from LDO1	$\overline{BATT\_CONN}$= low	-	-	200	mA
	I_{OUT} max from LDO2		-	-	200	mA
$V_{LDO1,2\_EN\_H}$	LDO1,2 enable input HIGH		1	-	-	V
$V_{LDO1,2\_EN\_L}$	LDO1,2 enable input LOW		-	-	0.5	V
Digital output						

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BATT\_CONN\_L}$	$\overline{BATT\_CONN}$ voltage drop	1 mA sink current; $\overline{BATT\_CONN}$ = low	40	70	150	mV
$V_{BATT\_CHG\_L}$	$\overline{BATT\_CHG}$ voltage drop	1 mA sink current; $\overline{BATT\_CHG}$ = low	40	70	150	mV

1. *Guaranteed by design, not tested in production.*

6 Functional description

The SPV1050 can be used as energy harvester or normal DC-DC converter, depending on the activation or deactivation of the embedded MPPT algorithm (by MPP_SET pin setting). Also, the IC offers both load over-voltage and under-voltage control, which fit with the most typical requirements of battery charger applications. The additional unregulated (STORE) and regulated (LDO1, LDO2) voltage rails makes the IC suitable to be used as power manager.

Independently by the activation/deactivation of the MPPT function, the DC-DC converter stage can be configured as boost or buck-boost by tying the CONF pin to the input source or to ground, respectively. See Figure 4. Boost configuration example and Figure 12. Buck-boost configuration example.

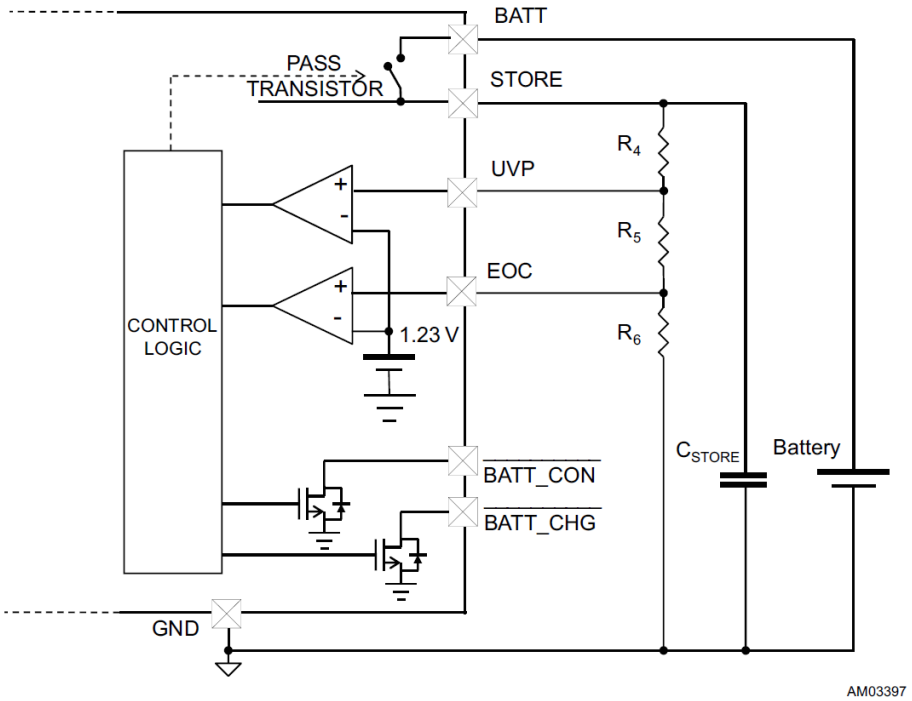
If the embedded MPPT algorithm is enabled (MPP and MPP_SET pins connected to input source by a resistor partitioning), the device periodically stops the switching of the DC-DC converter to do a sampling of the input voltage and to store it on the capacitor connected at MPP_REF pin. When the sampling time elapses, the IC restarts operating: if $V_{MPP} > V_{MPP\_REF}$, then the DC-DC can switch according the internal driving sequence purposing the optimization of the conversion efficiency. The selection of the resistor partitioning at the input stage, according to the electrical characteristic of the harvested source, allows the IC to maximize the power extracted: see further details in Section 6.2 Boost configuration,Section 6.3 Buck-boost configuration and Figure 19. MPPT setup circuitry.

The MPPT algorithm can be disabled by shorting the MPP_SET pin to the STORE pin. In this application case the MPP_REF pin is usually connected to a voltage reference. In case of low impedance source (e.g. USB), the MPP_REF is normally connected to GND: the IC tries switching at highest duty cycle. In case of high impedance source (limited current capability, i.e. the source in unable to sustain the continuous switching at maximum duty cycle), the MPP_REF pin can be connected to a reference voltage (V_{EXT_REF}) such that the IC stops switching when $V_{MPP} < V_{EXT\_REF}$. This voltage reference can be set through a resistor ladder connected to STORE rail or to any other voltage reference available.

6.1 Battery voltage control

The IC integrates a pass transistor between the STORE and BATT pins to implement both the undervoltage and the overvoltage protection thresholds. These thresholds are respectively controlled by the pins UVP and EOC, normally connected to the STORE pin by a resistor partitioning. The respective voltages (V_{UVP} and V_{EOC}) are compared with the IC internal voltage reference (V_{BG} = 1.23 V, typical value).
Those protection thresholds guarantee the lifetime and the safety of the battery.

Figure 2. Battery management section



Before the first startup (cold start) the pass transistor is open, so that the leakage from the output is lower than 1 nA. The pass transistor is closed once the (rising) voltage on the STORE pin triggers the overvoltage threshold $V_{STORE(EOC)}$ (corresponding to $V_{EOC} > V_{BG}$). An internal hysteresis (EOC_{HYS}) sets the restart voltage level for DC-DC converter. The IC also offers the undervoltage protection threshold: the pass transistor is opened once the (falling) voltage on the STORE pin decreases down to the undervoltage threshold $V_{STORE(UVP)}$ (corresponding to $V_{UVP} < V_{BG}$).
Referring to Figure 2. Battery management section, the design rules to set up the R4, R5 and R6 are the following:

Equation 1:
set the total output resistance ($R_{OUT(TOT)}$ = R1 + R2 + R3) to minimize its leakage:

- $10\ M\Omega \le R_{OUT(TOT)} \le 20\ M\Omega$

Equation 2:

- $R6 = (V_{BG} / V_{EOC}) \times R_{OUT(TOT)}$

Equation 3:

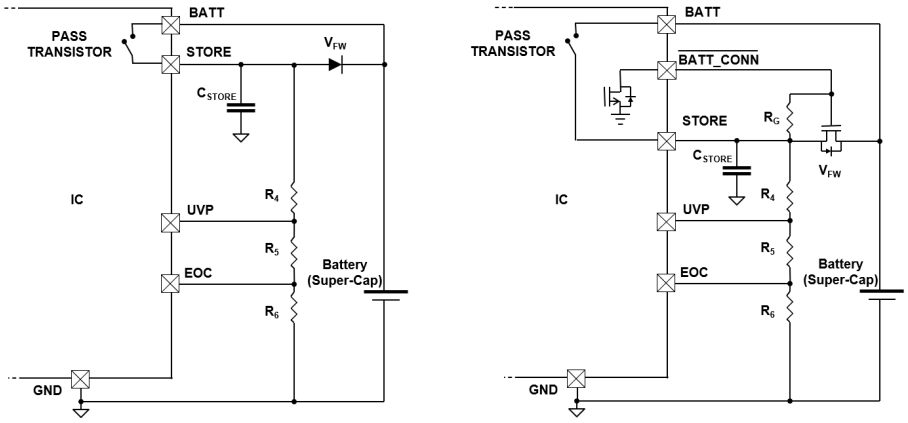
- $R5 = (V_{BG} / V_{UVP}) \times R_{OUT(TOT)} - R6$

In addition, the IC provides two open drain digital outputs to an external microcontroller:

- **$\overline{\text{BATT\_CONN}}$**
  This pin is pulled down when the pass transistor is closed. It will be released once the pass transistor will be opened. If used, this pin must be pulled up to the STORE rail by resistor (10 MΩ, typically) .
- **$\overline{\text{BATT\_CHG}}$**
  This pin is pulled down when the DC-DC converter is switching, while it's released when it is not switching, i.e. it is high after STORE triggers $V_{STORE(EOC)}$ and until it drops by EOC_{HYS} , or when the $UVLO_L$ threshold is triggered, or during the sampling period (T_{SAMPLE}) of the MPPT algorithm. If used, this pin must be pulled-up to the STORE rail by a resistor (10 MΩ, typically).

For some applications (typically with battery or super-cap connected to BATT pin) it could be necessary to implement a reactivation hysteresis after undervoltage event (pass transistors status changes from closed to open): it avoids the undesired continuous system reset loop due to full discharge of the C_{STORE} at every triggering of the overvoltage threshold. The application solution is simply based on a diode (or p-channel MOSFET driven by BATT_CONN) between STORE and BATT pins.

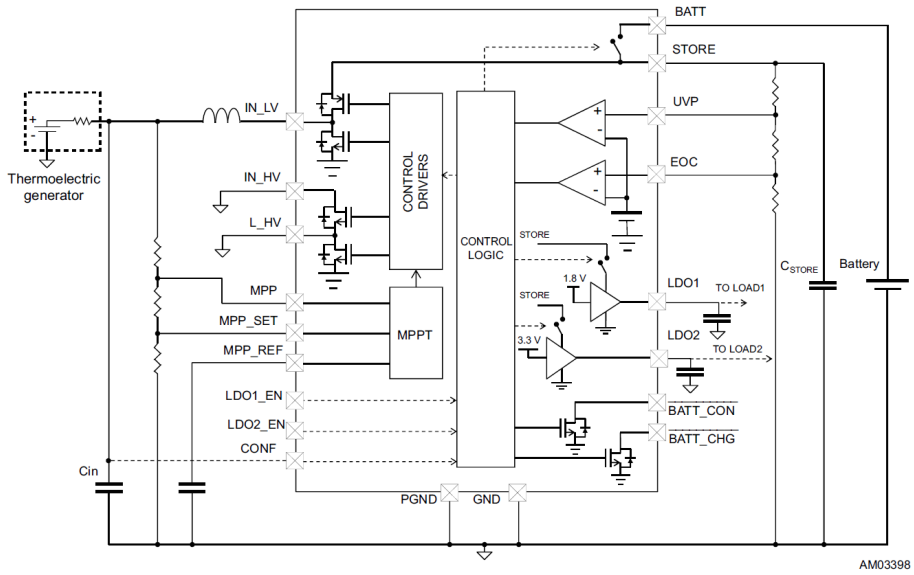
Figure 3. Implementations examples of larger UVP hysteresis



6.2 Boost configuration

Figure 4. Boost configuration example below shows an example of boost application circuit.

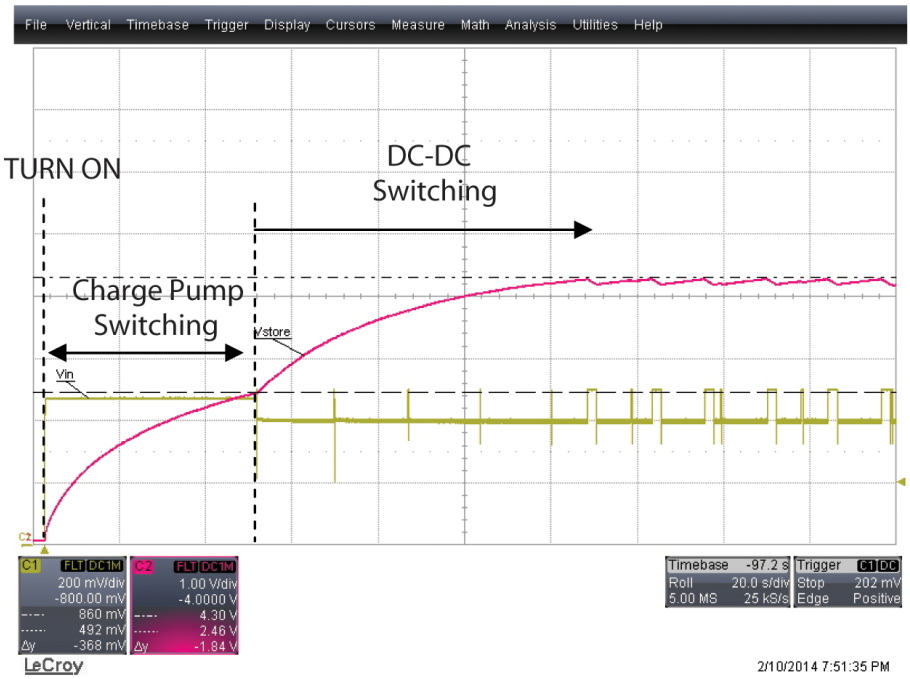
Figure 4. Boost configuration example



In case of boost configuration, once the source is connected, the SPV1050 will start boosting the voltage on the STORE rail. In the range of $0 \le V_{STORE} < 2.6$ V the voltage boost is carried on by an integrated high-efficiency charge pump, while the DC-DC converter stage remains OFF.

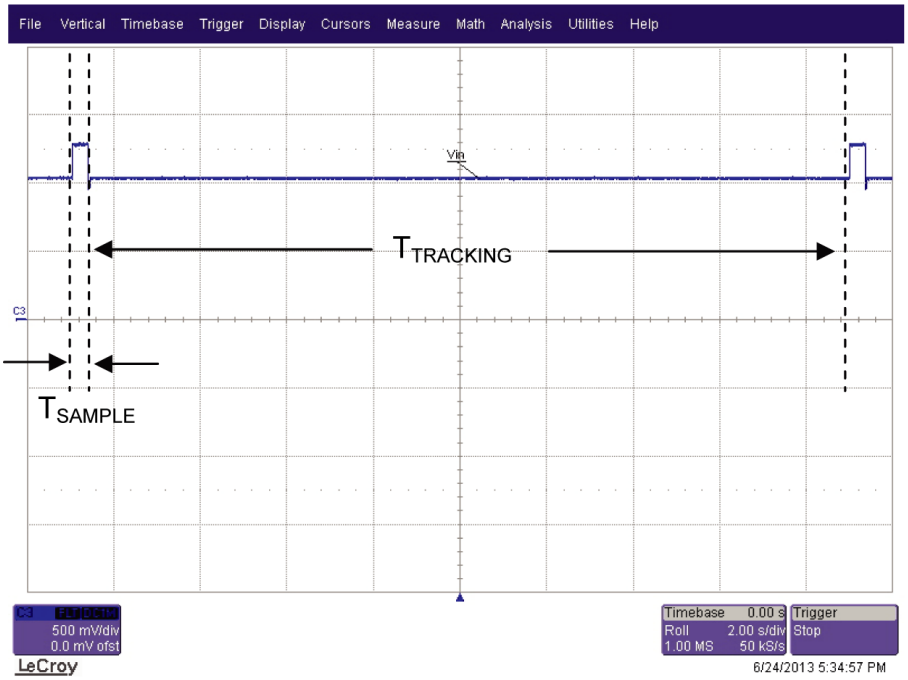
Figure 5. Boost start-up shows the behavior of input voltage V_{IN} (voltage supplied by the source) and V_{STORE} at the start-up.

Figure 5. **Boost start-up**



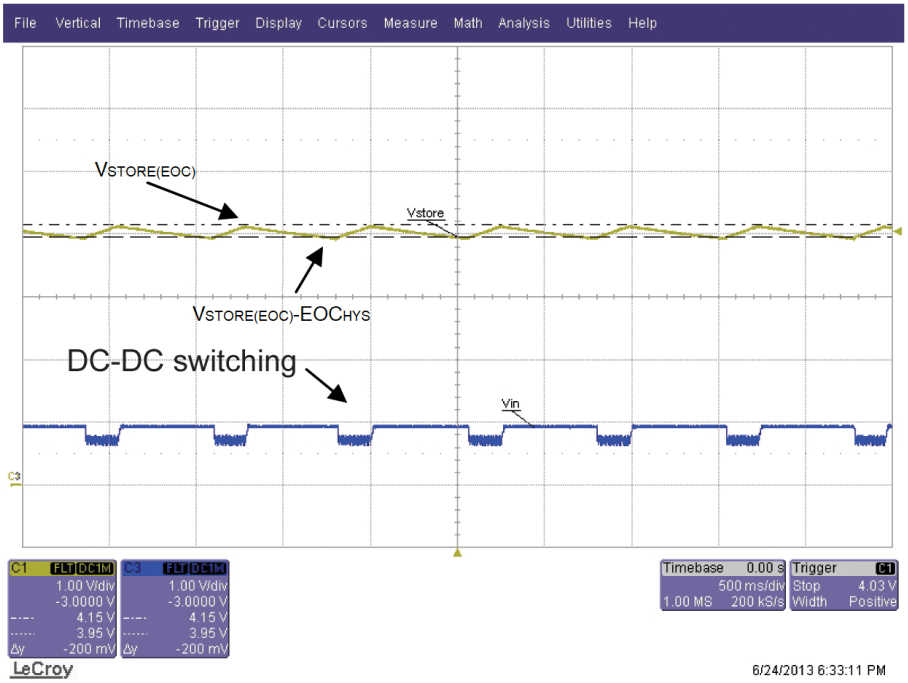
In the range 2.6 V ≤ V_{STORE} < $V_{STORE(EOC)}$ the voltage on STORE rail is boosted by the DC-DC converter that operates driven by internal logic until V_{MPP} > V_{MPP_REF}. Switching activity of the DC-DC is controlled by internal logic: ON phase stops at triggering of $I_{L(PEAK)}$ (peak current through the inductor) and can't be longer than $T_{ON(MAX)}$; OFF phase can't be shorter than $T_{OFF(MIN)}$. Also, purposing highest efficiency with low power source, the first ON phase after reactivation of the DC-DC is limited a triggering of $I_{L(PEAK)}$ / 2.
If the MPPT mode is active, then the IC stops switching for ~400 ms (T_{SAMPLE}) every ~16 seconds ($T_{TRACKING}$). During the T_{SAMPLE}, the IC goes in high impedance and the open circuit voltage V_{OC} at input stage is sampled and stored by charging the C_{REF} (capacitor on the MPP_REF pin) through the MPP_SET pin.
Once the T_{SAMPLE} is elapsed, the DC-DC converter will start switching back: the IC impedance is set featuring the V_{IN} stays as close as possible to the V_{MPP_REF}. The periodic sampling of V_{OC} guarantees the best MPPT in case of source condition variations (e.g. irradiation/thermal gradient and/or temperature changes).
A resistor partitioning connected between the source and the pins MPP and MPP_SET has to be properly selected, in order to match the source manufacturer's specs: refer to Section 6.4 MPPT setting for further details.
Figure 6. MPPT tracking shows the input voltage waveform of a PV panel supplying
V_{OC} = 1.25 V and V_{MP} = 1.05 V.

Figure 6. **MPPT tracking**



Once the voltage at STORE pin triggers the $V_{STORE(EOC)}$ the switching of the DC-DC converter stops until V_{STORE} decreases below the threshold defined by the internal hysteresis.

Figure 7. **Triggering of V_{EOC} (BATT pin floating)**



The following plots (Figure 8. Efficiency vs. input current; V_{OC} = 1.0 V, Figure 9. Efficiency vs. input current; V_{OC} = 1.5 V, Figure 10. Efficiency vs. input current; V_{OC} = 2.0 V, Figure 11. Efficiency vs. input current; V_{OC} = 2.5 V) show the power efficiency of the DC-DC converter configured in boost mode at T_{AMB} = 25 °C in some typical use cases at different open circuit voltages ($MPPT_{RATIO}$ = 83%):

Figure 8. Efficiency vs. input current; V_{OC} = 1.0 V

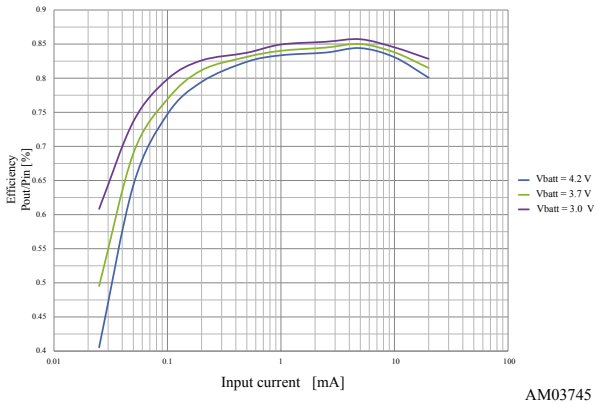


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Figure 9. Efficiency vs. input current; V_{OC} = 1.5 V

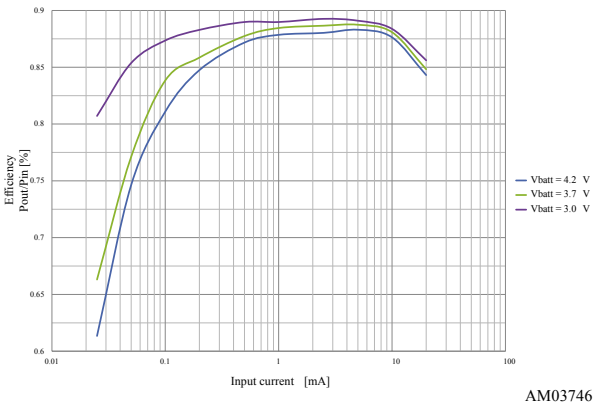

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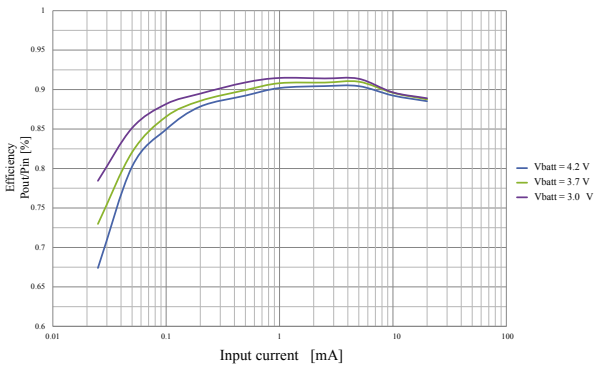
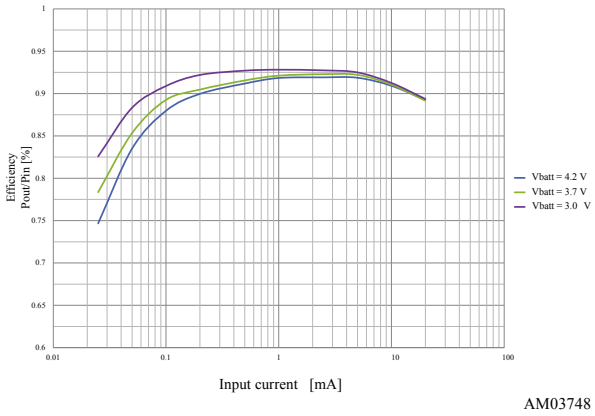
Figure 10. Efficiency vs. input current; V_{OC} = 2.0 V



AM03747

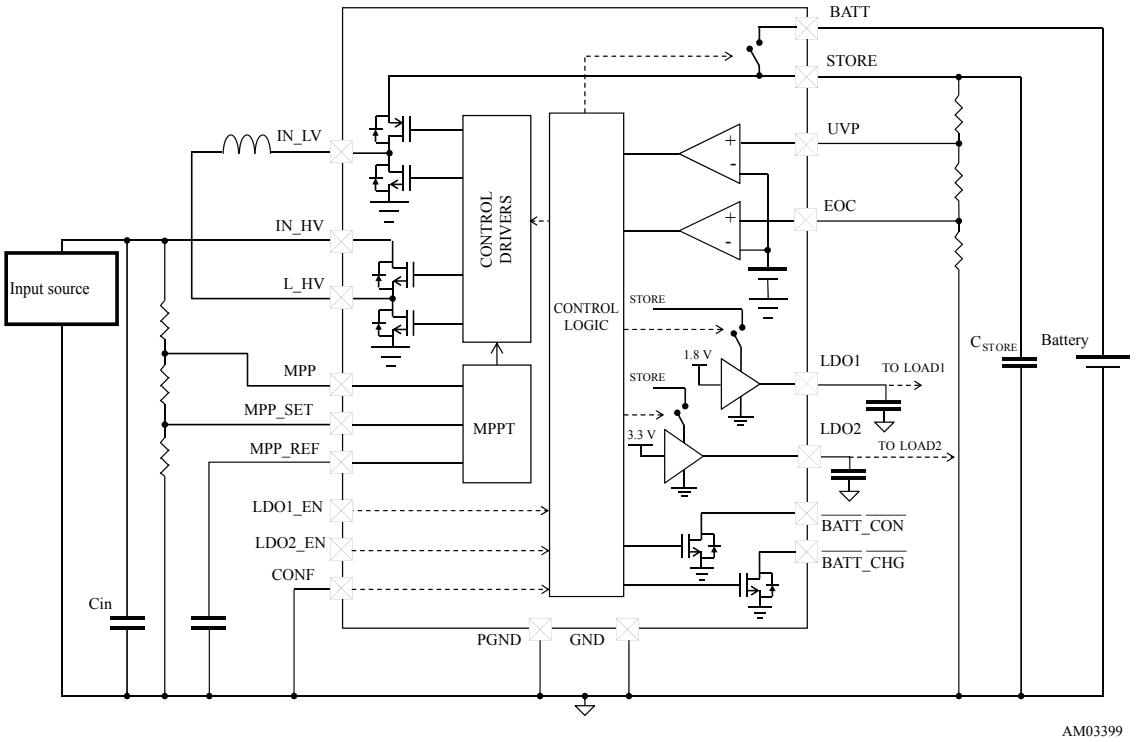
Figure 11. **Efficiency vs. input current; V_{OC} = 2.5 V**



6.3 Buck-boost configuration

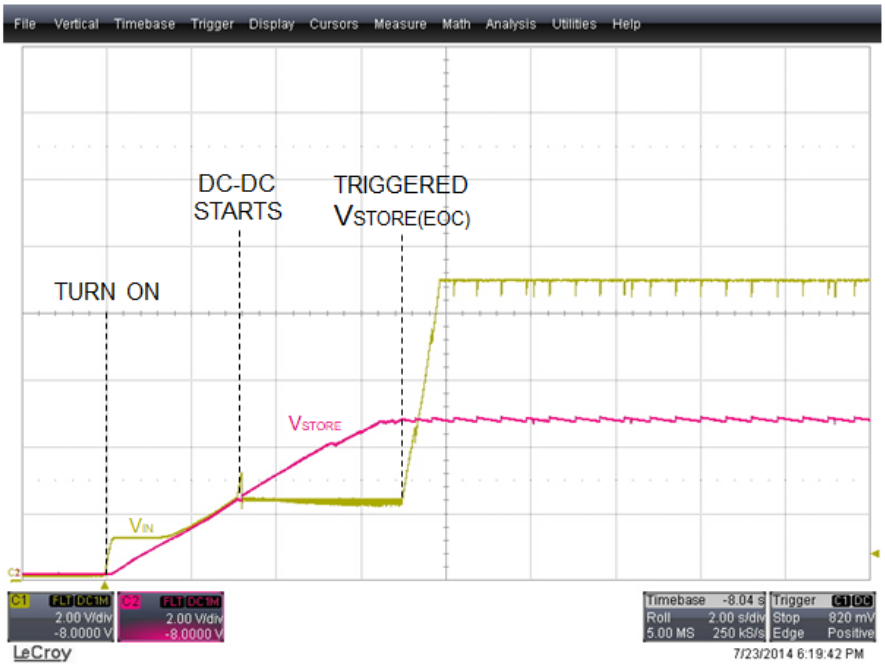
Figure 12. Buck-boost configuration example shows an example of buck-boost application circuit.

Figure 12. **Buck-boost configuration example**



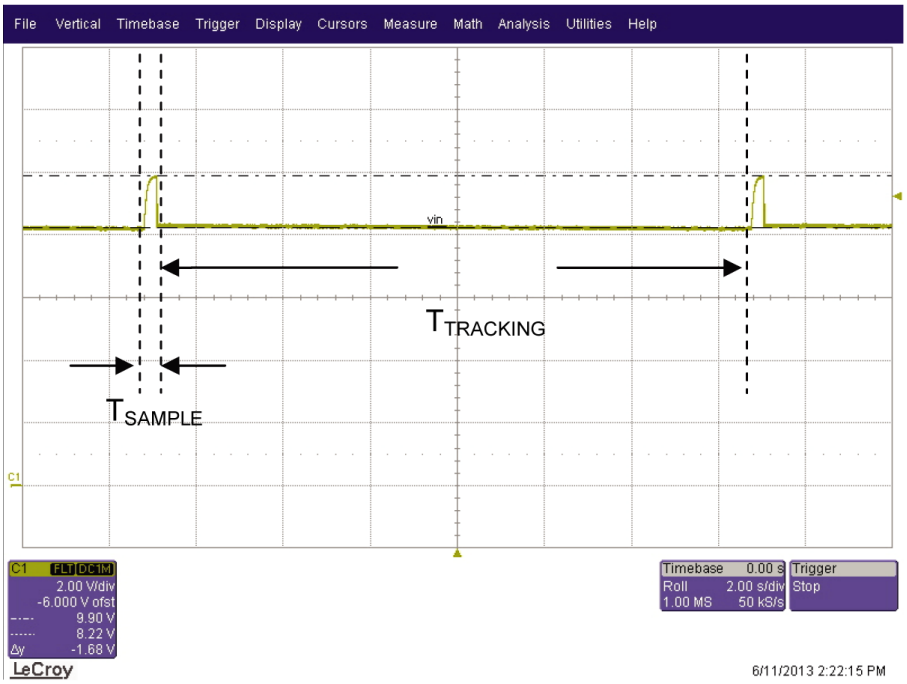
In case of buck-boost configuration, once the harvested source is connected, the IN_HV and STORE pins will be internally shorted until V_{STORE} < 2.6 V. Figure 13. Buck-boost start-up (I_{IN} = 5 µA) shows the behavior of the input voltage V_{IN_HV} and V_{STORE} at the start-up.

Figure 13. **Buck-boost start-up (I_{IN} = 5 µA)**



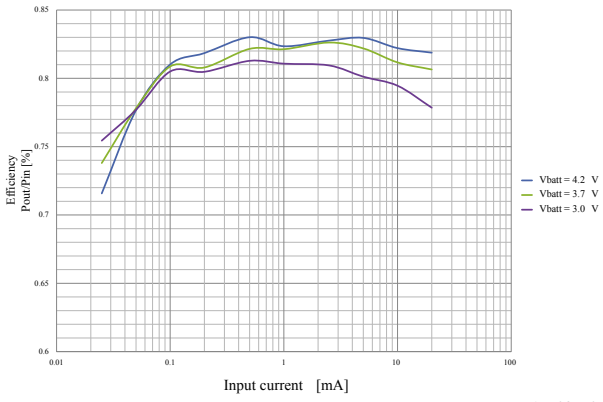
In the range 2.6 V ≤ V_{STORE} < $V_{STORE(EOC)}$ the integrated DC-DC switches until V_{MPP} > V_{MPP_REF}.
If the MPPT function is active, then the IC stops switching for ~400ms (T_{SAMPLE}) every ~16 seconds ($T_{TRACKING}$). During the T_{SAMPLE}, the open circuit voltage V_{OC} of the input source is sampled and stored by charging the C_{REF} (capacitor on the MPP_REF pin) through the MPP_SET pin. Once the T_{SAMPLE} is elapsed, the DC-DC converter operates again driven by the internal logic and such that V_{IN} (voltage supplied by the source) stays as close as possible to the maximum power point of the source. The periodic sampling of V_{OC} guarantees the best MPPT in case of source condition variations (e.g. irradiation and/or temperature changes).
A resistor partitioning connected between the source and the pins MPP and MPP_SET has to be properly selected in order to match the electrical characteristics of the source given by the manufacturer. Please refer to Section 6.4 MPPT setting for further details.
Figure 14. MPPT tracking shows the MPPT tracking form in case of V_{OC} = 9.9 V and voltage at maximum power point V_{MP} = 8.2 V.

Figure 14. **MPPT tracking**



The following plots (Figure 15. Efficiency vs. input current - V_{OC} = 6V , Figure 16. Efficiency vs. input current - V_{OC} = 9V , Figure 17. Efficiency vs. input current - V_{OC} = 12V , Figure 18. Efficiency vs. input current - V_{OC} = 15V) show the power efficiency of the DC-DC converter configured in buck-boost mode at T_{AMB} = 25 °C in some typical use cases ($MPPT_{RATIO}$ = 83%):

Figure 15. **Efficiency vs. input current - V_{OC} = 6V**



AM03750

Figure 16. **Efficiency vs. input current - V_{OC} = 9V**

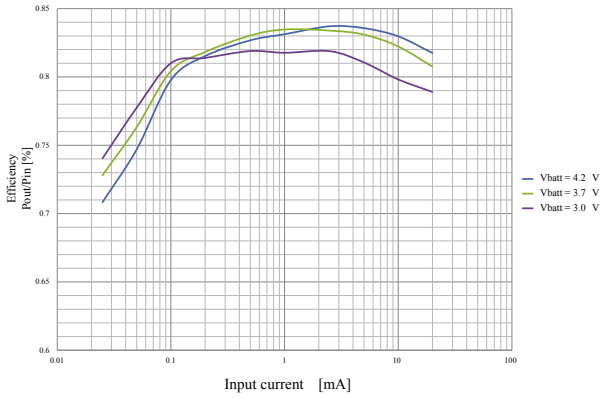


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Figure 17. **Efficiency vs. input current - V_{OC} = 12V**

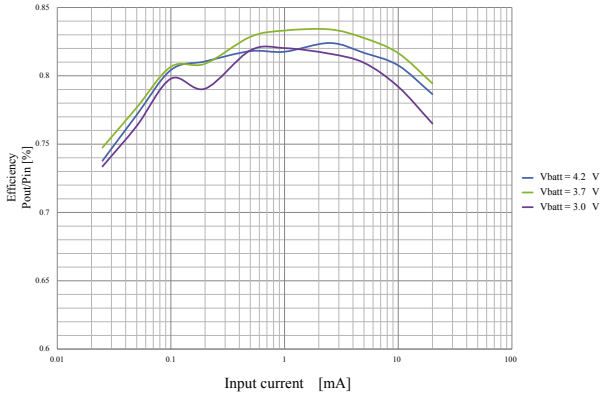

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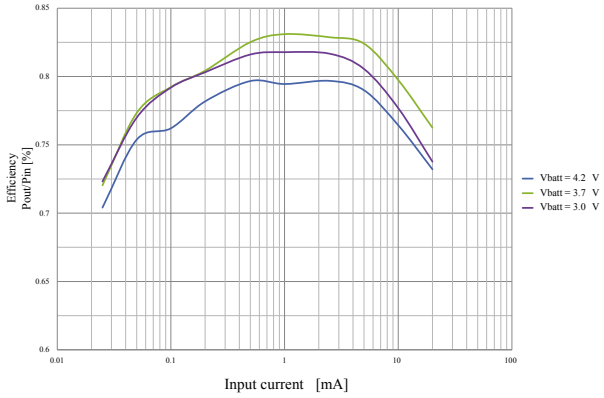
Figure 18. **Efficiency vs. input current - V_{OC} = 15V**



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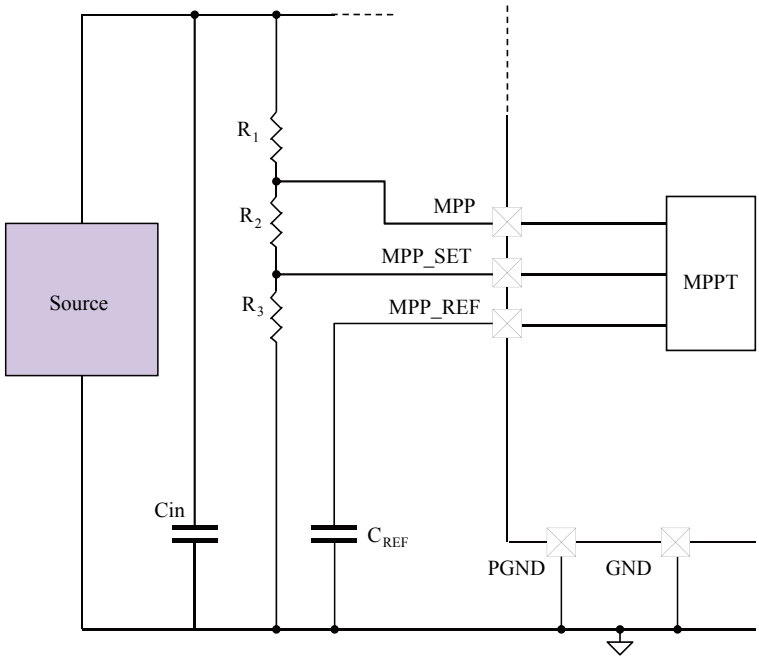
6.4 MPPT setting

When MPPT is enabled, the SPV1050 can regulate its impedance to extract the maximum power from the harvesting source. Typically, the datasheet of an harvesting source reports the main electrical characteristics: open circuit voltage (V_{OC}) and voltage at maximum power (V_{MP}); the $MPPT_{RATIO}$ is consequently calculated as V_{MP}/V_{OC}. Referring to PV panels and TEGs, the V_{MP} and V_{OC} can change according to the external conditions (light irradiation, temperature), but usually the effect on $MPPT_{RATIO}$ remains limited.
The highest MPPT accuracy of the SPV1050 can be achieved only by a proper selection of the resistors at the input stage (R1, R2, R3).

Figure 19. MPPT setup circuitry



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To select R1, R2 and R3 it is necessary to set some application parameters and then apply the below equations from 4 to 7.

- Electrical characteristics of the harvesting source
  - $V_{OC(MAX)}$, intended as V_{OC} at max operating condition of the source
  - $MPPT_{RATIO}$, intended as V_{MP}/V_{OC} at typical operating conditions of the source
- Application constraints
  - $I_{LEAKAGE}$, intended as the acceptable leakage through the resistors at the input stage
  - Usually, 0.1 µA ≤ $I_{LEAKAGE}$ ≤ 1 µA fits for most of the applications.
- SPV1050 constraints
  - $V_{EN\_TH\ (MAX)} \leq V_{MPP(MAX)} \leq (V_{UVP(MIN)} - 100\ mV) \Rightarrow$
    $150\ mV \leq V_{MPP(MAX)} \leq 2.1\ V$
  - $V_{MPP(MAX)} < V_{OC(MAX)}$

Equation 4:
$R_{IN(TOT)} = R1 + R2 + R3 > (V_{OC(MAX)} / I_{LEAKAGE}) \times MPPT_{RATIO}$
Equation 5:
$R1 = R_{IN(TOT)} \times [\, 1 - (V_{MPP(MAX)} / V_{OC(MAX)}) \,]$
Equation 6:
$R2 = R_{IN(TOT)} \times (V_{MPP(MAX)} / V_{OC(MAX)}) \times (1 - MPPT_{RATIO})$
Equation 7:
$R3 = R_{IN(TOT)} \times (V_{MPP(MAX)} / V_{OC(MAX)}) \times MPPT_{RATIO}$

***Example**:*
Harvesting source is a PV panel with $V_{MP(TYP)}$ = 1.5 V and $V_{OC(TYP)}$ = 2.0 V (⇒ $MPPT_{RATIO}$ = 75%). At maximum light irradiation $V_{OC(MAX)}$ = 2.2 V.
$V_{MPP(MAX)}$ could be set between 0.15 V and 2.1 V: in this example we can assume that $V_{MPP(MAX)}$ = 0.50 V (= 33% of $V_{MP(TYP)}$).
In general, $V_{MPP(MAX)}$ depends on the power supplied by the PV panel at low light irradiation and on the minimum acceptable conversion efficiency of the DC-DC.
Hence set

- *$V_{OC(MAX)}$ = 2.2 V*
- *$V_{MPP(MAX)}$ = 0.5 V*
- *$I_{LEAKAGE}$ = 0.1 µ A*

$R_{IN(TOT)}$ = (2.2 V / 0.1 uA) × 0.75 = 16.5 MΩ
R1 =16.5 MΩ × [1 - (0.5 V / 2.2 V)] = 12.75 MΩ
R2 =16.5 MΩ × (0.5 V/ 2.2 V) × (1- 0.75) = 0.94 MΩ
R3 =16.5 MΩ × (0.5 V/ 2.2 V) × 0.75 = 2.81 MΩ

Also, the MPPT accuracy can be strongly affected by an improper selection of the input capacitor. The input capacitance C_{IN} = 4.7 µF generally covers the most typical use cases.

The energy extracted from the source, and stored on C_{IN}, is transferred to the load by the DC-DC converter through the inductor. The energy extracted by the inductor depends by the sink current: the higher input currents cause higher voltage drop on the input capacitance and this may result a problem for low voltage (< 1 V) and high energy (> 20 mA) sources. In such application cases the input capacitance has to be increased or, alternatively the L1 inductance has to be reduced.

During the T_{SAMPLE} time frame the input capacitor C_{IN} is charged up to V_{OC} by the source with a time constant (T1) resulting from the capacitance and the equivalent resistance R_{EQ} of the source.

In case of PV source, being I_{MP} the minimum operating current for MPPT, the R_{EQ} can be calculated as following:

Equation 8:

- $R_{EQ} = (V_{OC} - V_{MP}) / I_{MP} = V_{OC} \times (1 - MPP_{RATIO}) / I_{MP}$

Thus C_{IN} is calculated by the following formula:

Equation 9:

- $C_{IN} \leq T1 / R_{EQ}$

The following plots (Figure 20. Energy harvester equivalent circuit, Figure 21. Voltage vs. time at different C values and fixed current) show the effect of different C_{IN} values on the time constant. If the capacitance is too high, the capacitor may not be charged within the T_{SAMPLE} = 400 ms time window, thus affecting the MPPT accuracy.

Figure 20. **Energy harvester equivalent circuit**

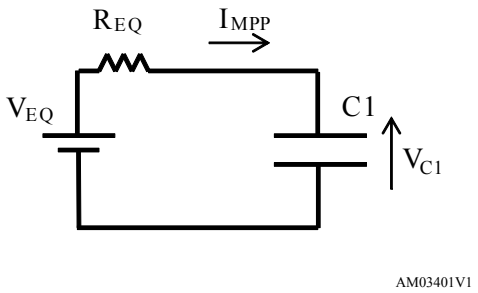
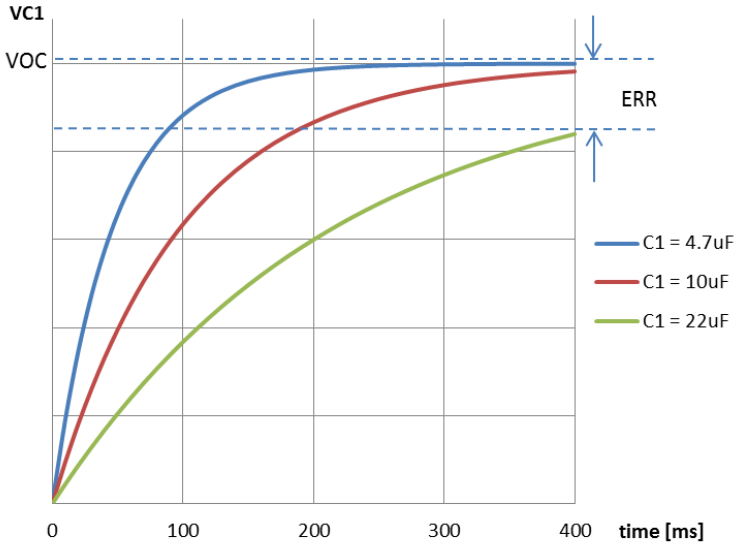


Figure 21. **Voltage vs. time at different C values and fixed current**



6.5 Power manager

The SPV1050 device works as a power manager by providing two regulated voltages on the LDO1 (1.8 V) and LDO2 (3.3 V) pins.

Each LDO can be selectively enabled or disabled by driving the related enable/disable pins LDO1_EN and LDO2_EN. The performances of the LDOs can be optimized by selecting a proper capacitor between the LDO output pin and ground. A 100 nF for each LDO pin is suitable for the most typical use cases.
Figure 22. LDO1 turn on with 100 mA load and Figure 23. LDO2 turn on with 100 mA load show the behavior of the LDOs when a 100 mA load is connected.

Figure 22. **LDO1 turn on with 100 mA load**

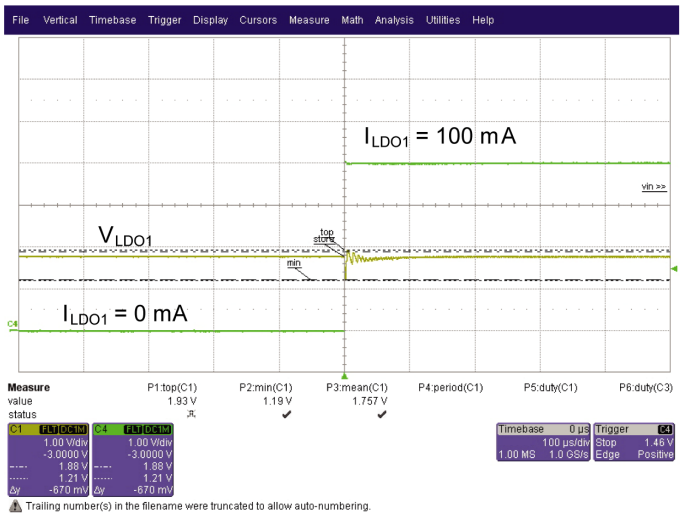
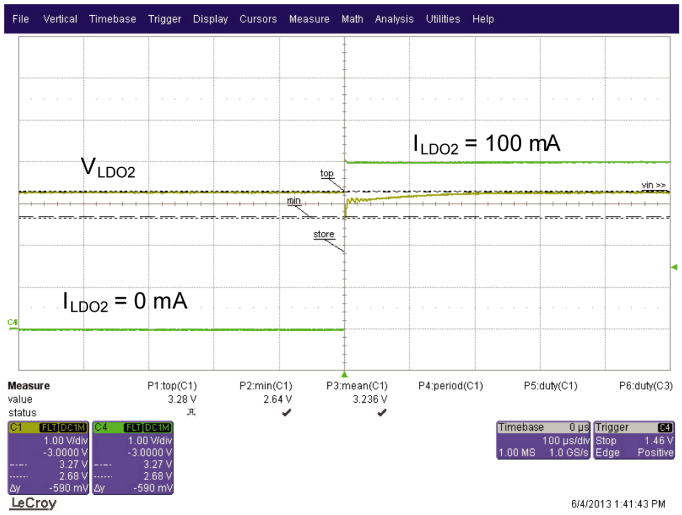


Figure 23. **LDO2 turn on with 100 mA load**



Note that the internal logic inhibits both LDOs when the embedded pass transistor is open, that is when the battery is not connected. Also, the LDOs are both supplied by the STORE rail: if the input source is unable to sustain the current required by the load, then the missing energy will be supplied by the battery connected to the BATT pin. In this case, the current from the battery causes a voltage drop between STORE and BATT pins due to the resistance of the pass transistor:
$V_{STORE} = V_{BATT} - (R_{BATT} * I_{LOAD})$.
If V_{STORE} drops and UVP pin triggers the undevoltage threshold, then the pass transistor gets open and the load is no longer supplied until next end of charge condition is reached.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 Package and packing information

Figure 24. VFQFPN20 3 x 3 x 1 mm - 20-lead pitch 0.4 package outline

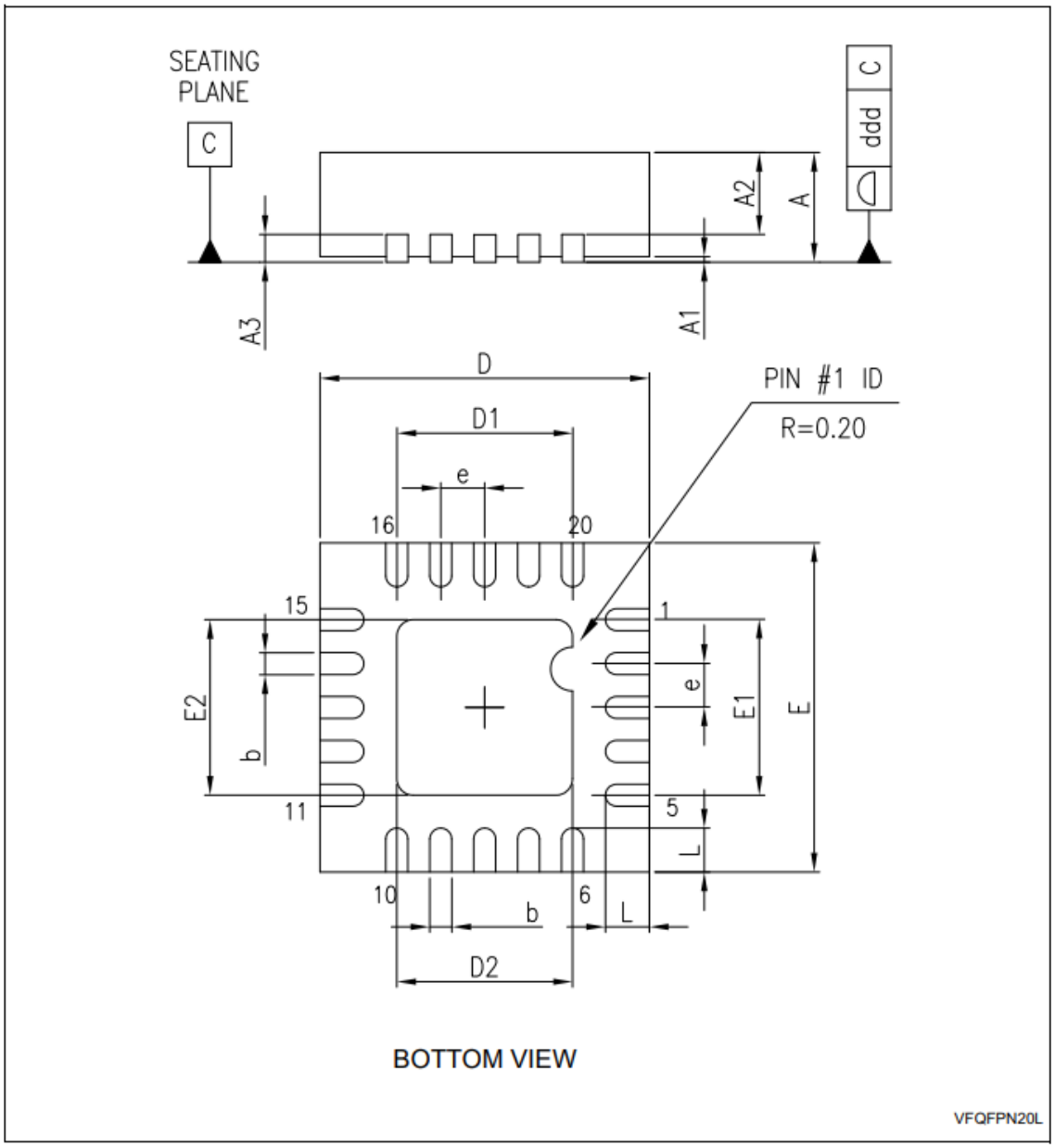


Table 4. VFQFPN20 3 x 3 x 1 mm - 20-lead pitch 0.4 package mechanical data

Symbol	Dimensions [mm][1]		
	Min.	Typ.	Max.
A	0.80	0.90	1.0
A1	-	0.02	0.05
A2	-	0.65	1.00
A3	-	0.20	-
b	0.15	0.20	0.25
D	2.85	3.00	3.15
D1	-	1.60	-
D2	1.50	1.60	1.70
E	2.85	3.00	3.15
E1	-	1.60	-
E2	1.50	1.60	1.70
e	0.35	0.40	0.45
L	0.30	0.40	0.50
ddd	-	-	0.07

1. *"VFQFPN" stands for "Thermally Enhanced Very thin Fine pitch Quad Packages No lead". Very thin: 0.80 < A ≤ 1.00 mm / fine pitch: e < 1.00 mm.*

Figure 25. Reccomended footprint of VFQFPN20 3 x 3 x 1 mm - 20-lead pitch 0.4

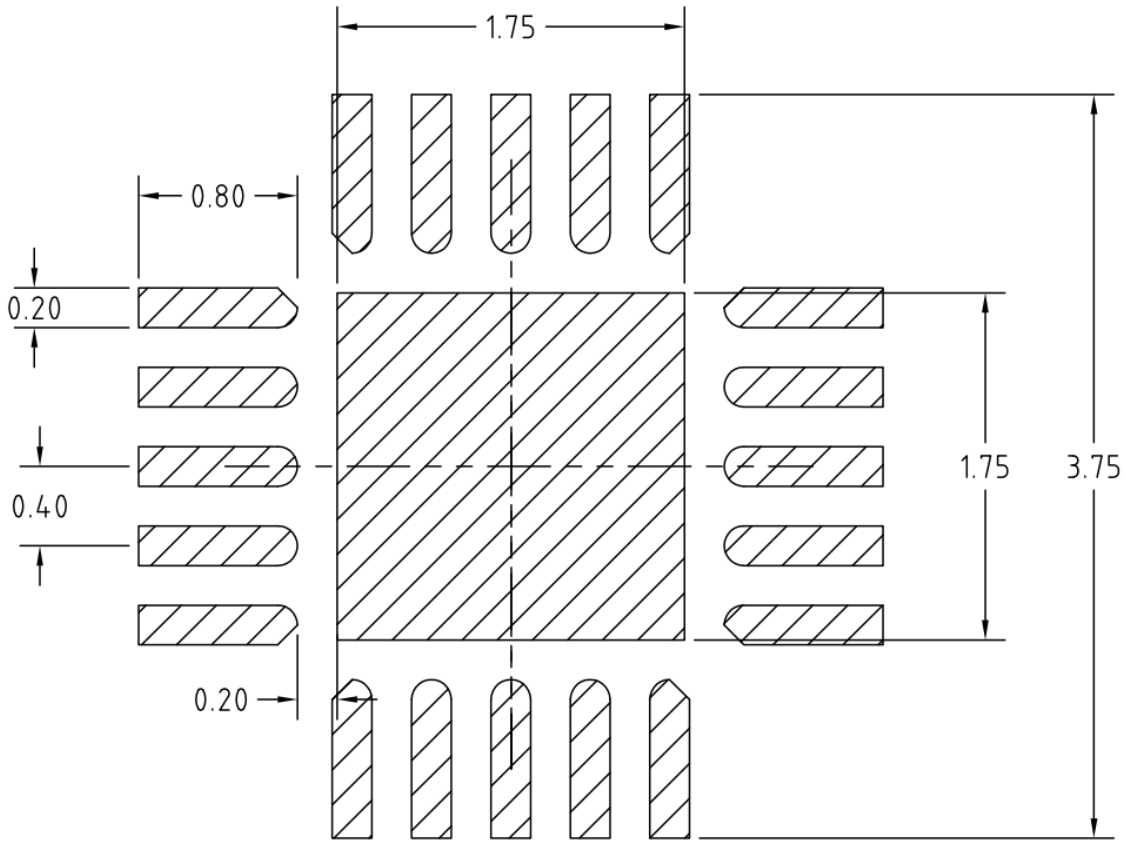
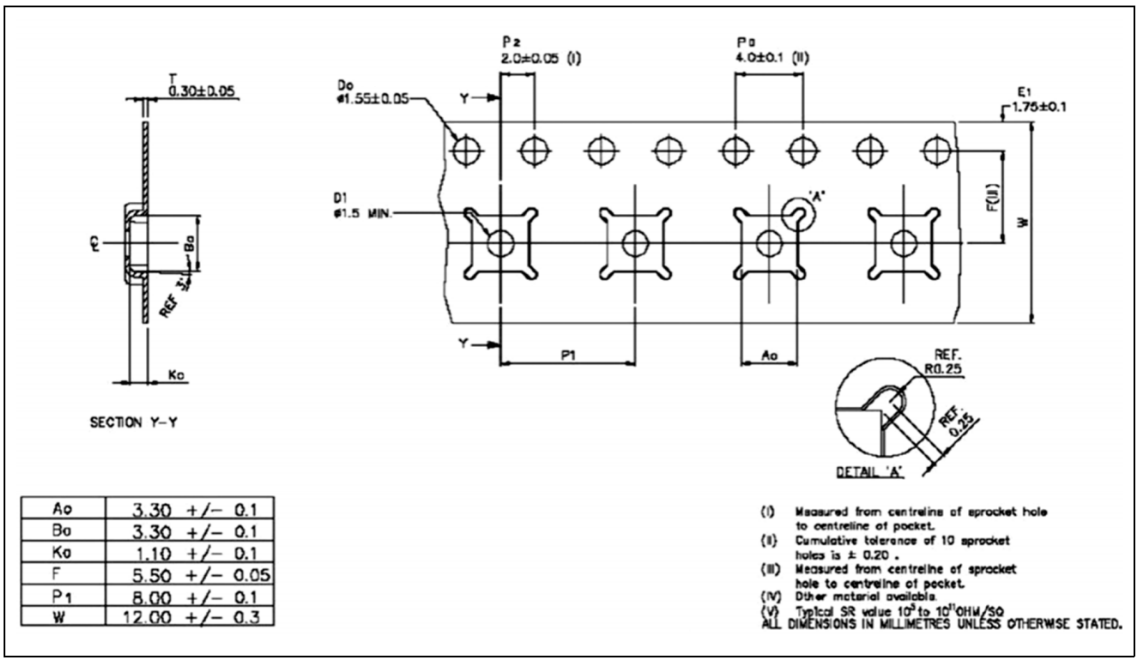


Figure 26. **Tape and reel design**



Ao	3.30 +/- 0.1
Bo	3.30 +/- 0.1
Ko	1.10 +/- 0.1
F	5.50 +/- 0.05
P1	8.00 +/- 0.1
W	12.00 +/- 0.3

Figure 27. **Die form pad position (top view)**

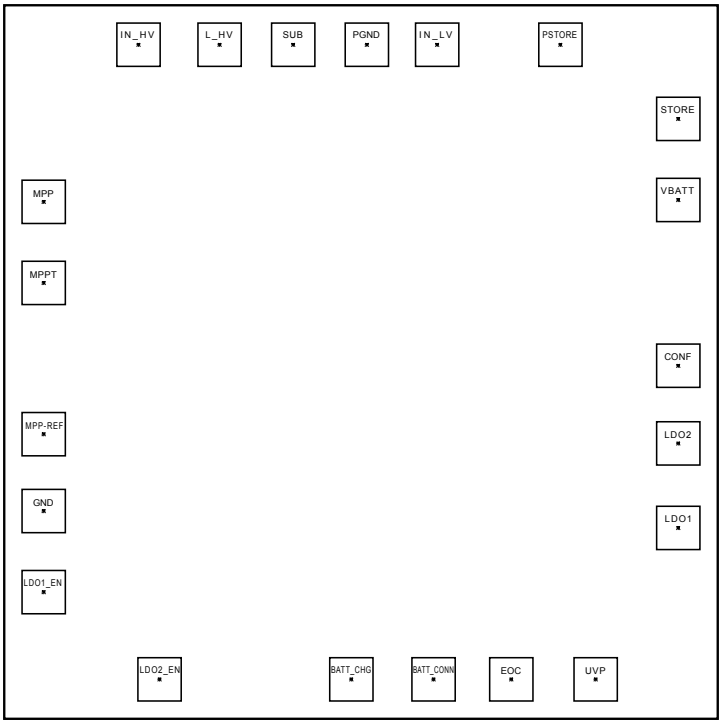


Table 5. Die pad coordinates and pad size

Symbol	Dimensions [mm][1]		
	X position [µm]	Y position [µm]	Pad dimension [µm]
IN_HV	-416.55	594.09	81.05 x 81.05
L_HV	-264.75	594.09	
SUB	-126.87	594.09	
PGND	10.99	594.09	
IN_LV	142.65	594.09	
PSTORE	373.43	594.09	
STORE	594.09	455.22	
BATT	594.09	303.42	
CONF	594.09	-6.9	
LDO2	594.09	-152.33	
LDO1	594.09	-310.59	
UVP	439.39	-594.09	
EOC	281.45	-594.09	
BATT_OK	135.88	-594.09	
BATT_CHG	-18.03	-594.09	
LDO2_EN	-377.15	-594.09	
LDO1_EN	-594.09	-430.77	
GND	-594.09	-278.97	
MPP_REF	-594.09	-135.06	
MPP_SET	-594.09	148.12	
MPP	-594.09	299.92	

1. *"VFQFPN" stands for "Thermally Enhanced Very thin Fine pitch Quad Packages No lead". Very thin: 0.80 < A ≤ 1.00 mm / fine pitch: e < 1.00 mm.*

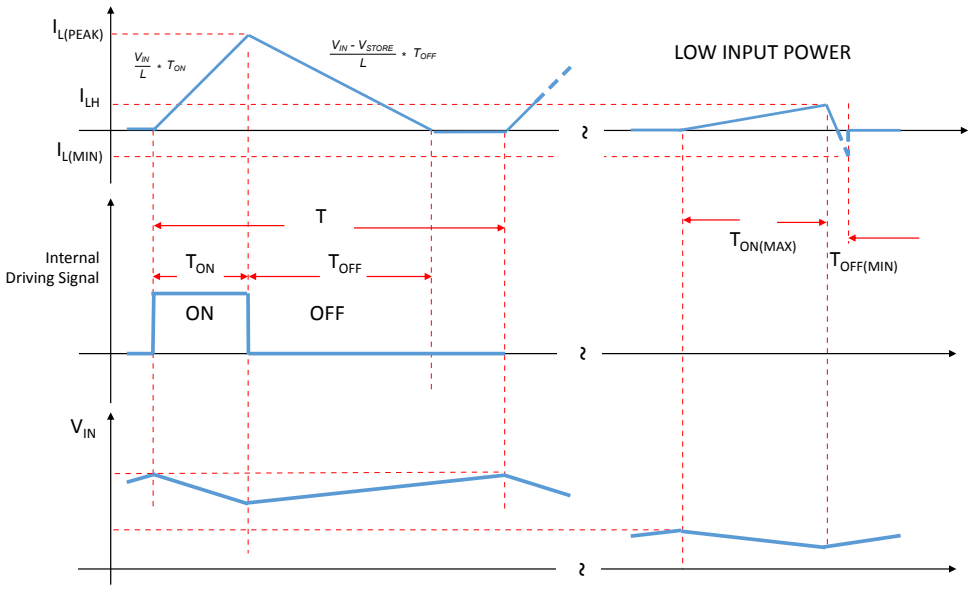
8 Ordering information

Order code	Op. temp. range [°C]	Package	Packing
SPV1050TTR	-40 to 85	VFQFPN 3 x 3 x 1 20L	Tape and reel
SPV1050-WST	-40 to 85	Die form	Sawn tested wafer

Appendix A Application tips

In the DC-DC converters the energy is transferred from the input to the output through the inductor. During the ON phase of the duty cycle the inductor stores energy; during the OFF phase of the duty cycle the energy is released toward the output stage.

Figure 28. Inductor current and input voltage waveforms



The SPV1050 activates the driving signal of the DC-DC when $V_{MPP} > V_{MPP\_REF}$. During the ON phase of the driving signal, the inductor is loaded for T_{ON} until one of the following events occurs:

- V_{STORE} triggers the overvoltage threshold
- The inductor current (I_L) triggers the internal threshold $I_{L(PEAK)}$ (= 140 mA, typ.)
- $T_{ON(MAX)}$ = 10 µs elapses

In the OFF phase the energy stored in the inductor will be released to the output stage: during T_{OFF} the I_L decreases to I_{LZC}. According to the internal controls of the IC, $T_{OFF(MIN)}$ = 0.2 µs: in order to prevent I_L goes negative, the application must be designed such that the energy stored in the inductor during T_{ON} is always greater than, or equal to, the energy released during T_{OFF}. This goal can be achieved through the proper selection of R2 + R3. Thus, in order to guarantee $I_{L(MIN)} > 0$, it must be:

Equation 10:

- $I_{L(MIN)} = I_H - (V_{STORE} - V_{IN}) \times (T_{OFF(MIN)}/L) > 0$

Equation 11:

- $I_{L(MIN)} = (V_{IN}/L) \times T_{ON(MAX)} - (V_{STORE} - V_{IN}) \times (T_{OFF(MIN)}/L) > 0$

leading

Equation 12:

- $V_{IN} > V_{STORE} \times (T_{OFF(MIN)}/(T_{ON(MAX)} + T_{OFF(MIN)})) = V_{STORE} / 51$

As worst case for the above equation it can be considered V_{STORE} at the overvoltage level.
The resistor R1, part of the partitioning at the input stage, can be used purposing the DC-DC switch-off before $I_{L(MIN)} \leq 0$.
$V_{MPP} = V_{IN} * (R2+R3)/(R1+R2+R3) < V_{EN\_TH}$

Revision history

Table 6. **Document revision history**

Date	Version	Changes
25-Nov-2013	1	Initial release.
28-Aug-2014	2	Document status promoted from preliminary data to production data, with comprehensive update of electrical characteristic sand graphic content throughout the document.
18-Dec-2014	3	Document status corrected to reflect current phase of product development.
06-Aug-2015	4	Minor text edits throughout the document. Added maximum values for $R_{th\ j\text{-}c}$ and $R_{th\ j\text{-}a}$ in Table 2: Thermal data, with associated footnote. Multiple changes to parameters, test conditions and values in Table 4: Electrical characteristics. Modified text in Section 6: Functional description and Section 6.4: MPPT setting. Removed order code SPV1050T from Table 7: Device summary, and modified package and packing values for order code SPV1050-WST. Added Appendix A: Application tips
17-May-2018	5	Added Figure 26 on page 32. Minor modifications throughout the document
12-Oct-2021	6	Changed datasheet formatting. Front page: rephrased Features list and Description; extended Application list. Block diagram: added details of the input stage with internal control thresholds. Pin Description: rephrased descriptions of input and output stage pins. Electrical characteristics: minor editing fixes; added V_{EN_TH}, $I_{L(PEAK)}$, $I_{L(ZC)}$, $T_{ON(MAX)}$ and $T_{OFF(MAX)}$ parameters. Chapter 6: minor editing; added application examples for the management of larger UVP hysteresis. Chapter 6.4: reviewed calculation of input resistor partitioning. Deleted Appendix A.

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