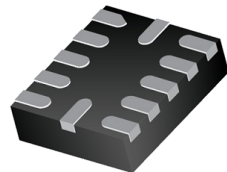


400 mA nano-quiescent synchronous step-down converter with digital voltage selection, Power Good and AUX switch



TQFN12 (2.0x1.7 mm)

Features

- 500 nA input quiescent current at $V_{IN} = 3.6\text{ V}$ (not switching)
- 92% typical efficiency at 10 mA load ($V_{IN} = 3.6\text{ V}$, $V_{OUT} = 2.5\text{ V}$)
- 100% duty cycle
- 1.8 V to 5.5 V input operating range
- Undervoltage lockout: 1.57 V (V_{IN} falling, typ.)
- Up to 400 mA output current capability
- Low power control operation for the best efficiency
- Embedded soft-start circuit
- Tiny external components: $L = 2.2\text{ }\mu\text{H}$ typ.
- Settable inductor current limitation
- Selectable output voltages: 1.0 V to 3.3 V
- Output voltage Power Good
- $\pm 1.5\%$ output voltage accuracy (V_{OUT} , $T_A = 25\text{ }^\circ\text{C}$)
- Dynamic output voltage selection (D0, D1 and D2)
- Auxiliary load switch Vout2 (AUX control input)
- Available in TQFN12 package

Applications

- Wearable applications
- Personal tracking monitors
- Smart watches, sport bands
- Energy harvesting, wireless sensors
- Wearable and fitness accessories
- Industrial sensors, portable low power devices
- Single cell Li-Ion battery applications
- Bluetooth[®] low energy
- Zigbee

Description

The ST1PS02 is a nano-quiescent miniaturized synchronous step-down converter, which is able to provide up to 400 mA output current with an input voltage ranging from 1.8 V to 5.5 V. This converter is specifically designed for applications where high efficiency, PCB size and thickness are the key factors. The output voltage can be set using three digital control inputs, a V_{OUT} from 1.0 V to 3.3 V can be dynamically selected. Thanks to the enhanced PCC (peak current control) the ST1PS02 reaches very high efficiency conversion using just a 2.2 μH inductor and two small capacitors. The device embeds a controlled load switch to supply a subsystem with same voltage rail. Advanced design circuitry is implemented to minimize the quiescent current. The device is available in thin plastic package.

| |
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| Product status link |
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| ST1PS02 |
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1 Application schematic

Figure 1. ST1PS02 application schematic

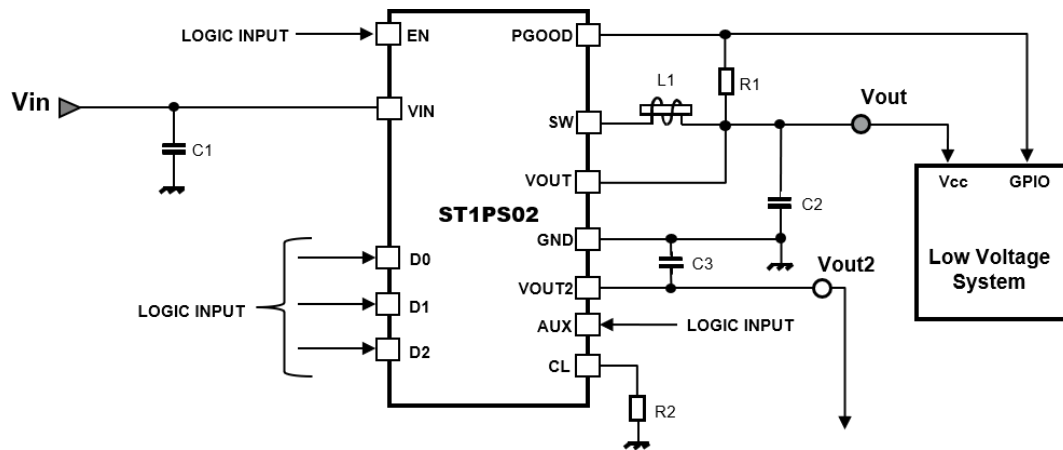


Table 1. Typical external components

| Component | Description | Value | Size - imperial (metric) |
|---------------------------------|---------------------------------------|--------------|--------------------------|
| C ₁ | Ceramic capacitor with low ESR values | 10 μ F | 0603 (1608) |
| C ₂ , C ₃ | Ceramic capacitor with low ESR values | | |
| L ₁ | Inductor | 2.2 μ H | 0806 (2016) |
| R ₁ | Pull-up resistor | 1 M Ω | 0402 (1005) |
| R ₂ | Current limit resistor | 0 Ω | |

2 Pin configuration

Figure 2. TQFN12 package (top through view)

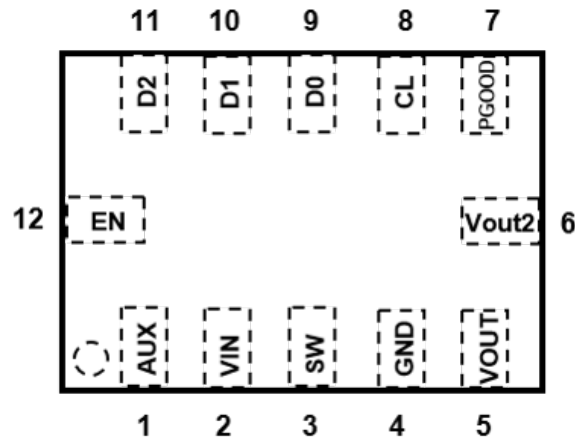


Table 2. Pin description

| Name | Bump name | Description |
|-------|-----------|--|
| AUX | 1 | Enable for the auxiliary output voltage |
| VIN | 2 | Input supply voltage. Bypass this pin to ground with a 10 μ F capacitor |
| SW | 3 | Switching output. Inductor connection |
| GND | 4 | Ground |
| VOUT | 5 | Sense pin used to monitor output voltage |
| Vout2 | 6 | Auxiliary output pin with OCP (100 mA max. load) |
| PGOOD | 7 | Open drain output. It is in high impedance when the output voltage reaches 97.5% of the target V_{OUT} |
| CL | 8 | Current limit set. Connect to GND sets the default value (750 mA min.). An external resistor connected to GND can be used to adjust this parameter with a lower value (resistor values are reported on Table 6. Electrical characteristics) |
| D0 | 9 | Output voltage selection inputs (refer to Table 7. Output voltage settings) |
| D1 | 10 | |
| D2 | 11 | |
| EN | 12 | Enable pin. High logic level turns on the IC |

3 Functional pin description

GND

Device ground pin.

VIN

Supply voltage. This pin supplies power to the internal analog and digital circuitries when voltage is higher than V_{UVLO} . Bypass this pin to GND with a 10 μ F ceramic capacitor. Input capacitor C_1 must be chosen with low ESR to reduce the input voltage ripple.

SW

Inductor connection to internal PMOS and NMOS switches.

VOUT

Output voltage sense input. It provides the feedback voltage level to the regulation circuitry. 10 μ F output capacitor C_2 must be connected close to the pin or through a short trace and should have low ESR to reduce the output voltage ripple.

EN

Enable pin. A logic low level on this pin disables the device. High level enables the device. Do not leave this pin floating.

D0, D1, D2

Output voltage selection pins. See [Table 7. Output voltage settings](#) for V_{OUT} selection. Do not leave these pins floating. These pins can be dynamically changed during operation.

PGOOD

Power Good open drain output. If used it requires a pull-up resistor to hold a high level signal. High impedance indicates that V_{OUT} is above proper good threshold.

AUX

Load switch selection pins. Vout2 output is activated when this pin is at high level. Held to ground if auxiliary output (Vout2) is not used or if it should be disabled.

Vout2

Auxiliary output. It provides the same regulated voltage level as main output (VOUT) less drop on the load switch circuitry. 10 μ F output capacitor C_3 must be connected close to the pin or through a short trace and should have low ESR to reduce the output voltage ripple. This output is controlled from a soft-start circuit, if unused can be left open.

CL

Current limit threshold input. Held to ground if not used and default current limitation is the proper value. For smaller current values a pull-down resistor must be used.

4 Maximum ratings

Table 3. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---------------------|---|------------------------|------|
| V_{IN} | Power and signal supply voltage | - 0.3 to + 6.5 | V |
| EN, D0, D1, D2, AUX | Logic input pins | - 0.3 to + 6.5 | V |
| CL | Current limitation input pin | - 0.3 to + 6.5 | V |
| V_{OUT} , SW | Output signal monitoring and switching pins | -0.3 to $V_{IN} + 0.3$ | V |
| Vout2 | Load switch output pin | - 0.3 to + 6.5 | V |
| PGOOD | Power Good open drain output pin | - 0.3 to + 6.5 | V |
| T_{AMB} | Operating ambient temperature | -40 to 85 | °C |
| T_J | Junction temperature | -40 to 125 | °C |
| T_{STG} | Storage temperature | -55 to 150 | °C |

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 4. Thermal data

| Symbol | Parameter | TQFN12 | Unit |
|------------|-------------------------------------|--------|------|
| R_{thJA} | Thermal resistance junction-ambient | 75 | °C/W |

Table 5. Recommended operating conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|----------|----------------------|------|------|------|------|
| V_{IN} | Input supply voltage | 1.8 | | 5.5 | V |

5 Electrical characteristics

$C_1 = 10 \mu\text{F}$, $C_2 = 10 \mu\text{F}$, $C_3 = 10 \mu\text{F}$, $L1 = 2.2 \mu\text{H}$, $R_1 = 1 \text{ M}\Omega$, $R_2 = 0 \Omega$, $V_{IN} = 3.6 \text{ V}$, $V_{EN} = V_{IN}$, $V_{OUT} = 1.8 \text{ V}$, $T_A = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

Table 6. Electrical characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--|---------------------------------------|---|------|------|------|----------|
| General section | | | | | | |
| IQ | Quiescent current | EN= V_{IN} , AUX=GND, device does not switch (V_{OUT} pin voltage > V_{OUT} setting value), $V_{IN} = V_{OUT_min.} + 0.3 \text{ V}$ (1.8 V min.) to 5.5 V | - | 500 | 1000 | nA |
| ISD | Shutdown current | EN=GND, shutdown current into V_{IN} | - | 10 | 200 | nA |
| V_{UVLO} | Undervoltage lockout threshold | V_{IN} rising | - | 1.63 | 1.72 | V |
| | | V_{IN} falling | 1.51 | 1.57 | - | V |
| | | Hysteresis | - | 65 | - | mV |
| $V_{th100\%+}$ | 100% mode leave threshold | V_{IN} rising, 100% mode is disabled with $V_{IN} = V_{OUTnom} + V_{th100\%+}$ | - | 300 | - | mV |
| $V_{th100\%-}$ | 100% mode enter threshold | V_{IN} falling, 100% mode is entered with $V_{IN} = V_{OUTnom} + V_{th100\%-}$ | - | 200 | - | |
| Output voltage | | | | | | |
| V_{OUT} | Output voltage range | Output voltages are selected with pins D0, D1, D2 | 1.0 | - | 3.3 | V |
| | Output voltage accuracy | $V_{IN} = 3.6 \text{ V}$, whole V_{OUT} range, $I_{OUT} = 100 \text{ mA}$ | -1.5 | - | 1.5 | % |
| t_{ONmin} | Minimum on-time | $V_{IN} = 3.6 \text{ V}$, $V_{OUT} = 2 \text{ V}$, $I_{OUT} = 0 \text{ A}$ | - | 225 | - | ns |
| t_{OFFmin} | Minimum off-time | $V_{IN} = 2.3 \text{ V}$ | - | 50 | - | ns |
| $t_{startupd}$ | Start-up delay time | V_{EN} from low to high, $V_{IN} = 3.6 \text{ V}$, $V_{OUT} = 1.8 \text{ V}$ | - | 1.7 | - | ms |
| R_{OUTDIS} | Output discharge MOSFET on-resistance | $V_{EN} = \text{GND}$ | - | 30 | - | Ω |
| Logic inputs (EN, D0, D1, D2) AUX | | | | | | |
| V_{IL} | Low level input voltage threshold | $V_{IN} = 1.8 \text{ V}$ to 5.5 V | - | - | 0.3 | V |
| V_{IH} | High level input voltage threshold | | 1.1 | - | - | |
| Power switch | | | | | | |
| $R_{DS(on)}$ | High-side MOSFET on-resistance | $V_{IN} = 3.6 \text{ V}$, $I_{sw} = 100 \text{ mA}$ | - | 0.45 | 0.60 | Ω |
| | Low-side MOSFET on-resistance | | - | 0.23 | 0.35 | |
| I_{LIM1} | High-side MOSFET switch current limit | For ST1PS02AQTR and ST1PS02DQTR: $1.8 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$, $CL = \text{GND}$ | 500 | 850 | 1150 | mA |
| | | For ST1PS02BQTR: $2.1 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$, $CL = \text{GND}$ | 650 | 850 | 1150 | |
| | | For ST1PS02CQTR: $2.9 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$, $CL = \text{GND}$ | 650 | 850 | 1150 | |

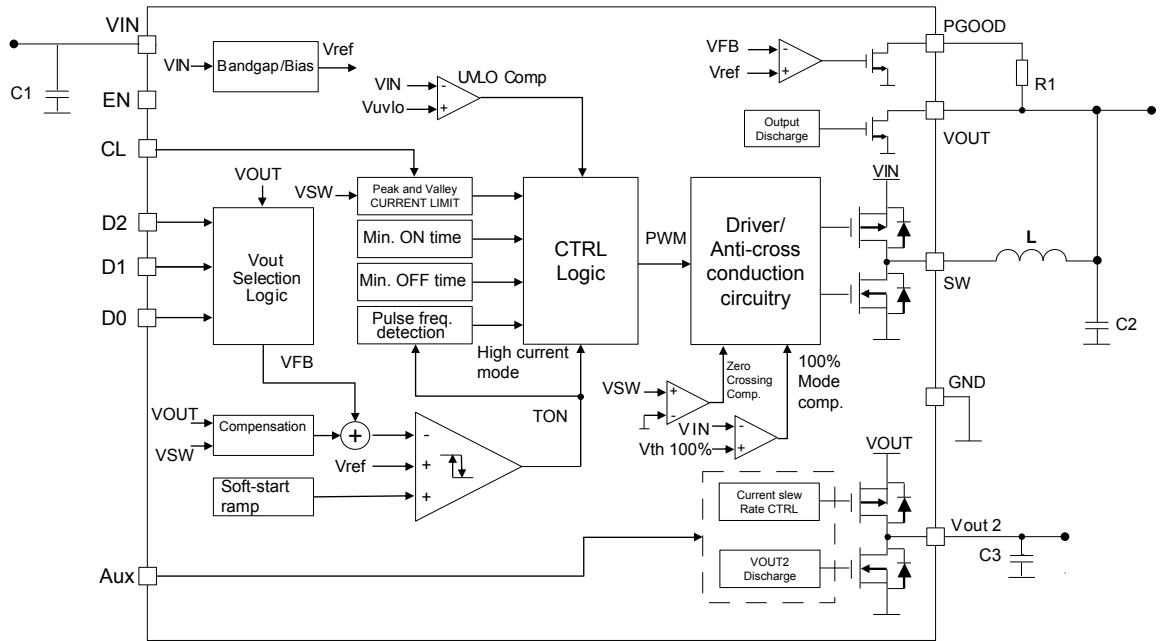
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------------|--|--|------|------|------|------|
| I _{LIM2} | High-side MOSFET switch current limit | 1.8 V ≤ V _{IN} ≤ 3.6 V, R2=1 MΩ | 500 | 650 | 800 | mA |
| I _{LIM3} | High-side MOSFET switch current limit | 1.8 V ≤ V _{IN} ≤ 3.6 V, R2=2.2 MΩ | 180 | 250 | 360 | mA |
| Power Good output (PGOOD) | | | | | | |
| V _{thpg} | Power Good threshold voltage | Rising output voltage on V _{OUT} pin, referred to V _{OUT} selected (D0, D1, D2) | 95 | 97.5 | - | % |
| V _{thpgH} | | Hysteresis | -4 | -3.5 | -2.5 | |
| V _{OL} | Low level output voltage | 1.8 V ≤ V _{IN} ≤ 5.5 V, E _N = GND, current into PGOOD pin, I _{PGOOD} = 4 mA | - | - | 0.23 | V |
| Auxiliary output (Vout2) | | | | | | |
| R _{AUX} | Load switch on-resistance | I _{OUT2} = 100 mA, Aux=V _{IN} , V _{OUT} =2 V | 0.5 | 0.75 | 0.95 | Ω |
| R _{disc2} | Auxiliary output discharge MOSFET on-resistance (discharger) | I _{OUT2} =-10 mA, Aux=GND | - | 30 | 50 | |
| tr _{aux} | V _{aux} rise time | Starting with AUX low-to-high transition, time to ramp V _{LOAD} from 0 V to 95% V _{OUT} = 1.4 V, for ST1PS02AQTR: V _{IN} = 3.6 V, I _{OUT2} = 1 mA | - | 300 | 650 | μs |
| | | Starting with AUX low-to-high transition, time to ramp V _{LOAD} from 0 V to 95% V _{OUT} = 1.8 V, for ST1PS02BQTR: V _{IN} = 3.6 V, I _{OUT2} = 1 mA | - | 400 | 700 | |
| | | Starting with AUX low-to-high transition, time to ramp V _{LOAD} from 0 V to 95% V _{OUT} = 2.6 V, for ST1PS02CQTR: V _{IN} = 3.6 V, I _{OUT2} = 1 mA | - | 400 | 700 | |
| | | Starting with AUX low-to-high transition, time to ramp V _{LOAD} from 0 V to 95% V _{OUT} = 1.1 V, for ST1PS02DQTR: V _{IN} = 3.6 V, I _{OUT2} = 1 mA | - | 300 | 600 | |

Table 7. Output voltage settings

| Device | D2 | D1 | D0 | V _{OUT} |
|-------------|----|----|----|------------------|
| ST1PS02AQTR | 0 | 0 | 0 | 1.40 V |
| | 0 | 0 | 1 | 1.45 V |
| | 0 | 1 | 0 | 1.50 V |
| | 0 | 1 | 1 | 1.55 V |
| | 1 | 0 | 0 | 1.60 V |
| | 1 | 0 | 1 | 1.65 V |
| | 1 | 1 | 0 | 1.70 V |
| | 1 | 1 | 1 | 1.75 V |
| ST1PS02BQTR | 0 | 0 | 0 | 1.8 V |
| | 0 | 0 | 1 | 1.9 V |
| | 0 | 1 | 0 | 2.0 V |
| | 0 | 1 | 1 | 2.1 V |
| | 1 | 0 | 0 | 2.2 V |
| | 1 | 0 | 1 | 2.3 V |
| | 1 | 1 | 0 | 2.4 V |
| | 1 | 1 | 1 | 2.5 V |
| ST1PS02CQTR | 0 | 0 | 0 | 2.6 V |
| | 0 | 0 | 1 | 2.7 V |
| | 0 | 1 | 0 | 2.8 V |
| | 0 | 1 | 1 | 2.9 V |
| | 1 | 0 | 0 | 3.0 V |
| | 1 | 0 | 1 | 3.1 V |
| | 1 | 1 | 0 | 3.2 V |
| | 1 | 1 | 1 | 3.3 V |
| ST1PS02DQTR | 0 | 0 | 0 | 1.10 V |
| | 0 | 0 | 1 | 1.15 V |
| | 0 | 1 | 0 | 1.20 V |
| | 0 | 1 | 1 | 1.25 V |
| | 1 | 0 | 0 | 1.30 V |
| | 1 | 0 | 1 | 1.35 V |
| | 1 | 1 | 0 | 1.00 V |
| | 1 | 1 | 1 | 1.05 V |

6 ST1PS02 block diagram

Figure 3. Block diagram



7 Operation description

The ST1PS02 is an ultra-low quiescent new generation buck converter. It targets a very small quiescent current consumption (typical 500 nA) and it guarantees high efficiency operation even down to few microampere loads. It is based on a hysteretic comparator that senses the coil ripple current that is held constant in all operation modes. The device has seamless transition between PFM (pulse frequency modulation) and PWM (pulse width modulation) mode with low ripple and good load transient response.

In order to maintain constant ripple current on the selected coil, the device changes switching frequency, which also depends on input supply voltage. During PWM mode (heavy load), the device operates in continuous conduction up to 400 mA and switching frequency can reach 2 MHz maximum.

7.1 Power save mode

At light load the device enters automatically power save mode with total current consumption from the input power supply of 500 nA typical; during this condition most of the internal blocks are turned off in order to reach ultra-low power consumption. During this time, the load current is supported by the output capacitor.

7.2 Output voltage

The device allows the output voltage selection without an external resistor divider. Standard digital inputs are used to configure the device to supply a fixed output voltage according to [Table 7. Output voltage settings](#). The V_{OUT} pin must be connected directly and as close as possible to the inductor terminal to obtain the best performance and get the best output voltage regulation. The output voltage can be dynamically changed to implement voltage scaling.

7.3 Output discharge and UVLO

The device embeds a fast output discharge circuitry active when the enable pin is held to ground (EN=gnd) or when the input supply voltage reaches the minimum voltage level set by the UVLO protection circuit (undervoltage lock-out protection circuit). The UVLO rising threshold at 1.63 V (typ.) guarantees a proper device supply voltage operation. The output discharge function is available for the ST1PS02xQTR versions.

7.4 Soft-start and current limitation

The device embeds a fixed soft-start circuit active during a limited time period (few ms). This feature allows the inrush current to be minimized from the power supply in case of weak source. During this period internal circuit reduces to 280 mA the typical switch current limit. The ST1PS02 embeds also a current limit on high side MOSFET to protect the device against overload or short circuit on the output, during normal operation conditions. In order to improve the flexibility, the current limit threshold can be set by an external resistor connected between CL pin and GND. As soon as an overload (or short-circuit) is detected, the output current provided is defined by R2 resistor. When the device enters 100% duty cycle operation condition and an overload (or short-circuit) occurs, the output voltage is set in shutdown in order to limit the power dissipation. To restart the device operation, a LOW to HIGH cycle on EN pin is necessary.

7.5 100% duty cycle operation

The device enters 100% duty cycle operation if the input voltage comes close to the selected output voltage. During this mode, the regulator is turned off and output pin is directly connected to the input pin through the high-side MOSFET. The output voltage follows the input level minus the voltage drop across the internal MOSFET and the inductor. Once the input voltage exceeds the 100% duty cycle leave threshold, the device restarts to switch and regulates the select output voltage again.

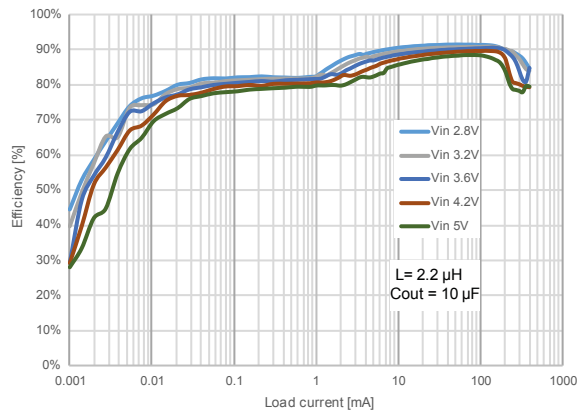
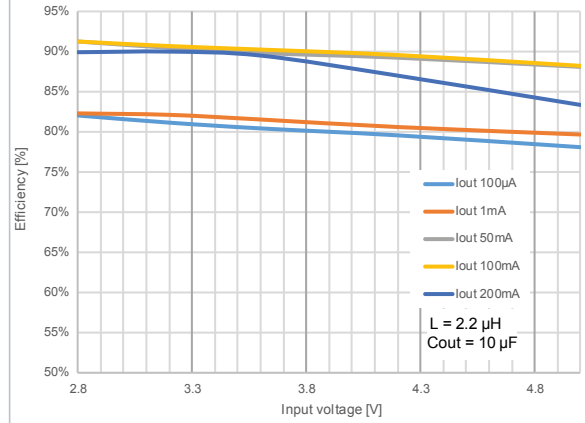
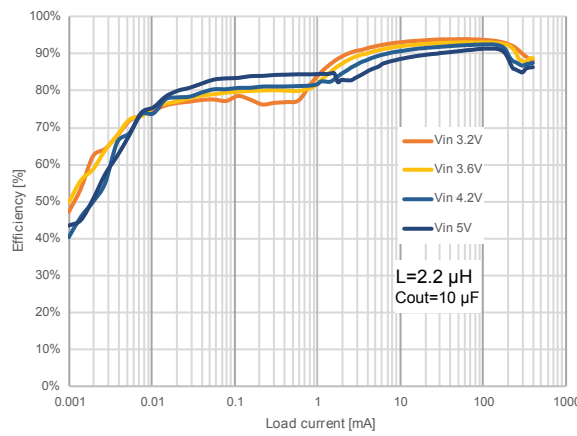
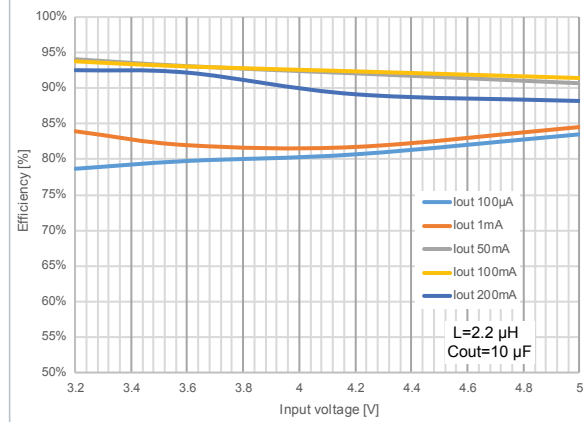
7.6 Auxiliary output (Vout2)

The Aux pin controls Vout2 output. It provides the same regulated voltage level as the main output (V_{OUT}) less drop on the load switch circuitry, when Aux pin tied high. The Vout2 pin allows connecting/disconnecting the other system load to the output of the ST1PS02.

7.7 Power Good flag

The Power Good comparator monitors the selected V_{OUT} voltage. The Power Good open drain output is in high impedance when the V_{OUT} reaches the correct voltage level while it switches to low level when V_{OUT} falls below the normal voltage level.

8 Typical performance characteristics

Figure 4. Efficiency vs load, $V_{OUT} = 1.8\text{ V}$

Figure 5. Efficiency vs V_{IN} , $V_{OUT} = 1.8\text{ V}$

Figure 6. Efficiency vs load, $V_{OUT} = 2.5\text{ V}$

Figure 7. Efficiency vs V_{IN} , $V_{OUT} = 2.5\text{ V}$


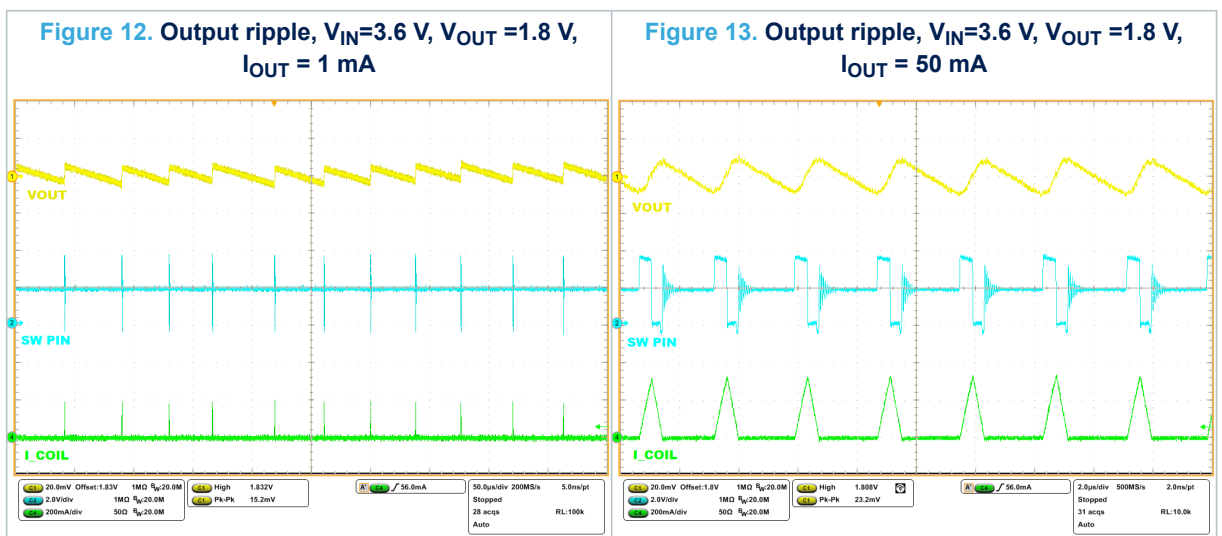
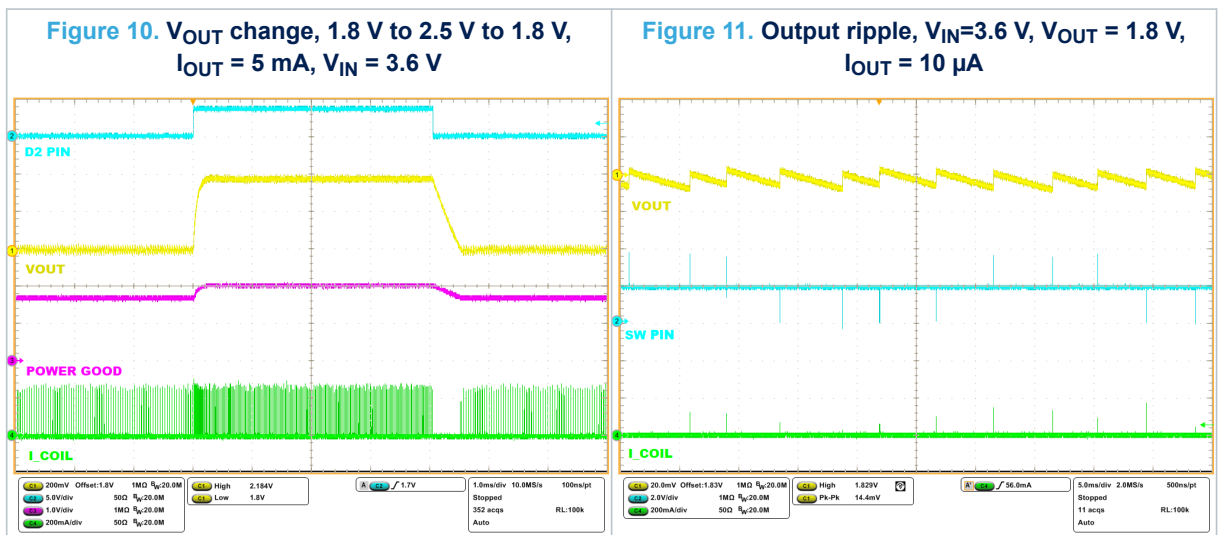
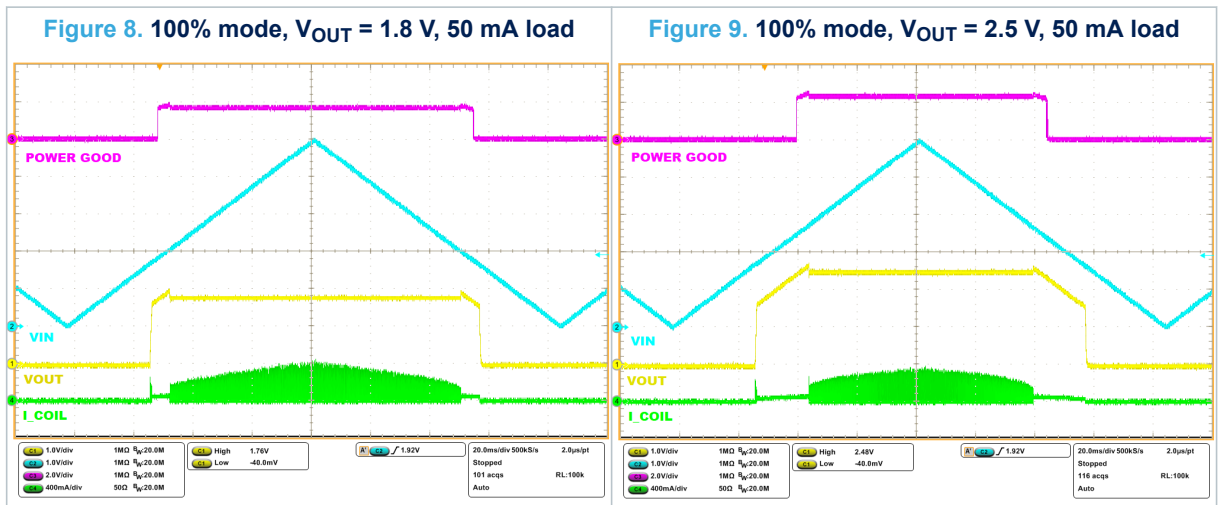


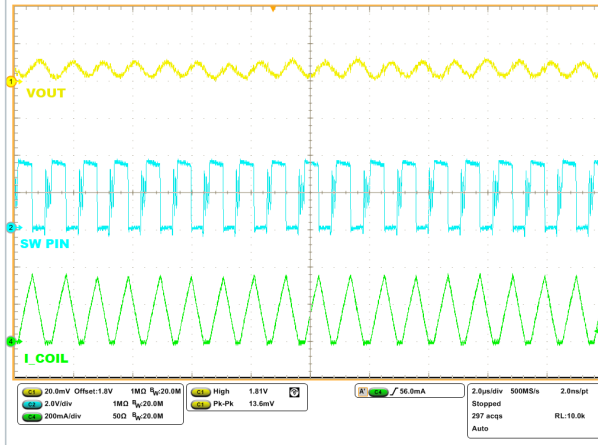
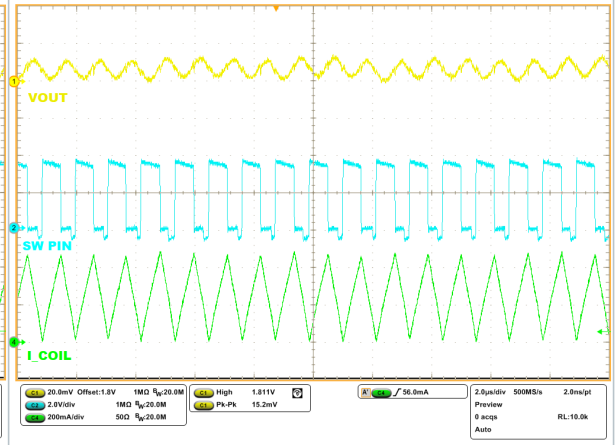
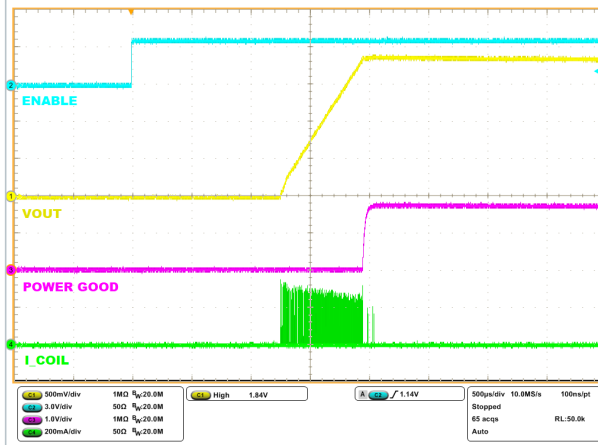
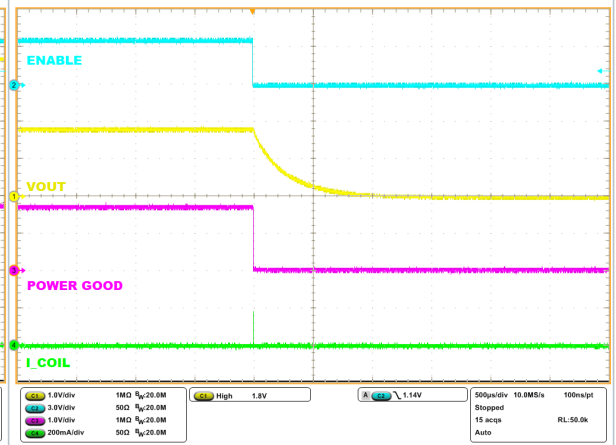
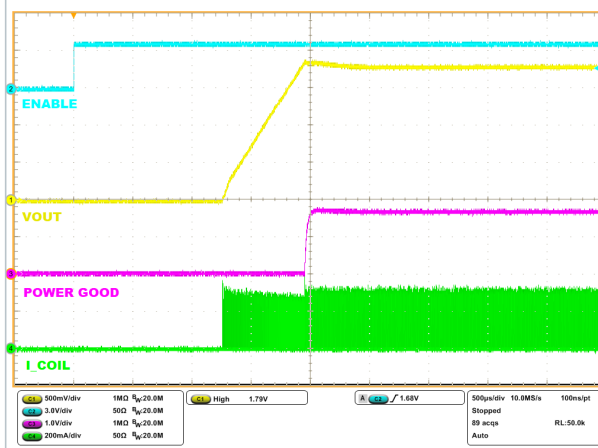
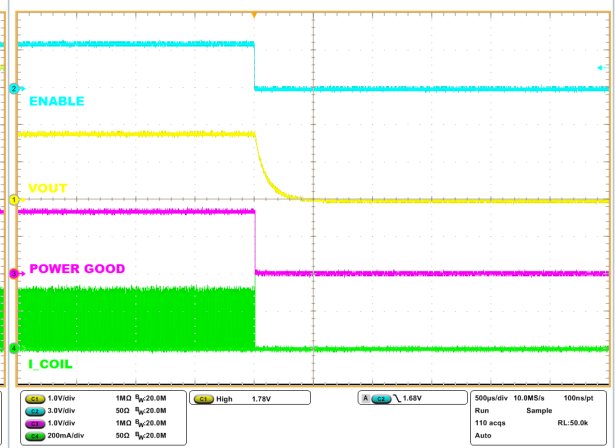
Figure 14. Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=150\text{ mA}$

Figure 15. Output ripple, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=250\text{ mA}$

Figure 16. Start-up, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, no load

Figure 17. Disable, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, no load

Figure 18. Start-up, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=100\text{ mA}$

Figure 19. Disable, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=100\text{ mA}$


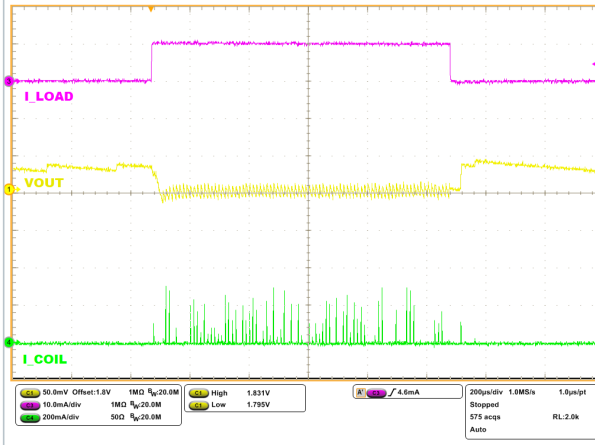
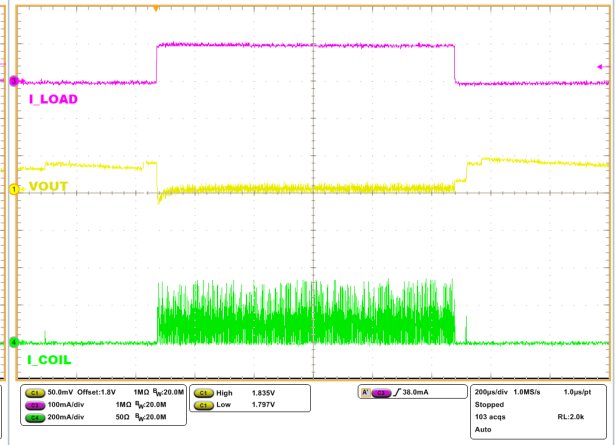
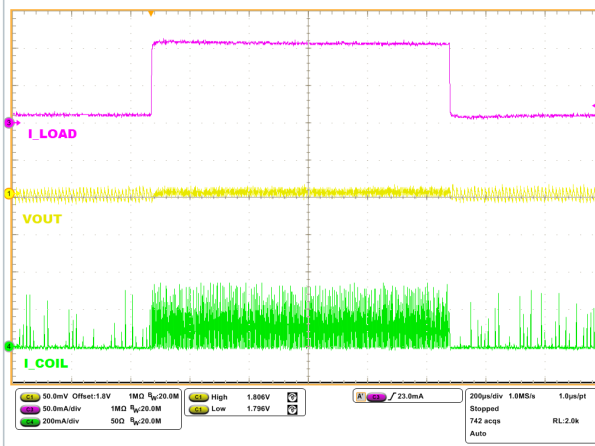
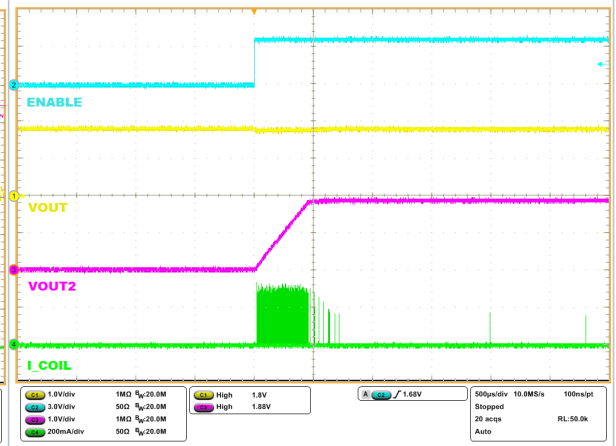
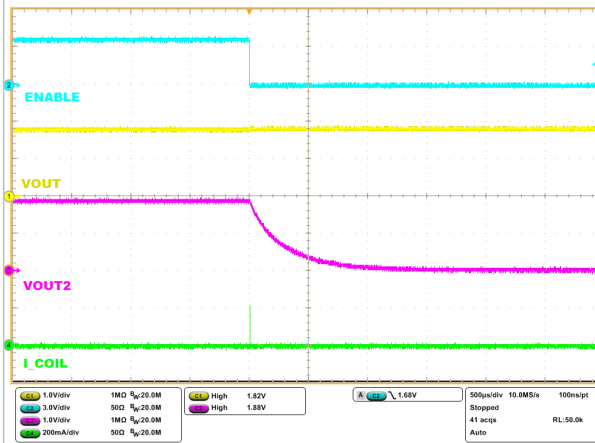
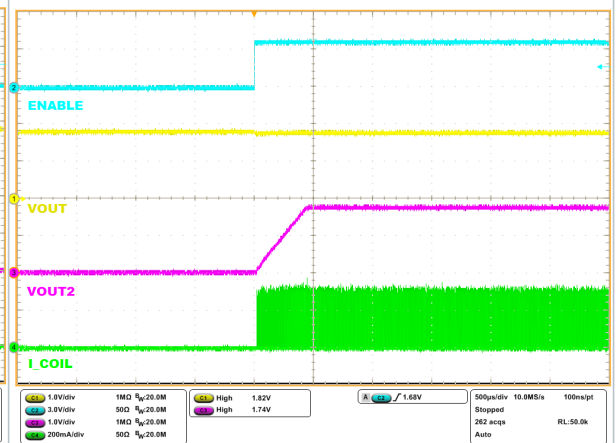
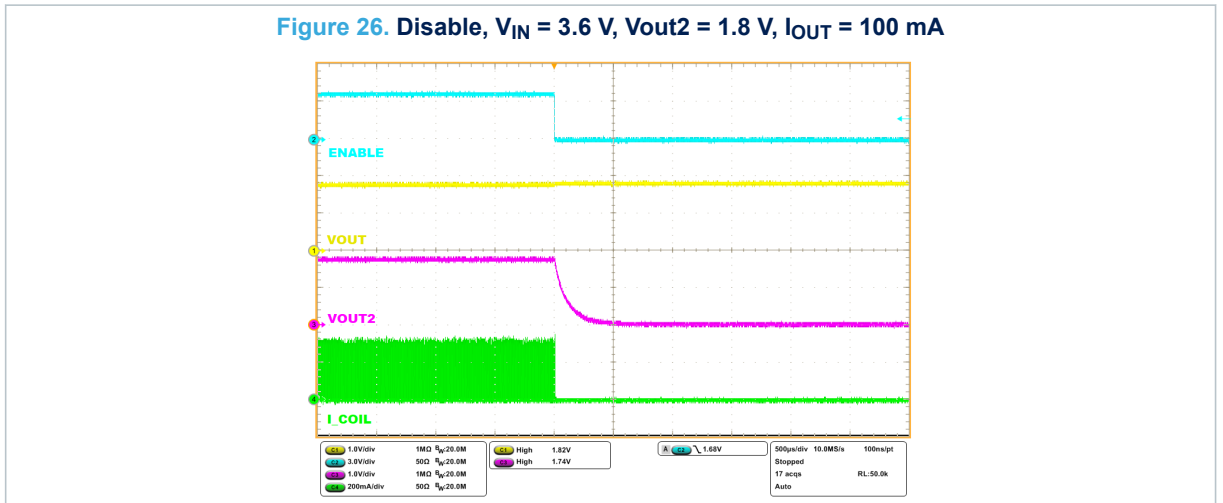
Figure 20. Load transient, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=50\ \mu\text{A}$ to 10 mA

Figure 21. Load transient, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=0$ to 100 mA

Figure 22. Load transient, $V_{IN}=3.6\text{ V}$, $V_{OUT}=1.8\text{ V}$, $I_{OUT}=10$ to 100 mA

Figure 23. Start-up, $V_{IN}=3.6\text{ V}$, $V_{OUT2}=1.8\text{ V}$, no load

Figure 24. Disable, $V_{IN}=3.6\text{ V}$, $V_{OUT2}=1.8\text{ V}$, no load

Figure 25. Start-up, $V_{IN}=3.6\text{ V}$, $V_{OUT2}=1.8\text{ V}$, $I_{OUT}=100\text{ mA}$


Figure 26. Disable, $V_{IN} = 3.6\text{ V}$, $V_{out2} = 1.8\text{ V}$, $I_{OUT} = 100\text{ mA}$



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 TQFN12 (2.0x1.7x0.55 mm) package information

Figure 27. TQFN12 (2.0x1.7x0.55 mm) package outline

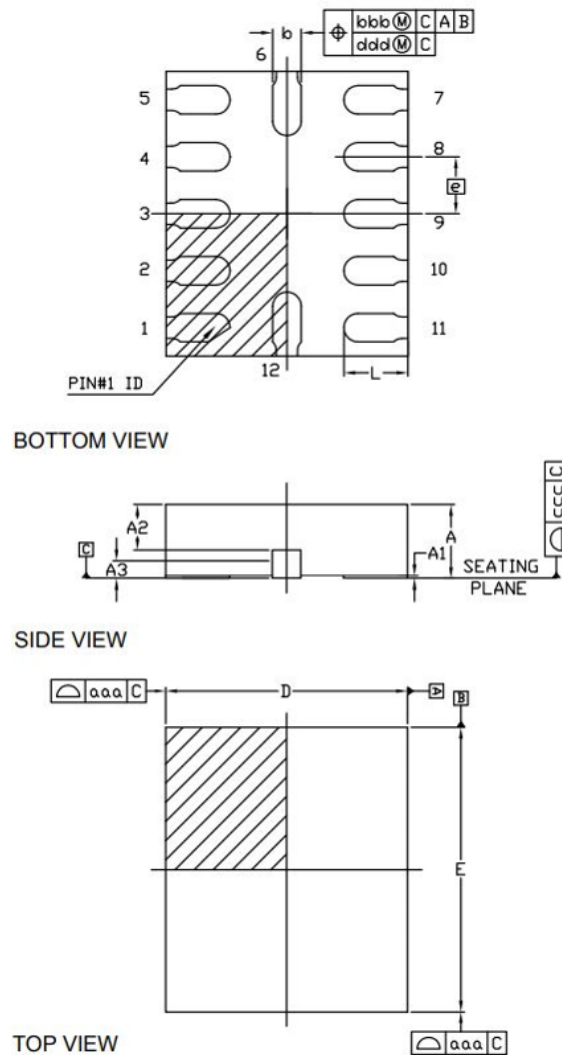
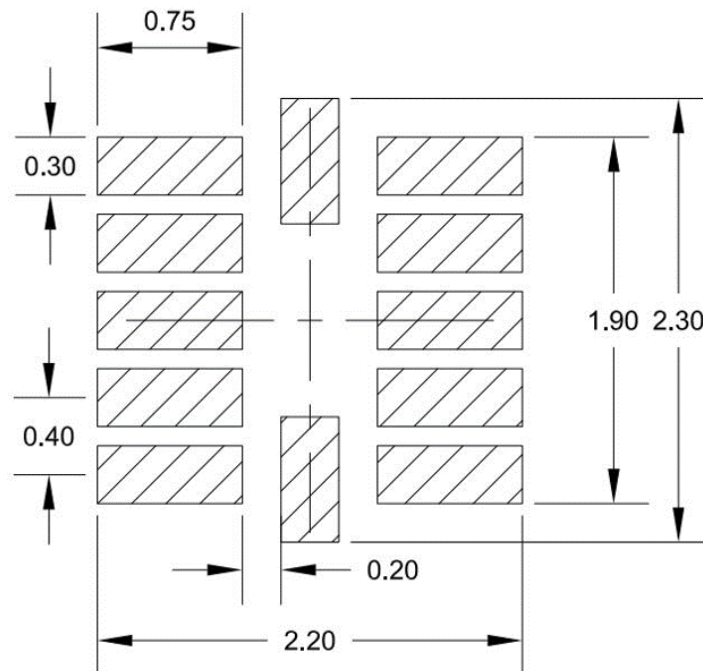
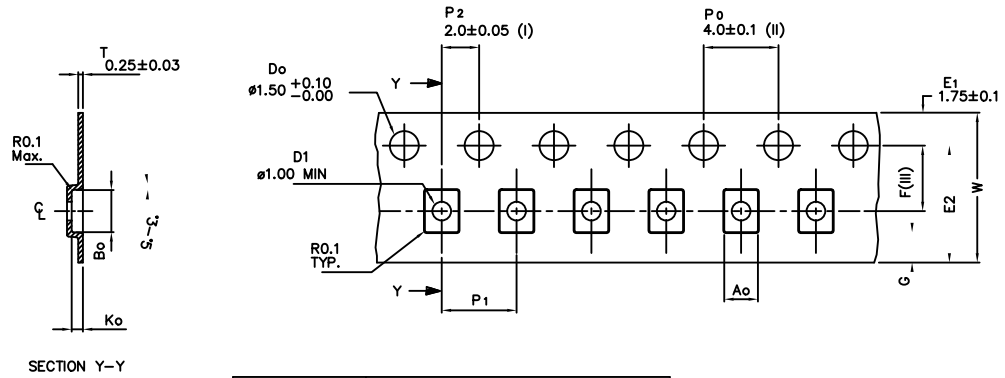


Table 8. TQFN12 (2.0x1.7x0.55 mm) mechanical data

| Symbol | Milimeters | | |
|--------|------------|-------|------|
| | Min. | Typ. | Max. |
| A | 0.40 | 0.50 | 0.55 |
| A1 | 0.00 | 0.03 | 0.05 |
| A2 | 0.28 | 0.38 | 0.48 |
| A3 | | 0.125 | |
| b | 0.15 | 0.20 | 0.25 |
| D | 1.60 | 1.70 | 1.80 |
| E | 1.90 | 2.00 | 2.10 |
| e | | 0.40 | |
| L | 0.35 | 0.45 | 0.55 |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.08 | |
| ddd | | 0.05 | |
| eee | | 0.10 | |

Figure 28. TQFN12 (2.0x1.7x0.55 mm) recommended footprint


9.2 TQFN12 (2.0x1.70x0.55 mm) packing information

Figure 29. TQFN12 (2.0x1.70x0.55 mm) carrier tape outline


| | |
|----|----------------|
| Ao | 1.80 +/−0.05 |
| Bo | 2.25 +/−0.05 |
| Ko | 0.60 +/−0.05 |
| F | 3.50 +/−0.05 |
| P1 | 4.00 +/−0.1 |
| D1 | 1.00 MIN |
| T | 0.25 +/−0.03 |
| G | 0.75 MIN. |
| E2 | 6.25 MIN. |
| W | 8.00 +0.3/−0.1 |

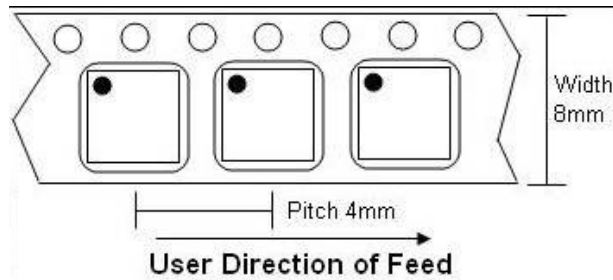
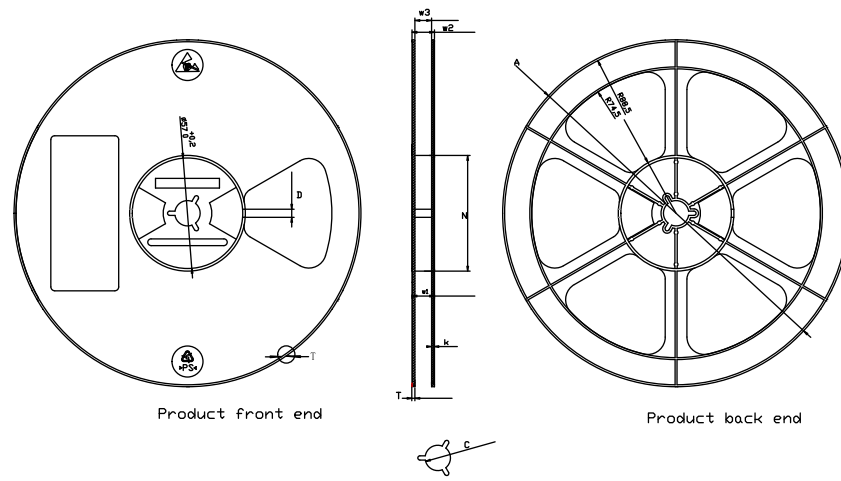
Figure 30. TQFN12 (2.0x1.70x0.55 mm) tape orientation


Figure 31. TQFN12 (2.0x1.70x0.55 mm) reel outline


| TYPE | A | N | C | D | w1 | w2 | w3 | T | k |
|------|--------|-------|----------|---------|-----------------------------------|--------|--------|----------|---------------------------------------|
| 8MM | ∅180±2 | ∅60±1 | 13,1±0,2 | 4,2±0,5 | 8,4 ⁺¹ _{-0,2} | 11,6±1 | 8,75±1 | 1,5±0,15 | 1,25 ^{+0,1} _{-0,05} |

10 Ordering information

Table 9. Ordering information

| Order codes | Output voltages | Output discharge | Package | Packing |
|--------------|-------------------------------|------------------|--|---------------|
| ST1PS02AQTR | 1.40 V to 1.75 V, 50 mV steps | Yes | TQFN12 (2.0x1.7 mm) 400 µm pitch | Tape and reel |
| ST1PS02A1QTR | | No | | |
| ST1PS02BQTR | 1.8 V to 2.5 V, 100 mV steps | Yes | | |
| ST1PS02B1QTR | | No | | |
| ST1PS02CQTR | 2.6 V to 3.3 V, 100 mV steps | Yes | | |
| ST1PS02C1QTR | | No | | |
| ST1PS02DQTR | 1.0 V to 1.35 V, 50 mV steps | Yes | | |
| ST1PS02D1QTR | | No | | |

Revision history

Table 10. Document revision history

| Date | Version | Changes |
|-------------|---------|--|
| 17-Feb-2020 | 1 | Initial release. |
| 17-Mar-2020 | 2 | Updated Section 5 Electrical characteristics. Minor text changes throughout the document. |
| 20-Mar-2020 | 3 | Updated PGOOD an EN description in Table 2, IQ test condition in Table 6 and Block diagram. |
| 05-Jul-2021 | 4 | Updated Figure 1. ST1PS02 application schematic. Updated Section 7.4 Soft-start and current limitation. Updated Table 6. Electrical characteristics. |

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