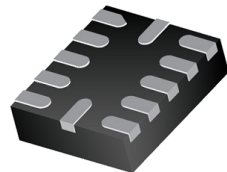


## 400 mA nano-quiescent synchronous step-down converter with digital voltage selection, Power Good and load switch



TQFN12 (2.0x1.7 mm)

### Features

- 500 nA input quiescent current at  $V_{IN} = 3.6$  V (not switching)
- 92% typical efficiency at 10 mA load ( $V_{IN} = 3.6$  V,  $V_{OUT} = 2.5$  V)
- 100% duty cycle
- 1.8 V to 5.5 V input operating range
- Undervoltage lockout: 1.57 V ( $V_{IN}$  falling, typ.)
- Up to 400 mA output current capability
- Low power control operation for the best efficiency
- Embedded soft-start circuit
- Tiny external components:  $L = 2.2$   $\mu$ H typ.
- Selectable output voltages: 1.6 V to 3.3 V
- Output voltage Power Good
- $\pm 1.5\%$  output voltage accuracy ( $V_{OUT}$ ,  $T_A = 25$  °C)
- Dynamic output voltage selection (D0, D1 and D2)
- Load switch controlled by AUX input
- Available in TQFN12 package

### Applications

- Wearable applications
- Personal tracking monitors
- Smart watches, sport bands
- Energy harvesting, wireless sensors
- Wearable and fitness accessories
- Industrial sensors, portable low power devices
- Single cell Li-Ion battery applications
- Bluetooth® Low Energy
- Zigbee

### Description

The ST1PS03 is a nano-quiescent miniaturized synchronous step-down converter, which is able to provide up to 400 mA output current with an input voltage ranging from 1.8 V to 5.5 V. This converter is specifically designed for applications where high efficiency, PCB size and thickness are the key factors.

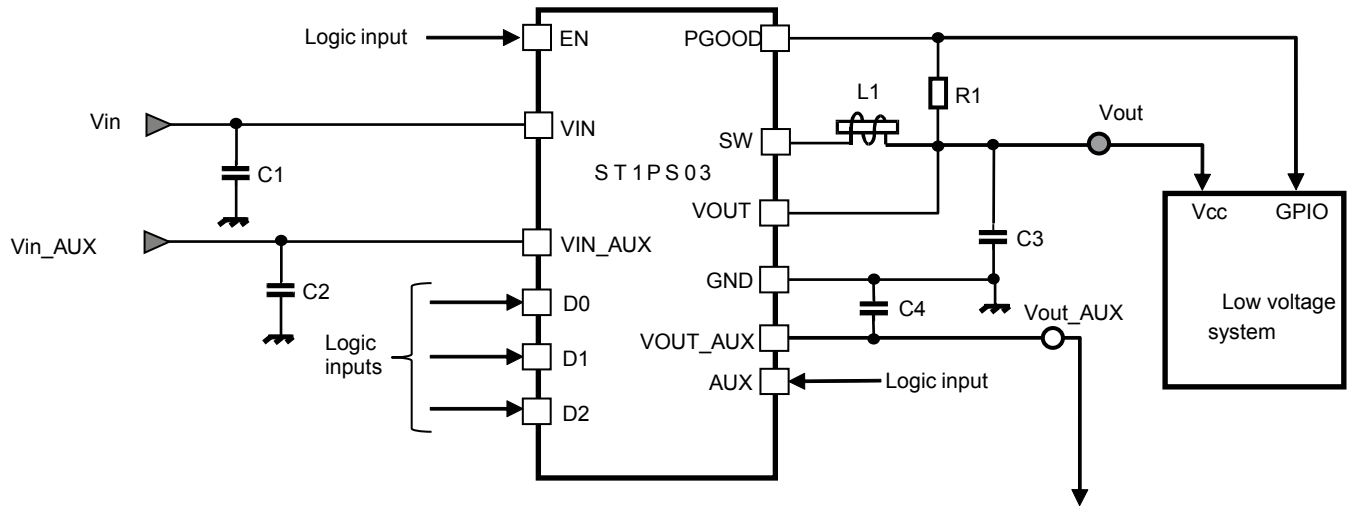
The output voltage can be set using three digital control inputs, a  $V_{OUT}$  from 1.6 V to 3.3 V can be dynamically selected. Thanks to the enhanced PCC (peak current control) the ST1PS03 reaches very high efficiency conversion using just a 2.2  $\mu$ H inductor and two small capacitors. An advanced design circuitry is developed to minimize the quiescent current. The device embeds a controlled switch accessible from VIN\_AUX, to supply a subsystem. Finally, it is available in thin plastic package.

Product status link

ST1PS03

# 1 Application schematic

**Figure 1. ST1PS03 application schematic**



**Table 1. Typical external components**

Component	Description	Value	Size - imperial (metric)
C <sub>1</sub> , C <sub>3</sub>	Ceramic capacitor with low ESR values	10 μF	0603 (1608)
C <sub>2</sub> , C <sub>4</sub>	Ceramic capacitor with low ESR values		
L1	Inductor	2.2 μH	0806 (2016)
R <sub>1</sub>	Pull-up resistor	1 MΩ	0402 (1005)

## 2 Pin configuration

Figure 2. TQFN12 package (top through view)

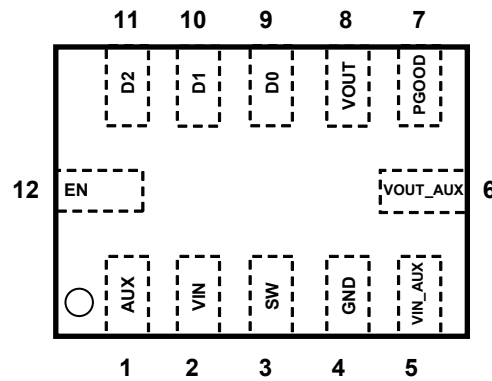


Table 2. Pin description

Name	Bump name	Description
AUX	1	Enable for the auxiliary output voltage
VIN	2	Input supply voltage. Bypass this pin to ground with a 10 $\mu$ F capacitor
SW	3	Switching output. Inductor connection
GND	4	Ground
VIN_AUX	5	Input for auxiliary channel
VOUT_AUX	6	Auxiliary output pin (100 mA max. load)
PGOOD	7	Open drain output. It is in high impedance when the output voltage reaches 97%
VOUT	8	Sense pin used to monitor output voltage
D0	9	Output voltage selection inputs
D1	10	
D2	11	
EN	12	Enable pin. High logic level turns on the IC. VIN threshold referred

### 3 Functional pin description

#### **GND**

**Device ground pin.**

#### **VIN**

**Supply voltage.** This pin supplies power to the internal analog and digital circuitries when voltage is higher than  $V_{UVLO}$ . Bypass this pin to GND with a 10  $\mu$ F ceramic capacitor. Input capacitor  $C_1$  must be chosen with low ESR to reduce the input voltage ripple.

#### **VIN\_AUX**

**Supply voltage pin for auxiliary channel.** This pin supplies internal switch "S3" and must be always  $\leq V_{IN}$ . It is recommended to have VIN\_AUX present before setting AUX pin to high, to avoid inrush current on VIN\_AUX supply voltage.

Bypass this pin to GND with a ceramic capacitor, see [Table 1. Typical external components](#). Input capacitor  $C_2$  must be chosen with low ESR to reduce the input voltage ripple.

#### **SW**

**Switching output pin.** Inductor connection to internal PMOS and NMOS switches.

#### **VOUT**

**Output voltage sense input pin.** It provides the feedback voltage level to the regulation circuitry. 10  $\mu$ F output capacitor  $C_3$  must be connected close to the pin or through a short trace and should have low ESR to reduce the output voltage ripple.

#### **EN**

**Enable pin.** A logic low level on this pin disables the device. High level enables the device. Do not leave this pin floating.

#### **D0, D1, D2**

**Output voltage selection pins.** See [Table 7. Output voltage settings](#) for  $V_{OUT}$  selection. Do not leave these pins floating. These pins can be dynamically changed during operation.

#### **PGOOD**

**Power Good open drain output pin.** If used it requires a pull-up resistor to hold a high level signal. High impedance indicates that  $V_{OUT}$  is above proper good threshold.

#### **AUX**

**Load switch selection pins.**

When this pin and EN are both set to high, VOUT\_AUX output is enabled. If EN low and AUX High VOUT\_AUX is disabled. Held to ground if auxiliary output (VOUT\_AUX) is not used or if it should be disabled.

#### **VOUT\_AUX**

**Auxiliary output pin.** 0.6 Ohm switch connect VIN\_AUX to this PIN when enabled. 10  $\mu$ F output capacitor  $C_4$  must be connected close to the pin or through a short trace. This output is controlled from a soft-start circuit and it is not current limited. If unused can be left open.

## 4 Maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{IN}$	Power and signal supply voltage	- 0.3 to + 6.5	V
VIN_AUX	Auxiliary input	- 0.3 to + 6.5	V
EN, D0, D1, D2, AUX	Logic input pins	- 0.3 to + 6.5	V
$V_{OUT, SW}$	Output signal monitoring and switching pins	-0.3 to $V_{IN} + 0.3$	V
VOUT_AUX	Load switch output pin	- 0.3 to + 6.5	V
PGOOD	Power Good open drain output pin	- 0.3 to + 6.5	V
$T_J$	Junction temperature	-40 to 125	°C
$T_{STG}$	Storage temperature	-55 to 150	°C

*Note:* Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

**Table 4. Thermal data**

Symbol	Parameter	TQFN12	Unit
$R_{thJA}$	Thermal resistance junction-ambient	75	°C/W

**Table 5. Recommended operating conditions**

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Input supply voltage	1.8		5.5	V
VIN_AUX	Auxiliary input	0		VIN	V
IOUT_AUX	Auxiliary output current			100	mA

## 5 Electrical characteristics

$C_1 = 10 \mu\text{F}$ ,  $C_2 = 10 \mu\text{F}$ ,  $C_3 = 10 \mu\text{F}$ ,  $C_4 = 10 \mu\text{F}$ ,  $L1 = 2.2 \mu\text{H}$ ,  $V_{\text{IN}} = 3.6 \text{ V}$ ,  $V_{\text{EN}} = V_{\text{IN}}$ ,  $V_{\text{OUT}} = 1.8 \text{ V}$ ,  $T_A = 25 \text{ }^\circ\text{C}$  unless otherwise specified.

**Table 6. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>General section</b>						
$I_{\text{Q}}$	Quiescent current	$V_{\text{EN}} = V_{\text{IN}}$ , $AUX = \text{GND}$ , device does not switch ( $V_{\text{OUT}}$ pin voltage > $V_{\text{OUT}}$ setting value)	-	500	850	nA
$I_{\text{SD}}$	Shutdown current	$V_{\text{EN}} = \text{GND}$ , shutdown current into $V_{\text{IN}}$	-	10	200	nA
$V_{\text{UVLO}}$	Undervoltage lockout threshold	$V_{\text{IN}}$ rising	-	1.63	1.72	V
		$V_{\text{IN}}$ falling	1.51	1.57	-	V
		Hysteresis	-	65	-	mV
$V_{\text{th}100\%+}$	100% mode leave threshold	$V_{\text{IN}}$ rising, 100% mode is disabled with $V_{\text{IN}} = V_{\text{OUTnom}} + V_{\text{th}100\%+}$	-	300	-	mV
$V_{\text{th}100\%-}$	100% mode enter threshold	$V_{\text{IN}}$ falling, 100% mode is entered with $V_{\text{IN}} = V_{\text{OUTnom}} + V_{\text{th}100\%-}$	-	200	-	
<b>Output voltage</b>						
$V_{\text{OUT}}$	Output voltage range	Output voltages are selected with pins D0, D1, D2	1.6	-	3.3	V
	Output voltage accuracy	$V_{\text{IN}} = 3.6 \text{ V}$ , whole $V_{\text{OUT}}$ range, $I_{\text{OUT}} = 100 \text{ mA}^{(1)}$	-1.5	-	1.5	%
$t_{\text{ONmin}}$	Minimum on-time	$V_{\text{IN}} = 3.6 \text{ V}$ , $V_{\text{OUT}} = 2.1 \text{ V}$ , $I_{\text{OUT}} = 0 \text{ A}$	-	225	-	ns
$t_{\text{OFFmin}}$	Minimum off-time	$V_{\text{IN}} = 2.3 \text{ V}$	-	50	-	ns
$t_{\text{startupd}}$	Start-up delay time	$V_{\text{EN}}$ from low to high, $V_{\text{IN}} = 3.6 \text{ V}$ , $V_{\text{OUT}} = 1.8 \text{ V}$	-	1.7	-	ms
$R_{\text{OUTDIS}}$	Output discharge MOSFET on-resistance	$V_{\text{EN}} = \text{GND}$ (For AQTR version only), $I_{\text{OUT}} = -10 \text{ mA}$	-	30	-	$\Omega$
<b>Logic inputs (EN, AUX)</b>						
$V_{\text{IL}L1}$	Low level input voltage threshold	$V_{\text{IN}} = 1.8 \text{ to } 5.5 \text{ V}$	-	-	0.3	V
$V_{\text{IH}L1}$	High level input voltage threshold		1.1	-	-	
<b>Logic inputs (D0, D1, D2)</b>						
$V_{\text{IL}L2}$	Low level input voltage threshold	$V_{\text{IN}} = 3.6 \text{ V}$			0.3	V
$V_{\text{IH}L2}$	High level input voltage threshold		1.1			
<b>Power switch</b>						
$R_{\text{DS(on)}}$	High-side MOSFET on-resistance	$V_{\text{IN}} = 3.6 \text{ V}$ , $I_{\text{sw}} = 100 \text{ mA}$	-	0.45	0.60	$\Omega$
	Low-side MOSFET on-resistance		-	0.23	0.35	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{LIM}$	High-side MOSFET switch current limit	$3.6\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	500		1150	mA
<b>Power Good output (PGOOD)</b>						
$V_{PG\_TH}$	Power Good threshold voltage	Rising output voltage on $V_{OUT}$ pin, referred to $V_{OUT}$ selected (D0, D1, D2)	95	97.5	-	%
$V_{PG\_TH\_Hy}$		Hysteresis	-4	-3.5	-2.5	
$V_{OL}$	Low level output voltage	$1.8\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ , $E_N = GND$ , current into PGOOD pin, $I_{PGOOD} = 4\text{ mA}$	-	-	0.23	V
<b>Auxiliary output (VOUT_AUX)</b>						
$R_{AUX}$	High-side Mosfet on-resistance	$I_{OUT\_AUX} = 100\text{ mA}$ , $AUX = VIN$ $VIN\_AUX = 2\text{ V}$		0.6	0.8	$\Omega$
$R_{OUTDIS\_AUX}$	Low-side Mosfet on-resistance (discharger)	$I_{OUT\_AUX} = -10\text{ mA}$ , $AUX = GND$	-	30	50	
$tr_{aux}$	Vaux rise time	$V_{IN} = 3.6\text{ V}$ $VIN\_AUX = 1.8\text{ V}$ , AUX low to high transition, time to ramp $V_{OUT\_AUX}$ from 0 to 95% of $VIN\_AUX$	-	400	850	$\mu\text{s}$
$LK_{AUX}$	Leakage from $VIN\_AUX$ <sup>(1)</sup>	$VIN = VIN\_AUX = 3.3\text{ V}$ , $AUX = GND$		0.3		nA

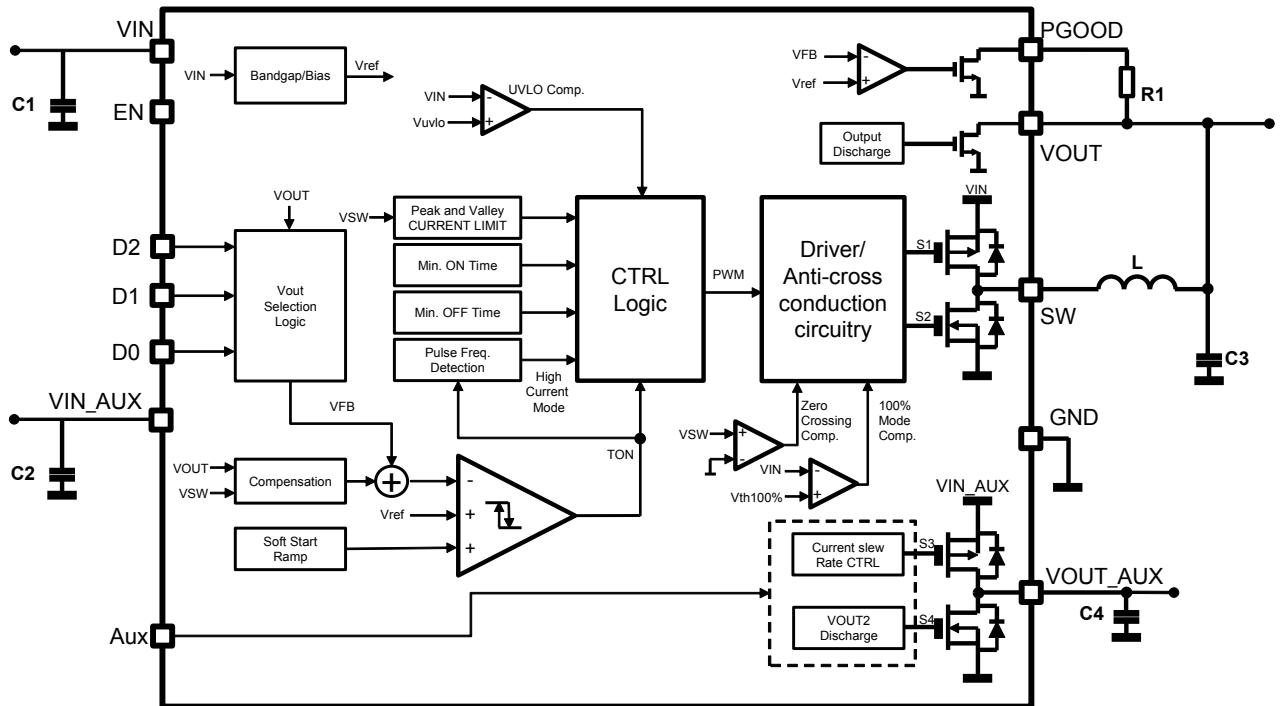
1. Specified by design – not tested in production.

**Table 7. Output voltage settings**

Device	D2	D1	D0	$V_{OUT}$
ST1PS03	0	0	0	1.8 V
	0	0	1	3.3 V
	0	1	0	2.8 V
	0	1	1	2.7 V
	1	0	0	3.0 V
	1	0	1	2.1 V
	1	1	0	1.6 V
	1	1	1	2.5 V

## 6 ST1PS03 block diagram

Figure 3. Block diagram





## 7 Operation description

The ST1PS03 is an ultra-low quiescent new generation buck converter. It targets a very small quiescent current consumption (typical 500 nA) and it guarantees high efficiency operation even down to few microampere loads. It is based on a hysteretic comparator that senses the coil ripple current that is held constant in all operation modes. The device has seamless transition between PFM (pulse frequency modulation) and PWM (pulse width modulation) mode with low ripple and good load transient response.

In order to maintain constant ripple current on the selected coil, the device changes switching frequency, which also depends on input supply voltage. During PWM mode (heavy load), the device operates in continuous conduction up to 400 mA and switching frequency can reach 2 MHz maximum.

### 7.1 Power save mode

At light load, the device enters automatically power save mode with total current consumption from the input power supply of 500 nA typical. During this condition most of the internal blocks are turned off in order to reach ultra-low power consumption. During this time, the load current is supported by the output capacitor.

### 7.2 Output voltage

The device allows the output voltage selection without an external resistor divider. Standard digital inputs are used to configure the device to supply a fixed output voltage according to [Table 7. Output voltage settings](#). The  $V_{OUT}$  pin must be connected directly and as close as possible to the inductor terminal to obtain the best performance and get the best output voltage regulation. The output voltage can be dynamically changed to implement voltage scaling.

### 7.3 Output discharge and UVLO

The device embeds a fast output discharge circuitry active when the enable pin is held to ground ( $EN = GND$ ) or when the input supply voltage reaches the minimum voltage level set by the UVLO protection circuit (undervoltage lock-out protection circuit). The UVLO rising threshold at 1.63 V (typ.) guarantees a proper device supply voltage operation. The output discharge function is available for the ST1PS03AQTR versions.

### 7.4 Soft-start and current limitation

The device embeds a fixed soft-start circuit active during a limited time period (few ms). This feature allows the inrush current to be minimized from the power supply in case of weak source. During this period internal circuit reduces to 280 mA the typical switch current limit. The ST1PS03 embeds also a current limit on high-side MOSFET to protect the device against overload or short-circuit on the output, during normal operation conditions. When the device enters 100% duty cycle operation condition and an overload (or short-circuit) occurs, the device reacts switching asynchronously between  $I_{lim}$  and  $I_{valley}$  with a given slope, dependent on L and  $C_{out}$ .

### 7.5 100% duty cycle operation

The device enters 100% duty cycle operation if the input voltage comes close to the selected output voltage. During this mode, the regulator is turned off and output pin is directly connected to the input pin through the high-side MOSFET. The output voltage follows the input level minus the voltage drop across the internal MOSFET and the inductor. Once the input voltage exceeds the 100% duty cycle leave threshold, the device restarts to switch and regulates the selected output voltage again.

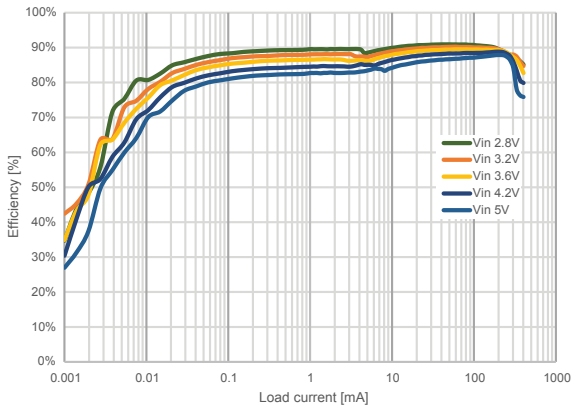
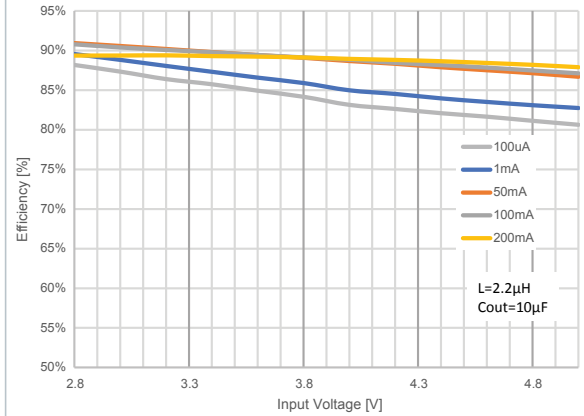
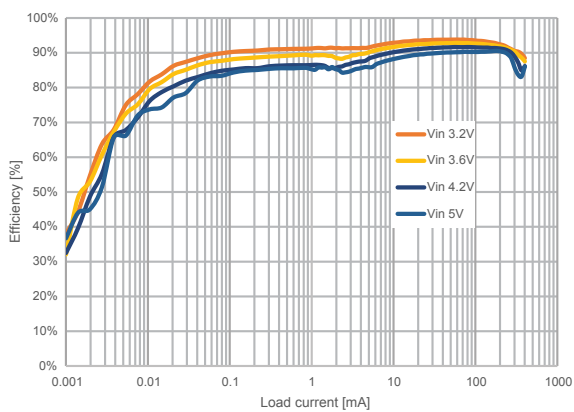
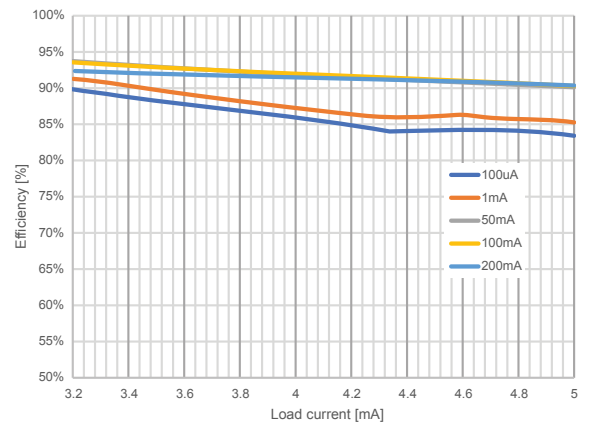
### 7.6 Auxiliary output (VOUT\_AUX)

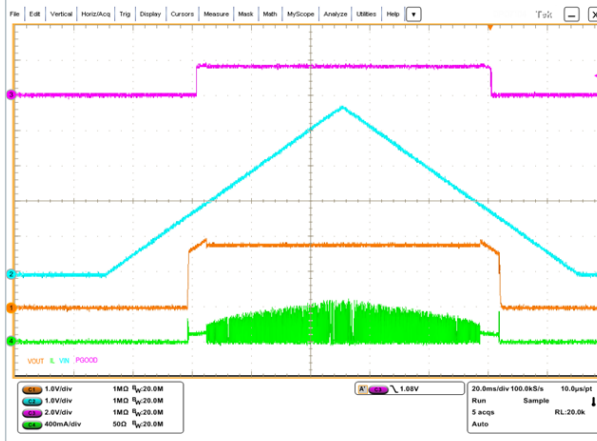
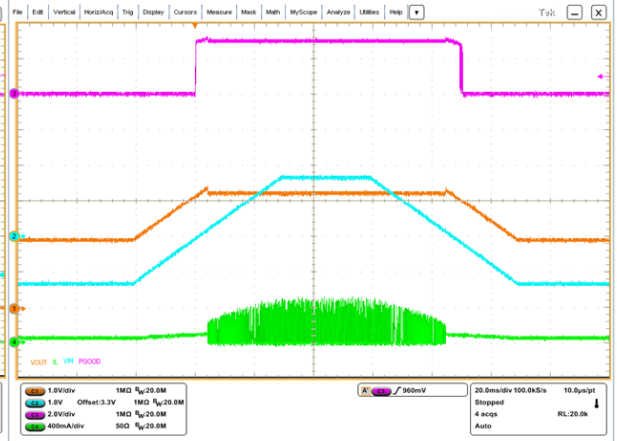
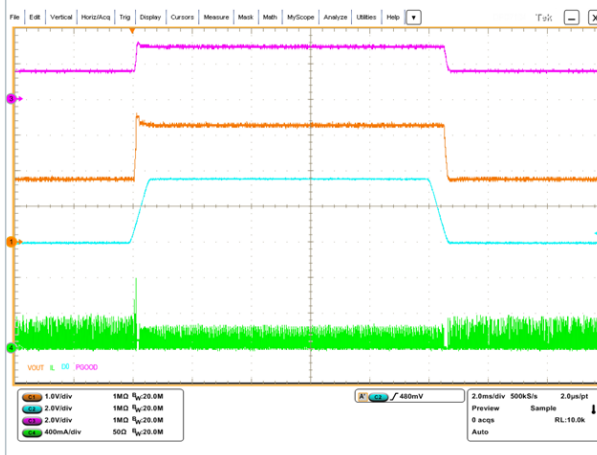
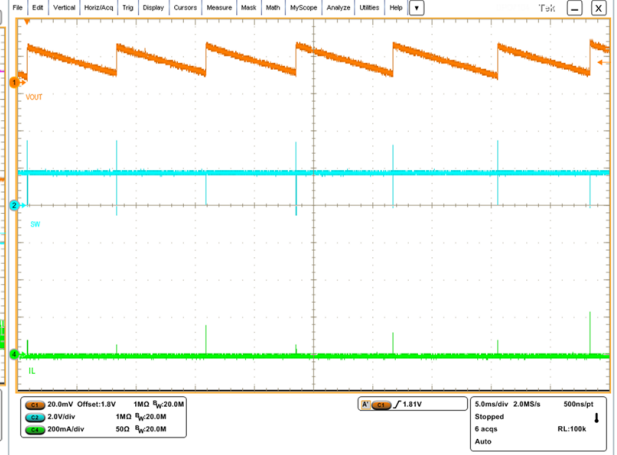
The AUX pin controls  $V_{OUT\_AUX}$  output. It provides the same regulated voltage level as  $V_{IN\_AUX}$  input voltage, less drop on the load switch circuitry, when AUX pin and EN tied high. The  $V_{OUT\_AUX}$  pin allows connecting/disconnecting the other system load to the output of the ST1PS03.

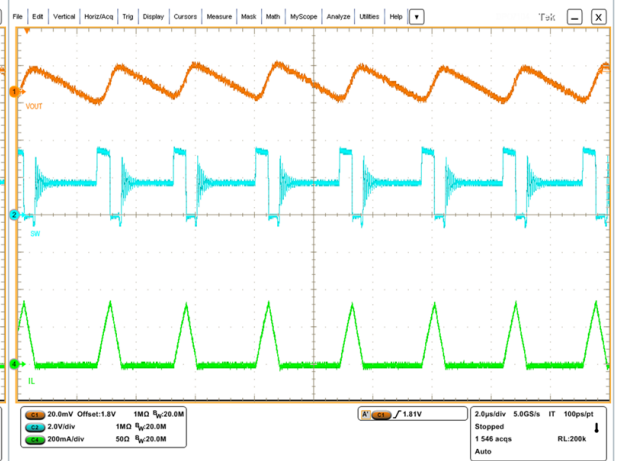
## 7.7 Power Good flag

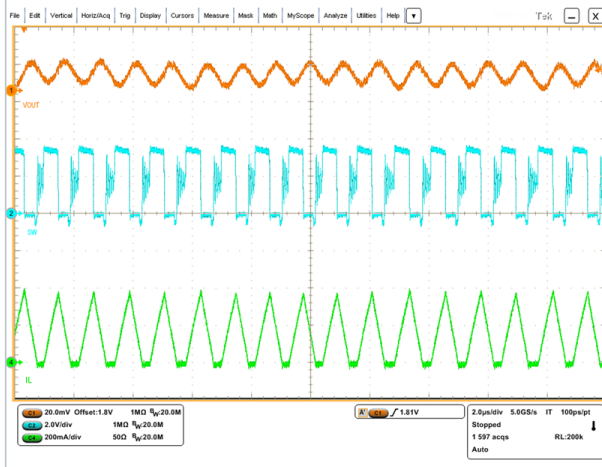
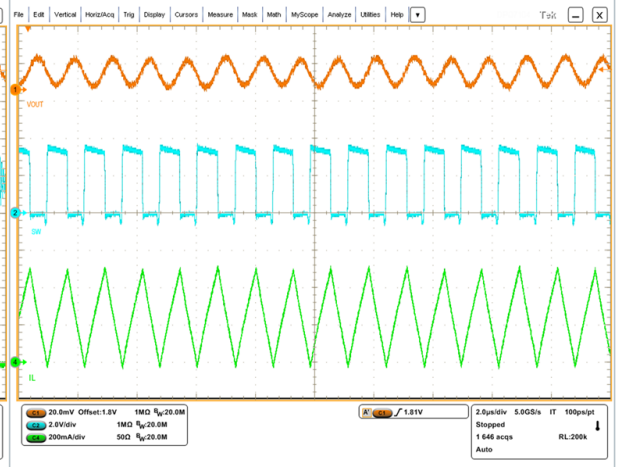
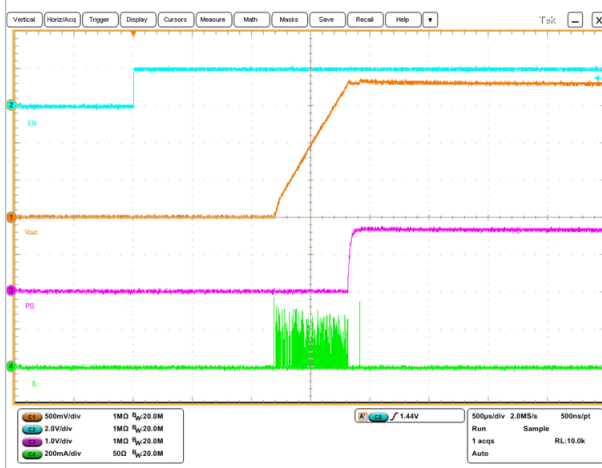
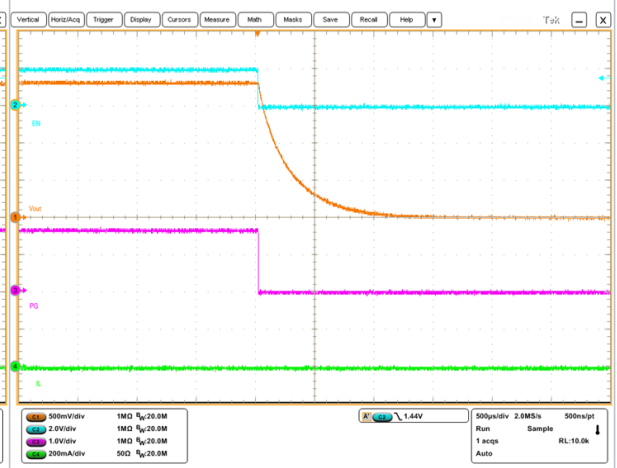
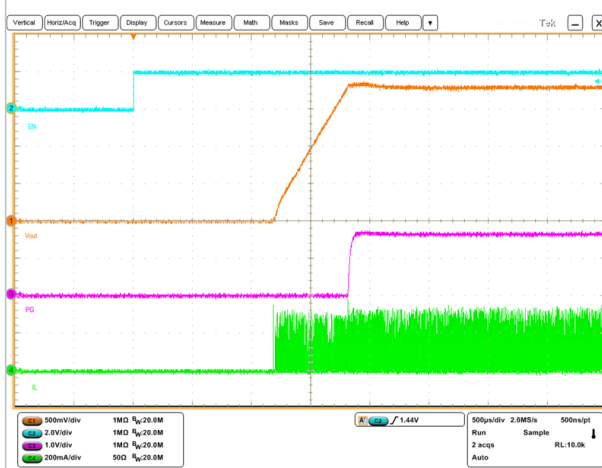
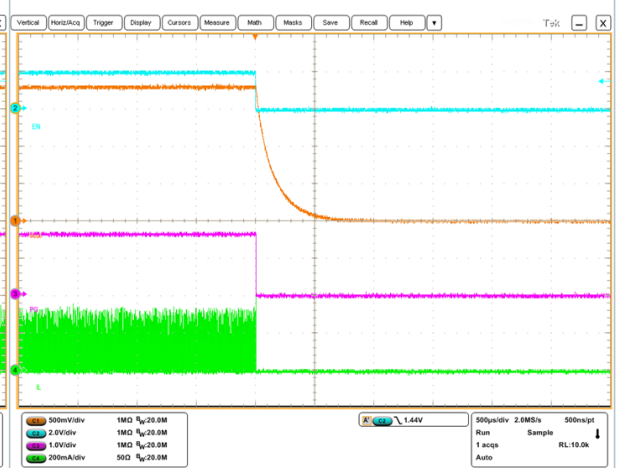
The Power Good comparator monitors the selected  $V_{OUT}$  voltage. The open drain output is in high impedance when the  $V_{OUT}$  reaches the correct voltage level while it switches to low level when  $V_{OUT}$  falls below the normal voltage level.

## 8 Typical performance characteristics

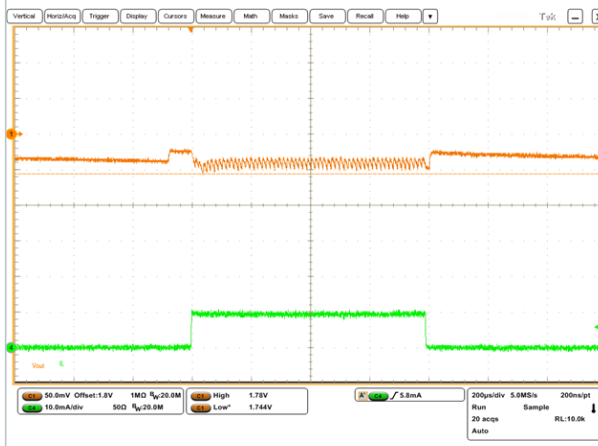
**Figure 4. Efficiency vs. load,  $V_{OUT} = 1.8\text{ V}$** 

**Figure 5. Efficiency vs.  $V_{IN}$ ,  $V_{OUT} = 1.8\text{ V}$** 

**Figure 6. Efficiency vs. load,  $V_{OUT} = 2.5\text{ V}$** 

**Figure 7. Efficiency vs.  $V_{IN}$ ,  $V_{OUT} = 2.5\text{ V}$** 


**Figure 8. 100% mode,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} 100\text{ mA}$ ,  $R_{load} = 18\text{ Ohm}$ ,  $V_{EN} = V_{IN}$ ,  $AUX = GND$** 

**Figure 9. 100% mode,  $V_{OUT} = 3.3\text{ V}$ ,  $I_{OUT} 100\text{ mA}$ ,  $R_{load} = 33\text{ Ohm}$ ,  $V_{EN} = V_{IN}$ ,  $AUX = GND$** 

**Figure 10.  $V_{in} = 3.6\text{ V}$ ,  $V_{out} = 1.8\text{ to }3.3\text{ V}$ ,  $R_{load} 33\text{ Ohm}$ ,  $AUX = GND$ ,  $V_{IN\_AUX} = \text{floating}$** 

**Figure 11. Output ripple,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} = 10\text{ }\mu\text{A}$** 

**Figure 12. Output ripple,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$** 

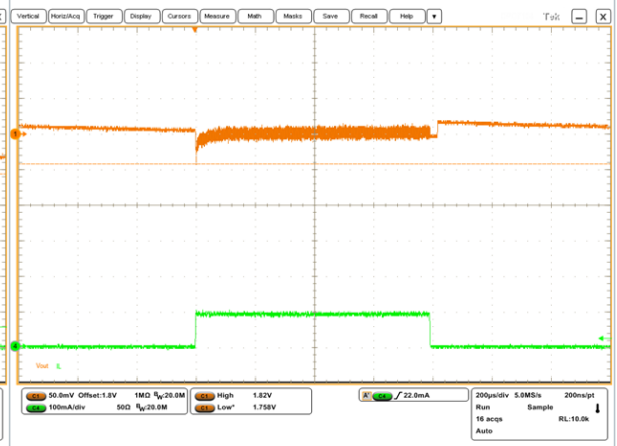
**Figure 13. Output ripple,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$** 


**Figure 14. Output ripple,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} = 150\text{ mA}$** 

**Figure 15. Output ripple,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} = 250\text{ mA}$** 

**Figure 16. Startup,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ , no load**

**Figure 17. Disable,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ , no load**

**Figure 18. Startup,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $R_{LOAD} = 18\text{ Ohm}$** 

**Figure 19. Disable,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $R_{LOAD} = 18\text{ Ohm}$** 


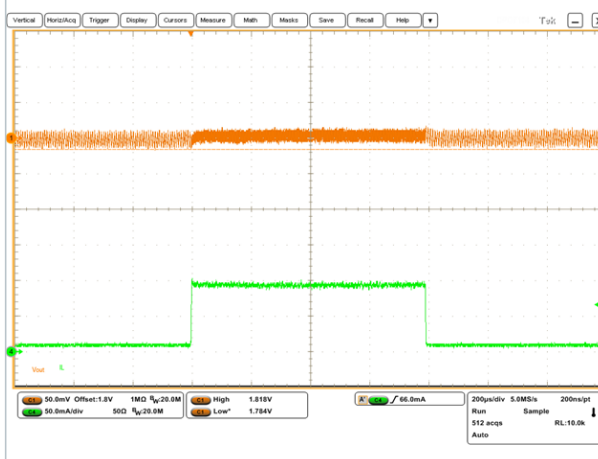
**Figure 20. Load transient,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} = 50\ \mu\text{A}$  to  $10\text{ mA}$**



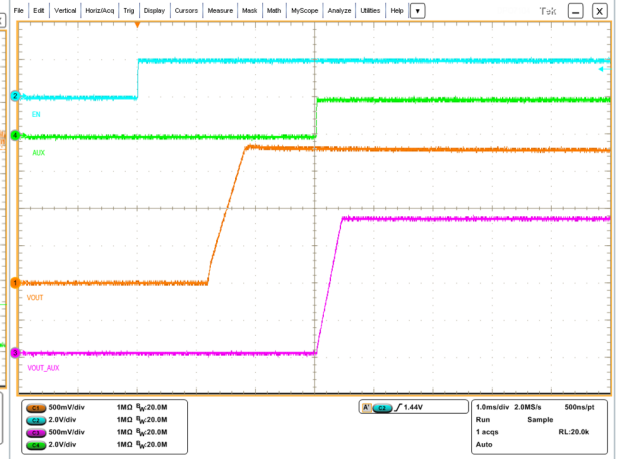
**Figure 21. Load transient,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} = 0$  to  $100\text{ mA}$**

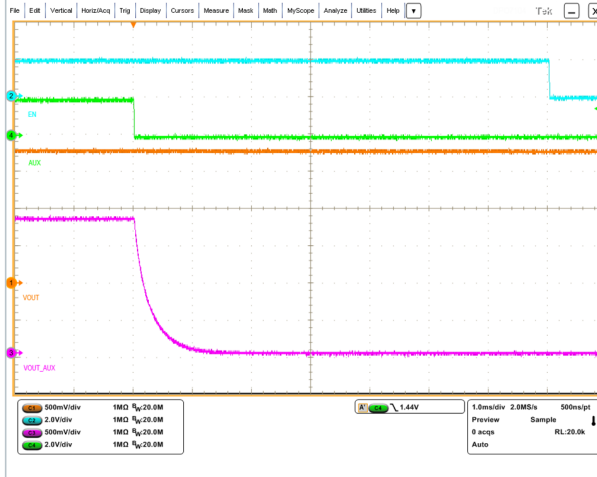
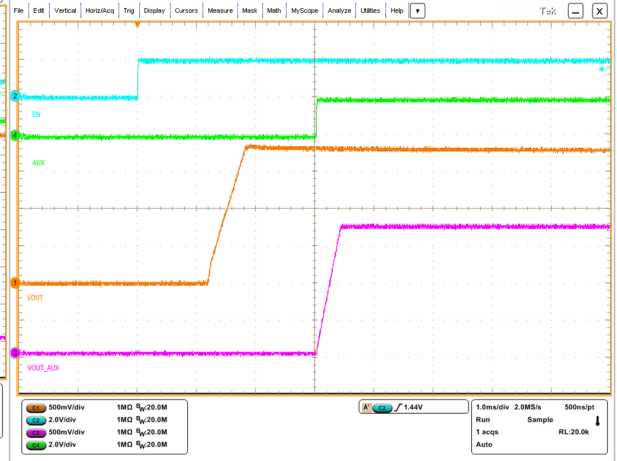
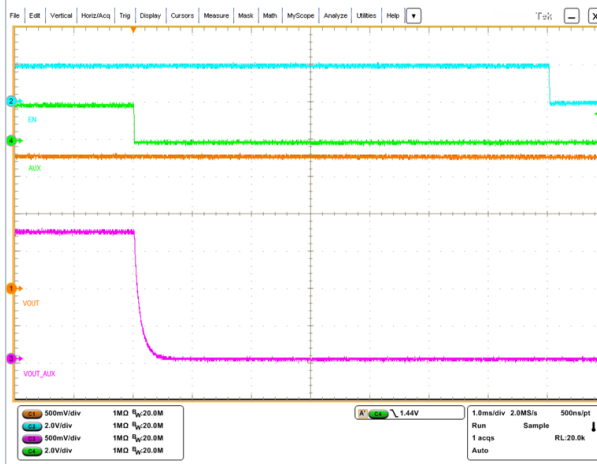
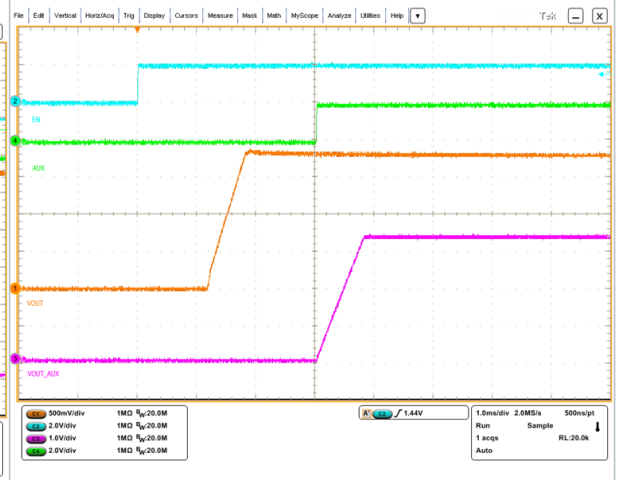
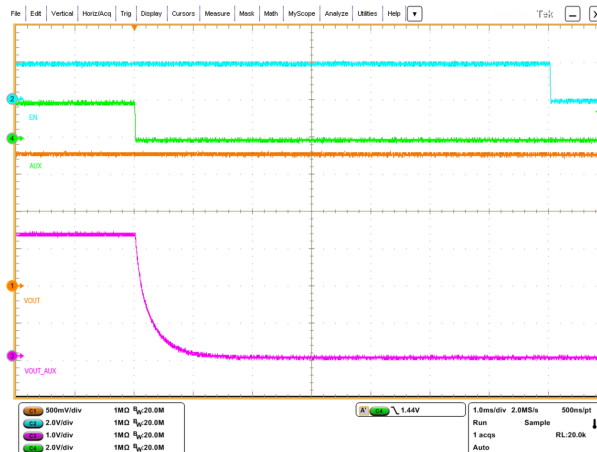


**Figure 22. Load transient,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $I_{OUT} = 10$  to  $100\text{ mA}$**



**Figure 23. Startup,  $V_{IN} = 3.6\text{ V}$ ,  $V_{IN\_AUX} = 1.8\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $V_{OUT\_AUX} = 1.8\text{ V}$ , no load**



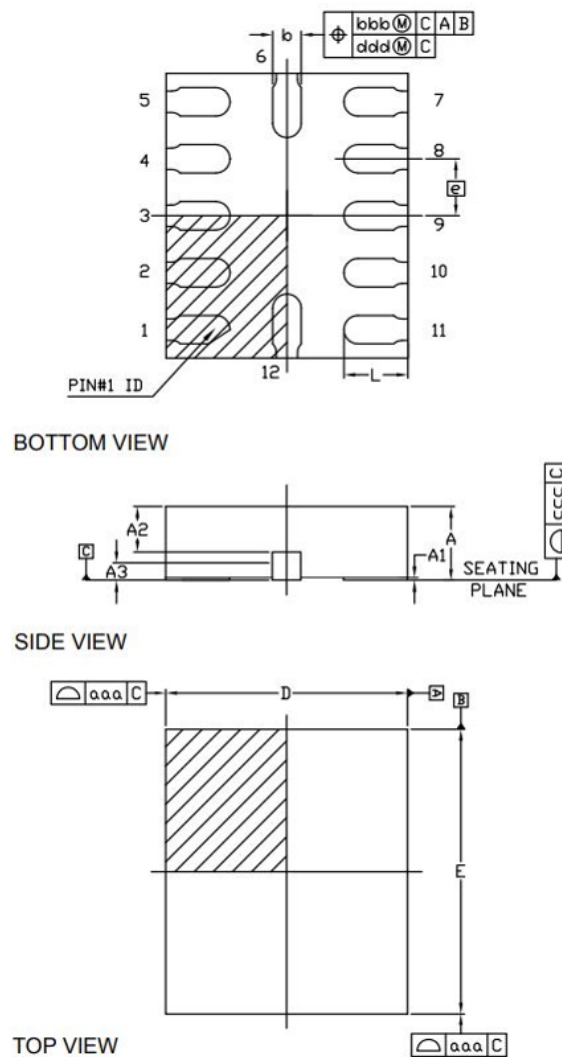
**Figure 24. Disable,  $V_{IN} = 3.6\text{ V}$ ,  $V_{IN\_AUX} = 1.8\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $V_{OUT\_AUX} = 1.8\text{ V}$ , no load**

**Figure 25. Startup,  $V_{IN} = 3.6\text{ V}$ ,  $V_{IN\_AUX} = 1.8\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $V_{OUT\_AUX} = 1.8\text{ V}$ ,  $R_{load} = 18\text{ Ohm}$ ,  $I_{OUT} = 100\text{ mA}$** 

**Figure 26. Disable,  $V_{IN} = 3.6\text{ V}$ ,  $V_{IN\_AUX} = 1.8\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $V_{OUT\_AUX} = 1.8\text{ V}$ ,  $R_{load} = 18\text{ Ohm}$ ,  $I_{OUT} = 100\text{ mA}$** 

**Figure 27. Startup,  $V_{IN} = 3.6\text{ V}$ ,  $V_{IN\_AUX} = 3.3\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $V_{OUT\_AUX} = 3.3\text{ V}$ , no load**

**Figure 28. Disable,  $V_{IN} = 3.6\text{ V}$ ,  $V_{IN\_AUX} = 1.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $V_{OUT\_AUX} = 3.3\text{ V}$ , no load**


## 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 9.1 TQFN12 (2.0x1.7x0.55 mm) package information

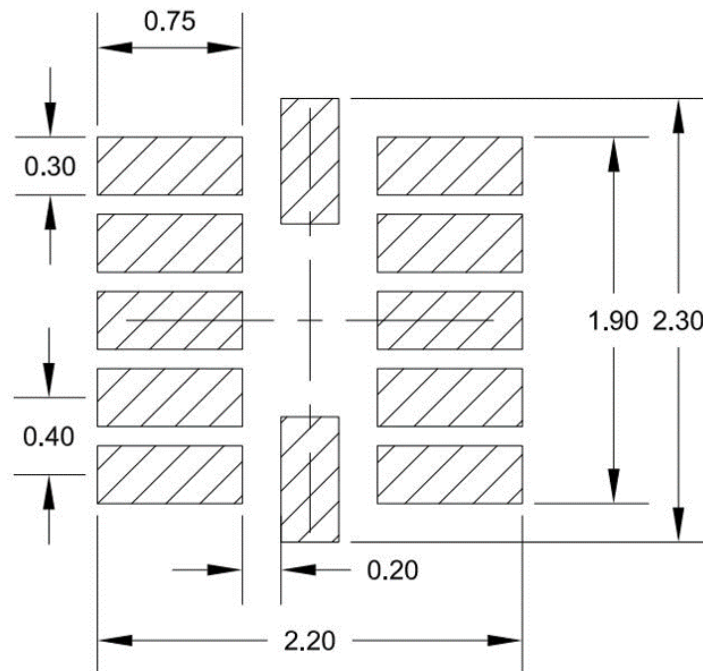
Figure 29. TQFN12 (2.0x1.7x0.55 mm) package outline



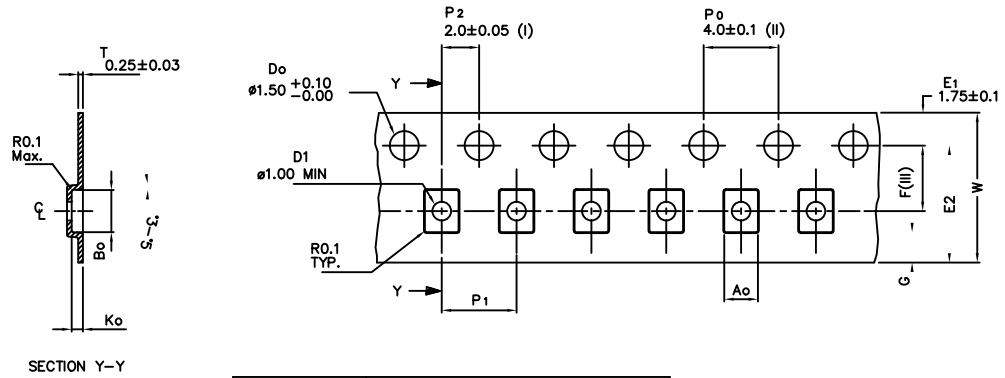


**Table 8. TQFN12 (2.0x1.7x0.55 mm) mechanical data**

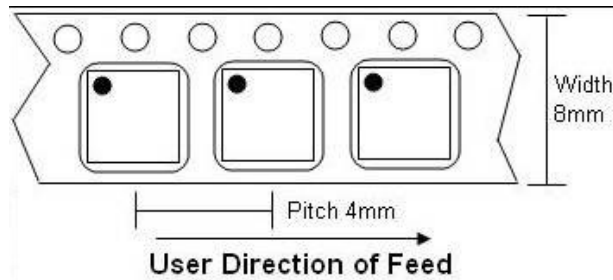
Symbol	Milimeters		
	Min.	Typ.	Max.
A	0.40	0.50	0.55
A1	0.00	0.03	0.05
A2	0.28	0.38	0.48
A3		0.125	
b	0.15	0.20	0.25
D	1.60	1.70	1.80
E	1.90	2.00	2.10
e		0.40	
L	0.35	0.45	0.55
aaa		0.15	
bbb		0.10	
ccc		0.08	
ddd		0.05	
eee		0.10	

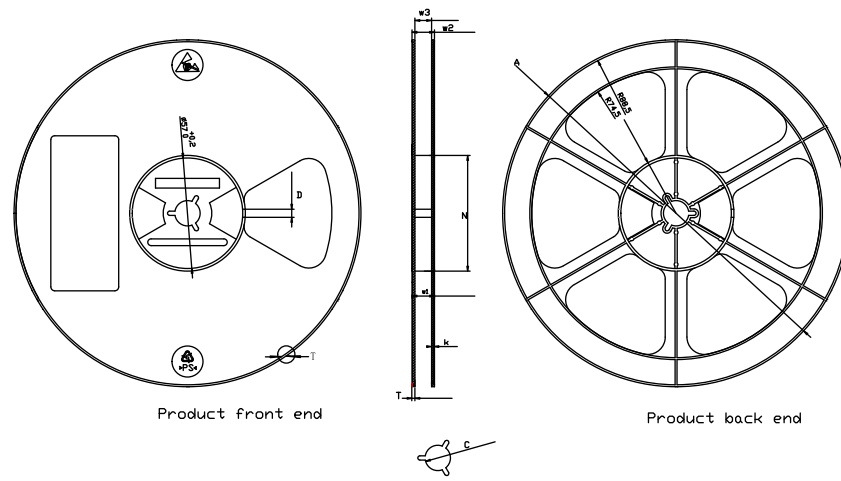
**Figure 30. TQFN12 (2.0x1.7x0.55 mm) recommended footprint**


## 9.2 TQFN12 (2.0x1.70x0.55 mm) packing information

**Figure 31. TQFN12 (2.0x1.70x0.55 mm) carrier tape outline**


Ao	1.80 +/−0.05
Bo	2.25 +/−0.05
Ko	0.60 +/−0.05
F	3.50 +/−0.05
P1	4.00 +/−0.1
D1	1.00 MIN
T	0.25 +/−0.03
G	0.75 MIN.
E2	6.25 MIN.
W	8.00 +0.3/−0.1

**Figure 32. TQFN12 (2.0x1.70x0.55 mm) tape orientation**


**Figure 33. TQFN12 (2.0x1.70x0.55 mm) reel outline**


TYPE	A	N	C	D	w1	w2	w3	T	k
8MM	$\phi 180 \pm 2$	$\phi 60 \pm 1$	$13.1 \pm 0.2$	$4.2 \pm 0.5$	$8.4^{+1}_{-0.2}$	$11.6 \pm 1$	$8.75 \pm 1$	$1.5 \pm 0.15$	$1.25^{+0.1}_{-0.05}$

## 10 Ordering information

**Table 9. Ordering information**

Order codes	Output voltages	Output discharge	Package	Packing
ST1PS03AQTR	1.60 V to 3.3 V	Yes	TQFN12 (2.0x1.7 mm) 400 µm pitch	Tape and reel
ST1PS03A1QTR		No		

## Revision history

**Table 10. Document revision history**

Date	Version	Changes
27-Sep-2021	1	Initial release.

## Contents

<b>1</b>	<b>Application schematic</b> .....	<b>2</b>
<b>2</b>	<b>Pin configuration</b> .....	<b>3</b>
<b>3</b>	<b>Functional pin description</b> .....	<b>4</b>
<b>4</b>	<b>Maximum ratings</b> .....	<b>5</b>
<b>5</b>	<b>Electrical characteristics</b> .....	<b>6</b>
<b>6</b>	<b>ST1PS03 block diagram</b> .....	<b>8</b>
<b>7</b>	<b>Operation description</b> .....	<b>9</b>
7.1	Power save mode .....	9
7.2	Output voltage .....	9
7.3	Output discharge and UVLO .....	9
7.4	Soft-start and current limitation .....	9
7.5	100% duty cycle operation .....	9
7.6	Auxiliary output (VOUT_AUX) .....	9
7.7	Power Good flag .....	10
<b>8</b>	<b>Typical performance characteristics</b> .....	<b>11</b>
<b>9</b>	<b>Package information</b> .....	<b>16</b>
9.1	TQFN12 (2.0x1.7x0.55 mm) package information .....	16
9.2	TQFN12 (2.0x1.70x0.55 mm) packing information .....	18
<b>10</b>	<b>Ordering information</b> .....	<b>20</b>
	<b>Revision history</b> .....	<b>21</b>

## List of tables

<b>Table 1.</b>	Typical external components . . . . .	2
<b>Table 2.</b>	Pin description. . . . .	3
<b>Table 3.</b>	Absolute maximum ratings . . . . .	5
<b>Table 4.</b>	Thermal data. . . . .	5
<b>Table 5.</b>	Recommended operating conditions. . . . .	5
<b>Table 6.</b>	Electrical characteristics . . . . .	6
<b>Table 7.</b>	Output voltage settings . . . . .	7
<b>Table 8.</b>	TQFN12 (2.0x1.7x0.55 mm) mechanical data . . . . .	17
<b>Table 9.</b>	Ordering information. . . . .	20
<b>Table 10.</b>	Document revision history . . . . .	21

## List of figures

<b>Figure 1.</b>	ST1PS03 application schematic . . . . .	2
<b>Figure 2.</b>	TQFN12 package (top through view) . . . . .	3
<b>Figure 3.</b>	Block diagram . . . . .	8
<b>Figure 4.</b>	Efficiency vs. load, $V_{OUT} = 1.8\text{ V}$ . . . . .	11
<b>Figure 5.</b>	Efficiency vs. $V_{IN}$ , $V_{OUT} = 1.8\text{ V}$ . . . . .	11
<b>Figure 6.</b>	Efficiency vs. load, $V_{OUT} = 2.5\text{ V}$ . . . . .	11
<b>Figure 7.</b>	Efficiency vs. $V_{IN}$ , $V_{OUT} = 2.5\text{ V}$ . . . . .	11
<b>Figure 8.</b>	100% mode, $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} 100\text{ mA}$ , $R_{load} = 18\text{ Ohm}$ , $V_{EN} = V_{IN}$ , $AUX = GND$ . . . . .	12
<b>Figure 9.</b>	100% mode, $V_{OUT} = 3.3\text{ V}$ , $I_{OUT} 100\text{ mA}$ , $R_{load} = 33\text{ Ohm}$ , $V_{EN} = V_{IN}$ , $AUX = GND$ . . . . .	12
<b>Figure 10.</b>	$V_{in} = 3.6\text{ V}$ , $V_{out} = 1.8\text{ to }3.3\text{ V}$ , $R_{load} 33\text{ Ohm}$ , $AUX = GND$ , $V_{IN\_AUX} = \text{floating}$ . . . . .	12
<b>Figure 11.</b>	Output ripple, $V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} = 10\text{ }\mu\text{A}$ . . . . .	12
<b>Figure 12.</b>	Output ripple, $V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} = 1\text{ mA}$ . . . . .	12
<b>Figure 13.</b>	Output ripple, $V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} = 50\text{ mA}$ . . . . .	12
<b>Figure 14.</b>	Output ripple, $V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} = 150\text{ mA}$ . . . . .	13
<b>Figure 15.</b>	Output ripple, $V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} = 250\text{ mA}$ . . . . .	13
<b>Figure 16.</b>	Startup, $V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , no load . . . . .	13
<b>Figure 17.</b>	Disable, $V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , no load . . . . .	13
<b>Figure 18.</b>	Startup, $V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $R_{LOAD} = 18\text{ Ohm}$ . . . . .	13
<b>Figure 19.</b>	Disable, $V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $R_{LOAD} = 18\text{ Ohm}$ . . . . .	13
<b>Figure 20.</b>	Load transient, $V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} = 50\text{ }\mu\text{A}$ to $10\text{ mA}$ . . . . .	14
<b>Figure 21.</b>	Load transient, $V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} = 0$ to $100\text{ mA}$ . . . . .	14
<b>Figure 22.</b>	Load transient, $V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $I_{OUT} = 10$ to $100\text{ mA}$ . . . . .	14
<b>Figure 23.</b>	Startup, $V_{IN} = 3.6\text{ V}$ , $V_{IN\_AUX} = 1.8\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $V_{OUT\_AUX} = 1.8\text{ V}$ , no load . . . . .	14
<b>Figure 24.</b>	Disable, $V_{IN} = 3.6\text{ V}$ , $V_{IN\_AUX} = 1.8\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $V_{OUT\_AUX} = 1.8\text{ V}$ , no load . . . . .	15
<b>Figure 25.</b>	Startup, $V_{IN} = 3.6$ , $V_{IN\_AUX} = 1.8\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $V_{OUT\_AUX} = 1.8\text{ V}$ , $R_{load} = 18\text{ Ohm}$ , $I_{OUT} = 100\text{ mA}$ . . . . .	15
<b>Figure 26.</b>	Disable, $V_{IN} = 3.6\text{ V}$ , $V_{IN\_AUX} = 1.8\text{ V}$ , $V_{OUT} = 1.8\text{ V}$ , $V_{OUT\_AUX} = 1.8\text{ V}$ , $R_{load} = 18\text{ Ohm}$ , $I_{OUT} = 100\text{ mA}$ . . . . .	15
<b>Figure 27.</b>	Startup, $V_{IN} = 3.6\text{ V}$ , $V_{IN\_AUX} = 3.3\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , $V_{OUT\_AUX} = 3.3\text{ V}$ , no load . . . . .	15
<b>Figure 28.</b>	Disable, $V_{IN} = 3.6\text{ V}$ , $V_{IN\_AUX} = 1.8\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , $V_{OUT\_AUX} = 3.3\text{ V}$ , no load . . . . .	15
<b>Figure 29.</b>	TQFN12 (2.0x1.7x0.55 mm) package outline . . . . .	16
<b>Figure 30.</b>	TQFN12 (2.0x1.7x0.55 mm) recommended footprint . . . . .	17
<b>Figure 31.</b>	TQFN12 (2.0x1.70x0.55 mm) carrier tape outline . . . . .	18
<b>Figure 32.</b>	TQFN12 (2.0x1.70x0.55 mm) tape orientation . . . . .	18
<b>Figure 33.</b>	TQFN12 (2.0x1.70x0.55 mm) reel outline . . . . .	19



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