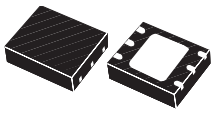
ST1S03A

1.5 A, 1.5 MHz adjustable, with inhibit function step-down switching regulator

Features

- Step-down current mode PWM (1.5 MHz) DC-DC converter
- 2 % DC output voltage tolerance
- Internal soft start for start-up current limitation and power on delay of 50-100 µs
- Typical efficiency: > 85 %
- Inhibit function
- 1.5 A output current capability
- Not switching quiescent current: max 1.5 mA over temperature range
- Switch V_{DS}: max 200 mV @ I_{SW} = 750 mA
- Uses tiny capacitors and inductors
- Available in DFN6D 3x3 exposed pad



DFN6D (3x3 mm)

Description

The ST1S03A is a step down DC-DC converter optimized for powering low-voltage digital core in HDD applications and, generally, to replace the high current linear solution when the power dissipation may cause an high heating of the application environment. It provides up to 1.5 A over an input voltage range of 3 V to 5.5 V. An high switching frequency (1.5 MHz) allows the use of tiny surface-mount components: as well as the resistor divider to set the output voltage value, only an inductor, a schottky diode and two capacitors are required. Besides, a low output ripple is guaranteed by the current mode PWM topology and by the use of low ESR SMD ceramic capacitors. The device is thermal protected and current limited to prevent damages due to accidental short circuit. The ST1S03A is available in DFN6D (3x3 mm).

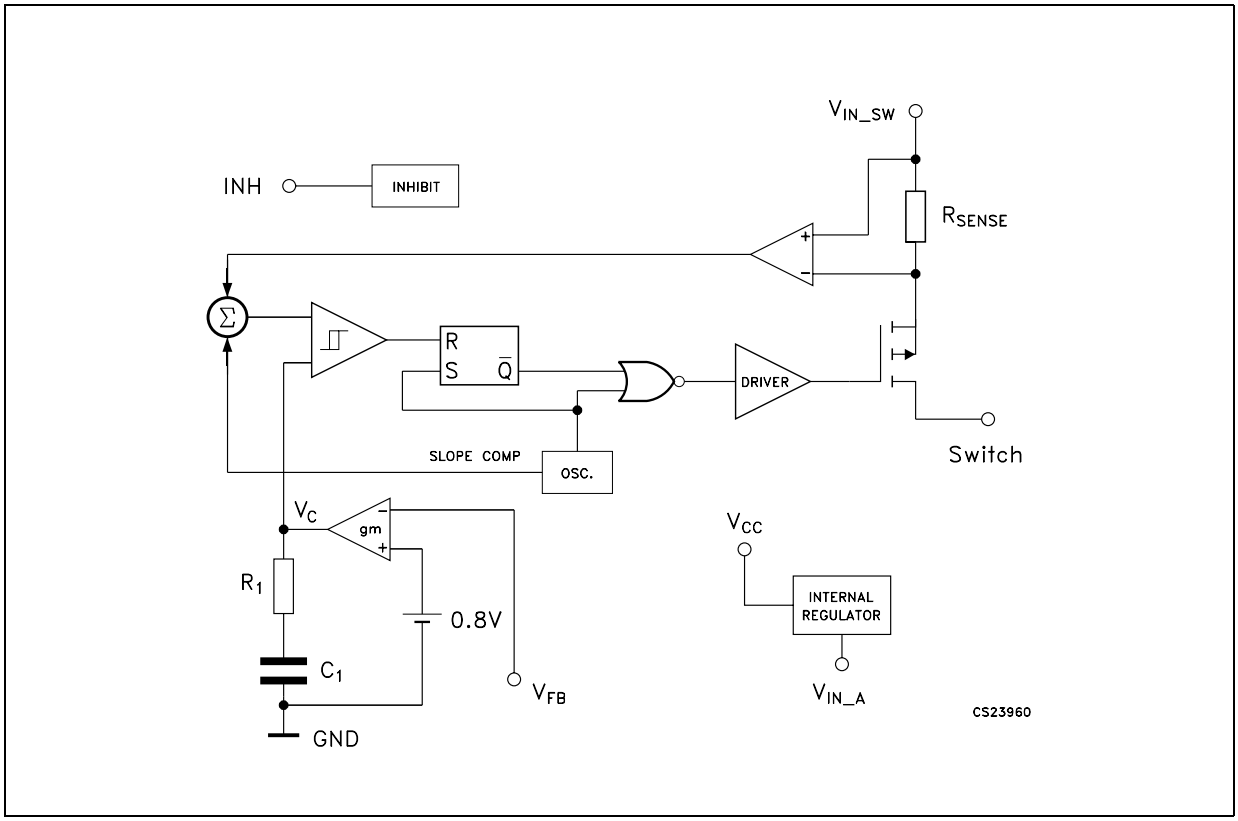
Table 1. Device summary

Order codes	Packaging	Package
ST1S03APUR	Tape and reel	DFN6D (3x3 mm)
ST1S03AIPUR	Tape and reel	DFN6D (3x3 mm)

Contents

1 Diagram

Figure 1. Schematic diagram



2 Pin configuration

Figure 2. Pin configuration (top view)

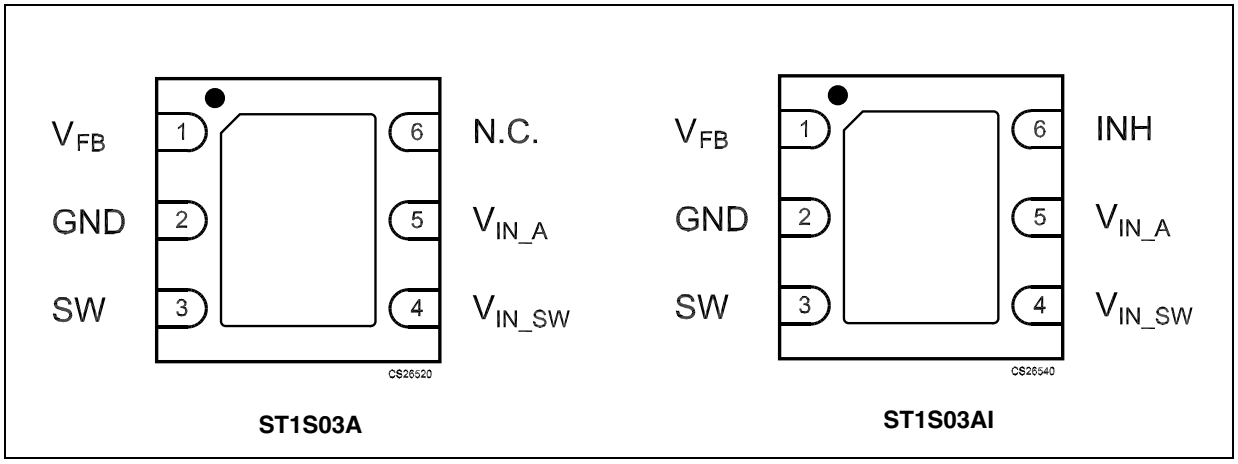


Table 2. Pin description

Pin n°	Symbol	Name and function
1	V_{FB}	Voltage of feedback
2	GND	System ground
3	SW	Output of the internal power switch
4	V_{IN_SW}	Power supply for the mosfet switch
5	V_{IN_A}	Power supply for the analog circuit
6	N.C./INH	Not connected / or inhibit

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN_SW}	Positive power supply voltage	-0.3 to 7	V
V_{IN_A}	Positive power supply voltage	-0.3 to 7	V
V_{INH}	Max voltage of inhibit pin	-0.3 to 6	V
SWITCH Voltage	Max voltage of output pin	-0.3 to 7	V
V_{FB}	Feedback voltage	2.5	V
I_{VFB}	Common mode input voltage	1	mA
T_J	Max junction temperature	150	°C
T_{STG}	Storage temperature range	-25 to 150	°C
T_{LEAD}	Lead temperature (soldering) 10 sec	300	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	55	°C/W
R_{thJC}	Thermal resistance junction-case	10	°C/W

4 Electrical characteristics

Table 5. Electrical characteristics

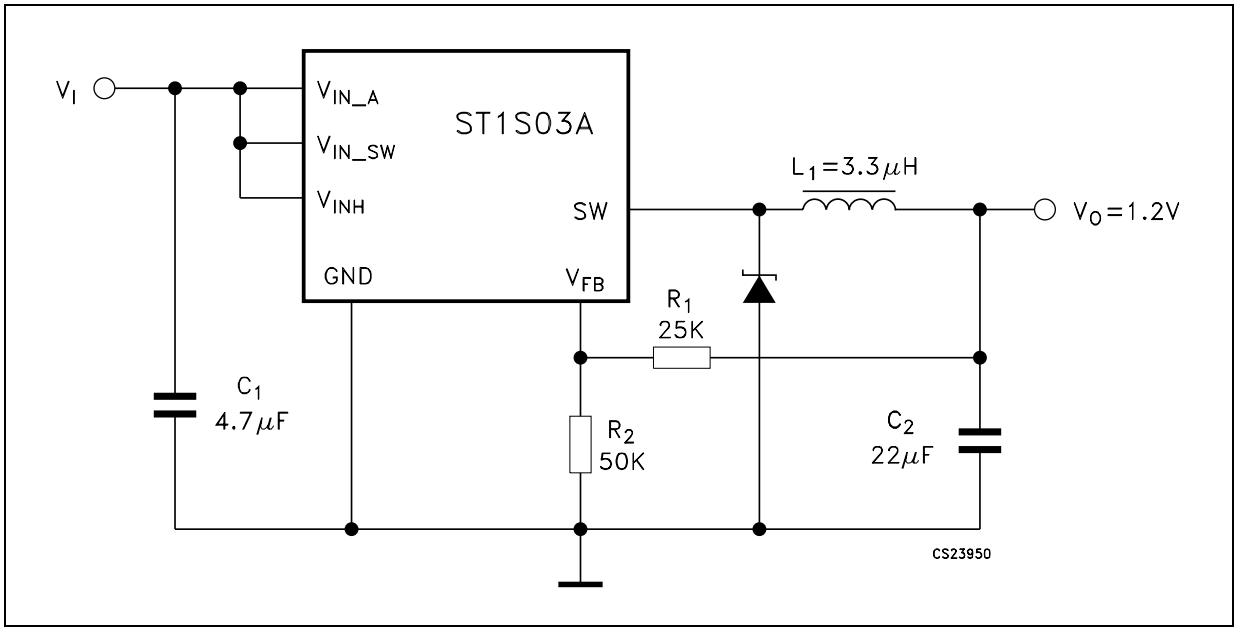
(V_{IN_SW} = V_{IN_A} = V_{INH} = 5 V, C_I = 4.7 µF, C_O = 22 µF, L1 = 3.3 µH, T_J = 0 to 125 °C (unless otherwise specified. Typical values are referred to 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
FB	Feedback voltage		784	800	816	mV
I_{FB}	V_{FB} pin bias current				600	nA
I_Q	Quiescent current	V_{INH} > 1.2V			1.5	mA
		V_{INH} < 0.4V			1	µA
V_{INH}	Inhibit threshold	Device ON	1.2			V
		Device OFF			0.4	
I_O	Output current	V_I = 2.7 to 5.5V	1.5			A
I_{MIN}	Minimum output current		1			mA
$\%V_O/\Delta V_I$	Reference line regulation	V_I = 2.7V to 5.5V		0.2		$\%V_O/\Delta V_I$
$\%V_O/\Delta I_O$	Reference load regulation	I_O = 10mA to 1.5A		0.2		$\%V_O/\Delta I_O$
$PWMf_S$	PWM switching frequency	V_{FB} = 0.7V, T_A = 25°C *Note 1*	1.2	1.5	1.8	MHz
D_{MAX}	Maximum duty cycle	V_{FB} = 0.7V		87		%
I_{SW}	Switching current limitation		2.5			A
V_{DS}	Switch V_{DS}	I_{SW} = 800mA			200	mV
ν	Efficiency	I_O = 10mA to 100mA, V_O = 3.3V	70			%
		I_O = 100mA to 1.5A, V_O = 3.3V	85			
T_{SHDN}	Thermal shutdown	*Note 1*	130	150		°C
T_{HYS}	Thermal shutdown hysteresis	*Note 1*		15		°C
$\%V_O/\Delta I_O$	Load transient response	I_O = 100mA to 1.5A, T_A = 25°C $t_R = t_F \geq$ 100ns, *Note 1*	-3		+3	$\%V_O$
$\%V_O/\Delta I_O$ @ I_O=Short	Short circuit removal response	I_O = 10mA to short, T_A = 25°C *Note 1*	-10		+10	$\%V_O$

Note: 1 Guaranteed by design, but not tested in production

5 Typical application

Figure 3. Application circuits



6 Application notes

The ST1S03A is an adjustable current mode PWM step-down DC-DC converter with internal 1.5 A power switch, packaged in a 6-lead DFN 3x3 mm.

It's a complete 1.5 A switching regulator with its internal compensation eliminating additional component.

The constant frequency, current mode, PWM architecture and stable operation with ceramic capacitors results in low, predictable output ripple. However, in order to maximize the power conversion efficiency with light load, the regulator reduces automatically the switching frequency when the output load becomes less than 250 mA typically.

To clamp the error amplifier reference voltage a soft start control block generating a voltage ramp, has been implemented. Besides an on-chip power on reset of 50 = 100 µs ensure the proper operation when switching on the power supply. other circuits fitted to the device protection are the thermal shutdown block which turn off the regulator when the junction temperature exceeds 150 °C typically and the cycle-by-cycle current limiting that provides protection against shorted outputs.

Being the ST1S03A an adjustable regulator, the output voltage is determined by an external resistor divider. The desired value is given by the following equation:

$V_O = V_{FB} [1 + R1 / R2]$

To make the device working, only other four external components are required: an inductor a schottky and two capacitors. The chosen inductor must be able to not saturate at the peak current level. Besides, its value can be selected keeping in account that a large inductor value increases the efficiency at low output current and reduces output voltage ripple, while a smaller inductor can be chosen when it is important to reduce the package size and the total cost of the application. Finally, the ST1S03A has been designed to work properly with X5R or X7R SMD ceramic capacitors both at the input and at the output this kind of capacitors, thanks to their very low series resistance (ESR), minimize the output voltage ripple. Other low ESR capacitors can be used according to the need of the application without invalidate the right functioning of the device.

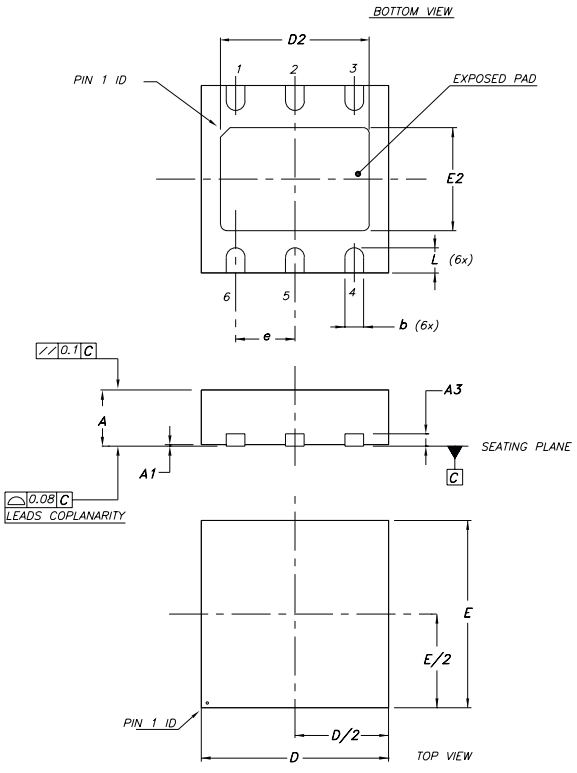
Due to the high switching frequency and peak current, it is important to optimize the application environment reducing the length of the PCB traces and placing all the external component near the device.

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

DFN6D (3x3 mm) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.00	0.031		0.039
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.23		0.45	0.009		0.018
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.23		2.50	0.088		0.098
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50		1.75	0.059		0.069
e		0.95			0.037	
L	0.30	0.40	0.50	0.012	0.016	0.020



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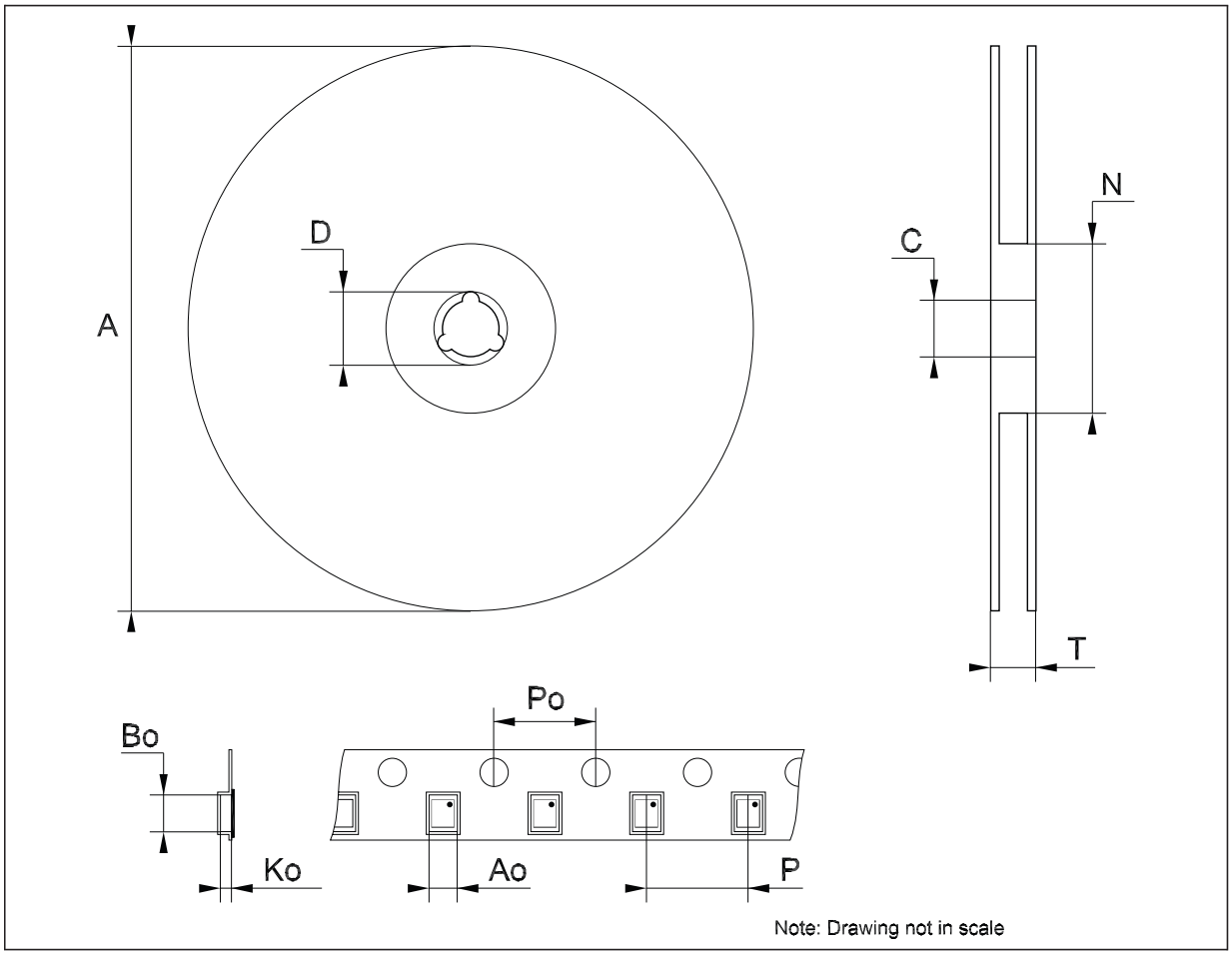
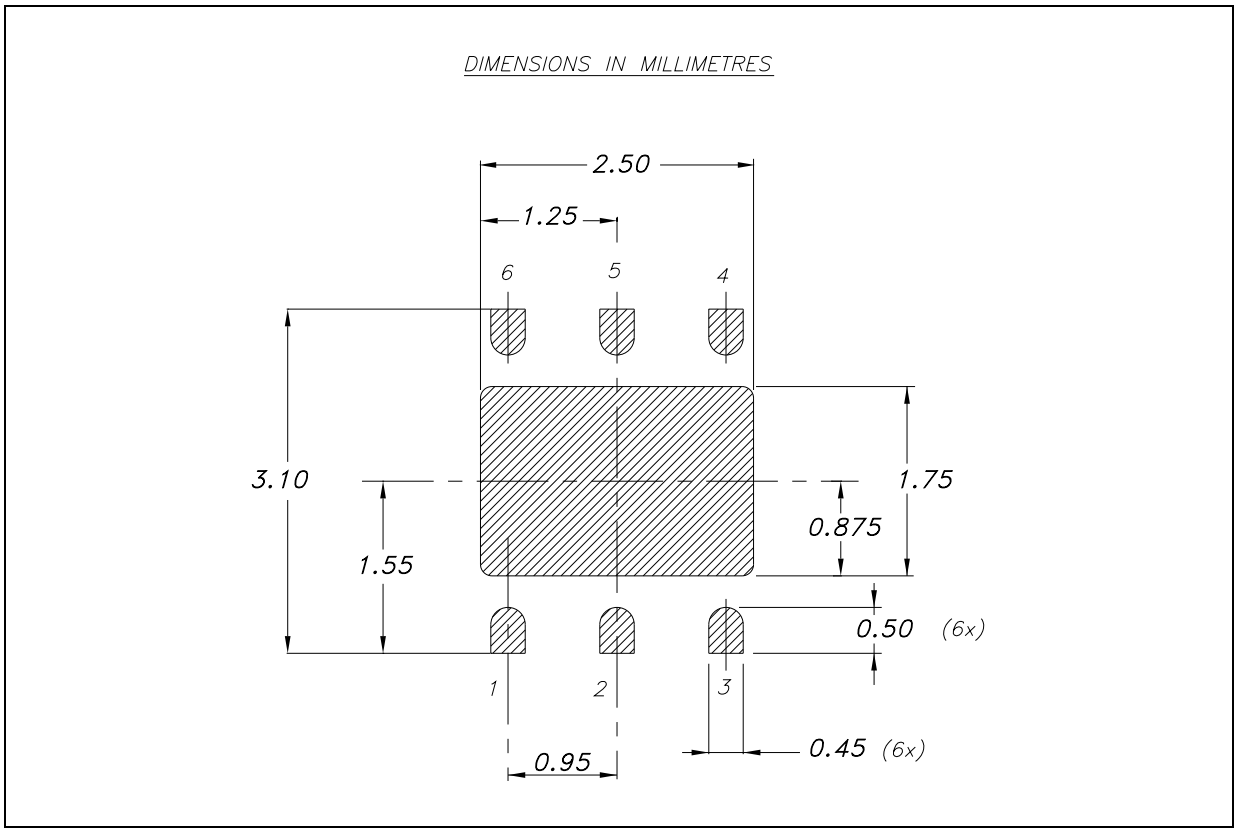
Tape & Reel QFNxx/DFNxx (3x3) Mechanical Data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Note: Drawing not in scale

Figure 4. DFN6 (3x3 mm) footprint recommended data



8 Revision history

Table 6. Document revision history

Date	Revision	Changes
04-May-2006	1	First release.
06-Jun-2006	2	*Table 3* has been updated.
29-May-2007	3	Add new mechanical data DFN6D and order codes updated.
12-Mar-2008	4	Added: *Table 1 on page 1* and *Figure 4 on page 12*.
16-May-2008	5	Modified: *Table 4 on page 5*.
03-Jun-2008	6	Modified: *Table 5 on page 6*.

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