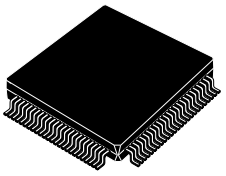
ST7590

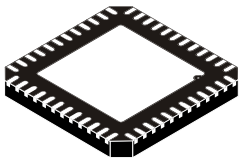
Narrow-band OFDM power line networking PRIME compliant system-on-chip

Features

- Fully integrated narrow-band power line networking system-on-chip
- High performing DSP engine with embedded turn-key firmware for Orthogonal frequency division multiplexing (OFDM) modulation, featuring:
  - 96 sub-carriers in CENELEC A band
  - BDPSK, QDPSK, 8DPSK programmable modulations
  - Programmable bit rate up to 128 kbps
  - Convolutional coding and Viterbi decoding
  - Signal to noise ratio and channel quality estimation
  - Full PRIME compliant PHY
- On chip peripherals:
  - Host controller UART/SPI interface
  - I2C/SPI external data memory interface
  - High speed SRAM controller for optional external SRAM program code execution
  - Watchdog timer
- On chip 128 bit AES encryption HW block
- Fully integrated analog front end:
  - ADC and DAC
  - High sensitivity receiver
  - High linearity transmitter with intelligent gain control
- Fully integrated power line driver
  - Up to 1 Arms, 14 Vpp single ended
  - Configurable active filtering topology
  - Ultra low distortion
  - Embedded temperature sensor
  - Current control
- 3.3 V or 5 V I/O digital I/O supply
- Integrated 5 V and 1.8 V linear regulators for AFE and digital core supply
- 8 V to 18 V line driver power supply



TQFP 100



QFN-48
(7 x 7 mm)

- Suitable for applications compliant with EN50065 and FCC part 15 specifications
- -40 °C to +85 °C temperature range
- QFN48 7x7 (ST7590) and TQFP 100 14x14 (ST7590T) exposed pad package options

Application

PRIME compliant smart metering and smart grid applications.

Description

ST7590 is the first complete Narrowband OFDM power line communication system-on-chip made using a multi-power technology with state of the art VLSI CMOS lithography. The ST7590 is based on dual core architecture to assure outstanding communication performance with a very high level of flexibility and programmability for either open standard or fully customized implementations.

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1 Device description

ST7590 is available in two different package options: TQFP100 and QFN48.

In the TQFP100 package option, order code ST7590T, the device comes with a dedicated FW implementing PRIME compliant PHY protocol Layer and a boot loader procedure that enables the IC to boot PRIME MAC, PRIME CL432 Convergence Layer and IEC 61334-4-32 LLC Layer from an external Serial NV memory connected through SPI interface.

In the QFN 48 package option, ST7590 comes with a dedicated FW implementing the full PRIME protocol stack (PHY, MAC and Convergence Layer), so without the need for external memories to run the protocol.

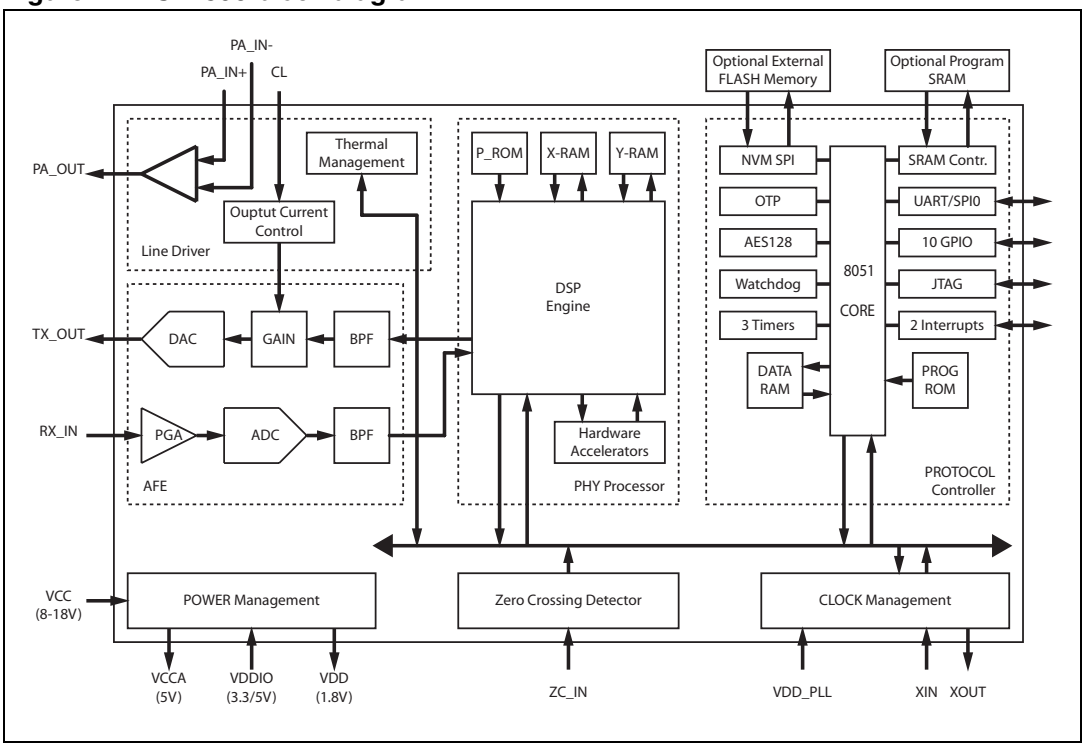
The on-chip analog front end, featuring analog to digital and digital to analog conversion and automatic gain control, plus the integrated power amplifier delivering up to 1 Arms (typical) output current, makes the ST7590 the first complete Narrowband OFDM power line communication system-on-chip ideal for PRIME compliant applications.

An HW 128-bit AES encryption block with PRIME compliant management is available on chip when secure communication is requested.

Line coupling network design is also extremely simplified, leading to a very low cost Bill Of Material.

Safe operations are assured while keeping power consumption and distortion levels very low, so making ST7590 an ideal platform for the most stringent application requirements and regulatory standards compliance.

Figure 1. ST7590 block diagram



2 Pin connection

Figure 2. TQFP100 pin connection

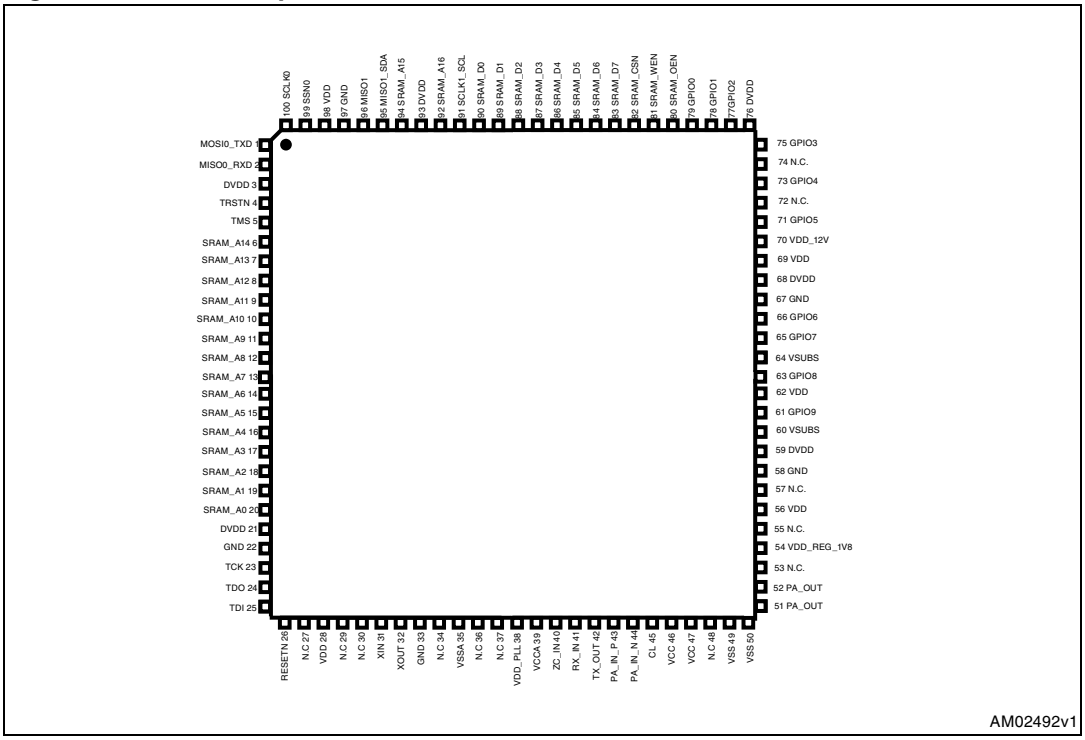


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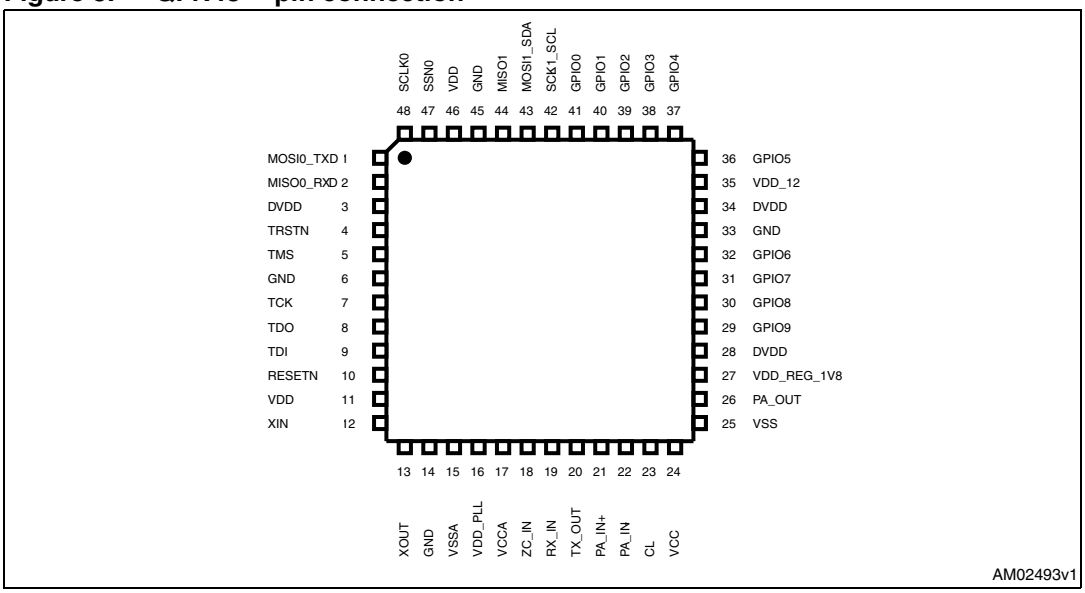
Figure 3. QFN48[(a)] pin connection



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a. The QFN48 package option does not allow the connection with an external memory; in this configuration the ST7590 will run the code present in the embedded ROM only.

Table 1. Pin description

Name	Pin		Type	Description
	TQFP	QFN		
SCLK0	100	48	Digital input	SPI0 serial clock
SSN0	99	47	Digital input	SPII0 slave select (active low)
VDD	98	46	Power	Digital power supply (1.8 V)
GND	97	45	Power	Ground
MISO1	96	44	Digital input	SPI1 data in
MOSI1_SDA	95	43	Digital I/O	SPI1 data out, I2C data in (I2C always selected at boot)
SRAM_A15	94	-	Digital output	External SRAM Address
VDDIO	93	-	Power	3.3 V - 5 V I/O supply
SRAM_A16	92	-	Digital output	External SRAM Address
SCLK1_SCL	91	42	Digital output	SPI1 serial clock, I2C serial clock ((I2C always selected at boot)
SRAM_D0	90	-	Digital I/O (1)	External SRAM data I/O
SRAM_D1	89	-	Digital I/O (1)	External SRAM data I/O
SRAM_D2	88	-	Digital I/O (1)	External SRAM data I/O
SRAM_D3	87	-	Digital I/O (1)	External SRAM data I/O
SRAM_D4	86	-	Digital I/O (1)	External SRAM data I/O
SRAM_D5	85	-	Digital I/O (1)	External SRAM data I/O
SRAM_D6	84	-	Digital I/O (1)	External SRAM data I/O
SRAM_D7	83	-	Digital I/O (1)	External SRAM data I/O
SRAM_CSN	82	-	Digital output	External SRAM chip select
SRAM_WEN	81	-	Digital output	External SRAM write enable
SRAM_OEN	80	-	Digital output	External SRAM output enable
GPIO0	79	41	Digital I/O	General purpose I/O
GPIO1	78	40	Digital I/O	General purpose I/O
GPIO2	77	39	Digital I/O	General purpose I/O
VDDIO	76	-	Power	3.3 V - 5 V I/O supply
GPIO3	75	38	Digital I/O	General purpose I/O
N.C	74	-		Not connected
GPIO4	73	37	Digital I/O	General purpose I/O
N.C	72	-		Not connected
GPIO5	71	36	Digital I/O	General purpose I/O
VDD_12V	70	35	Power	OTP programming voltage (12 V)
VDD	69	-	Power	Digital power supply (1.8 V)
VDDIO	68	34	Power	3.3 V - 5 V I/O supply
GND	67	33	Power	Ground

Table 1. Pin description (continued)

Name	Pin		Type	Description
	TQFP	QFN		
GPIO6	66	32	Digital I/O	General purpose I/O
GPIO7	65	31	Digital I/O	General purpose I/O
VSUBS	64	-	Power	Analog ground
GPIO8	63	30	Digital I/O	General purpose I/O
VDD	62	-	Power	Digital power supply (1.8 V)
GPIO9	61	29	Digital I/O	General purpose I/O
VSUBS	60	-	Power	Substrate ground
VDDIO	59	28	Power	3.3 V - 5 V I/O supply
GND	58	-	Power	Ground
N.C	57	-		Not connected
VDD	56	-	Power	Digital power supply (1.8 V)
N.C	55	-		Not connected
VDD_REG_1V8	54	27	Power	1.8 V digital power supply, internal regulator output
N.C	53	-		Not connected
PA_OUT	52	26	Analog output	Power amplifier output
PA_OUT	51	-	Analog output	Power amplifier output
VSS	50	25	Power	Power ground
VSS	49	-	Power	Power ground
N.C	48	-		Not connected
VCC	47	24	Power	12 V to 20 V power supply
VCC	46	-	Power	12 V to 20 V power supply
CL	45	23	Analog Input	Current limiting feedback
PA_IN_N	44	22	Analog Input	Power amplifier inverting input
PA_IN_P	43	21	Analog Input	Power amplifier non-inverting input
TX_OUT	42	20	Analog Output	Transmission analog output
RX_IN	41	19	Analog Input	Reception analog input
ZC_IN	40	18	Analog Input	Zero crossing detection input
VCCA	39	17	Power	5 V analog supply, internal regulator output
VDD_PLL	38	16	Power	1.8 V PLL supply voltage
N.C	37	-		Not connected
N.C	36	-		Not connected
VSSA	35	15	Power	Analog ground
N.C	34	-		Not connected
GND	33	14	Power	Ground

Table 1. Pin description (continued)

Name	Pin		Type	Description
	TQFP	QFN		
XOUT	32	13	Analog	Crystal oscillator output
XIN	31	12	Analog	Crystal oscillator input
N.C	30	-		Not connected
N.C	29	-		Not connected
VDD	28	11	Power	Digital power supply (1.8 V)
N.C	27	-		Not connected
RESETN	26	10	Digital input	System reset (active low)
TDI	25	9	Digital input (1)	System/M851EW JTAG interface data in
TDO	24	8	Digital I/O	System/M851EW JTAG interface data out
TCK	23	7	Digital input	System/M851EW JTAG interface clock
GND	22	6	Power	Ground
VDDIO	21	-	Power	3.3 V - 5 V I/O supply
SRAM_A0	20	-	Digital output	External SRAM address
SRAM_A1	19	-	Digital output	External SRAM address
SRAM_A2	18	-	Digital output	External SRAM address
SRAM_A3	17	-	Digital output	External SRAM address
SRAM_A4	16	-	Digital output	External SRAM address
SRAM_A5	15	-	Digital output	External SRAM address
SRAM_A6	14	-	Digital output	External SRAM address
SRAM_A7	13	-	Digital output	External SRAM address
SRAM_A8	12	-	Digital output	External SRAM address
SRAM_A9	11	-	Digital output	External SRAM address
SRAM_A10	10	-	Digital output	External SRAM address
SRAM_A11	9	-	Digital output	External SRAM address
SRAM_A12	8	-	Digital output	External SRAM address
SRAM_A13	7	-	Digital output	External SRAM address
SRAM_A14	6	-	Digital output	External SRAM address
TMS	5	5	Digital input (1)	System/M8051EW JTAG interface test mode selection
TRSTN	4	4	Digital input (1)	System/M8051EW JTAG interface reset (active low)
VDDIO	3	3	Power	3.3 V - 5 V I/O supply
MISO0_RXD	2	2	Digital I/O	UART data in, SPI0 data out
MOSI0_TXD	1	1	Digital I/O	UART data out, SPI0 data in

1. Active Pull up (only in input mode for bi-directional pins)

3 Maximum ratings

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
VCC	Power supply voltage	-0.3	20	V
VSSA-GND	Voltage between VSSA and GND	-0.3	0.3	V
VDDIO	I/O supply voltage	-0.3	5.5	V
VI	Digital input voltage	GND-0.3	VDDIO+0.3	V
VO	Digital output voltage	GND-0.3	VDDIO+0.3	V
V(PA_IN)	PA inputs voltage range	VSS-0.3	VCC+0.3	V
V(PA_OUT)	PA_OUT voltage range	VSS-0.3	VCC+0.3	V
V(RX_IN)	RX_IN voltage range	-(VCCA+0.3)	VCC+0.3	V
V(ZC_IN)	ZC_IN voltage range	-(VCCA+0.3)	VCCA+0.3	V
V(TX_OUT, CL)	TX_OUT, CL voltage range	VSSA-0.3	VCCA+0.3	V
V(XIN)	XIN voltage range	GND-0.3	VDDIO+0.3	V
I(PA_OUT)	Power amplifier output non-repetitive peak current		5	Apeak
I(PA_OUT)	Power amplifier output non-repetitive rms current		1.4	Arms
T_{amb}	Operating ambient temperature	-40	85	ºC
T_{stg}	Storage temperature	-50	150	ºC
V(ESD)	Maximum withstanding voltage range test condition: cdf-aec-q100-002 “human body model” acceptance criteria: “normal performance”	-2	+2	kV

3.2 Thermal data

Table 3. Thermal characteristics (1)

Symbol	Parameter	QFN48	TQFP100	Unit
R_{thJA1}	Maximum thermal resistance junction-ambient steady state(2)	58	50	°C/W
R_{thJA2}	Maximum thermal resistance junction-ambient steady state(3)	32	25	°C/W

1. Typical values.
2. Mounted on a 2s PCB.
3. Mounted on a 2s2p PCB, with a dissipating surface, connected through vias, on the bottom side of the PCB.

3.3 Electrical characteristics

T_A = -40 to +85 °C, T_J < 125 °C, V_{CC} = 18 V unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.
Power supply			
V_{CC}	Power supply voltage		8
$I_{(VCC)\ RX}$	Power supply current - Rx mode	VCCA externally supplied	
$I_{(VCC)\ TX}$	Power supply current - Tx mode, no load		
$V_{CC\ UVLO\_TL}$	V_{CC} under voltage lock out low threshold		6.1
$V_{CC\ UVLO\_TH}$	V_{CC} under voltage lock out high threshold		6.8
$V_{CC\ UVLO\_HYST}$	V_{CC} under voltage lock out hysteresis		250 (1)
V_{CCA}	Analog supply voltage	Externally supplied	-5%
$I_{(VCCA)\ RX}$	Analog supply current - Rx mode		
$I_{(VCCA)\ TX}$	Analog supply current - Tx mode	$V_{(TX\_OUT)}$ =5 V p-p, No load	
V_{DD}	Digital core supply voltage	Externally supplied	-10%
$I_{(VDD)}$	Digital core supply current		
$I_{(VDD)}$	Digital core supply current in RESET state		
V_{DD_PLL}	PLL supply voltage		
$I_{(VDD\_PLL)}$	PLL supply current		
V_{DDIO}	Digital I/O supply voltage	Externally supplied	-10%
$V_{DDIO\ UVLO\_TL}$	I/O supply voltage under voltage lock out low threshold		2.25
$V_{DDIO\ UVLO\_TH}$	I/O supply voltage under voltage lock out high threshold		2.45
$V_{DDIO\ UVLO\_HYST}$	I/O supply voltage under voltage lock out hysteresis		

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.
		Analog front end	
Power amplifier			
$V_{(PA\_OUT)BIAS}$	Power amplifier output bias voltage - Rx mode		
GBWP	Power amplifier gain-bandwidth product		100
$I_{(PA\_OUT)MAX}$	Power amplifier maximum output current		
$V_{(PA\_OUT)\ TOL}$	Power amplifier output tolerance (2)		-3%
$V_{(PA\_OUT)\ HD2}$	Transmitter output 2nd harmonic distortion	V_{CC}=13 V, $V_{(PA\_OUT)}$ = 7 V p-p, $V_{(PA\_OUT)\ BIAS}$ = VCC/2, R_{LOAD}=50 Ω see *Figure 4*	
$V_{(PA\_OUT)\ HD3}$	Transmitter output 3rd harmonic distortion		
$V_{(PA\_OUT)\ THD}$	Transmitter output total harmonic distortion		
$V_{(PA\_OUT)\ HD2}$	Transmitter output 2nd harmonic distortion	V_{CC}=18 V, $V_{(PA\_OUT)}$ = 14 V p-p, $V_{(PA\_OUT)\ BIAS}$ = VCC/2, R_{LOAD}=50 Ω see *Figure 4*	
$V_{(PA\_OUT)\ HD3}$	Transmitter output 3rd harmonic distortion		
$V_{(PA\_OUT)\ THD}$	Transmitter output total harmonic distortion		
$C_{(PA\_IN)}$	Power amplifier input capacitance	PA_IN+ vs. V_{SS} (2)	
		PA_IN- vs. V_{SS} (2)	
PSRR	Power supply rejection ratio	dc to 3 kHz	
		1 kHz	
		100 kHz	
C_{L_TH}	Current sense high threshold on CL pin		
C_{L_RATIO}	Ratio between PA_OUT and CL output current		
Transmitter			
$V_{(TX\_OUT)\ BIAS}$	Transmitter output bias voltage - Rx mode		
$V_{(TX\_OUT)\ MAX}$	Transmitter output maximum voltage swing	Maximum output level, no load V_{CCA} = 5 V	4.8
TXGAIN	Transmitter output digital gain range		-21
TX_GAIN TOL	Transmitter output digital gain tolerance		-0.35

Table 4. Electrical characteristics (continued)

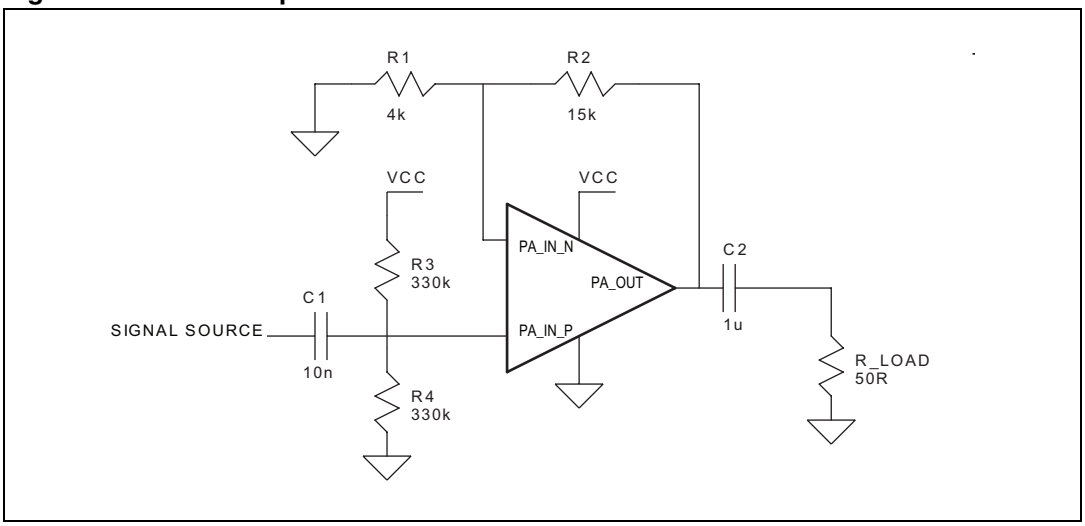
Symbol	Parameter	Test conditions	Min.
$R_{(TX\_OUT)}$	Transmitter output resistance	RX mode	
$V_{(TX\_OUT)\ HD2}$	Transmitter output 2nd harmonic distortion	$V_{(TX\_OUT)}$ = 4 Vpp (TXOUT)MAX, No load, f_C = 82 kHz	
$V_{(TX\_OUT)\ HD3}$	Transmitter output 3rd harmonic distortion		
$V_{(TX\_OUT)\ THD}$	Transmitter output total harmonic distortion		
Receiver			
$V_{(RX\_IN)\ MAX}$	Receiver input maximum voltage	V_{CC} = 18 V	
$V_{(RX\_IN)\ BIAS}$	Receiver input bias voltage		
$Z_{(RX\_IN)}$	Receiver input impedance		
PGA_MIN	PGA minimum gain		
PGA_MAX	PGA maximum gain		
Oscillator			
$V_{(XIN)}$	Oscillator input voltage swing	Clock frequency supplied externally	
$V_{(XIN)\ TH}$	Oscillator input voltage threshold		0.8
$V_{(XIN)}$ f_{OSC}	Crystal oscillator frequency		
F(XIN) TOL	External quartz crystal frequency tolerance		-150
ESR	External quartz crystal ESR value		
C_L	External quartz crystal load capacitance		
Temperature sensor			
T_TH_1	Temperature threshold 1	(2)	63
T_TH_2	Temperature threshold 2	(2)	90
T_TH_3	Temperature threshold 3	(2)	112
T_TH_4	Temperature threshold 4	(2)	153
Zero crossing comparator			
$V_{(ZC\_IN)\ MAX}$	Zero crossing detection input voltage range		

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.
$V_{(ZC\_IN)\ TL}$	Zero crossing detection input low threshold		-44
$V_{(ZC\_IN)\ TH}$	Zero crossing detection input high threshold		26
$V_{(ZC\_IN)\ HYST}$	Zero crossing detection input hysteresis		
Digital section			
Digital I/O			
$R_{PULL-UP}$	Internal pull-up resistors	VDDIO = 3.3 V	
		VDDIO = 5 V	
V_{IH}	High logic level input voltage		0.65*VDDIO
V_{IL}	Low logic level input voltage		-0.3
V_{OH}	High logic level output Voltage	I_{OH}= -4 mA	VDDIO-0.4
V_{OL}	Low logic level output voltage	I_{OL}= 4 mA	
UART interface			
Data bits			
Stop bits			
Parity bits			
Baud rate			-1.5%
			-1.5%
			-1.5%
			-1.5%
Reset and power on			
t_{RESETN}	Minimum valid reset pulse duration		
$t_{STARTUP}$	Start-up time at power on or after a reset event	(3)	

1. Referred to T_A = -40°C
2. This parameter does not include the tolerance of external components
3. Referred to IC start up, uploading code from external NVM and its execution from external RAM may require some second.

Figure 4. Power amplifier test circuit

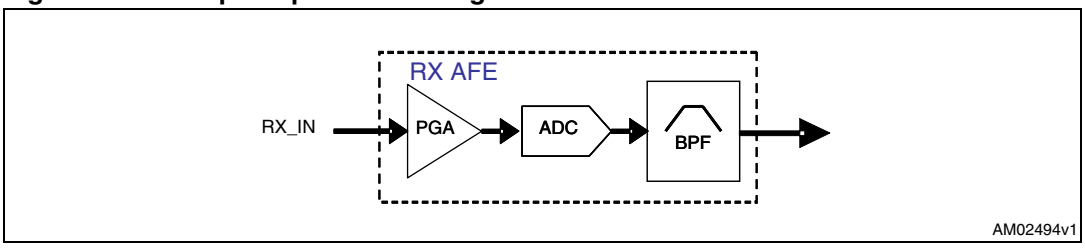


4 Analog front end (AFE)

4.1 Reception path

Figure 5 shows the block diagram of the ST7590 input receiving path. The reception AFE main blocks are a wide input range analog PGA (programmable gain amplifier) and the ADC (analog to digital converter).

Figure 5. Reception path block diagram



The PGA is controlled by a loop algorithm that detects the amplifier output signal amplitude and adapts the gain of the amplifier in order to have the optimum input voltage range for the ADC. The PGA gain ranges from -18 dB up to 30 dB (typical), with steps of 6 dB (typical), as described in Table 5.

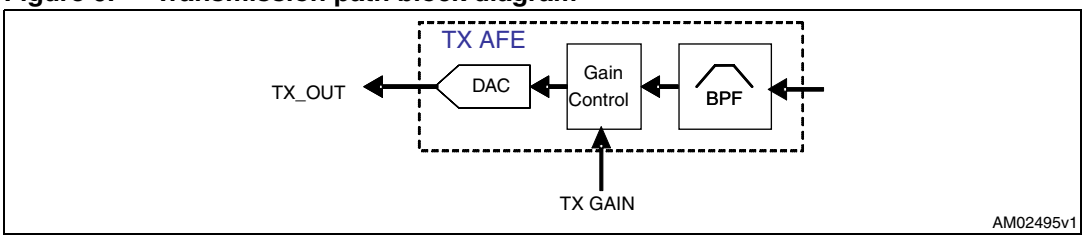
Table 5. PGA gain table

PGA code	PGA gain (typical)	RX_IN max range
	[dB]	[V p-p]
0	-18	16
1	-12	8
2	-6	4
3	0	2
4	6	1
5	12	0.500
6	18	0.250
7	24	0.125
8	30	0.0625

4.2 Transmission path

Figure 6 shows the transmission path block diagram. It is mainly based on a digital to analog converter (DAC), capable to generate a very linear signal up to its full scale output. A gain control block before the DAC gives the possibility to scale down the output signal to match the desired transmission level.

Figure 6. Transmission path block diagram



According to PRIME Specifications the output level can be set on a 8-step logarithmic scale between a Maximum Output Level (MOL) and a minimum output level (MOL - 21dB), with steps of 3dB (typical). The maximum level corresponds to the TX_OUT full range.

4.3 Power amplifier

The integrated Power Amplifier is characterized by very high linearity, required to comply with the different international regulations (CENELEC, FCC etc.) limiting the spurious conducted emissions on the mains, and a current capability of 1Arms (typical) that allows the amplifier driving even very low impedance points of the network.

All pins of the Power Amplifier are accessible, making it possible to build an Active Filter network to increase the linearity of the output signal.

4.4 Thermal shutdown and temperature control

The ST7590 performs an automatic shutdown of the power amplifier circuitry when the internal temperature exceeds 170 °C. After a Thermal shutdown event, the temperature must get below 125 °C before the ST7590 power amplifier comes back to operation.

Moreover a digital thermometer is embedded to identify the internal temperature among four zones, as indicated in *Table 6*.

Table 6. Temperature zones

Temperature zone	Temperature range (Typ.)
1	$T < T\_TH_1$
2	$T\_TH_1 < T < T\_TH_2$
3	$T\_TH_2 < T < T\_TH_3$
4	$T > T\_TH_3$

4.5 Zero-crossing detector

The ST7590 embeds an analog comparator with hysteresis, used for zero-crossing detection. Information about zero crossing events is managed as specified in PRIME protocol specifications.

4.6 One time programmable (OTP) memory array

ST7590 comes with an embedded 64 bit OTP array. This OTP memory is used to store hardware trimming values and the unique identifier EUI48, used for unique addressing in PRIME MAC protocol.

OTP array is composed of 4 16 bit words, indexed from 0 to 3, where the first (index 0) contains hardware trimming values, while the others contain the EUI48 address as specified in *Table 7*.

Table 7. OTP memory array

Index	LSB	MSB
0	Reserved – hardware trimming	
1	EUI48[0..7]	EUI48[8..15]
2	EUI48[16..23]	EUI48[24..31]
3	EUI48[32..39]	EUI48[40..47]

4.7 Power management

Figure 7 shows the power supply structure for the ST7590. The ST7590 operates from two external supply voltages:

- VCC (8 to 18 V) as the main power supply;
- VDDIO (3.3 or 5 V) for the I/O and digital sections.

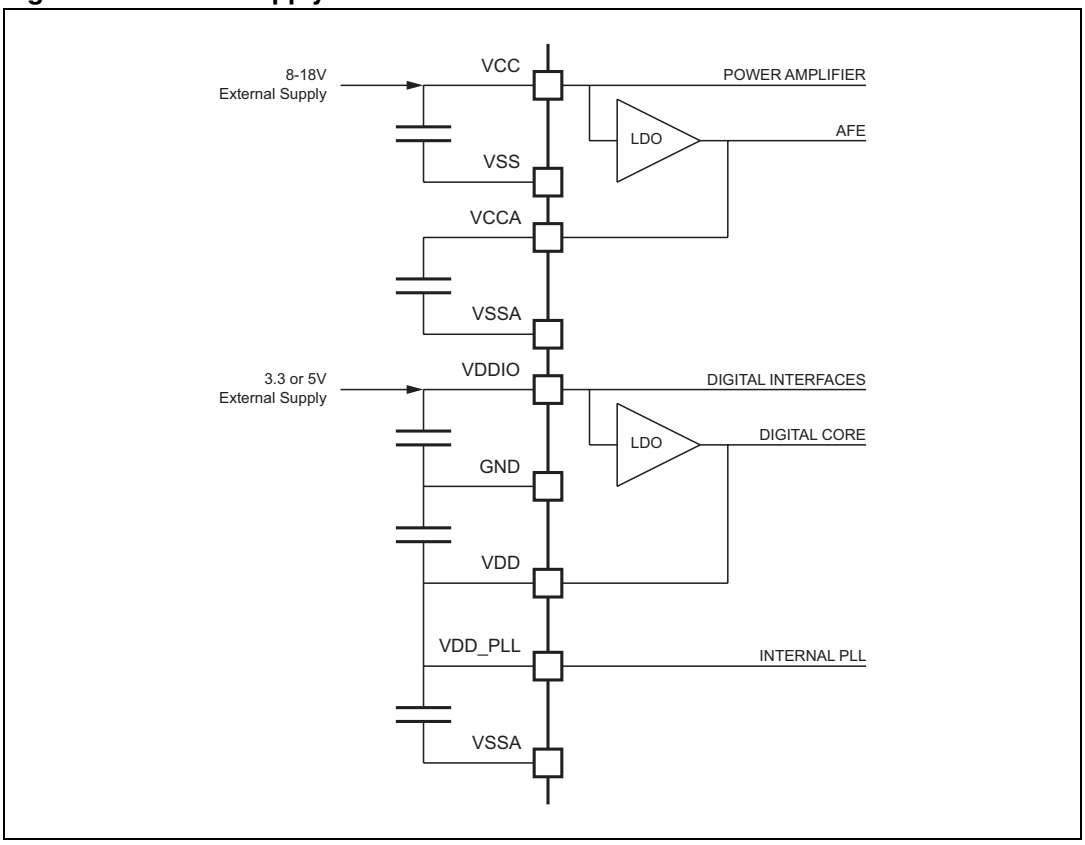
Two internal linear regulators provide the remaining required voltages:

- 5 V regulator (used by the analog front end blocks), generated from the VCC voltage and connected to the VCCA pin;
- 1.8 V regulator (required for the DSP and microcontroller cores, the digital blocks, the PLL and the oscillator), generated from the VDDIO voltage and connected to the VDD_REG_1V8 pin.

All the supply voltages must be properly filtered, to their respective ground, using external capacitors close to each supply pin (see *Figure 7*).

Note: The internal regulators connected to VDD_REG_1V8 and VCCA are not designed to supply external circuitry; their output is externally accessible for filtering purpose only.

Figure 7. Power supply internal scheme



4.8 Clock management

The main clock source is an 8 MHz crystal connected to the internal oscillator through XIN and XOUT pins. Both XIN and XOUT pins have a 32 pF integrated capacitor, in order to drive a crystal having a load capacitance of 16 pF with no additional components.

Alternatively, an 8 MHz external clock can be directly supplied to XIN pin, leaving XOUT floating.

A PLL internally connected to the output of the oscillator generates the internal clocks needed by the digital part.

5 Application information

Figure 8. TQFP100 128 Kb external memory application example

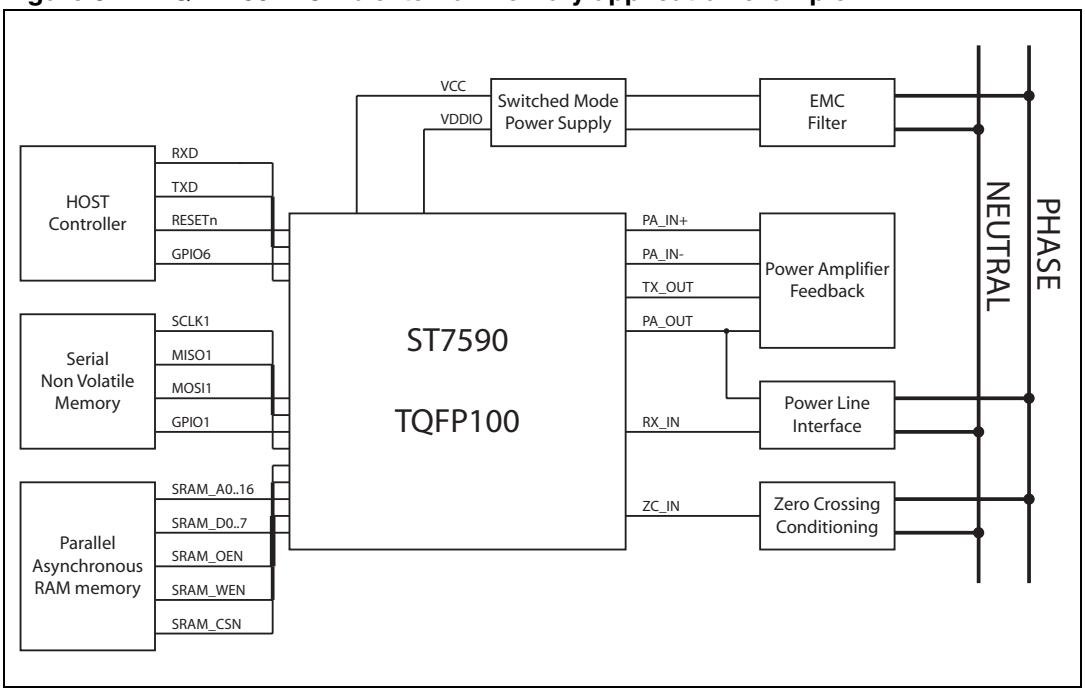
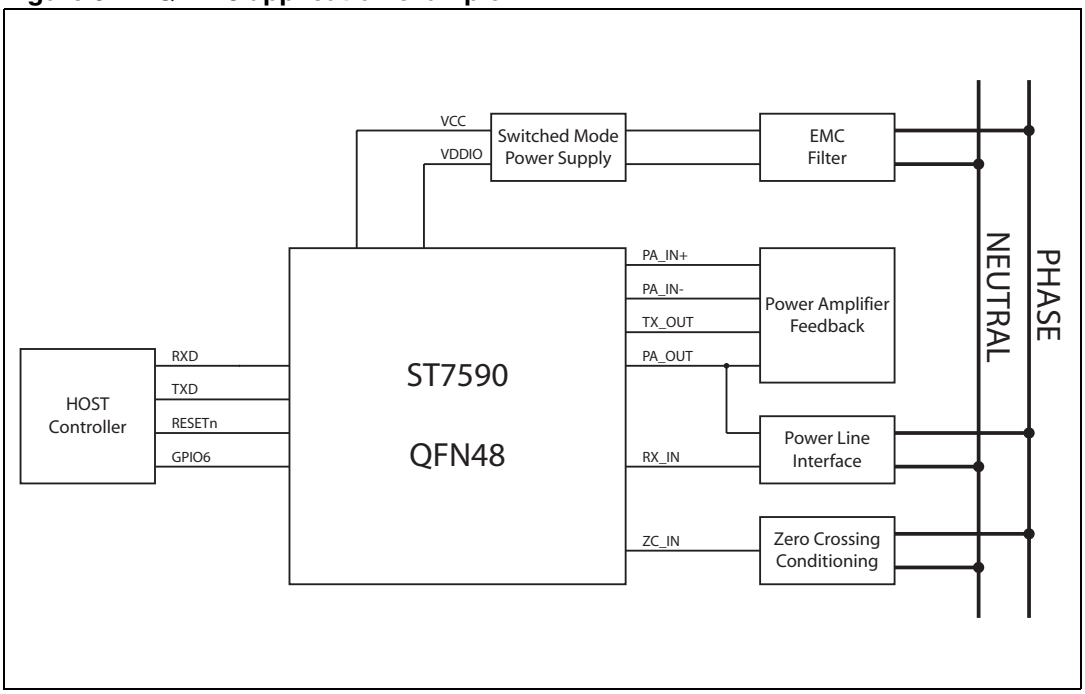


Figure 9. QFN48 application example



6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TQFP 100 package mechanical data

Dim.	(mm)		
	Min.	Typ.	Max.
A			1.2
A1	0.05		0.15
A2	0.95	1	1.05
b	0.17	0.22	0.27
c	0.09		0.2
D	15.8	16	16.2
D1	13.8	14	14.2
D2		5.00	5.50
D3		12	
E	15.8	16	16.2
E1	13.8	14	14.2
E2		5.00	5.50
E3		12	
e		0.5	
L	0.45	0.6	0.75
L1		1	
k	0	3.5	7
ccc			0.08

Figure 10. TQFP 100 package outline

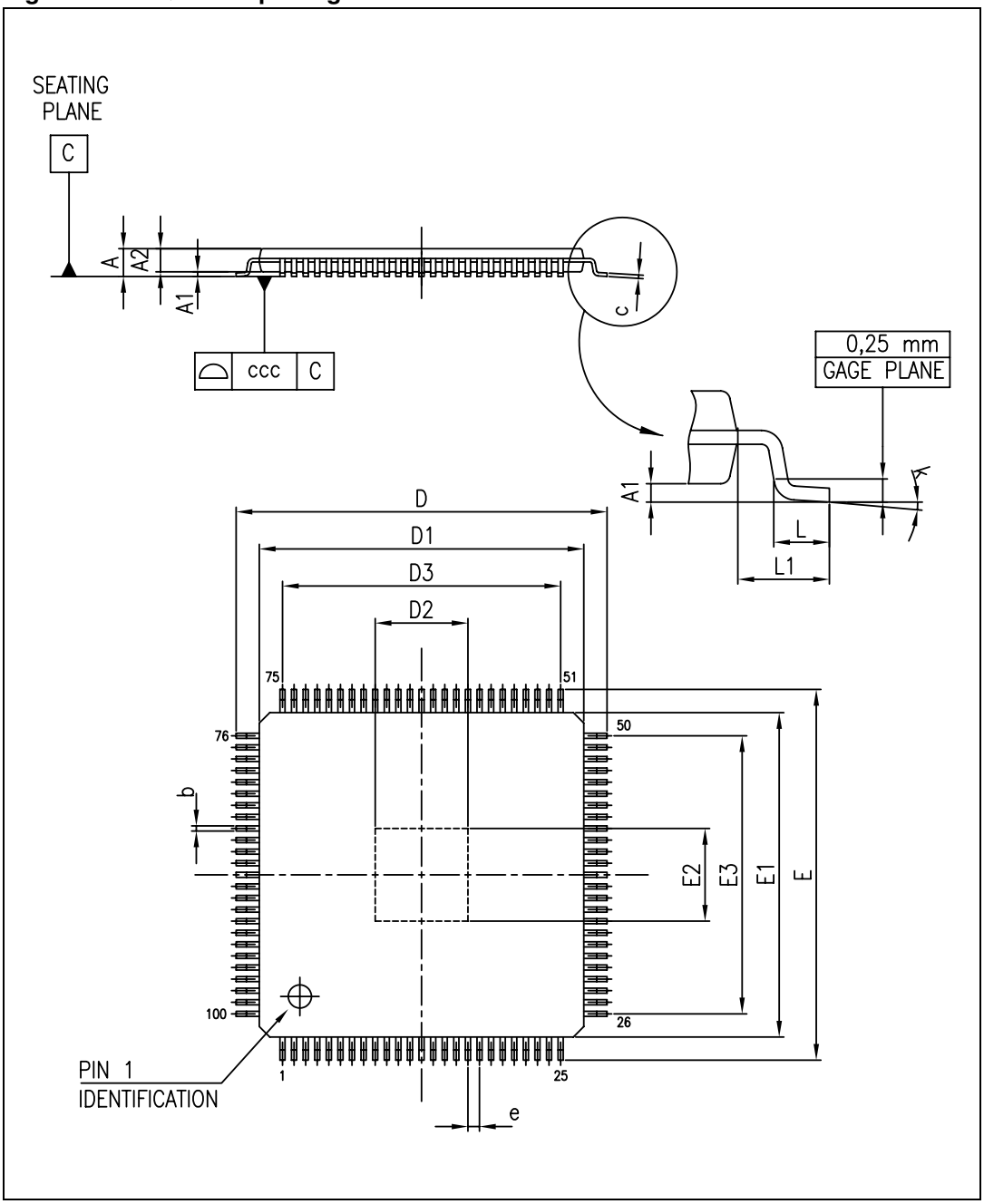
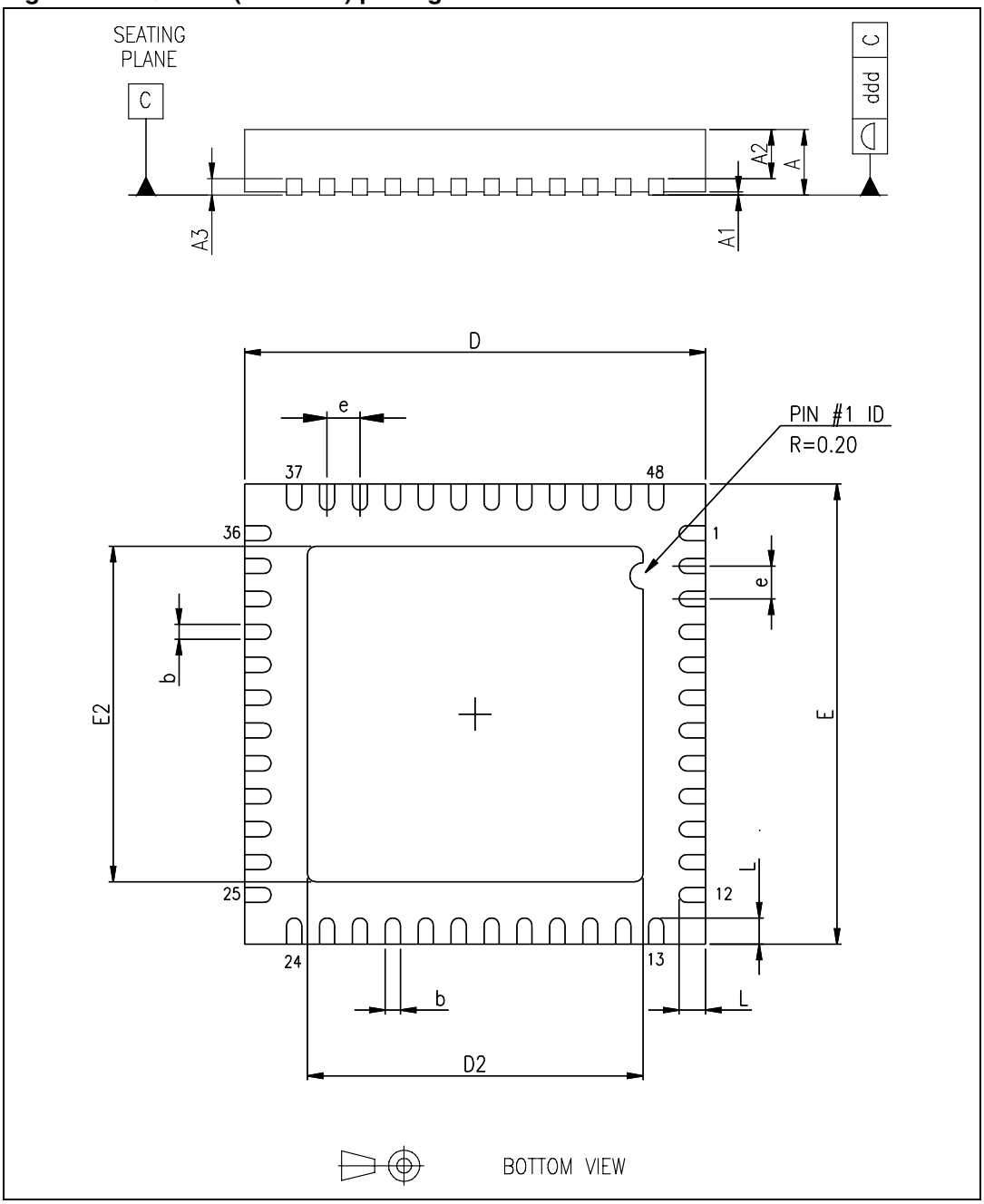


Table 9. QFN-48 (7 x 7 mm) package mechanical data

Dim.	(mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A2		0.65	1.00
A3		0.25	
b	0.18	0.23	0.30
D	6.85	7.00	7.15
D2	4.95	5.10	5.25
E	6.85	7.00	7.15
E2	4.95	5.10	5.25
e	0.45	0.50	0.55
L	0.30	0.40	0.50
ddd			0.08

Figure 11. QFN-48 (7 x 7 mm) package outline



7 Revision history

Table 10. Document revision history

Date	Revision	Changes
19-Oct-2011	1	Initial release

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