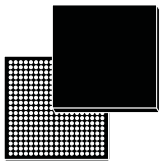
STA108x, STA109x

Accordo2 family – Automotive dual core processor for car radio and display audio application

Datasheet - production data



LFBGA361
(16x16x1.7, 0.8mm pitch)

GAPGPS00902

Features

- AEC-Q100 qualified

Core and infrastructure

- ARM Cortex-R4 MCU running at up to 600 MHz
- MCU memory organization
  - L1 Cache: 32K instruction, 32K data
  - 32 KB ITCM + 32 KB DTCM
  - 1.25 MB embedded SRAM
  - STA109x SDRAM controller: 16/32-bit data up to 166 MHz
  - STA108x SDRAM controller: 16-bit data up to 166 MHz
  - Serial QIO NOR interface executable in place
  - 16-bit parallel NAND/NOR controller
- 32-bit watchdog timer
- 16-channel DMA
- 8x 32-bit free running times/counters
- 5x 16-bit extended function timer (EFT) with input capture/output compare and PWM
- Real time clock (RTC) with fraction readout

Audio Subsystem

- Sound processing DSPs (450MIPS)
- 1x 6 stereo channels hardware Sample Rate Converter
- 6x audio DAC with 103 dB SNR A-Weighted
- 9x Rx / 8x Tx audio interfaces (I^2S/ multichannel ports)
- 1x single ended stereo ADC for AUX IN/Tuner with internal switching logic; 98 dB SNR A-Weighted
- 1x differential Mono ADC for Voice/Tel-IN with internal switching logic; 105 dB SNR

Media Interfaces

- 2x Secure-Digital Multimedia Memory Card Interface (SD3.0/MMC4.4/SDIO)
- 2x USB 2.0 (1x Host and 1x Dual Role) with integrated PHY and support of the charging function
- SPDIF with CDROM block decoder support

Display Subsystem

- STA109x
  - TFT controller up to 1024x1024, 18bpp
  - Resistive Touch Screen Controller
  - Video Input Port, ITU-601/656
  - Graphics acceleration
- STA108x
  - not present

Embedded Isolated Vehicle Interface

- Dedicated Cortex-M3 core
- 256KB isolated embedded memory
- Secured NOR interface

I/O Interfaces

- 1x 10 channels 10-bits ADC
- 3x I^2C multi-master/slave interfaces
- 4x UART Controllers
- 3x Synchronous Serial Port (SSP/SPI)
- GPIO ports
  - STA109x: 7x 32-bit (179 GPIOs)
  - STA108x: 6x 32-bit (130 GPIOs)
- JTAG based in-circuit emulator (ICE) with Embedded Trace Module
- CAN ports
  - STA10x5: 2
  - STA10x0: not present

Operating Conditions

- VDD: 1.14 V - 1.26 V
- VDD_IO: 3.3 V ±10%
- VDD_IO_ON: 3.3 V ±10%,
- Ambient temperature range: -40 / +85 °C

Table 1. Device summary

Root Part Number	Package	Packaging
STA1080 STA1085 STA1090 STA1095	LFBGA 361 16x16x1.7 mm	Tray / Tape and Reel

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1 Description

Accordo2 is a device that provides a cost effective microprocessor solution for modern automotive car radio systems, with an embedded powerful Digital Sound Processing subsystem, as well as a MIPS efficient ARM Cortex-R4 processor.

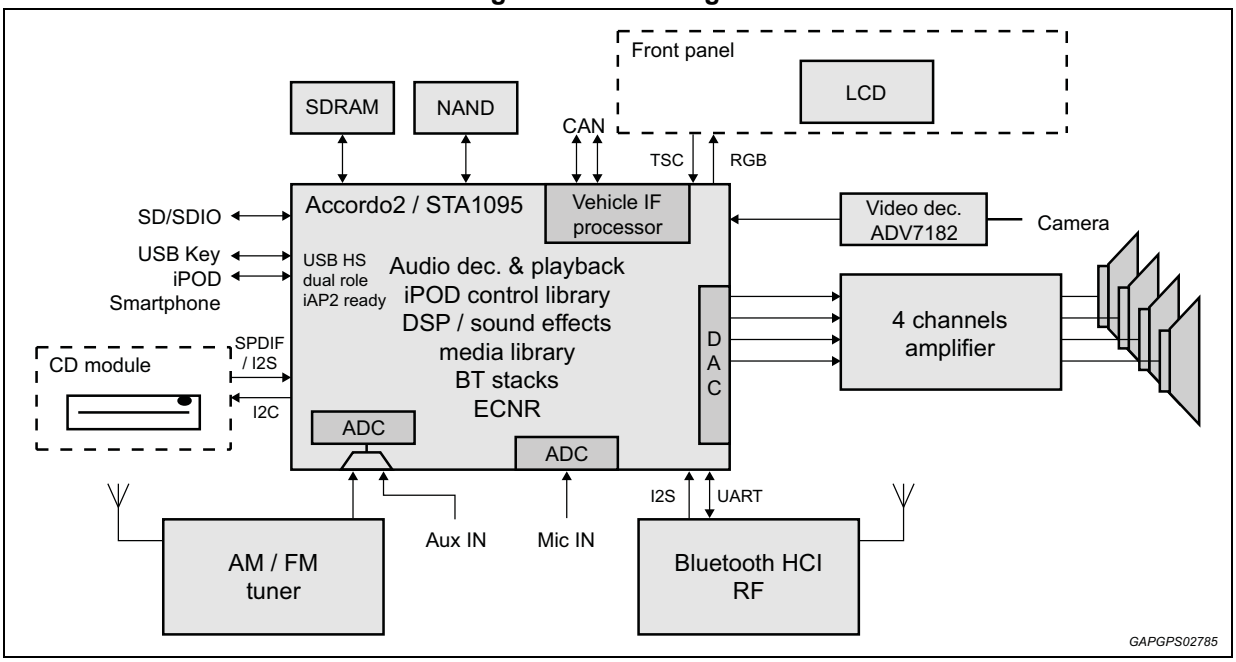
In addition, an ARM Cortex-M3 controller is dedicated for real-time Vehicle Interface Processing.

In terms of peripherals, Accordo2 comes with an exhaustive set of common interfaces (UART/I^2S/I^2C/USB/MMC) which make the device optimal for implementing a feature reach system as well as a cost effective solution.

The solution is bundled with a complete software package, which allows a very fast system implementation.

Accordo2 manages the entire audio chain from analog or digital inputs to analog or digital outputs, including digital audio media decoding, sample rate conversion among various sources, intelligent routing and audio effects / DSP post processing. With its flexible memory configuration, it allows implementing from very low cost systems based on real time OS, scaling up to demanding applications based on Linux OS.

Figure 1. Block diagram



2 System description

2.1 Processor MCU

Accordo2 processing capability relies on an ARM Cortex-R4 running up to 600 MHz, delivering up to 1000 MIPS with very low heat dissipation requirements. The MCU has 32 KB of instruction cache and 32 KB of data cache, as well as 32 KB + 32 KB of TCM Memory dedicated respectively to instructions and data for high throughput and low latency tasks.

2.2 Memory controller

2.2.1 Embedded memory

Accordo2 embeds 1.25 MB of 64-bits SRAM memory clocked at 200 MHz, which can be used for data or code storage delivering 1.6 GB/s throughput.

Embedded memory can be used in conjunction with execution In Place (XIP) NOR devices to implement cost effective solutions. The whole embedded memory is also cacheable and can be accessed by DMA.

2.2.2 SDRAM controller

SDRAM controller supports SDRAM JEDEC interface 16-bit (STA108x) or 32-bit (STA109x) wide, clocked at up to 166 MHz, which allows to interface automotive SDRAM memory devices to handle high footprint applications.

Such memory is cacheable, and can be accessed by DMA.

2.2.3 SQI executable in place

The SQIO controller allows interfacing Serial Quad I/O flash memories up to 133MHz (SDR)

The main features are:

- Direct flash memory access
- Fast memory access through page buffer (256 bytes)
- Programmable single or quad I/O flash interface

SQI memory space can be partitioned to reserve a portion of the NOR device to the Secure CAN Subsystem.

2.2.4 Parallel memory interface

FSMC static memory controller, provides a generic 16-bit parallel interface suitable to connect to NOR devices as well as SRAM and NAND devices. This peripheral allows execution in-place from NOR/SRAMs, as well as DMA accesses.

NOR memory space can be partitioned so to reserve a portion of the parallel NOR device to the Embedded Vehicle Interface subsystem.

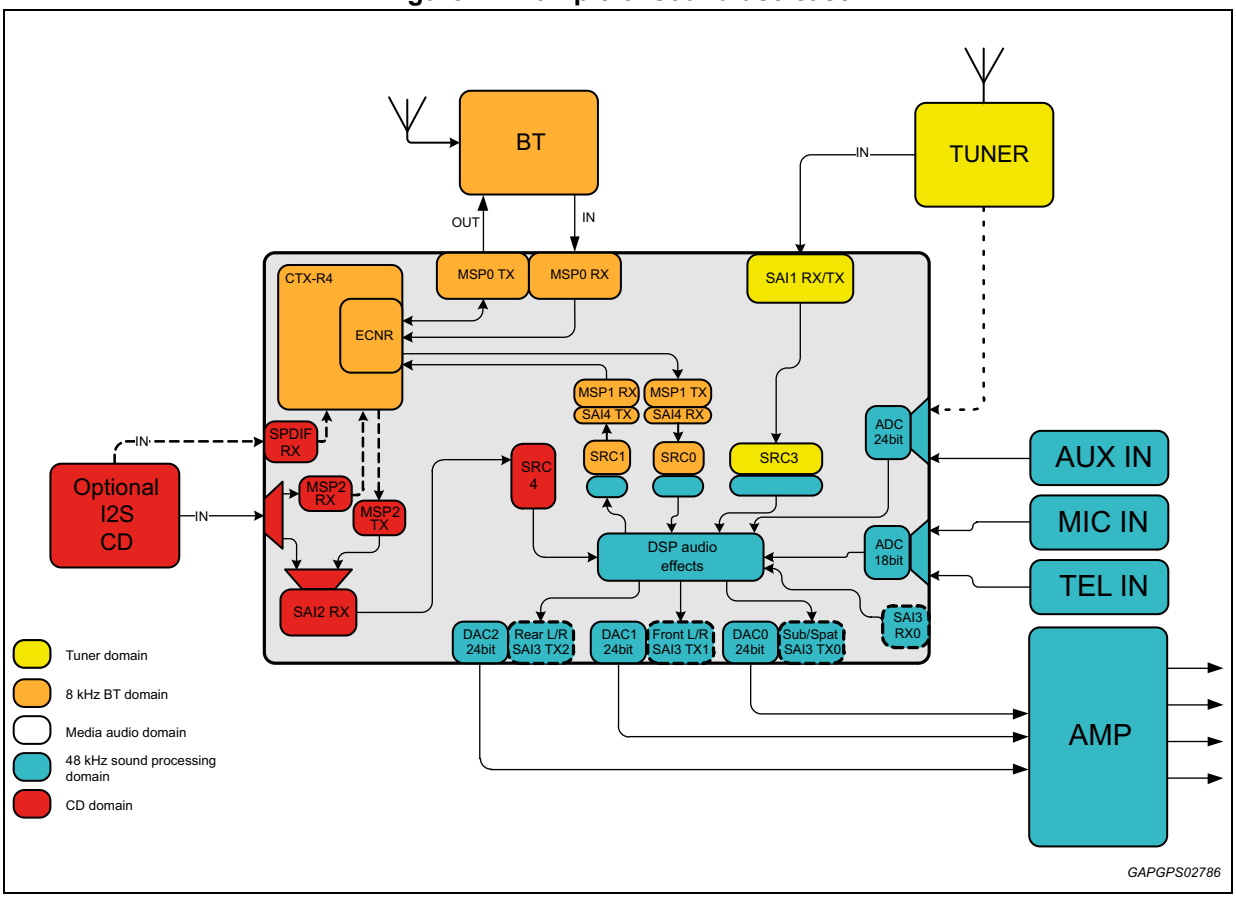
2.3 USB

Accordo2 has one USB HS host interface and one Dual role USB HS, both with embedded PHY, allowing to efficiently connect to mass storage devices, as well as portable devices (phones, pads). Along with USB connectivity, Accordo2 fully supports USB charger specification. The controller supports HS 480-Mbps using an EHCI Host Controller, as well as FS and LS modes through an integrated OHCI interface.

2.4 Sound subsystem

Accordo2 implements a sound subsystem which allows to efficiently handle sound processing tasks, such as spatialization and equalizer, without loading the main CPU with interrupt intensive tasks.

Figure 2. Example of sound use case



2.4.1 Audio interfaces

A complete set of audio interfaces is provided, in order to simplify integration with amplifiers, and input sources. Each interface can be routed to the sound subsystem. A complete list of audio interfaces is provided below:

- 1x AUDIO ADC
  - Shared between AUX LINE and TUNER LINE
  - 18 bits $\Delta\sum$
  - 98 dB A-Weighted Dynamic Range, room temperature
  - -80 dB THD internally, over temperature
  - ADC Inputs are single ended 3.3 V
- 1x Voice ADC
  - Shared among Voice and TEL-IN lines with embedded multiplexer
  - 18 bit $\Delta\sum$
  - 105 dB Dynamic Range, room temperature
  - -80 dB THD, over temperature
  - Both Mic and Tel-In lines are differential inputs.
- 3x Stereo DAC delivering:
  - 24 bits
  - 103 dB A-Weighted Dynamic Range
  - 90 dB THD.
  - DAC outputs are single ended, delivering 730 mVrms.
- 3x I^2S IN
  - SAI1: 1Ch
  - SAI2: 1Ch (either TX or RX), TDM Capable up to 8x
  - SAI3: 3Ch, TDM Capable up to 8x
  - SAI4: 3Ch, TDM Capable up to 8x
  - MSP0: 1Ch TDM capable, PCM Capable
  - MSP2: 1Ch (as alternate to SAI2) TDM capable, PCM Capable
- 3x I^2S OUT
  - SAI2: 1Ch (either TX or RX), TDM Capable up to 8x
  - SAI3: 3Ch, TDM Capable up to 8x
  - SAI4: 3Ch, TDM Capable up to 8x
  - MSP0: 1Ch TDM capable, PCM Capable
- 1x SPDIF IN for CD/CDROM input with Hardware Block Decoder for CDROM error correction.

2.4.2 Routing and sample rate converters

Each audio interface can be routed in both directions (IN/OUT) through sample rate converters, which allow normalizing the sampling rate to the sound processing engine. The audio routing infrastructure is designed to deliver high quality sample rate conversion on multiple channels, allowing simultaneous audio streams, such as Bluetooth Hands Free and audio media playback, to be handled without CPU load.

In order to generate multiple sampling rate audio frequencies, a dedicated fractional PLL is also provided. This PLL also allows an efficient implementation of iPOD playback, by dynamically adjusting the reconstructed audio sampling rate without CPU overload.

2.4.3 Sound DSP

Accordo2 is equipped with three (3) 150 MIPS DSPs (for a total of 450 MIPS) dedicated to sound processing, fully integrated with the sound subsystem with a specific isochronous bus. DSPs are provided with an integrated sound processing library implementing effects like Spatialization, Balancing and Equalizer.

The DSP Core is a 24-bit fixed point Harvard architecture and is equipped with:

- 6 k x 32 bit (64 kByte) program PRAM
- 4 k x 24 bit (18 kByte) data XRAM
- 4 k x 24 bit (18 kByte) data YRAM

Each DSP is connected to other DSPs and audio peripherals by means of an isochronous bus infrastructure which guarantees a controlled throughput and latency for all audio transfers.

2.5 SDMMC

Accordo2 is equipped with 2 SDMMC controllers, allowing mass storage devices or Wi-Fi modems.

Both interfaces implement the following specification:

- eMMC - MultiMedia Card 4.4
  - 26/52 MHz
  - 1,4,8 bit of data
- SD/SDIO 4.0
  - 4 bit interface
  - SDSC/SDHC/SDXC limited to 50MHz SDR freq.

Both interfaces can be used in conjunction with DMA to efficiently implement data transfer with minimal CPU load for handling interrupts.

2.6 DMA

DMA is designed to efficiently perform memory to memory, and memory to peripherals transfers, offloading such tasks from the processor, thus reducing interrupt handling load. DMA provides 16 independent channels which can be dynamically assigned to different data-paths. Complex Scatter/gather transfers can be implemented by programming specific DMA command linked lists.

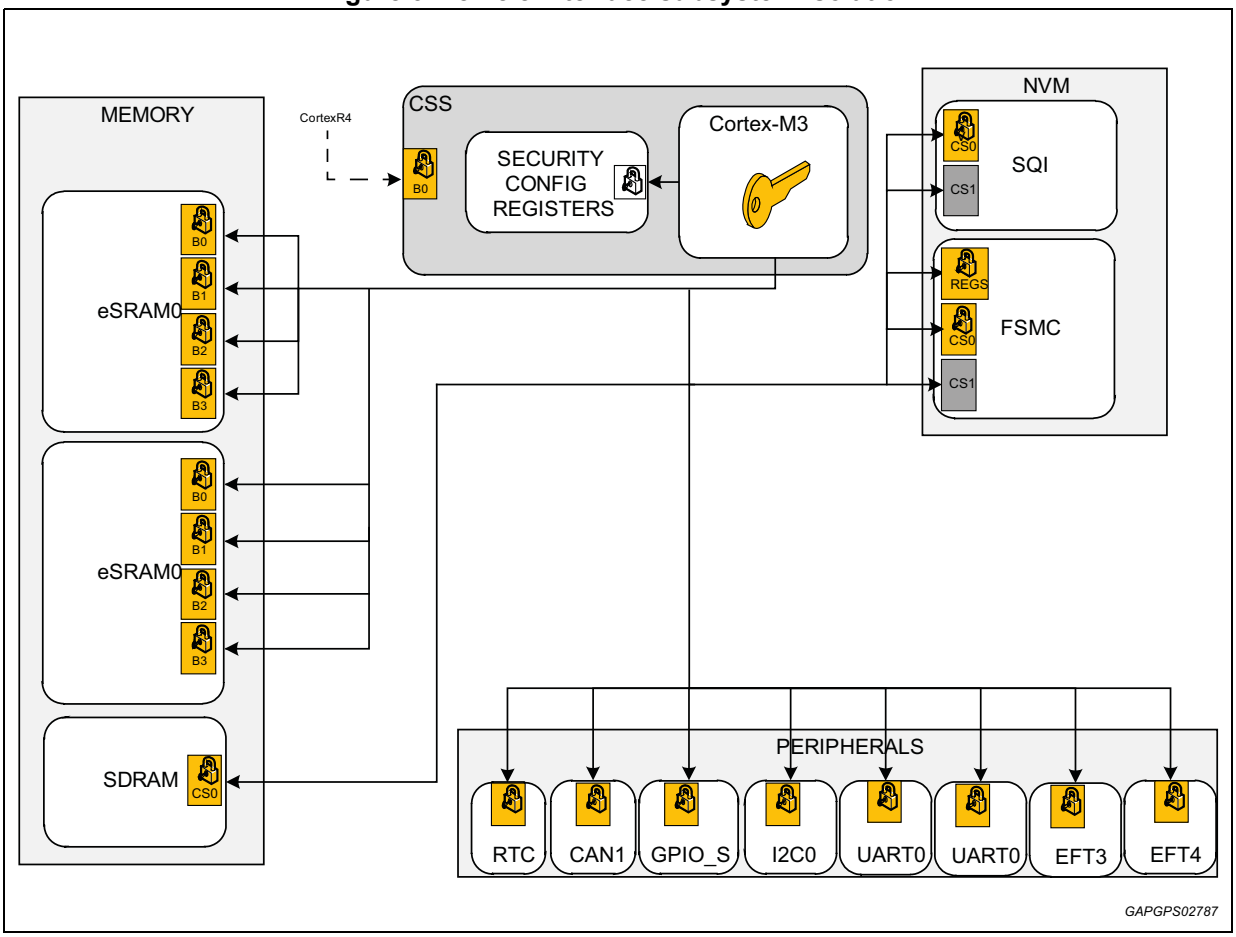
2.7 Embedded isolated vehicle interface subsystem

Accordo2 allows isolating critical code from the main application by implementing a dedicated subsystem based on ARM Cortex-M3, along with:

- 256 KB dedicated embedded SRAM
- Interrupt controller
- timers
- CAN controller
- Dedicated GPIOs
- Dedicated Wakeup lines
- Back-up RAM in always on domain
- Local RTC

In order to guarantee the security of CAN network, all of the above can be completely isolated from the rest of the system, in such a way that no application running on Cortex-R4 can access CAN specific resources by any means (STA10x5). This subsystem can also be dedicated to implement secure features, such as boot authentication, as well as interrupt intensive tasks to offload main CPU. The secure subsystem communicates with the application running on Cortex-R4 using a Hardware Mailbox interrupt based mechanism.

Figure 3. Vehicle Interface subsystem isolation



A specific set of peripherals can be reserved and locked to be only accessible from Cortex-M3, thus allowing a complete independent subsystem to be realized. In addition to that, specific secure GPIOs as well as wake signals are reserved for such subsystem.

2.8 General purpose ADC

Accordo2 has a 10-input SAR ADC with 10-bit resolution and sampling frequency up to 2.5 MHz.

2.9 GPIOs

Accordo2 has 179 GPIOs in STA109x and 130 in STA108x (16 of which are dedicated to Embedded Isolated Vehicle Interface subsystem). They can be independently configured either as INPUT or OUTPUT. In order to make the system flexible, these IOs are multiplexed on PINs with other peripherals (the alternate function scheme is provided as a separate document).

2.10 Generic interfaces

2.10.1 4x UARTS:

- Programmable baud rates up to 3 Mbps
- Hardware Flow control
- DMA capability.

2.10.2 3x I^2C:

- Master/slave modes in multi-master environment
- Multiple baud rates supported: 100/400/1000/3400 Kbps
- DMA capability.

2.10.3 3xSSP/SPI ports supporting:

- Motorola SPI-compatible interface
- Texas Instrument synchronous serial interface
- National Semiconductor Microwire interface
- Unidirectional interface
- DMA capability.

2.11 Input capture / Output compare

5 EFT (Enhanced Function timers) implement a very flexible input capture and output compare feature set. Each EFT block can provide 2 Input capture and 2 output PWM lines. EFT are based on 16-bit counters with dedicated prescaler.

2.12 Watchdog and timers

Cortex-R4 has:

- 2x MTU timers each providing access to four programmable 32-bit Free-Running decrementing Counters (FRCs)
- 1x Watchdog (WDT) unit that provides a way to recover from software crashes.
- 1x RTC counter clocked with 32 KHz Oscillator.

Cortex-M3 has:

- 1x MTU timers providing access to four programmable 32-bit Free-Running decrementing Counters (FRCs)
- 1x Watchdog (WDT) unit that provides a way to recover from software crashes.

2.13 Power modes

Accordo2 supports the following power modes:

- Normal
- Software Standby
- Deep Standby
- Power Off

The SoC requires three power lines for internal logic (excluding analog block power lines), which are identified as:

- 3V3 standby
- 3V3 IOs, switchable
- 1V2 Core, switchable

In each power state, the SoC is permanently protected from Voltage drops by means of a brownout logic, which would trigger a system reset in case a low voltage condition is detected.

The following table summarizes the condition of each Accordo2 power state.

Table 2. Summarized conditions of each Accordo2 power state

Power Mode	3V3 Standby	3V3 IO	1V2 Core	Analog	Clocks	RTC	Wake Modes
Normal	ON	ON	ON	ON	Active	Active	N.A.
Soft Standby	ON	ON	ON	ON	Gated	Active	IRQ
Deep Standby	ON	OFF	OFF	OFF	OFF	Optional	WAKE Lines
Power Off	OFF	OFF	OFF	OFF	OFF	OFF	PowerOn

2.14 Video input port (VIP) - Only available in STA109x

The Video Input Port (VIP) allows to grab images from external devices, supporting parallel CCIR-656 interface up to 54 MHz. Both embedded synchronization and external synchronization are supported. VIP supports both interlaced or progressive mode.

The VIP is synchronized with display controller to prevent from tearing effects, and is used in conjunction with SGA to implement the fly YUV → RGB color conversion and bilinear interpolated re-scaling.

2.15 Smart graphics accelerator (SGA) - Only available in STA109x

The aim of the Smart Graphic Accelerator (SGA) is to provide an efficient 2D and 3D primitive drawing tool that offloads the CPU, reducing MIPS and power consumption for pixel processing.

- Control and synchronization:
  - Instruction Automatic Fetch from a program file
  - Flow Control: goto/gosub/wait/interrupt instructions
  - Can synchronize itself on external hardware triggers
- 2D-Graphic features:
  - 2D Rendering Speed: up to 208 MPixel/s
  - Pixel, Line, Filled Triangle, Filled Rectangle primitives
  - Line-Stippling, Filling Pattern
  - Flat and Gradient colour fill (in triangle & rectangles)
- Video overlay features:
  - BitBlitting on Rectangle, Triangle shapes
  - Image Resizing (Bilinear Interpolation Filter or Sub/OverSampling)
  - Image Rotation (with any angle)
  - Colour Conversion (YUV-to-RGB or RGB-to-YUV, 16-235 clamping possible)
  - Transparency extraction (exact Colour Keying or Colour Cube (triple interval)
  - Colour Swap with Colour Keying
  - AlphaBlending of 3 sources to a destination, ROP boolean operations
  - Dithering operator
- 3D features:
  - 3D Rendering Speed: up to 52 MFragment/s, impacted by memory access delays
  - FrameBuffer and DepthBuffer Cache: 256 Bytes, Fully Associative
  - Texture Cache: 2 kBytes, 4 associative ways
  - Early Z-Test (lowers texture calls)
  - 16-bit Z-Buffering
  - Double Texture Blending Units
  - Texture Perspective Correction
  - Texture Nearest and Bilinear Filtering
  - Texture MipMap selection on a Per-Triangle basis

- Texture Flexible Wrap Mode (Repeat, Clamp, Mirrored_Repeat, ...)
- Primary Colour Interpolation (Gouraud Shading), Fog Blending
- Alpha, Depth, Stencil Tests

2.16 Display controller - Only available in STA109x

The main features of the LCD Controller are:

- Supports single and dual panel monochrome STN displays with 4 or 8 bits interfaces
- Supports single and dual panel color STN displays with 8 bits interfaces
- Supports TFT color displays
- Supports AD-TFT and HR-TFT color displays
- Resolution programmable up to 1024 lines of 1024 pixels
- 1,2,4 or 8 bpp palettized color displays
- 12-bpp (4:4:4), 15+I bpp (I:5:5:5) or 16 bpp (5:6:5) true-color
- 24-bpp packed and non-packed true-color (non-palettized)
- Programmable timing for different display panels
- 256 entry, 16-bit palette RAM
- Frame, line and pixel clock signals generation
- Color enhancement (16-bpp to 18-bpp conversion) for addressing 18-bit (RGB 666) TFTpanels using only 16-bpp resolution
- Supports little and big-endian, as well as WinCE formats
- Interrupt and synchro generation event

2.17 Touch screen controller - Only available in STA109x

The Touch Screen Controller consists of a 4-wire touch-screen controller and an 8-input ADC. It is enhanced with a movement tracking algorithm, 128 depth buffer and a programmable active window feature.

The main features are:

- Integrated 4 wire touchscreen controller
- Interrupt output pin
- 8 analog input, 10-bit resolution ADC
- 128-depth buffer touchscreen controller
- Programmable active window feature
- Touch Screen movement detection algorithm to avoid excessive data

3 Signal description

3.1 Functional signal list

3.1.1 System and power management

Table 3. System and power management

Name	GPIOs	Balls	DIR	Power domain	Description
CLKOUT0	M3_GPIO13	A12	O	VDD_IO	Programmable clock output 0.
CLKOUT1	GPIO49	F5	O	VDD_IO	Programmable clock output 1.
DEBUGCFG	M3_GPIO13	A12	I	VDD_IO	DBGCFG. This pin is latched on the rising edge of POR reset to define the target connected by default to the JTAG . 0b: Cortex-M3 1b: Cortex-R4 After reset this pin can be used as GPIO.
JTAGSEL	-	E11	T	VDD_IO	Test Signal. It selects whether the JTAG is used for ATE test or as debug port. Connect it to GND in the application (debug port).
M3_CLK32KOUT	-	D13	O	VDD_IO_AON	Output 32 kHz clock.
M3_IGNKEY	-	A15	I	VDD_IO_AON	PMU Ignition Key signal. Used by PMU to change the state of the system.
M3_LVI	-	B14	I	VDD_IO_AON	PMU Low Voltage Indication. Used by PMU to change the state of the system (Normal, Standby).
M3_ONOFF	-	A13	I	VDD_IO_AON	PMU ON/OFF. Connect it to the On/off Car Radio push button.
M3_PWREN	-	B15	O	VDD_IO_AON	PMU Power Enable. Used by the PMU to enable external voltage regulator, when moving out of Standby state.
M3_SXTALI	-	C14	I	VDD_IO_AON	Crystal input. 32 kHz RTC clock.
M3_SXTALO	-	D14	O	VDD_IO_AON	Crystal output.
M3_VDDOK	-	A14	I	VDD_IO_AON	PMU VDDOK. This signal is used by the PMU to detect if the external power is valid. The PMU moves to Normal state if VDDOK=1.
MXTALI	-	N19	I	VDD_IO	Crystal input. 24/26MHz crystal.
MXTALO	-	N18	O	VDD_IO	Crystal output.
OTP_FUSE_HV	-	A1	P	Power	OTP programming voltage. Leave it floating in the application.

Table 3. System and power management (continued)

Name	GPIOs	Balls	DIR	Power domain	Description
REMAP0	M3_GPIO14	C3	I	VDD_IO	Memory Remap pin. This pin is latched on the rising edge of POR reset and it defines the boot device. After reset these pins can be used as GPIO.
REMAP1	M3_GPIO15	B2	I	VDD_IO	Memory Remap pin. This pin is latched on the rising edge of POR reset and it defines the boot device. After reset these pins can be used as GPIO.
SYSRSTn	-	B6	I	VDD_IO	System Reset not.
TEST_CLK	-	-	I	VDD_IO	ATE TEST clock. Not used in the application.
WAKE0	M3_GPIO0	C15	I	VDD_IO_AON	Wake up signal line 0. An event on this line wakes the system up from Stand-By state.
WAKE1	M3_GPIO1	D15	I	VDD_IO_AON	Wake up signal line 1. An event on this line wakes the system up from Stand-By state.
WAKE2	M3_GPIO2	B16	I	VDD_IO_AON	Wake up signal line 2. An event on this line wakes the system up from Stand-By state.
WAKE3	M3_GPIO3	C16	I	VDD_IO_AON	Wake up signal line 3. An event on this line wakes the system up from Stand-By state.
WAKE4	M3_GPIO4	D16	I	VDD_IO_AON	Wake up signal line 4. An event on this line wakes the system up from Stand-By state.
WAKE5	M3_GPIO5	A16	I	VDD_IO_AON	Wake up signal line 5. An event on this line wakes the system up from Stand-By state.
WAKE6	M3_GPIO6	A17	I	VDD_IO_AON	Wake up signal line 6. An event on this line wakes the system up from Stand-By state.
WAKE7	M3_GPIO7	A18	I	VDD_IO_AON	Wake up signal line 7. An event on this line wakes the system up from Stand-By state.

3.1.2 Analog audio

Table 4. Analog audio signals

Name	GPIOs	Balls	DIR	Power domain	Description
ADC0_AIN1_L	-	F18	I	ADC0_1_AVDD	ADC0 (AUX). Analog input 1 left.
ADC0_AIN1_R	-	F19	I	ADC0_1_AVDD	ADC0 (AUX). Analog input 1 right.
ADC0_AIN2_L	-	F16	I	ADC0_1_AVDD	ADC0 (AUX). Analog input 2 left.
ADC0_AIN2_R	-	F17	I	ADC0_1_AVDD	ADC0 (AUX). Analog input 2 left.
ADC1_AIN1_N	-	H19	I	ADC0_1_AVDD	ADC1 (Voice). Analog auxiliary differential input 1 negative.
ADC1_AIN1_P	-	H18	I	ADC0_1_AVDD	ADC1 (Voice). Analog auxiliary differential input 1 positive.
ADC1_MICIN_N	-	G19	I	ADC0_1_AVDD	ADC1 (Voice). Analog MIC differential input negative.
ADC1_MICIN_P	-	G18	I	ADC0_1_AVDD	ADC1 (Voice). Analog MIC differential input positive.
DAC_OUT0L	-	C18	O	DAC_I/O_AVDD	DAC0. Analog output Channel 0 left .
DAC_OUT0R	-	D18	O	DAC_I/O_AVDD	DAC0. Analog output channel 0 right.
DAC_OUT1L	-	B18	O	DAC_I/O_AVDD	DAC1. Analog output channel 1 left.
DAC_OUT1R	-	D19	O	DAC_I/O_AVDD	DAC1. Analog output channel 1 right.
DAC_OUT2L	-	C19	O	DAC_I/O_AVDD	DAC2. Analog output channel 2 left.
DAC_OUT2R	-	B19	O	DAC_I/O_AVDD	DAC2. Analog output channel 2 right.

3.1.3 Digital audio

Table 5. Digital audio signals

Name	GPIOs	Balls	DIR	Power domain	Description
AUDIO_REFCLK	GPIO7	B10	I/O	VDD_IO	Audio Master Clock. Input: it can be used as master audio clock for MSP peripherals . Output: audio master clock running at 512*Fs.
I2S0_BCLK		L1	I/O	VDD_IO	I^2S0 (MSP0). Bit clock line.
I2S0_FS		L2	I/O	VDD_IO	I^2S0 (MSP0). Frame Synchronization line.
I2S0_RX		K2	I	VDD_IO	I^2S0 (MSP0). Receive data line.
I2S0_TX		K1	O	VDD_IO	I^2S0 (MSP0). Transmit data line.
I2S2_BCLK	GPIO16	C9	I/O	VDD_IO	I^2S2 (MSP2). Bit clock line.
I2S2_FS	GPIO17	D10	I/O	VDD_IO	I^2S2 (MSP2). Frame Synchronization line.
I2S2_RX	GPIO18	D11	I	VDD_IO	I^2S2 (MSP2). Receive data line.
SAI1_BCLK	GPIO19	C10	I	VDD_IO	SAI1. Serial Audio Interface 1 bit clock line. Slave only configuration.

Table 5. Digital audio signals (continued)

Name	GPIOs	Balls	DIR	Power domain	Description
SAI1_FS	GPIO20	B11	I	VDD_IO	SAI1. Serial Audio Interface 1 frame synchronization line. Slave only configuration.
SAI1_RX	GPIO21	A10	I	VDD_IO	SAI1. Serial Audio Interface 1 receive data line.
SAI2_BCLK	GPIO16	C9	I	VDD_IO	SAI2. Serial Audio Interface 2 bit clock line. Slave configuration only.
SAI2_FS	GPIO17	D10	I	VDD_IO	SAI2. Serial Audio Interface 2 frame synchronization line. Slave only configuration.
SAI2_RX/TX	GPIO7 GPIO18	B10 D11	I/O	VDD_IO	SAI2. Serial Audio Interface 2 receive/transmit data line .
SAI3_BCLK	GPIO8	A9	O	VDD_IO	SAI3. Serial Audio Interface 3 bit clock
SAI3_FS	GPIO9	A8	O	VDD_IO	SAI3. Serial Audio Interface 3 frame synchronization line.
SAI3_RX0	GPIO13	B8	I	VDD_IO	SAI3. Serial Audio Interface 3 receive data line 0.
SAI3_RX1	GPIO14	A7	I	VDD_IO	SAI3. Serial Audio Interface 3 receive data line 1.
SAI3_RX2	GPIO15	A6	I	VDD_IO	SAI3. Serial Audio Interface 3 receive data line 3.
SAI3_TX0	GPIO10	C8	O	VDD_IO	SAI3. Serial Audio Interface 3 transmit data line 0.
SAI3_TX1	GPIO11	D9	O	VDD_IO	SAI3. Serial Audio Interface 3 transmit data line 1.
SAI3_TX2	GPIO12	B9	O	VDD_IO	SAI3. Serial Audio Interface 3 transmit data line 2.
SAI4_BCLK	GPIO0	A11	I/O	VDD_IO	SAI4. Serial Audio Interface 4 bit clock.
SAI4_FS	GPIO1	B12	I/O	VDD_IO	SAI4. Serial Audio Interface 4 frame synchronization line.
SAI4_RX0	GPIO5	B13	I	VDD_IO	SAI4. Serial Audio Interface 4 receive data line 0.
SAI4_RX1	GPIO13	B8	I	VDD_IO	SAI4. Serial Audio Interface 4 receive data line 1.
SAI4_RX2	GPIO8	A9	I	VDD_IO	SAI4. Serial Audio Interface 4 receive data line 2.
SAI4_TX0	GPIO2	C12	O	VDD_IO	SAI4. Serial Audio Interface 4 transmit data line 0.
SAI4_TX1	GPIO3	D12	O	VDD_IO	SAI4. Serial Audio Interface 4 transmit data line 1.
SAI4_TX2	GPIO4	C13	O	VDD_IO	SAI4. Serial Audio Interface 4 transmit data line 2.
SPDIF_RX	GPIO18	D11	I	VDD_IO	SPIDIF. Data input line.

3.1.4 Peripherals (CAN, I²C, UART,SPI)

Table 6. Peripherals signals

Name	GPIOs	Balls	DIR	Power domain	Description
CAN0_RX	M3_GPIO9	C6	I	VDD_IO	CAN0. Receive signal line.(1)
CAN0_TX	M3_GPIO8	B7	O	VDD_IO	CAN0. Transmit signal line.(1)
CAN1_RX	S_GPIO0	D6	I	VDD_IO	CAN1. Receive signal line.(1)
CAN1_TX	S_GPIO1	D7	O	VDD_IO	CAN1. Transmit signal line.(1)
I2C0_SCL	-	C7	I/O	VDD_IO	I²C0. Clock line. It needs an external pull-up.
I2C0_SDA	-	D8	I/O	VDD_IO	I²C0. Data line. It needs an external Pull-up.
I2C1_SCL	GPIO30 GPIO35 GPIO43	M1 B3 A4	I/O	VDD_IO	I²C1. Clock line . It needs an external Pull-up.
I2C1_SDA	GPIO31 GPIO34 GPIO42	M4 B4 A3	I/O	VDD_IO	I²C1. Data line. It needs an external pull-up.
I2C2_SCL	GPIO14 GPIO46	A7 D5	I/O	VDD_IO	I²C2. Clock line. It needs an external pull-up.
I2C2_SDA	GPIO15 GPIO45	A6 C4	I/O	VDD_IO	I²C2. Data line. It needs an external pull-up.
SPI0_RXD	-	N3	I	VDD_IO	SPI0. Receive data line.
SPI0_SCK	-	N1	I/O	VDD_IO	SPI0. Clock signal line.
SPI0_SS	-	N2	I/O	VDD_IO	SPI0. Frame signal line.
SPI0_TXD	-	N4	O	VDD_IO	SPI0. Transmit data line
SPI1_RXD	GPIO32	M3	I	VDD_IO	SPI1. Receive data line.
SPI1_SCK	GPIO33	M2	I/O	VDD_IO	SPI1. Clock signal line.
SPI1_SS	GPIO30	M1	I/O	VDD_IO	SPI1. Frame signal.
SPI1_TXD	GPIO31	M4	O	VDD_IO	SPI1. Transmit data line.
SPI2_RXD	GPIO20 GPIO24	B11 R3	I	VDD_IO	SPI2. Receive data line
SPI2_SCK	GPIO21 GPIO25	A10 R4	I/O	VDD_IO	SPI2. Clock signal line.
SPI2_SS	GPIO22 GPIO99	R1 H2	I/O	VDD_IO	SPI2. Frame signal line.
SPI2_TXD	GPIO19 GPIO23	C10 R2	O	VDD_IO	SPI2. Transmit data line.
UART0_CTS	-	L3	I	VDD_IO	UART0. Clear to send.
UART0_RTS	-	L4	O	VDD_IO	UART0. Request to send.

Table 6. Peripherals signals (continued)

Name	GPIOs	Balls	DIR	Power domain	Description
UART0_RX	-	K3	I	VDD_IO	UART0. Received serial data.
UART0_TX	-	K4	O	VDD_IO	UART0. Transmitted serial data.
UART1_CTS	GPIO40	B1	I	VDD_IO	UART1. Clear to send.
UART1_RTS	GPIO41	A2	O	VDD_IO	UART1. Request to send.
UART1_RX	GPIO25 GPIO35 GPIO37	R4 B3 T16	I	VDD_IO	UART1. Received serial data.
UART1_TX	GPIO24 GPIO34 GPIO36	R3 B4 T17	O	VDD_IO	UART1. Transmitted serial data.
UART2_RX	GPIO9 GPIO38	A8 T18	I	VDD_IO	UART2. Received serial data.
UART2_TX	GPIO12 GPIO39	B9 R19	O	VDD_IO	UART2. Transmitted serial data.
UART3_RX	GPIO33 GPIO40	M2 B1	I	VDD_IO	UART3. Received serial data.
UART3_TX	GPIO32 GPIO41	M3 A2	O	VDD_IO	UART3. Transmitted serial data.

1. Only available in STA10x5.

3.1.5 PWM and input capture

Table 7. EFT signals

Name	GPIOs	Balls	DIR	Power Domain	Description
EFT0_EXTCK	GPIO22 GPIO30	R1 M1	I	VDD_IO	EFT0. External Input Clock.
EFT0_ICAP0	GPIO22 GPIO42	R A3	I	VDD_IO	EFT0. Input Capture 0.
EFT0_ICAP1	GPIO23 GPIO43	R2 A4	I	VDD_IO	EFT0. Input Capture 1.
EFT0_OCMP0	GPIO24 GPIO42	R3 A3	O	VDD_IO	EFT0. Output compare 0.
EFT0_OCMP1	GPIO25 GPIO43	R4 A4	O	VDD_IO	EFT0. Output compare 1.
EFT1_EXTCK	GPIO26 GPIO31	N16 M4	I	VDD_IO	EFT1 External Input Clock
EFT1_ICAP0	GPIO26 GPIO34	N16 B4	I	VDD_IO	EFT1. Input Capture 0.

Table 7. EFT signals (continued)

Name	GPIOs	Balls	DIR	Power Domain	Description
EFT1_ICAP1	GPIO27 GPIO35	N17 B3	I	VDD_IO	EFT1. Input Capture 1.
EFT1_OCMP0	GPIO28 GPIO33	M19 M2	O	VDD_IO	EFT1. Output compare 0.
EFT1_OCMP1	GPIO29 GPIO32	P19 M3	O	VDD_IO	EFT1. Output compare 1.
EFT2_EXTCK	GPIO21 GPIO44	A10 B5	I	VDD_IO	EFT2. External Input Clock.
EFT2_ICAP0	GPIO40 GPIO44	B1 B5	I	VDD_IO	EFT2. Input Capture 0.
EFT2_ICAP1	GPIO11 GPIO41	D9 A2	I	VDD_IO	EFT2. Input Capture 1.
EFT2_OCMP0	GPIO19 GPIO44	C10 B5	O	VDD_IO	EFT2. Output compare 0.
EFT2_OCMP1	GPIO10 GPIO20	C8 B11	O	VDD_IO	EFT2. Output compare 1.
EFT3_EXTCK	S_GPIO4 S_GPIO5	P4 P3	I	VDD_IO	EFT3. External input clock.
EFT3_ICAP0	S_GPIO0 S_GPIO4	D6 P4	I	VDD_IO	EFT3. Input Capture 0.
EFT3_ICAP1	S_GPIO1 S_GPIO5	D7 P3	I	VDD_IO	EFT3 Input Capture 1
EFT3_OCMP0	S_GPIO0 S_GPIO4	D6 P4	O	VDD_IO	EFT3. Output compare 0.
EFT3_OCMP1	S_GPIO1 S_GPIO5	D7 P3	O	VDD_IO	EFT3. Output compare 1.
EFT4_EXTCK	S_GPIO2 S_GPIO6	C5 P2	I	VDD_IO	EFT4. External input clock.
EFT4_ICAP0	S_GPIO2 S_GPIO6	C5 P2	I	VDD_IO	EFT4. Input Capture 0.
EFT4_ICAP1	S_GPIO3 S_GPIO7	A5 P1	I	VDD_IO	EFT4. Input Capture 1.
EFT4_OCMP0	S_GPIO2 S_GPIO6	C5 P2	O	VDD_IO	EFT4. Output compare 0.
EFT4_OCMP1	S_GPIO3 S_GPIO7	A5 P1	O	VDD_IO	EFT4. Output compare 1.

3.1.6 SDIO/SD/MMC

Table 8. SD MMC Signals

Name	GPIOs	Balls	DIR	Power Domain	Description
SDMMC0_CLK	-	R18	O	VDD_IO	SD/MMC0. Clock line.
SDMMC0_CMD	-	P18	I/O	VDD_IO	SD/MMC0. Command line.
SDMMC0_CMDDIR	GPIO23	R2	O	VDD_IO	SD/MMC0. Command line direction control.
SDMMC0_DAT0_DIR	GPIO14 GPIO45	A7 C4	O	VDD_IO	SD/MMC0. Data 0 line direction control.
SDMMC0_DAT2_DIR	GPIO0 GPIO15	A11 A6	O	VDD_IO	SD/MMC0. Data 2 line direction control.
SDMMC0_DAT31_DIR	GPIO1 GPIO29 GPIO46	B12 P19 D5	O	VDD_IO	SD/MMC0. Data lines 3:1 direction control.
SDMMC0_DATA_0	-	R16	I/O	VDD_IO	SD/MMC0. Data line 0.
SDMMC0_DATA_1	-	P16	I/O	VDD_IO	SD/MMC0. Data line 1.
SDMMC0_DATA_2	-	P17	I/O	VDD_IO	SD/MMC0. Data line 2.
SDMMC0_DATA_3	-	R17	I/O	VDD_IO	SD/MMC0. Data line 3.
SDMMC0_DATA_4	GPIO2 GPIO36	C12 T17	I/O	VDD_IO	SD/MMC0. Data line 4.
SDMMC0_DATA_5	GPIO3 GPIO37	D12 T16	I/O	VDD_IO	SD/MMC0. Data line 5.
SDMMC0_DATA_6	GPIO4 GPIO38	C13 T18	I/O	VDD_IO	SD/MMC0. Data line 6.
SDMMC0_DATA_7	GPIO5 GPIO39	B13 R19	I/O	VDD_IO	SD/MMC0. Data line 7.
SDMMC0_FBCLK	GPIO27	N17	I	VDD_IO	SD/MMC0. Feedback clock line.
SDMMC0_PWR	GPIO28	M19	O	VDD_IO	SD/MMC0. Power enable.
SDMMC1_CLK	GPIO1 GPIO9	B12 A8	O	VDD_IO	SD/MMC1. Clock line.
SDMMC1_CMD	GPIO0 GPIO8	A11 A9	I/O	VDD_IO	SD/MMC1. Command line.
SDMMC1_CMDDIR	GPIO47	E3	O	VDD_IO	SD/MMC1. Command line direction line.
SDMMC1_DAT0_DIR	GPIO6	E2	O	VDD_IO	SD/MMC1. Data 0 line direction control.
SDMMC1_DAT2_DIR	GPIO49	F5	O	VDD_IO	SD/MMC1. Data 2 line direction control.
SDMMC1_DAT31_DIR	GPIO7 GPIO48	B10 E4	O	VDD_IO	SD/MMC1. Data lines 3:1 direction control.
SDMMC1_DATA_0	GPIO2 GPIO10	C12 C8	I/O	VDD_IO	SD/MMC1. Data line 0.
SDMMC1_DATA_1	GPIO3 GPIO11	D12 D9	I/O	VDD_IO	SD/MMC1. Data line 1.

Table 8. SD MMC Signals (continued)

Name	GPIOs	Balls	DIR	Power Domain	Description
SDMMC1_DATA_2	GPIO4 GPIO12	C13 B9	I/O	VDD_IO	SD/MMC1. Data line 2.
SDMMC1_DATA_3	GPIO5 GPIO13	B13 B8	I/O	VDD_IO	SD/MMC1. Data line 3.

3.1.7 General Purpose ADCs

Table 9. General Purpose ADC

Name	GPIOs	Balls	DIR	Power Domain	Description
ADC2_AIN0_XP	-	H17	I	VDD_IO	ADC2 (SAR) CH 0/Touch screen panel signal XP.(1)
ADC2_AIN1_XN	-	J19	I	VDD_IO	ADC2 (SAR) CH 1/Touch screen panel signal XN.(1)
ADC2_AIN2_YP	-	G17	I	VDD_IO	ADC2 (SAR) CH 2/Touch screen panel signal YP.(1)
ADC2_AIN3_YN	-	G16	I	VDD_IO	ADC2 (SAR) CH3/Touch screen panel signal YN.(1)
ADC2_AIN4	-	E19	I	VDD_IO	ADC2 (SAR) CH4.
ADC2_AIN5	-	H16	I	VDD_IO	ADC2 (SAR) CH5.
ADC2_AIN6	-	E17	I	VDD_IO	ADC2 (SAR) CH6.
ADC2_AIN7	-	E18	I	VDD_IO	ADC2 (SAR) CH7.
ADC2_AIN8	-	J18	I	VDD_IO	ADC2 (SAR) CH8.
ADC2_AIN9	-	E16	I	VDD_IO	ADC2 (SAR) CH9.

1. Touch screen controller only available in STA109x.

3.1.8 USB Host and Dual Role

Table 10. USB Signals

Name	GPIOs	Balls	DIR	Power Domain	Description
USB_BGEXT	-	K14	T	VDD_IO	Test signal. Leave it unconnected.
USB_REXT	-	M18	P	USBx_VDD3V3	Connect to GND with a 3 kOhm 1% resistor.
USB0_DN	-	L18	I/O	USB0_VDD3V3	USB0. Differential line D-.
USB0_DP	-	L19	I/O	USB0_VDD3V3	USB0. Differential line D+.
USB1_DN	-	K18	I/O	USB1_VDD3V3	USB1. Differential line D-.
USB1_DP	-	K19	I/O	USB1_VDD3V3	USB1. Differential line D+.
USB1_DRVVBUS	GPIO26 M3_GPIO12	N16 C11	O	VDD_IO	It can be used to enable the VBUS when USB1 is in host mode

3.1.9 Power

Table 11. Power signals

Name	GPIOs	Balls	DIR	Power Domain	Description
ADC0_1_AGND	-	J14	P	Power	ADC0 and ADC1 analog 3.3V supply ground.
ADC0_1_AVDD	-	H14	P	Power	ADC0 and ADC1 analog 3.3V supply.
ADC0_1_VCM	-	J17	P	Power	ADC0, ADC1 common voltage. Connect 10nF and 10uF capacitors connected to GND.
ADC0_1_VRFN	-	J16	P	Power	ADC0 and ADC1 Vref negative. Connect it to GND.
ADC0_1_VRFP	-	J15	P	Power	ADC0 and ADC1 Vref positive. Connect 10nF and 10uF capacitors connected to GND.
ADC2_AGND	-	F13	P	Power	ADC2 (SAR) analog 3.3V supply ground.
ADC2_AVDD	-	G13	P	Power	ADC2 (SAR) analog 3.3V supply.
ADC2_VREFN	-	E12	P	Power	ADC2 (SAR) Vref negative. Connect it to GND.
ADC2_VREFP	-	F15	P	Power	ADC2 Vref positive. Connect it to 3.3V.
COMP0	-	L16	P	Power	Compensation cell input. Connect to external 121Kohm res. 1% to GND.
DAC_AGND	-	F14	P	Power	DAC analog supply ground.
DAC_AVDD	-	G15	P	Power	DAC analog 3.3V supply.
DAC_I/O_AGND	-	G14	P	Power	DAC0, DAC1, DAC2 I/O analog 3.3V supply.

Table 11. Power signals (continued)

Name	GPIOs	Balls	DIR	Power Domain	Description
DAC_I/O_AVDD	-	H15	P	Power	DAC0, DAC1, DAC2 I/O analog 3.3V supply ground.
DAC_VCOM	-	D17	P	Power	DAC0, DAC1, DAC2 common voltage. Connect 10nF and 10uF capacitors connected to DAC_AGND.
DAC_VHI	-	B17	P	Power	DAC0, DAC1, DAC2 analog positive reference. Connect 10nF and 10uF capacitors to DAC_AGND.
DAC_VLO	-	C17	P	Power	DAC0, DAC1, DAC2 analog negative reference. Connect it to DAC_AGND.
GND	-	A19, F11, F12, G7, G8, G9, G10, G11, G12, H7, H8, H9, H10, H11, H12, J7, J8, J9, J10, J11, J12, K7, K8, K9, K10, K11, K12, L7, L8, L9, L10, L11, L12, W1,W19	P	Power	GND
PLL_GND	-	M15	P	Power	Analog ground for PLL.
OSC32K_GND	-	F10	P	Power	Analog ground for 32K oscillator.
MIC_BIAS	-	E15	O	VDD_IO	Bias voltage for Microphone. 2.5V +/- 5%.
PLL_VDD2.5V	-	M16	P	Power	2.5V LDO (PLL) output voltage. Connect it to a 4.7uF capacitor to GND.
PLL_VREG3.3V	-	N15	P	Power	LDO 2.5V (PLL) 3.3V supply. Connect it to VDDIO.
USB_1.1VREG	-	K16	P	Power	LDO 1.1V (USB) output. Connect it to 4.7 uF capacitor to GND.
USB_1.8VREG	-	K15	P	Power	LDO 1.8V (USB) output. Connect it to 4.7 uF capacitor to GND.
USB_KELVIN_TERM	-	L15	T	VDD_IO	Test signal. Leave it unconnected.

Table 11. Power signals (continued)

Name	GPIOs	Balls	DIR	Power Domain	Description
USB_KELVIN_TERM	-	L15	T	VDD_IO	Test signal. Leave it unconnected.
USB_VCOD1V48	GPIO28	M19	T	VDD_IO	Test signal. Not used in the application.
USB_VREG3V3_1V1	-	H13	P	Power	LDO 1.1V (USB) 3.3V supply.
USB_VREG3V3_1V8	-	J13	P	Power	LDO 1.8V (USB) 3.3V supply.
USB0_AGND	-	K17	P	Power	USB0 analog supply ground.
USB0_VDD3V3	-	L14	P	Power	USB0 3.3V supply.
USB1_AGND	-	L17	P	Power	USB1 analog supply ground.
USB1_VDD3V3	-	K13	P	Power	USB1 3.3V supply.
VDD	-	E9, E10, F6, F9, G5, H5, J5, K5, L5, M5, N5, N6, N10, N11, N12, N13	P	Power	1.2V switchable domain digital power supply.
VDD_IO	-	E6, E7, E8, F7, F8, G6, H6, J6, K6, L6, L13, M6, M7, M8, M9, M10, M11, M12, M13, M14, N7, N8, N9	P	Power	3.3V Digital I/O supply.
VDD_IO_ON	-	E13	P	Power	3.3V always on digital power supply.
VDD_ON_VREG	-	E14	P	Power	LDO 1.2V (always on domain). Connect it to 2.2nF capacitor.
VREG_BYPASS	-	M17	T	VDD_IO	Test signal. Connect it to GND on the application board.
XOSC_VDD	-	M16	P	Power	To be shorted with PLL_VDD_2.5V. Only on QFP package.

3.1.10 Memory interfaces (SDRAM, NAND, NOR)

Table 12. Memory signals

Name	GPIOs	Balls	DIR	Power Domain	Description
FSMC_ADVn	GPIO83 GPIO140(1)	W6 U6	O	VDD_IO	FSMC Address Valid. It indicates that address is valid on SMADQ bus (active low) .
FSMC_BLn_0	GPIO88 GPIO145(1)	W16 T8	O	VDD_IO	FSMC Byte Lane 0 enable not. Lower byte lane enable for SRAM memories (active LOW)
FSMC_BLn_1	GPIO67 GPIO146(1)	W18 U8	O	VDD_IO	FSMC Byte Lane 1 enable not. Upper byte lane enable for SRAM memories (active LOW)
FSMC_BUSYn	GPIO79 GPIO100	W2 H3	I	VDD_IO	FSMC Busy. Busy signal for NAND flash memory (active low).
FSMC_CLK	GPIO78	V2	O	VDD_IO	FSMC. Clock for synchronous SRAM and NOR access.
FSMC_DACK	GPIO80	V3	I	VDD_IO	FSMC. External DMA transfer request acknowledge.
FSMC_DREQ	GPIO79	W2	O	VDD_IO	FSMC. External DMA transfer request.
FSMC_NAND_CS0N	GPIO105	J4	O	VDD_IO	FSMC. NAND chip select 256MB address space from 0xC000000 to 0xCFFFFFFF.
FSMC_NOR_CS0N	GPIO69 GPIO144(1)	U19 U3	O	VDD_IO	FSMC. NOR/SRAM chip select 0. 64MB address space from 0x80000000 to 0x83FFFFFF.
FSMC_NOR_CS1N	GPIO86 GPIO149(1)	V7 P6	O	VDD_IO	FMSC. NOR/SRAM chip select 1. 64MB address space from 0x84000000 to 0x87FFFFFF.
FSMC_OEn	GPIO70 GPIO101	T19 H4	O	VDD_IO	FSMC. Output enable signal (active low).
FSMC_RSTn	GPIO73	W4	O	VDD_IO	FSMC. Reset signal for NOR-Flash Memories (active LOW). This signal is an output and is used to reset or control the power-down of the flash memory devices.
FSMC_SMAD0	GPIO68	U18	O	VDD_IO	FSMC. Address line 0.
FSMC_SMAD1	GPIO104	J3	O	VDD_IO	FSMC. Address line 1.
FSMC_SMAD10	GPIO77	V1	O	VDD_IO	FSMC. Address line 10.
FSMC_SMAD11	GPIO51	W7	O	VDD_IO	FSMC. Address line 11.
FSMC_SMAD12	GPIO50	V8	O	VDD_IO	FSMC. Address line 12.
FSMC_SMAD13	GPIO54	W8	O	VDD_IO	FSMC. Address line 13.
FSMC_SMAD14	GPIO64	V9	O	VDD_IO	FSMC. Address line 14.

Table 12. Memory signals (continued)

Name	GPIOs	Balls	DIR	Power Domain	Description
FSMC_SMAD15	GPIO63	W9	O	VDD_IO	FSMC. Address line 15.
FSMC_SMAD16/CLE	GPIO58 GPIO104	V12 J3	O	VDD_IO	FSMC. Address line 16 - NAND CLE .
FSMC_SMAD17/ALE	GPIO59 GPIO103	W11 J2	O	VDD_IO	FSMC. Address line 17 - NAND ALE.
FSMC_SMAD18	GPIO60 GPIO137(1)	V11 T7	O	VDD_IO	FSMC. Address line 18.
FSMC_SMAD19	GPIO82 GPIO138(1)	V6 U7	O	VDD_IO	FSMC. Address line 19.
FSMC_SMAD2	GPIO103	J2	O	VDD_IO	FSMC. Address line 2.
FSMC_SMAD20	GPIO81 GPIO139(1)	W5 T6	O	VDD_IO	FSMC. Address line 20.
FSMC_SMAD21	GPIO74 GPIO141(1)	V4 T5	O	VDD_IO	FSMC. Address line 21.
FSMC_SMAD22	GPIO62 GPIO142(1)	V10 R6	O	VDD_IO	FSMC. Address line 22.
FSMC_SMAD23	GPIO61 GPIO143(1)	W10 U4	O	VDD_IO	FSMC. Address line 23.
FSMC_SMAD24	GPIO66 GPIO147(1)	V19 P5	O	VDD_IO	FSMC. Address line 24.
FSMC_SMAD25	GPIO49 GPIO65 GPIO150(1)	F5 V18 U5	O	VDD_IO	FSMC. Address line 25.
FSMC_SMAD3	GPIO102	J1	O	VDD_IO	FSMC. Address line 3.
FSMC_SMAD4	GPIO101	H4	O	VDD_IO	FSMC. Address line 4.
FSMC_SMAD5	GPIO100	H3	O	VDD_IO	FSMC. Address line 5.
FSMC_SMAD6	GPIO98	H1	O	VDD_IO	FSMC. Address line 6.
FSMC_SMAD7	GPIO97	G4	O	VDD_IO	FSMC. Address line 7.
FSMC_SMAD8	GPIO96	G3	O	VDD_IO	FSMC. Address line 8.
FSMC_SMAD9	GPIO83	W6	O	VDD_IO	FSMC. Address line 9.
FSMC_SMADQ_0	GPIO71 GPIO97	V17 G4	I/O	VDD_IO	FSMC. Multiplexed address/data line 0.
FSMC_SMADQ_1	GPIO85 GPIO96	V16 G3	I/O	VDD_IO	FSMC. Multiplexed address/data line 1.
FSMC_SMADQ_10	GPIO81 GPIO154(1)	W5 R8	I/O	VDD_IO	FSMC. Multiplexed address/data line 10.
FSMC_SMADQ_11	GPIO74 GPIO153(1)	V4 P8	I/O	VDD_IO	FSMC. Multiplexed address/data line 11.

Table 12. Memory signals (continued)

Name	GPIOs	Balls	DIR	Power Domain	Description
FSMC_SMADQ_12	GPIO62 GPIO152(1)	V10 R7	I/O	VDD_IO	FSMC. Multiplexed address/data line 12.
FSMC_SMADQ_13	GPIO61 GPIO151(1)	W10 P7	I/O	VDD_IO	FSMC. Multiplexed address/data line 13.
FSMC_SMADQ_14	GPIO66 GPIO150(1)	V19 U5	I/O	VDD_IO	FSMC. Multiplexed address/data line 14.
FSMC_SMADQ_15	GPIO65 GPIO149(1)	V18 P6	I/O	VDD_IO	FSMC. Multiplexed address/data line 15.
FSMC_SMADQ_2	GPIO87 GPIO95	V15 G2	I/O	VDD_IO	FSMC. Multiplexed address/data line 2.
FSMC_SMADQ_3	GPIO52 GPIO94	W14 G1	I/O	VDD_IO	FSMC. Multiplexed address/data line 3.
FSMC_SMADQ_4	GPIO53 GPIO93	V14 F4	I/O	VDD_IO	FSMC. Multiplexed address/data line 4.
FSMC_SMADQ_5	GPIO55 GPIO92	W13 F3	I/O	VDD_IO	FSMC. Multiplexed address/data line 5.
FSMC_SMADQ_6	GPIO56 GPIO91	V13 F2	I/O	VDD_IO	FSMC. Multiplexed address/data line 6.
FSMC_SMADQ_7	GPIO57 GPIO90	W12 F1	I/O	VDD_IO	FSMC. Multiplexed address/data line 7.
FSMC_SMADQ_8	GPIO48 GPIO72	E4 W17	I/O	VDD_IO	FSMC. Multiplexed address/data line 8.
FSMC_SMADQ_9	GPIO47 GPIO89	E3 W15	I/O	VDD_IO	FSMC. Multiplexed address/data line 9.
FSMC_WAITn	GPIO76 GPIO148(1)	U1 R5	I	VDD_IO	FSMC Wait. Wait signal for NOR flash memory (active low).
FSMC_WEn	GPIO84 GPIO102	V5 J1	O	VDD_IO	FSMC Write Enable. For SRAM/NOR-Flash and NAND-Flash (active low).
FSMC_WPn	GPIO75 GPIO98	W3 H1	O	VDD_IO	FSMC Write protect. Used for NOR-Flash memories (active LOW).
SDRAM_ADD_0	GPIO64	V9	O	VDD_IO	SDR SDRAM. Address line 0.
SDRAM_ADD_1	GPIO63	W9	O	VDD_IO	SDR SDRAM. Address line 1.
SDRAM_ADD_10	GPIO54	W8	O	VDD_IO	SDR SDRAM. Address line 10.
SDRAM_ADD_11	GPIO53	V14	O	VDD_IO	SDR SDRAM. Address line 11.
SDRAM_ADD_12	GPIO52	W14	O	VDD_IO	SDR SDRAM. Address line 12.
SDRAM_ADD_2	GPIO62	V10	O	VDD_IO	SDR SDRAM. Address line 2.

Table 12. Memory signals (continued)

Name	GPIOs	Balls	DIR	Power Domain	Description
SDRAM_ADD_3	GPIO61	W10	O	VDD_IO	SDR SDRAM. Address line 3.
SDRAM_ADD_4	GPIO60	V11	O	VDD_IO	SDR SDRAM. Address line 4.
SDRAM_ADD_5	GPIO59	W11	O	VDD_IO	SDR SDRAM. Address line 5.
SDRAM_ADD_6	GPIO58	V12	O	VDD_IO	SDR SDRAM. Address line 6.
SDRAM_ADD_7	GPIO57	W12	O	VDD_IO	SDR SDRAM. Address line 7.
SDRAM_ADD_8	GPIO56	V13	O	VDD_IO	SDR SDRAM. Address line 8.
SDRAM_ADD_9	GPIO55	W13	O	VDD_IO	SDR SDRAM. Address line 9.
SDRAM_BA_0	GPIO51	W7	O	VDD_IO	SDR SDRAM. Bank address 0 line.
SDRAM_BA_1	GPIO50	V8	O	VDD_IO	SDR SDRAM. Bank address 1 line.
SDRAM_CASn	GPIO82	V6	O	VDD_IO	SDR SDRAM. Column address strobe.
SDRAM_CKE	GPIO87	V15	O	VDD_IO	SDR SDRAM. Clock enable.
SDRAM_CLK	GPIO89	W15	O	VDD_IO	SDR SDRAM. Clock signal.
SDRAM_CS0n	GPIO86	V7	O	VDD_IO	SDR SDRAM. Chip select 0.
SDRAM_CS1n	GPIO28 GPIO136(1)	M19 U17	O	VDD_IO	SDR SDRAM. Chip select 1.
SDRAM_Data_0	GPIO80	V3	I/O	VDD_IO	SDR SDRAM. Data line 0.
SDRAM_Data_1	GPIO79	W2	I/O	VDD_IO	SDR SDRAM. Data line 1.
SDRAM_Data_10	GPIO70	T19	I/O	VDD_IO	SDR SDRAM. Data line 10.
SDRAM_Data_11	GPIO69	U19	I/O	VDD_IO	SDR SDRAM. Data line 11.
SDRAM_Data_12	GPIO68	U18	I/O	VDD_IO	SDR SDRAM. Data line 12.
SDRAM_Data_13	GPIO67	W18	I/O	VDD_IO	SDR SDRAM. Data line 13.
SDRAM_Data_14	GPIO66	V19	I/O	VDD_IO	SDR SDRAM. Data line 14.
SDRAM_Data_15	GPIO65	V18	I/O	VDD_IO	SDR SDRAM. Data line 15.
SDRAM_Data_16(1)	GPIO137(1)	T7	I/O	VDD_IO	SDR SDRAM. Data line 16.
SDRAM_Data_17(1)	GPIO138(1)	U7	I/O	VDD_IO	SDR SDRAM. Data line 17.
SDRAM_Data_18(1)	GPIO139(1)	T6	I/O	VDD_IO	SDR SDRAM. Data line 18.
SDRAM_Data_19(1)	GPIO140(1)	U6	I/O	VDD_IO	SDR SDRAM. Data line 19.
SDRAM_Data_2	GPIO78	V2	I/O	VDD_IO	SDR SDRAM. Data line 2.
SDRAM_Data_20(1)	GPIO141(1)	T5	I/O	VDD_IO	SDR SDRAM. Data line 20.
SDRAM_Data_21(1)	GPIO142(1)	R6	I/O	VDD_IO	SDR SDRAM. Data line 21.
SDRAM_Data_22(1)	GPIO143(1)	U4	I/O	VDD_IO	SDR SDRAM. Data line 22.
SDRAM_Data_23(1)	GPIO144(1)	U3	I/O	VDD_IO	SDR SDRAM. Data line 23.
SDRAM_Data_24(1)	GPIO147(1)	P5	I/O	VDD_IO	SDR SDRAM. Data line 24.
SDRAM_Data_25(1)	GPIO148(1)	R5	I/O	VDD_IO	SDR SDRAM. Data line 25.

Table 12. Memory signals (continued)

Name	GPIOs	Balls	DIR	Power Domain	Description
SDRAM_Data_26(1)	GPIO149(1)	P6	I/O	VDD_IO	SDR SDRAM. Data line 26.
SDRAM_Data_27(1)	GPIO150(1)	U5	I/O	VDD_IO	SDR SDRAM. Data line 27.
SDRAM_Data_28(1)	GPIO151(1)	P7	I/O	VDD_IO	SDR SDRAM. Data line 28.
SDRAM_Data_29(1)	GPIO152(1)	R7	I/O	VDD_IO	SDR SDRAM. Data line 29
SDRAM_Data_3	GPIO77	V1	I/O	VDD_IO	SDR SDRAM. Data line 3.
SDRAM_Data_30(1)	GPIO153(1)	P8	I/O	VDD_IO	SDR SDRAM. Data line 30.
SDRAM_Data_31(1)	GPIO154(1)	R8	I/O	VDD_IO	SDR SDRAM. Data line 31.
SDRAM_Data_4	GPIO76	U1	I/O	VDD_IO	SDR SDRAM. Data line 4.
SDRAM_Data_5	GPIO75	W3	I/O	VDD_IO	SDR SDRAM. Data line 5.
SDRAM_Data_6	GPIO74	V4	I/O	VDD_IO	SDR SDRAM. Data line 6.
SDRAM_Data_7	GPIO73	W4	I/O	VDD_IO	SDR SDRAM. Data line 7.
SDRAM_Data_8	GPIO72	W17	I/O	VDD_IO	SDR SDRAM. Data line 8.
SDRAM_Data_9	GPIO71	V17	I/O	VDD_IO	SDR SDRAM. Data line 9.
SDRAM_DQM0	GPIO84	V5	O	VDD_IO	SDR SDRAM. Data mask 0, data[7:0].
SDRAM_DQM1	GPIO85	V16	O	VDD_IO	SDR SDRAM. Data mask 1, data[15:8].
SDRAM_DQM2(1)	GPIO145(1)	T8	O	VDD_IO	SDR SDRAM. Data mask 2, data[23:16].
SDRAM_DQM3(1)	GPIO146(1)	U8	O	VDD_IO	SDR SDRAM. Data mask 3, data[31:24].
SDRAM_FBCLK	GPIO88	W16	I	VDD_IO	SDR SDRAM. Feedback clock line. Connect it to SDRAM device clock.
SDRAM_RASn	GPIO83	W6	O	VDD_IO	SDR SDRAM. Row address strobe
SDRAM_WEn	GPIO81	W5	O	VDD_IO	SDR SDRAM. Write enable strobe.
SQI_CE0n	-	D3	O	VDD_IO	SQI. Chip select 0 (active low).
SQI_CE1n	GPIO99	H2	O	VDD_IO	SQI. Chip select 1 (active low).
SQI_FDBSCK	GPIO6 GPIO99	E2 H2	I	VDD_IO	SQI. Feedback clock. It must be used for clock frequencies above 60MHz.
SQI_SCK	-	D1	O	VDD_IO	SQI. Clock line.
SQI_SIO0	-	D4	I/O	VDD_IO	SQI. Data line 0.
SQI_SIO1	-	D2	I/O	VDD_IO	SQI. Data line 1.
SQI_SIO2	-	E1	I/O	VDD_IO	SQI. Data line 2.

1. Only available on STA109x.

3.1.11 Display - Only available in STA109x

Table 13. Display signals

Name	GPIOs	Balls	DIR	Power Domain	Description
CLCD_COLOR0	GPIO136	U17	O	VDD_IO	LCD. Display data line 0.
CLCD_COLOR1	GPIO135	U16	O	VDD_IO	LCD. Display data line 1.
CLCD_COLOR10	GPIO126	U14	O	VDD_IO	LCD. Display data line 10.
CLCD_COLOR11	GPIO125	P13	O	VDD_IO	LCD. Display data line 11.
CLCD_COLOR12	GPIO124	R13	O	VDD_IO	LCD. Display data line 12.
CLCD_COLOR13	GPIO123	T13	O	VDD_IO	LCD. Display data line 13.
CLCD_COLOR14	GPIO122	U13	O	VDD_IO	LCD. Display data line 14.
CLCD_COLOR15	GPIO121	P12	O	VDD_IO	LCD. Display data line 15.
CLCD_COLOR16	GPIO29 GPIO107	P19 T11	O	VDD_IO	LCD. Display data line 16.
CLCD_COLOR17	GPIO27 GPIO108	N17 R11	O	VDD_IO	LCD. Display data line 17.
CLCD_COLOR2	GPIO134	P15	O	VDD_IO	LCD. Display data line 2.
CLCD_COLOR3	GPIO133	T15	O	VDD_IO	LCD. Display data line 3.
CLCD_COLOR4	GPIO132	R15	O	VDD_IO	LCD. Display data line 4.
CLCD_COLOR5	GPIO131	U15	O	VDD_IO	LCD. Display data line 5.
CLCD_COLOR6	GPIO130	N14	O	VDD_IO	LCD. Display data line 6.
CLCD_COLOR7	GPIO129	P14	O	VDD_IO	LCD. Display data line 7.
CLCD_COLOR8	GPIO128	R14	O	VDD_IO	LCD. Display data line 8.
CLCD_COLOR9	GPIO127	T14	O	VDD_IO	LCD. Display data line 9.
CLCD_DE	GPIO120	R12	O	VDD_IO	LCD. Display data enable line.
CLCD_HSYNCH	GPIO119	T12	O	VDD_IO	LCD. Display horizontal synchronization line.
CLCD_PIXCLK	GPIO117	P11	O	VDD_IO	LCD. Display pixel clock line.
CLCD_VSYNCH	GPIO118	U12	O	VDD_IO	LCD. Display vertical synchronization line.

3.1.12 VIP - Only available in STA109x

Table 14. Video input signals

Name	GPIOs	Balls	DIR	Power Domain	Description
VIP_DAT0	GPIO116	T9	O	VDD_IO	Video Input Port. Data 0.
VIP_DAT1	GPIO115	R9	O	VDD_IO	Video Input Port. Data 1
VIP_DAT2	GPIO114	P9	O	VDD_IO	Video Input Port. Data 2.
VIP_DAT3	GPIO113	U10	O	VDD_IO	Video Input Port. Data 3.
VIP_DAT4	GPIO112	T10	O	VDD_IO	Video Input Port. Data 4.
VIP_DAT5	GPIO111	R10	O	VDD_IO	Video Input Port. Data 5.
VIP_DAT6	GPIO110	P10	O	VDD_IO	Video Input Port. Data 6.
VIP_DAT7	GPIO109	U11	O	VDD_IO	Video Input Port. Data 7.
VIP_HSYNCH	GPIO107	T11	O	VDD_IO	Video Input Port. Horizontal synchronization pulse signal.
VIP_PIXCLK	GPIO106	U9	O	VDD_IO	Video Input Port. Pixel clock.
VIP_VSYNCH	GPIO108	R11	O	VDD_IO	Video Input Port. Vertical synchronization pulse signal.

3.1.13 Debug

Table 15. Debug signals

Name	GPIOs	Balls	DIR	Power Domain	Description
ETM_CLK	GPIO13 GPIO103 GPIO119(1)	B8 J2 T12	O	VDD_IO	ETM. TRACE clock output. The trace port must be sampled on both edges of this clock. There is no requirement for this to be linked to the core clock.
ETM_CTL	GPIO14 GPIO104 GPIO120(1)	A7 J3 R12	O	VDD_IO	ETM. ETM control line. This signal indicates whether trace can be stored this cycle, in conjunction with TRACEDATA[0]. This signal does not have to be stored.
ETM_D0	GPIO0 GPIO90 GPIO121(1)	A11 F1 P12	O	VDD_IO	ETM. TRACEDATA0.
ETM_D1	GPIO1 GPIO91 GPIO122(1)	B12 F2 U13	O	VDD_IO	ETM. TRACEDATA1.
ETM_D10	GPIO10 GPIO100 GPIO131(1)	C8 H3 U15	O	VDD_IO	ETM. TRACEDATA10.

Table 15. Debug signals (continued)

Name	GPIOs	Balls	DIR	Power Domain	Description
ETM_D11	GPIO11 GPIO101 GPIO132(1)	D9 H4 R15	O	VDD_IO	ETM. TRACEDATA11.
ETM_D12	GPIO12 GPIO102 GPIO133(1)	B9 J1 T15	O	VDD_IO	ETM. TRACEDATA12.
ETM_D13	GPIO16 GPIO30 GPIO134(1)	C9 M1 P15	O	VDD_IO	ETM. TRACEDATA13.
ETM_D14	GPIO17 GPIO31 GPIO135(1)	D10 M4 U16	O	VDD_IO	ETM. TRACEDATA14.
ETM_D15	GPIO19 GPIO33 GPIO136(1)	C10 M2 U17	O	VDD_IO	ETM. TRACEDATA15.
ETM_D2	GPIO2 GPIO92 GPIO123(1)	C12 F3 T13	O	VDD_IO	ETM. TRACEDATA2.
ETM_D3	GPIO3 GPIO93 GPIO124(1)	D12 F4 R13	O	VDD_IO	ETM. TRACEDATA3.
ETM_D4	GPIO4 GPIO94 GPIO125(1)	C13 G1 P13	O	VDD_IO	ETM. TRACEDATA4.
ETM_D5	GPIO5 GPIO95 GPIO126(1)	B13 G2 U14	O	VDD_IO	ETM. TRACEDATA5.
ETM_D6	GPIO6 GPIO96 GPIO127(1)	E2 G3 T14	O	VDD_IO	ETM. TRACEDATA6.
ETM_D7	GPIO7 GPIO97 GPIO128(1)	B10 G4 R14	O	VDD_IO	ETM. TRACEDATA7.
ETM_D8	GPIO8 GPIO98 GPIO129(1)	A9 H1 P14	O	VDD_IO	ETM. TRACEDATA8.
ETM_D9	GPIO9 GPIO99 GPIO130(1)	A8 H2 N14	O	VDD_IO	ETM. TRACEDATA9.
FORCE_CS_HIGH	GPIO105	J4	O	VDD_IO	Test Signal. It must be driven High when ETM is enabled, to prevent conflict with NAND.
JTAG_TCK		T3	I	VDD_IO	JTAG. Test clock.

Table 15. Debug signals (continued)

Name	GPIOs	Balls	DIR	Power Domain	Description
JTAG_TDI		T1	I	VDD_IO	JTAG. Test Data In.
JTAG_TDO		T2	O	VDD_IO	JTAG. Test Data Output.
JTAG_TMS		T4	I	VDD_IO	JTAG. Test Mode Select.
JTAG_TRSTn		U2	I	VDD_IO	JTAG. TRSTn. If the Debug Port is not used, the JTAG_TRSTn can be left unconnected (internal pull-down).
JTAG1_TCK	GPIO109(1) S_GPIO4	U11 P4	I	VDD_IO	JTAG1. Test Clock. This is an optional JTAG interface, not enabled by default. If enabled, it connects to Cortex-R4 only and allows the parallel debugging of the Cortex-R4 and Cortex-M3 processors without chaining them but using two separate JTAG interfaces. If JTAG1 is not enabled, the debug interface is controlled through the JTAG dedicated interface only.
JTAG1_TDI	GPIO118(1) S_GPIO1	U12 D7	I	VDD_IO	JTAG1. Test Data In. This is an optional JTAG interface, not enabled by default. If enabled, it connects to Cortex-R4 only and allows the parallel debugging of the Cortex-R4 and Cortex-M3 processors without chaining them but using two separate JTAG interfaces. If JTAG1 is not enabled, the debug interface is controlled through the JTAG dedicated interface only.
JTAG1_TDO	GPIO117(1) S_GPIO0	P11 D6	O	VDD_IO	JTAG1. Test Data Out. This is an optional JTAG interface, not enabled by default. If enabled, it connects to Cortex-R4 only and allows the parallel debugging of the Cortex-R4 and Cortex-M3 processors without chaining them but using two separate JTAG interfaces. If JTAG1 is not enabled, the debug interface is controlled through the JTAG dedicated interface only.

Table 15. Debug signals (continued)

Name	GPIOs	Balls	DIR	Power Domain	Description
JTAG1_TMS	GPIO107[1] S_GPIO2	T11 C5	I	VDD_IO	JTAG1. Test Mode Select. This is an optional JTAG interface, not enabled by default. If enabled, it connects to Cortex-R4 only and allows the parallel debugging of the Cortex-R4 and Cortex-M3 processors without chaining them but using two separate JTAG interfaces. If JTAG1 is not enabled, the debug interface is controlled through the JTAG dedicated interface only.
JTAG1_TRSTn	GPIO108[1] S_GPIO3	R11 A5	I	VDD_IO	JTAG1. Test Reset not. This is an optional JTAG interface, not enabled by default. If enabled, it connects to Cortex-R4 only and allows the parallel debugging of the Cortex-R4 and Cortex-M3 processors without chaining them but using two separate JTAG interfaces. If JTAG1 is not enabled, the debug interface is controlled through the JTAG dedicated interface only.

1. Only available on STA109x.

3.1.14 GPIO and alternate functions

Table 16. STA1080, STA1085 GPIO and alternate functions

GPIO	Ball	ALT A	ALT B	ALT C	DEBUG 0
GPIO0	A11	SDMMC1_CMD	SDMMC0_DAT2_DIR	SAI4_BCLK	ETM_D0
GPIO1	B12	SDMMC1_CLK	SDMMC0_DAT31_DIR	SAI4_FS	ETM_D1
GPIO2	C12	SDMMC1_DATA_0	SDMMC0_DATA_4	SAI4_TX0	ETM_D2
GPIO3	D12	SDMMC1_DATA_1	SDMMC0_DATA_5	SAI4_TX1	ETM_D3
GPIO4	C13	SDMMC1_DATA_2	SDMMC0_DATA_6	SAI4_TX2	ETM_D4
GPIO5	B13	SDMMC1_DATA_3	SDMMC0_DATA_7	SAI4_RX0	ETM_D5
GPIO6	E2	SQI_FDBSCK	CD_SS_MON_1	SDMMC1_DAT0_DIR	ETM_D6
GPIO7	B10	AUDIO_REFCLK	SAI2_RX/TX	SDMMC1_DAT31_DIR	ETM_D7
GPIO8	A9	SAI3_BCLK	SDMMC1_CMD	SAI4_RX2	ETM_D8
GPIO9	A8	SAI3_FS	SDMMC1_CLK	UART2_RX	ETM_D9
GPIO10	C8	SAI3_TX0	SDMMC1_DATA_0	EFT2_OCMP1	ETM_D10
GPIO11	D9	SAI3_TX1	SDMMC1_DATA_1	EFT2_ICAP1	ETM_D11
GPIO12	B9	SAI3_TX2	SDMMC1_DATA_2	UART2_TX	ETM_D12
GPIO13	B8	SAI3_RX0	SDMMC1_DATA_3	SAI4_RX1	ETM_CLK
GPIO14	A7	SAI3_RX1	SDMMC0_DAT0_DIR	I2C2_SCL	ETM_CTL
GPIO15	A6	SAI3_RX2	SDMMC0_DAT2_DIR	I2C2_SDA	-
GPIO16	C9	SAI2_BCLK	-	I2S2_BCLK	ETM_D13
GPIO17	D10	SAI2_FS	-	I2S2_FS	ETM_D14
GPIO18	D11	SAI2_RX/TX	SPDIF_RX	I2S2_RX	-
GPIO19	C10	SAI1_BCLK	SPI2_TXD	EFT2_OCMP0	ETM_D15
GPIO20	B11	SAI1_FS	SPI2_RXD	EFT2_OCMP1	-
GPIO21	A10	SAI1_RX	SPI2_SCK	EFT2_EXTCK	-
GPIO22	R1	EFT0_ICAP0	EFT0_EXTCK	SPI2_SS	-
GPIO23	R2	EFT0_ICAP1	SDMMC0_CMDDIR	SPI2_TXD	-
GPIO24	R3	EFT0_OCMP0	UART1_TX	SPI2_RXD	-
GPIO25	R4	EFT0_OCMP1	UART1_RX	SPI2_SCK	-
GPIO26	N16	EFT1_ICAP0	EFT1_EXTCK	USB1_DRVVBUS	-
GPIO27	N17	EFT1_ICAP1	SDMMC0_FBCLK	CLCD_COLOR17	-
GPIO28	M19	EFT1_OCMP0	SDMMC0_PWR	SDRAM_CS1n	USB_VCOD1V48
GPIO29	P19	EFT1_OCMP1	SDMMC0_DAT31_DIR	CLCD_COLOR16	-
GPIO30	M1	SPI1_SS	EFT0_EXTCK	I2C1_SCL	ETM_D13
GPIO31	M4	SPI1_TXD	EFT1_EXTCK	I2C1_SDA	ETM_D14
GPIO32	M3	SPI1_RXD	EFT1_OCMP1	UART3_TX	-

Table 16. STA1080, STA1085 GPIO and alternate functions (continued)

GPIO	Ball	ALT A	ALT B	ALT C	DEBUG 0
GPIO33	M2	SPI1_SCK	EFT1_OCMP0	UART3_RX	ETM_D15
GPIO34	B4	I2C1_SDA	UART1_TX	EFT1_ICAP0	-
GPIO35	B3	I2C1_SCL	UART1_RX	EFT1_ICAP1	-
GPIO36	T17	UART1_TX	SDMMC0_DATA_4	SDMMC1_DATA_4	-
GPIO37	T16	UART1_RX	SDMMC0_DATA_5	SDMMC1_DATA_5	-
GPIO38	T18	UART2_RX	SDMMC0_DATA_6	SDMMC1_DATA_6	-
GPIO39	R19	UART2_TX	SDMMC0_DATA_7	SDMMC1_DATA_7	-
GPIO40	B1	UART3_RX	UART1_CTS	EFT2_ICAP0	-
GPIO41	A2	UART3_TX	UART1_RTS	EFT2_ICAP1	-
GPIO42	A3	I2C1_SDA	EFT0_OCMP0	EFT0_ICAP0	-
GPIO43	A4	I2C1_SCL	EFT0_OCMP1	EFT0_ICAP1	-
GPIO44	B5	EFT2_ICAP0	EFT2_OCMP0	EFT2_EXTCK	-
GPIO45	C4	I2C2_SDA	SDMMC0_DAT0_DIR	CD_SS_MON_0	-
GPIO46	D5	I2C2_SCL	SDMMC0_DAT31_DIR	-	-
GPIO47	E3	FSMC_SMADQ_9	-	SDMMC1_CMDDIR	-
GPIO48	E4	FSMC_SMADQ_8	-	SDMMC1_DAT31_DIR	-
GPIO49	F5	FSMC_SMAD25	CLKOUT1	SDMMC1_DAT2_DIR	-
GPIO50	V8	SDRAM_BA_1	FSMC_SMAD12	-	-
GPIO51	W7	SDRAM_BA_0	FSMC_SMAD11	-	-
GPIO52	W14	SDRAM_Add_12	FSMC_SMADQ_3	-	-
GPIO53	V14	SDRAM_Add_11	FSMC_SMADQ_4	-	-
GPIO54	W8	SDRAM_Add_10	FSMC_SMAD13	-	-
GPIO55	W13	SDRAM_Add_9	FSMC_SMADQ_5	-	-
GPIO56	V13	SDRAM_Add_8	FSMC_SMADQ_6	-	-
GPIO57	W12	SDRAM_Add_7	FSMC_SMADQ_7	-	-
GPIO58	V12	SDRAM_Add_6	FSMC_SMAD16/CLE	-	-
GPIO59	W11	SDRAM_Add_5	FSMC_SMAD17/ALE	-	-
GPIO60	V11	SDRAM_Add_4	FSMC_SMAD18	-	-
GPIO61	W10	SDRAM_Add_3	FSMC_SMAD23	FSMC_SMADQ_13	-
GPIO62	V10	SDRAM_Add_2	FSMC_SMAD22	FSMC_SMADQ_12	-
GPIO63	W9	SDRAM_Add_1	FSMC_SMAD15	-	-
GPIO64	V9	SDRAM_Add_0	FSMC_SMAD14	-	-
GPIO65	V18	SDRAM_Data_15	FSMC_SMAD25	FSMC_SMADQ_15	-
GPIO66	V19	SDRAM_Data_14	FSMC_SMAD24	FSMC_SMADQ_14	-
GPIO67	W18	SDRAM_Data_13	FSMC_BLn_1	-	-

Table 16. STA1080, STA1085 GPIO and alternate functions (continued)

GPIO	Ball	ALT A	ALT B	ALT C	DEBUG 0
GPIO68	U18	SDRAM_Data_12	FSMC_SMAD0	-	-
GPIO69	U19	SDRAM_Data_11	FSMC_NOR_CS0n	-	-
GPIO70	T19	SDRAM_Data_10	FSMC_OEn	-	-
GPIO71	V17	SDRAM_Data_9	FSMC_SMADQ_0	-	-
GPIO72	W17	SDRAM_Data_8	FSMC_SMADQ_8	-	-
GPIO73	W4	SDRAM_Data_7	FSMC_RSTn	-	-
GPIO74	V4	SDRAM_Data_6	FSMC_SMAD21	FSMC_SMADQ_11	-
GPIO75	W3	SDRAM_Data_5	FSMC_WPn	-	-
GPIO76	U1	SDRAM_Data_4	FSMC_WAITn	-	-
GPIO77	V1	SDRAM_Data_3	FSMC_SMAD10	-	-
GPIO78	V2	SDRAM_Data_2	FSMC_CLK	-	-
GPIO79	W2	SDRAM_Data_1	FSMC_DREQ	FSMC_BUSYn	-
GPIO80	V3	SDRAM_Data_0	FSMC_DACK	-	-
GPIO81	W5	SDRAM_WEn	FSMC_SMAD20	FSMC_SMADQ_10	-
GPIO82	V6	SDRAM_CASn	FSMC_SMAD19	-	-
GPIO83	W6	SDRAM_RASn	FSMC_SMAD9	FSMC_ADVn	-
GPIO84	V5	SDRAM_DQM0	FSMC_WEn	-	-
GPIO85	V16	SDRAM_DQM1	FSMC_SMADQ_1	-	-
GPIO86	V7	SDRAM_CS0n	FSMC_NOR_CS1n	-	-
GPIO87	V15	SDRAM_CKE	FSMC_SMADQ_2	-	-
GPIO88	W16	SDRAM_FBCLK	FSMC_BLn_0	-	-
GPIO89	W15	SDRAM_CLK	FSMC_SMADQ_9	-	-
GPIO90	F1	FSMC_SMADQ_7	-	-	ETM_D0
GPIO91	F2	FSMC_SMADQ_6	-	-	ETM_D1
GPIO92	F3	FSMC_SMADQ_5	-	-	ETM_D2
GPIO93	F4	FSMC_SMADQ_4	-	-	ETM_D3
GPIO94	G1	FSMC_SMADQ_3	-	-	ETM_D4
GPIO95	G2	FSMC_SMADQ_2	-	-	ETM_D5
GPIO96	G3	FSMC_SMADQ_1	FSMC_SMAD8	-	ETM_D6
GPIO97	G4	FSMC_SMADQ_0	FSMC_SMAD7	-	ETM_D7
GPIO98	H1	FSMC_WPn	FSMC_SMAD6	-	ETM_D8
GPIO99	H2	SQI_CE1n	SPI2_SS	SQI_FDBSCK	ETM_D9
GPIO100	H3	FSMC_BUSYn	FSMC_SMAD5	-	ETM_D10
GPIO101	H4	FSMC_OEn	FSMC_SMAD4	-	ETM_D11
GPIO102	J1	FSMC_WEn	FSMC_SMAD3	-	ETM_D12

Table 16. STA1080, STA1085 GPIO and alternate functions (continued)

GPIO	Ball	ALT A	ALT B	ALT C	DEBUG 0
GPIO103	J2	FSMC_SMAD17/ALE	FSMC_SMAD2	-	ETM_CLK
GPIO104	J3	FSMC_SMAD16/CLE	FSMC_SMAD1	-	ETM_CTL
GPIO105	J4	FSMC_NAND_CS0n	-	-	FORCE_CS_HIGH
GPIO106	Not available				
GPIO107	Not available				
GPIO108	Not available				
GPIO109	Not available				
GPIO110	Not available				
GPIO111	Not available				
GPIO112	Not available				
GPIO113	Not available				
GPIO114	Not available				
GPIO115	Not available				
GPIO116	Not available				
GPIO117	Not available				
GPIO118	Not available				
GPIO119	Not available				
GPIO120	Not available				
GPIO121	Not available				
GPIO122	Not available				
GPIO123	Not available				
GPIO124	Not available				
GPIO125	Not available				
GPIO126	Not available				
GPIO127	Not available				
GPIO128	Not available				
GPIO129	Not available				
GPIO130	Not available				
GPIO131	Not available				
GPIO132	Not available				
GPIO133	Not available				
GPIO134	Not available				
GPIO135	Not available				
GPIO136	Not available				
GPIO137	Not available				

Table 16. STA1080, STA1085 GPIO and alternate functions (continued)

GPIO	Ball	ALT A	ALT B	ALT C	DEBUG 0
GPIO138	Not available				
GPIO139	Not available				
GPIO140	Not available				
GPIO141	Not available				
GPIO142	Not available				
GPIO143	Not available				
GPIO144	Not available				
GPIO145	Not available				
GPIO146	Not available				
GPIO147	Not available				
GPIO148	Not available				
GPIO149	Not available				
GPIO150	Not available				
GPIO151	Not available				
GPIO152	Not available				
GPIO153	Not available				
GPIO154	Not available				
S_GPIO0	D6	EFT3_ICAP0	EFT3_OCMP0	CAN1_RX(1)	JTAG1_TDO
S_GPIO1	D7	EFT3_ICAP1	EFT3_OCMP1	CAN1_TX(1)	JTAG1_TDI
S_GPIO2	C5	EFT4_ICAP0	EFT4_OCMP0	EFT4_EXTCK	JTAG1_TMS
S_GPIO3	A5	EFT4_ICAP1	EFT4_OCMP1	-	JTAG1_TRSTn
S_GPIO4	P4	EFT3_ICAP0	EFT3_OCMP0	EFT3_EXTCK	JTAG1_TCK
S_GPIO5	P3	EFT3_ICAP1	EFT3_OCMP1	EFT3_EXTCK	-
S_GPIO6	P2	EFT4_ICAP0	EFT4_OCMP0	EFT4_EXTCK	-
S_GPIO7	P1	EFT4_ICAP1	EFT4_OCMP1	-	-
M3_GPIO0	C15	WAKE0	-	-	-
M3_GPIO1	D15	WAKE1	-	-	-
M3_GPIO2	B16	WAKE2	-	-	-
M3_GPIO3	C16	WAKE3	-	-	-
M3_GPIO4	D16	WAKE4	-	-	-
M3_GPIO5	A16	WAKE5	-	-	-
M3_GPIO6	A17	WAKE6	-	-	-
M3_GPIO7	A18	WAKE7	-	-	-
M3_GPIO8	B7	CAN0_TX(1)	-	-	-
M3_GPIO9	C6	CAN0_RX(1)	-	-	-

Table 16. STA1080, STA1085 GPIO and alternate functions (continued)

GPIO	Ball	ALT A	ALT B	ALT C	DEBUG 0
M3_GPIO10	E5	-	-	-	-
M3_GPIO11	C1	-	-	-	-
M3_GPIO12	C11	USB1_DRVVBUS	-	-	-
M3_GPIO13	A12	CLKOUT0	-	DEBUGCFG	-
M3_GPIO14	C3	-	-	REMAP0	-
M3_GPIO15	B2	-	-	REMAP1	-

1. Only available for STA1085.

Table 17. STA1090, STA1095 GPIO and alternate functions

GPIO	Ball	ALT A	ALT B	ALT C	DEBUG 0
GPIO0	A11	SDMMC1_CMD	SDMMC0_DAT2_DIR	SAI4_BCLK	ETM_D0
GPIO1	B12	SDMMC1_CLK	SDMMC0_DAT31_DIR	SAI4_FS	ETM_D1
GPIO2	C12	SDMMC1_DATA_0	SDMMC0_DATA_4	SAI4_TX0	ETM_D2
GPIO3	D12	SDMMC1_DATA_1	SDMMC0_DATA_5	SAI4_TX1	ETM_D3
GPIO4	C13	SDMMC1_DATA_2	SDMMC0_DATA_6	SAI4_TX2	ETM_D4
GPIO5	B13	SDMMC1_DATA_3	SDMMC0_DATA_7	SAI4_RX0	ETM_D5
GPIO6	E2	SQI_FDBSCK	CD_SS_MON_1	SDMMC1_DAT0_DIR	ETM_D6
GPIO7	B10	AUDIO_REFCLK	SAI2_RX/TX	SDMMC1_DAT31_DIR	ETM_D7
GPIO8	A9	SAI3_BCLK	SDMMC1_CMD	SAI4_RX2	ETM_D8
GPIO9	A8	SAI3_FS	SDMMC1_CLK	UART2_RX	ETM_D9
GPIO10	C8	SAI3_TX0	SDMMC1_DATA_0	EFT2_OCMP1	ETM_D10
GPIO11	D9	SAI3_TX1	SDMMC1_DATA_1	EFT2_ICAP1	ETM_D11
GPIO12	B9	SAI3_TX2	SDMMC1_DATA_2	UART2_TX	ETM_D12
GPIO13	B8	SAI3_RX0	SDMMC1_DATA_3	SAI4_RX1	ETM_CLK
GPIO14	A7	SAI3_RX1	SDMMC0_DAT0_DIR	I2C2_SCL	ETM_CTL
GPIO15	A6	SAI3_RX2	SDMMC0_DAT2_DIR	I2C2_SDA	-
GPIO16	C9	SAI2_BCLK	-	I2S2_BCLK	ETM_D13
GPIO17	D10	SAI2_FS	-	I2S2_FS	ETM_D14
GPIO18	D11	SAI2_RX/TX	SPDIF_RX	I2S2_RX	-
GPIO19	C10	SAI1_BCLK	SPI2_TXD	EFT2_OCMP0	ETM_D15
GPIO20	B11	SAI1_FS	SPI2_RXD	EFT2_OCMP1	-
GPIO21	A10	SAI1_RX	SPI2_SCK	EFT2_EXTCK	-
GPIO22	R1	EFT0_ICAP0	EFT0_EXTCK	SPI2_SS	-
GPIO23	R2	EFT0_ICAP1	SDMMC0_CMDDIR	SPI2_TXD	-
GPIO24	R3	EFT0_OCMP0	UART1_TX	SPI2_RXD	-

Table 17. STA1090, STA1095 GPIO and alternate functions (continued)

GPIO	Ball	ALT A	ALT B	ALT C	DEBUG 0
GPIO25	R4	EFT0_OCMP1	UART1_RX	SPI2_SCK	-
GPIO26	N16	EFT1_ICAP0	EFT1_EXTCK	USB1_DRVVBUS	-
GPIO27	N17	EFT1_ICAP1	SDMMC0_FBCLK	CLCD_COLOR17	-
GPIO28	M19	EFT1_OCMP0	SDMMC0_PWR	SDRAM_CS1n	USB_VCOD1V48
GPIO29	P19	EFT1_OCMP1	SDMMC0_DAT31_DIR	CLCD_COLOR16	-
GPIO30	M1	SPI1_SS	EFT0_EXTCK	I2C1_SCL	ETM_D13
GPIO31	M4	SPI1_TXD	EFT1_EXTCK	I2C1_SDA	ETM_D14
GPIO32	M3	SPI1_RXD	EFT1_OCMP1	UART3_TX	-
GPIO33	M2	SPI1_SCK	EFT1_OCMP0	UART3_RX	ETM_D15
GPIO34	B4	I2C1_SDA	UART1_TX	EFT1_ICAP0	-
GPIO35	B3	I2C1_SCL	UART1_RX	EFT1_ICAP1	-
GPIO36	T17	UART1_TX	SDMMC0_DATA_4	SDMMC1_DATA_4	-
GPIO37	T16	UART1_RX	SDMMC0_DATA_5	SDMMC1_DATA_5	-
GPIO38	T18	UART2_RX	SDMMC0_DATA_6	SDMMC1_DATA_6	-
GPIO39	R19	UART2_TX	SDMMC0_DATA_7	SDMMC1_DATA_7	-
GPIO40	B1	UART3_RX	UART1_CTS	EFT2_ICAP0	-
GPIO41	A2	UART3_TX	UART1_RTS	EFT2_ICAP1	-
GPIO42	A3	I2C1_SDA	EFT0_OCMP0	EFT0_ICAP0	-
GPIO43	A4	I2C1_SCL	EFT0_OCMP1	EFT0_ICAP1	-
GPIO44	B5	EFT2_ICAP0	EFT2_OCMP0	EFT2_EXTCK	-
GPIO45	C4	I2C2_SDA	SDMMC0_DAT0_DIR	CD_SS_MON_0	-
GPIO46	D5	I2C2_SCL	SDMMC0_DAT31_DIR	-	-
GPIO47	E3	FSMC_SMADQ_9	-	SDMMC1_CMDDIR	-
GPIO48	E4	FSMC_SMADQ_8	-	SDMMC1_DAT31_DIR	-
GPIO49	F5	FSMC_SMAD25	CLKOUT1	SDMMC1_DAT2_DIR	-
GPIO50	V8	SDRAM_BA_1	FSMC_SMAD12	-	-
GPIO51	W7	SDRAM_BA_0	FSMC_SMAD11	-	-
GPIO52	W14	SDRAM_Add_12	FSMC_SMADQ_3	-	-
GPIO53	V14	SDRAM_Add_11	FSMC_SMADQ_4	-	-
GPIO54	W8	SDRAM_Add_10	FSMC_SMAD13	-	-
GPIO55	W13	SDRAM_Add_9	FSMC_SMADQ_5	-	-
GPIO56	V13	SDRAM_Add_8	FSMC_SMADQ_6	-	-
GPIO57	W12	SDRAM_Add_7	FSMC_SMADQ_7	-	-
GPIO58	V12	SDRAM_Add_6	FSMC_SMAD16/CLE	-	-
GPIO59	W11	SDRAM_Add_5	FSMC_SMAD17/ALE	-	-

Table 17. STA1090, STA1095 GPIO and alternate functions (continued)

GPIO	Ball	ALT A	ALT B	ALT C	DEBUG 0
GPIO60	V11	SDRAM_Add_4	FSMC_SMAD18	-	-
GPIO61	W10	SDRAM_Add_3	FSMC_SMAD23	FSMC_SMADQ_13	-
GPIO62	V10	SDRAM_Add_2	FSMC_SMAD22	FSMC_SMADQ_12	-
GPIO63	W9	SDRAM_Add_1	FSMC_SMAD15	-	-
GPIO64	V9	SDRAM_Add_0	FSMC_SMAD14	-	-
GPIO65	V18	SDRAM_Data_15	FSMC_SMAD25	FSMC_SMADQ_15	-
GPIO66	V19	SDRAM_Data_14	FSMC_SMAD24	FSMC_SMADQ_14	-
GPIO67	W18	SDRAM_Data_13	FSMC_BLn_1	-	-
GPIO68	U18	SDRAM_Data_12	FSMC_SMAD0	-	-
GPIO69	U19	SDRAM_Data_11	FSMC_NOR_CS0n	-	-
GPIO70	T19	SDRAM_Data_10	FSMC_OEn	-	-
GPIO71	V17	SDRAM_Data_9	FSMC_SMADQ_0	-	-
GPIO72	W17	SDRAM_Data_8	FSMC_SMADQ_8	-	-
GPIO73	W4	SDRAM_Data_7	FSMC_RSTn	-	-
GPIO74	V4	SDRAM_Data_6	FSMC_SMAD21	FSMC_SMADQ_11	-
GPIO75	W3	SDRAM_Data_5	FSMC_WPn	-	-
GPIO76	U1	SDRAM_Data_4	FSMC_WAITn	-	-
GPIO77	V1	SDRAM_Data_3	FSMC_SMAD10	-	-
GPIO78	V2	SDRAM_Data_2	FSMC_CLK	-	-
GPIO79	W2	SDRAM_Data_1	FSMC_DREQ	FSMC_BUSYn	-
GPIO80	V3	SDRAM_Data_0	FSMC_DACK	-	-
GPIO81	W5	SDRAM_WEn	FSMC_SMAD20	FSMC_SMADQ_10	-
GPIO82	V6	SDRAM_CASn	FSMC_SMAD19	-	-
GPIO83	W6	SDRAM_RASn	FSMC_SMAD9	FSMC_ADVn	-
GPIO84	V5	SDRAM_DQM0	FSMC_WEn	-	-
GPIO85	V16	SDRAM_DQM1	FSMC_SMADQ_1	-	-
GPIO86	V7	SDRAM_CS0n	FSMC_NOR_CS1n	-	-
GPIO87	V15	SDRAM_CKE	FSMC_SMADQ_2	-	-
GPIO88	W16	SDRAM_FBCLK	FSMC_BLn_0	-	-
GPIO89	W15	SDRAM_CLK	FSMC_SMADQ_9	-	-
GPIO90	F1	FSMC_SMADQ_7	-	-	ETM_D0
GPIO91	F2	FSMC_SMADQ_6	-	-	ETM_D1
GPIO92	F3	FSMC_SMADQ_5	-	-	ETM_D2
GPIO93	F4	FSMC_SMADQ_4	-	-	ETM_D3
GPIO94	G1	FSMC_SMADQ_3	-	-	ETM_D4

Table 17. STA1090, STA1095 GPIO and alternate functions (continued)

GPIO	Ball	ALT A	ALT B	ALT C	DEBUG 0
GPIO95	G2	FSMC_SMADQ_2	-	-	ETM_D5
GPIO96	G3	FSMC_SMADQ_1	FSMC_SMAD8	-	ETM_D6
GPIO97	G4	FSMC_SMADQ_0	FSMC_SMAD7	-	ETM_D7
GPIO98	H1	FSMC_WPn	FSMC_SMAD6	-	ETM_D8
GPIO99	H2	SQI_CE1n	SPI2_SS	SQI_FDBSCK	ETM_D9
GPIO100	H3	FSMC_BUSYn	FSMC_SMAD5	-	ETM_D10
GPIO101	H4	FSMC_OEn	FSMC_SMAD4	-	ETM_D11
GPIO102	J1	FSMC_WEn	FSMC_SMAD3	-	ETM_D12
GPIO103	J2	FSMC_SMAD17/ALE	FSMC_SMAD2	-	ETM_CLK
GPIO104	J3	FSMC_SMAD16/CLE	FSMC_SMAD1	-	ETM_CTL
GPIO105	J4	FSMC_NAND_CS0n	-	-	FORCE_CS_HIGH
GPIO106	U9	VIP_PIXCLK	-	-	-
GPIO107	T11	VIP_HSYNCH	CLCD_COLOR16	-	JTAG1_TMS
GPIO108	R11	VIP_VSYNCH	CLCD_COLOR17	-	JTAG1_TRSTn
GPIO109	U11	VIP_DAT7	-	-	JTAG1_TCK
GPIO110	P10	VIP_DAT6	-	-	-
GPIO111	R10	VIP_DAT5	-	-	-
GPIO112	T10	VIP_DAT4	-	-	-
GPIO113	U10	VIP_DAT3	-	-	-
GPIO114	P9	VIP_DAT2	-	-	-
GPIO115	R9	VIP_DAT1	-	-	-
GPIO116	T9	VIP_DAT0	-	-	-
GPIO117	P11	CLCD_PIXCLK	-	-	JTAG1_TDO
GPIO118	U12	CLCD_VSYNCH	-	-	JTAG1_TDI
GPIO119	T12	CLCD_HSYNCH	-	-	ETM_CLK
GPIO120	R12	CLCD_DE	-	-	ETM_CTL
GPIO121	P12	CLCD_COLOR15	-	-	ETM_D0
GPIO122	U13	CLCD_COLOR14	-	-	ETM_D1
GPIO123	T13	CLCD_COLOR13	-	-	ETM_D2
GPIO124	R13	CLCD_COLOR12	-	-	ETM_D3
GPIO125	P13	CLCD_COLOR11	-	-	ETM_D4
GPIO126	U14	CLCD_COLOR10	-	-	ETM_D5
GPIO127	T14	CLCD_COLOR9	-	-	ETM_D6
GPIO128	R14	CLCD_COLOR8	-	-	ETM_D7
GPIO129	P14	CLCD_COLOR7	-	-	ETM_D8

Table 17. STA1090, STA1095 GPIO and alternate functions (continued)

GPIO	Ball	ALT A	ALT B	ALT C	DEBUG 0
GPIO130	N14	CLCD_COLOR6	-	-	ETM_D9
GPIO131	U15	CLCD_COLOR5	-	-	ETM_D10
GPIO132	R15	CLCD_COLOR4	-	-	ETM_D11
GPIO133	T15	CLCD_COLOR3	-	-	ETM_D12
GPIO134	P15	CLCD_COLOR2	-	-	ETM_D13
GPIO135	U16	CLCD_COLOR1	-	-	ETM_D14
GPIO136	U17	CLCD_COLOR0	SDRAM_CS1n	-	ETM_D15
GPIO137	T7	SDRAM_Data_16	FSMC_SMAD18	-	-
GPIO138	U7	SDRAM_Data_17	FSMC_SMAD19	-	-
GPIO139	T6	SDRAM_Data_18	FSMC_SMAD20	-	-
GPIO140	U6	SDRAM_Data_19	FSMC_ADVn	-	-
GPIO141	T5	SDRAM_Data_20	FSMC_SMAD21	-	-
GPIO142	R6	SDRAM_Data_21	FSMC_SMAD22	-	-
GPIO143	U4	SDRAM_Data_22	FSMC_SMAD23	-	-
GPIO144	U3	SDRAM_Data_23	FSMC_NOR_CS0n	-	-
GPIO145	T8	SDRAM_DQM2	FSMC_BLn_0	-	-
GPIO146	U8	SDRAM_DQM3	FSMC_BLn_1	-	-
GPIO147	P5	SDRAM_Data_24	FSMC_SMAD24	-	-
GPIO148	R5	SDRAM_Data_25	FSMC_WAITn	-	-
GPIO149	P6	SDRAM_Data_26	FSMC_SMADQ_15	FSMC_NOR_CS1n	-
GPIO150	U5	SDRAM_Data_27	FSMC_SMADQ_14	FSMC_SMAD25	-
GPIO151	P7	SDRAM_Data_28	FSMC_SMADQ_13	-	-
GPIO152	R7	SDRAM_Data_29	FSMC_SMADQ_12	-	-
GPIO153	P8	SDRAM_Data_30	FSMC_SMADQ_11	-	-
GPIO154	R8	SDRAM_Data_31	FSMC_SMADQ_10	-	-
S_GPIO0	D6	EFT3_ICAP0	EFT3_OCMP0	CAN1_RX(1)	JTAG1_TDO
S_GPIO1	D7	EFT3_ICAP1	EFT3_OCMP1	CAN1_TX(1)	JTAG1_TDI
S_GPIO2	C5	EFT4_ICAP0	EFT4_OCMP0	EFT4_EXTCK	JTAG1_TMS
S_GPIO3	A5	EFT4_ICAP1	EFT4_OCMP1	-	JTAG1_TRSTn
S_GPIO4	P4	EFT3_ICAP0	EFT3_OCMP0	EFT3_EXTCK	JTAG1_TCK
S_GPIO5	P3	EFT3_ICAP1	EFT3_OCMP1	EFT3_EXTCK	-
S_GPIO6	P2	EFT4_ICAP0	EFT4_OCMP0	EFT4_EXTCK	-
S_GPIO7	P1	EFT4_ICAP1	EFT4_OCMP1	-	-
M3_GPIO0	C15	WAKE0	-	-	-
M3_GPIO1	D15	WAKE1	-	-	-

Table 17. STA1090, STA1095 GPIO and alternate functions (continued)

GPIO	Ball	ALT A	ALT B	ALT C	DEBUG 0
M3_GPIO2	B16	WAKE2	-	-	-
M3_GPIO3	C16	WAKE3	-	-	-
M3_GPIO4	D16	WAKE4	-	-	-
M3_GPIO5	A16	WAKE5	-	-	-
M3_GPIO6	A17	WAKE6	-	-	-
M3_GPIO7	A18	WAKE7	-	-	-
M3_GPIO8	B7	CAN0_TX(1)	-	-	-
M3_GPIO9	C6	CAN0_RX(1)	-	-	-
M3_GPIO10	E5	-	-	-	-
M3_GPIO11	C1	-	-	-	-
M3_GPIO12	C11	USB1_DRVVBUS	-	-	-
M3_GPIO13	A12	CLKOUT0	-	DEBUGCFG	-
M3_GPIO14	C3	-	-	REMAP0	-
M3_GPIO15	B2	-	-	REMAP1	-

1. Only available for STA1095.

4 Electrical Characteristics

4.1 Parameter Conditions

Unless otherwise specified, all voltages are referred to GND.

4.2 Minimum and Maximum Values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C and T_A = 85°C.

The ‘Limit Values’ data is explained and identified with a letter as listed below, and reported in the NOTE field of the following tables where applicable:

- **<SR>**: System requirements, i.e.conditions that must be provided to ensure normal device operation.
- **<P>**: Data tested in production.
- **<C>**: Data based on engineering characterization, not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).
- **<V>**: Data based on design validation performed on three sample devices, not tested in production.
- **<S>**: Data based on design guidelines and simulation, not tested in production.Typical curves.

4.3 Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages.

Table 18 lists the absolute maximum rating for the Accordo2 families of processors.

Table 18. Voltage Characteristics

Symbol		Parameter	Limit Values		Unit
			Min	Max	
VDD_IO_ON	SR	Power Supply pins for the IO buffers of the always ON section	V_{GND} - 0.3	V_{GND} + 3.90	V
VDD_IO	SR	Power Supply pins for the IO buffer in switchable domain.	V_{GND} - 0.3	V_{GND} + 3.90	V
V_{DD}	SR	Power Supply pins for the Internal logic of switchable domain	V_{GND} - 0.3	V_{GND} + 1.50	V
ADC2_AVDD	SR	Analog Power supply for SAR ADC	V_{ADC2_GND} - 0.3	V_{ADC2_AGND} + 3.90	V
ADC2_VREFP	SR	Positive reference voltage for SAR ADC	V_{ADC2_GND} - 0.3	V_{ADC2_AGND} + 3.90	V
DAC_AVDD	SR	Analog Voltage supply for DAC.	V_{DAC_AGND} - 0.3	V_{DAC_AGND} + 3.90	V
DAC_I/O_AVDD	SR	Power supply of IO buffer in DAC/Stereo/Microphone ΣΔ ADC section	V_{DAC_I/O_AGND} - 0.3	V_{DAC_I/O_AGND} + 3.90	V
ADC0_1_VDD	SR	Analog power supply for Stereo/Microphone SDADC	$V_{ADC0\_1\_GND}$ - 0.3	$V_{ADC0\_1\_GND}$ + 3.90	V
USB_VREG3V3_1V1	SR	Voltage supply for 3V3TO1V1 regulator used within USB subsystem	V_{USB_AGND} - 0.3	V_{USB_AGND} + 3.90	V
USB_VREG3V3_1V8	SR	Voltage supply for 3V3TO1V8 regulator used within USB subsystem	V_{USB_AGND} - 0.3	V_{USB_AGND} + 3.90	V
USB0_VDD3V3	SR	Voltage supply for Host USB (USB0)	V_{USB_AGND} - 0.3	V_{USB_AGND} + 3.90	V
USB1_VDD3V3	SR	Voltage supply for dual role USB (USB)	V_{USB_AGND} - 0.3	V_{USB_AGND} + 3.90	V
PLL_VREG3.3V	SR	Voltage supply for 3V3TO2V5 regulator used by PLL and 24 MHz OSC	V_{GND} - 0.3	V_{GND} + 3.90	V

Table 18. Voltage Characteristics (continued)

Symbol		Parameter	Limit Values		Unit
			Min	Max	
V_{INPUT}	SR	Voltage applied to any pin of the VDD_IO domain	V_{GND} - 0.3	VDD_IO + 0.3	V
	SR	Voltage applied to any pin of the VDD_IO_ON domain	V_{GND} - 0.3	VDD_IO_ON + 0.3	V
	SR	Voltage applied to any SAR ADC2 pin	A_{GND} - 0.3	AVDD + 0.3	V
	SR	Voltage applied to any USB pin	(1)		V
$V_{ESD-HBM}$	SR	Electrostatic Discharge, Human Body Model	2000		V
$V_{ESD-CDM}$	SR	Electrostatic discharge, charge device model	500		V

1. Voltage, current, impedance on the USB_DP and USB_DN pins should strictly be compliant to the USB 2.0 standard, including the following engineering charge notice (ECN) issued by the USB Implementers Forum: 5V Short Circuit Withstand Requirement Change ECN.

Warning: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.4 Thermal Characteristics

Devices are available in both Consumer Grade and Automotive Grade Qualification (AEC-Q100 Grade 3).

Table 19. Thermal Characteristics

Symbol		Parameter	Limit values		Unit
			Min	Max	
T_{oper}	SR	Operative ambient temperature	-40	+85	°C
T_j	SR	Operative junction temperature	-40	+125	°C
T_{st}	SR	Storage temperature	-55	+125	°C

Table 20. Frequency Limits

Symbol		Parameter	Test condition	Limit values			Unit
				Min	Typ	Max	
F_{CLK-R}(1)	P	Operating frequency Cortex-R4 CP. ECO Version (-E)	V_{DD}= 1.14 V T_C = 85 °C	-	-	450	MHz
F_{CLK-R} (1)	P	Operating frequency Cortex-R4 CPU. High Version (-H)		-	-	533	MHz
F_{CLK-R} (1)	P	Operating frequency Cortex-R4 CPU. Premium Version (-P)		-	-	600	MHz
F_{CLK-M} (1)	P	Operating Cortex - M3CPU frequency		-	-	208	MHz
F_{HCLK}(1)	P	Operating frequency for Bus Matrix and APB bridges		-	-	208	MHz
F_{52M_CLK}(1)	P	Master clock for I^2C0/1, UART0/1, MSP0/1/2, EFT0/1		-	-	52	MHz
F_{CANSS_CLK}(1)	P	Master clock for CAN1, local eSRAM Cortex-M3		-	-	104	MHz
F_{VIP_PIXCLK}(1)	P	Operating frequency for VIP pixel clock		-	-	60	MHz
F_{SSP_CLK}(1)	P	SSP0/1/2 controller master clock		-	-	104	MHz
F_{SSI_SCK}(1)	P	Operating frequency for SPI (SSP0/1/2) serial clock in master mode		-	-	52	MHz
F_{SAI_BCLK}(1)	P	Operating frequency for SAI bitclock		-	-	25	MHz
F_{I2S_BCLK}(1)	P	Operating frequency for I^2S bitclock		-	-	25	MHz
F_{SQI_CLK}(1)	P	SQI controller master clock		-	-	250	MHz
F_{SQI_SCK}(1)	P	Operating frequency for SQI serial bit clock		-	-	125	MHz
F_{SDRAM_CLK}(1)	P	Operating frequency for SDRAM		-	-	166	MHz
F_{CLCD_CLK}(1)	P	Master clock for LCD controller		-	-	156	MHz
F_{CLCD_PIXCLK}(1)	P	Operating frequency for LCD controller pixel clock		-	-	78	MHz
F_{SDMMC_CLK}(1)	P	Operating frequency for SDMMC0/1 data clock		-	-	52	MHz
F_{JTAG_TCK}(1)	P	Operating frequency for JTAG		-	-	30	MHz

1. Values programmable through configurable PLL. Refer to SRC chapter for details.

This is a full static design. All frequencies can vary from the minimum of 0 MHz up to the maximum value reported in the table.

Table 21. Current Consumption

Symbol		Parameter	Test condition	Limit values			Notes	Unit
				Min	Typ	Max		
$I_{DD\text{-}A2}$	V	VDD (STA1095/1090)	Normal Mode	-	300	450	(1)	mA
$I_{DD\text{-}A2}$	V	VDD (STA1085/1080)	Normal Mode	-	200	390	(2)	mA
I_{DD_STBY1}	V	VDD	Soft STAND_BY1	7	-	-	(3)	mA
I_{DD_STBY2}	V	VDD	Soft STAND_BY2	17	-	-	(4)	mA
$I_{DDIO\text{-}A2}$	V	VDD_IO (STA1095/1090)	Normal Mode	-	100	170	(1)(5)	mA
$I_{DDIO\text{-}A2}$	V	VDD_IO (STA1085/1080)	Normal Mode	-	90	120	(2)(5)	mA
I_{DDIO_STBY1}	V	VDD_IO	Soft STAND_BY1	3	-	-	(3)	mA
I_{DDIO_STBY2}	V	VDD_IO	Soft STAND_BY2	5	-	-	(4)	mA
I_{DDIO_ON}	V	$V_{DD\_IO\_ON}$	Normal Mode	-	100	200	(6)	µA
$I_{DDIO\_ON\_STANDBY}$	P	$V_{DD\_IO\_ON}$	Deep STAND_BY	-	30	50	(6)	µA
$I_{DD\_ADC0\_1}$	V	$V_{ADC0\_1\_AVDD}$	Normal Mode	-	19	-	(7)	mA
I_{DD_ADC2}	V	V_{ADC2_AVDD}	Normal Mode	-	0.6	1	-	mA
I_{DD_DAC}	V	V_{DAC_AVDD}	Normal Mode	-	12	-	(8)	mA
$I_{DD\_USB\_VREG3V3\_1V1}$	V	$V_{USB\_VREG\_3V3\_1V1}$	Normal Mode	-	-	17	(9)	mA
$I_{DD\_USB\_VREG3V3\_1V8}$	V	$V_{DD\_USB\_VREG3V3\_1V8}$	Normal Mode	-	-	23	(10)	mA
$I_{DD\_USB0\_VDD3V3}$	V	$V_{DD\_USB0\_VDD3V3}$	Normal Mode					mA
$I_{DD\_USB1\_VDD3V3}$	V	$V_{DD\_USB1\_VDD3V3}$	Normal Mode					mA

1. MP3 playback from USB + Graphic Application. Cortex-R4 running @ 450.67 MHz, Cortex-M3 running @ 208 MHz, 32-bit SDRAM @ 169 MHz, all DSP enabled, all DAC enabled, 18-bit LCD interface.
2. MP3 playback from USB. Cortex-R4 running @ 450 MHz, Cortex-M3 running @ 208 MHz, 16-bit SDRAM @ 169 MHz, all DSP enabled, all DAC enabled.
3. Cortex-R4 in WFI, Cortex-M3 in WFI, device running off internal ring oscillator (4 MHz), all clocks disabled, all GPIOs in input mode.
4. Cortex-R4 in WFI, Cortex-M3 in WFI, device running off crystal oscillator (24 MHz), all clocks disabled, all GPIOs in input mode.
5. This figure includes both digital VDDIO and analog consumption (USB, DAC, ADC, PLL).
6. RTC enabled.
7. ADC0 (Aux) 12.5 mA, ADC1 (Microphone) 6.5 mA.
8. All DACs active.
9. Both USB ports active.
10. Both USB ports active. Supplies are shorted internally to the device.

4.5 Recommended DC Operating Conditions

Table 22 lists the functional recommended operating DC parameters for STA10xx.

Table 22. Recommended DC Operating Conditions

Symbol		Parameter	Limit Values			Unit
			Min	Typ	Max	
V_{DD}	SR	Digital supply voltage	1.14	1.2	1.26	V
V_{DD_IO}	SR	I/O supply voltage (I/Os is switchable domain)	3.0	3.3	3.6	V
$V_{DD\_IO\_ON}$	SR	I/O supply voltage (I/Os in always ON domain)	3.0	3.3	3.6	V
V_{ADC2_AVDD}	SR	Analog supply voltage for SAR ADC	3.0	3.3	3.6	V
V_{DAC_AVDD}	SR	Analog supply voltage for DAC	3.0	3.3	3.6	V
$V_{DAC\_IO\_AVDD}$	SR	IO supply voltage for in DAC/SDADC IO ring section.	3.0	3.3	3.6	V
$V_{USB\_VREG\_3V3\_1V1}$	SR	Voltage Supply for 3V3TO1V1 USB Regulator.	3.0	3.3	3.6	V
$V_{DD\_USB\_VREG3V3\_1V8}$	SR	Voltage supply for 3V3TO1V8 USB Regulator. (1)	3.0	3.3	3.6	V
$V_{DD\_USB0\_VDD3V3}$	SR	3.3V dedicated power supply to USB0 PHY. (1)	3.0	3.3	3.6	V
$V_{DD\_USB1\_VDD3V3}$	SR	3.3V dedicated power supply to USB0 PHY. (1)	3.0	3.3	3.6	V
$V_{DD\_PLL\_VREG3V3}$	SR	Voltage power supply for SOC PLL. (2)	3.0	3.3	3.6	V
$V_{ADC0\_1\_AVDD}$	SR	Voltage power supply for ADC0 and ADC1.	3.0	3.3	3.6	V

1. $V_{DD\_USB0\_VDD3V3}$, $V_{DD\_USB1\_VDD3V3}$ and $V_{DD\_USB\_VREG3V3\_1V8}$ are internally shorted.
2. $V_{DD\_PLL\_VREG3V3}$ is internally shorted with V_{DD_IO}.

4.6 DC Characteristics

IOs in Accordo2 fall into single category:

- Logical CMOS function

Table 23 lists the functional operating DC characteristics.

Table 23. Digital DC Characteristics

Symbol		Parameter	Test condition	Limit values			Unit	Notes
				Min	Typ	Max		
V_{IL}(1)	P	Logical input low level voltage	V_{DDIO} = 3.3V	- 0.3	-	0.8	V	(2)
V_{IH}(3)	P	Logical input high level voltage	V_{DDIO} = 3.3V	2.0	-	V_{DDIO}+0.3	V	(2)
V_{HYST}	S	Schmitt-trigger hysteresis	-	250	-	-	mV	(4)
V_{TH+}	S	Schmitt-trigger high threshold	-	1.49	-	-	V	-
V_{TL-}	S	Schmitt-trigger low threshold	-	-	-	1.39	V	-
R_{PU}	P	Equivalent pull-up	-	32	50	60	kΩ	-
R_{PD}	P	Equivalent pull-down	-	32	50	60	kΩ	
V_{OL}	P	Low level output voltage	I_{OL}=4mA/8mA	-	-	0.4	V	(5)
V_{OH}	P	High level output voltage	I_{OH}=4mA/8mA	V_{DDIO} - 0.4	-	-	V	(5)
I_{IH}	S	High level input current	-	-	-	< 1	µA	(6)
I_{IL}	S	Low level input current	-	-	-	< 1	µA	(6)
C_{IN}	S	Input Pin Capacitance	-	-	-	1.5	pF	-

1. V_{IL} undershoot: -0.5 V. Duration of the undershoot pulse cannot be greater than one third of the cycle rate.
2. Excludes oscillator inputs SXTALI and MXTALI. Refer to oscillator electrical specifications.
3. V_{IH} overshoot: VDDIO + 0.5 V. Duration of the overshoot pulse cannot be greater than one third of the cycle rate.
4. Apply to all digital inputs unless specified otherwise.
5. I_{OH}/I_{OL} is the maximum source/sink current drive that guarantees the V_{OH}/V_{OL} level, depending on the IO buffer drive capability level (4 or 8 mA, not programmable).
6. Pull-up or pull-down disabled.

4.7 AC Characteristics

4.7.1 Oscillator Electrical Specifications

This device contains two oscillators:

- a 32.768 kHz oscillator
- a 24-26 MHz oscillator

Each requires a specific crystal, with parameters that must be as close as possible to the following recommended values.

Clock from external source can also be applied on input pins.

4.7.2 32.768 kHz Oscillator Specifications

The internal oscillator amplifier specifications are shown in *Table 24*:

Table 24. Oscillator Amplifier Specifications

Symbol		Parameter	Limit Values			Unit
			Min	Typ	Max	
T_{SXTAL}	V	Startup Time	-	15 x L_m/R_m	1.5	s
$T_{duty\ cycle(Zi\ \&\ NZi)}$	V	Duty Cycle	40	50	60	%
A_{SXTALO}	V	Amplitude of OSCILLATION at M3_SXTALO	1.6	-	2.6	V
P_{SXTAL}	S	Power Consumption during Stable Oscillation	-	10	-	µA
$GM_{0\text{-}SXTAL}$	P	Transconductance	28	-	56	µA/V
R_{neg}	S	Negative Resistance	350	-	500	kΩ
Fs	S	Frequency Stability	-	-	25	PPM

The 32.768 kHz oscillator is connected between M3_SXTALI (oscillator amplifier input) and M3_SXTALO (oscillator amplifier output). It also requires two external capacitors of C_L pF, as shown on *Figure 4*.

The specifications of a typical external crystal are shown in *Table 25*:

Table 25. Typical Crystal Recommended Specifications

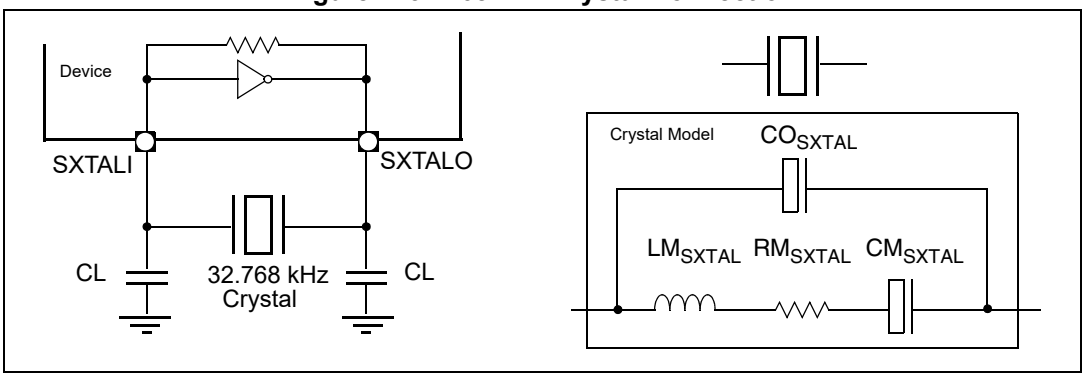
Symbol		Parameter	Limit values			Unit
			Min	Typ	Max	
F_{SXTAL}	SR	Crystal frequency	-	32.768	-	kHz
LM_{SXTAL}		Motion inductance	-	11.8	-	mH
CM_{SXTAL}		Motional capacitance	-	2.0	-	fF
RM_{SXTAL}		Motional resistance	-	50	-	kΩ

Table 25. Typical Crystal Recommended Specifications (continued)

Symbol		Parameter	Limit values			Unit
			Min	Typ	Max	
CO_{SXTAL}		Shunt capacitance	-	3.5	-	pF
CL_{SXTAL}		Load capacitance(1)	-	22	-	pF

1. Total capacitance, including board and package parasitics.

Figure 4. 32.768 kHz Crystal Connection



To drive the 32.768 kHz crystal pins from an external clock source:

- Bypass mode (for test). Enable the bypass mode (bit XCOSC32K_BYPASS= 1b in PMU_CTRL register). Apply external single ended clock at M3_SXTALI. Input clock should be of CMOS level (Low = GND, High = VDDIO_IO_ON)
- Force Through Mode. Apply external single ended clock at M3_SXTALI. Input clock should be of CMOS level (Low = GND, High = VDDIO_IO_ON). Clock is available after OSC startup time.The node M3_SXTALO must not be tied high as this may cause large current to enter amplifier and damage it permanently.

4.7.3 24 - 26 MHz Oscillator Specifications

The internal oscillator amplifier specifications are shown in *Table 26*:

Table 26. Oscillator Amplifier Specifications

Symbol		Parameter	Limit values			Unit
			Min	Typ	Max	
T_{MXTAL}	V	Startup Time	-	-	3.4	ms
$T_{duty\ cycle(Zi\ \&\ NZi)}$	V	Duty Cycle	40	50	60	%
A_{MXTALO}	V	Amplitude of OSCILLATION at MXTALO	0.4	-	1.6	V
P_{SXTAL}	S	Power Consumption during Stable Oscillation	-	-	8	µA
$GM_{0\text{-}MXTAL}$	P	Transconductance	8.5	-	15.8	mA/V
R_{neg}	S	Negative Resistance	175	-	285	Ω
Fs	S	Frequency Stability	-	-	25	PPM

The 24 to 26 MHz oscillator is connected between MXTALI (oscillator amplifier input) and MXTALO (oscillator amplifier output). It also requires two external load capacitors of C_L pF, as shown in *Figure 5*.

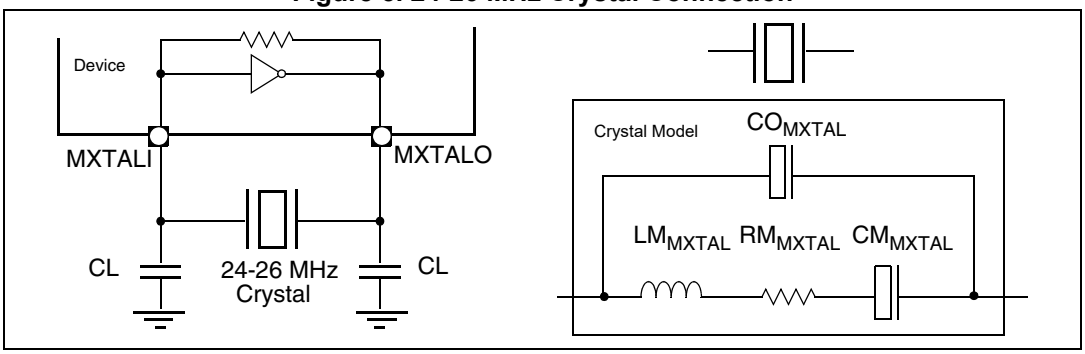
The specifications of a typical external crystal are shown in *Table 27*:

Table 27. Typical Crystal Recommended Specifications

Symbol		Parameter	Limit values			Unit
			Min	Typ	Max	
F_{MXTAL}	SR	Crystal Frequency	-	24	-	MHz
LM_{MXTAL}, 24MHz XTAL			-	4.0	-	mH
CM_{MXTAL}, 24MHz XTAL			-	10.1	-	fF
RM_{MXTAL}		Motional Resistance	-	20	-	Ω
CO_{MXTAL}		Shunt Capacitance	-	-	4.0	pF
CL_{MXTAL}		Load Capacitance(1)	-	-	30	pF

1. Total capacitance, including package and board parasitics.

Figure 5. 24-26 MHz Crystal Connection



To drive the 24/26 MHz crystal pins from an external clock source:

– Force Through Mode. Bias MXTALO at 1.25 V. Apply external single ended square clock at MXTALI. Input clock should be of CMOS level (Low = GND, High = 2.5 V). Clock is available after OSC startup time.

4.8 Sound Subsystem

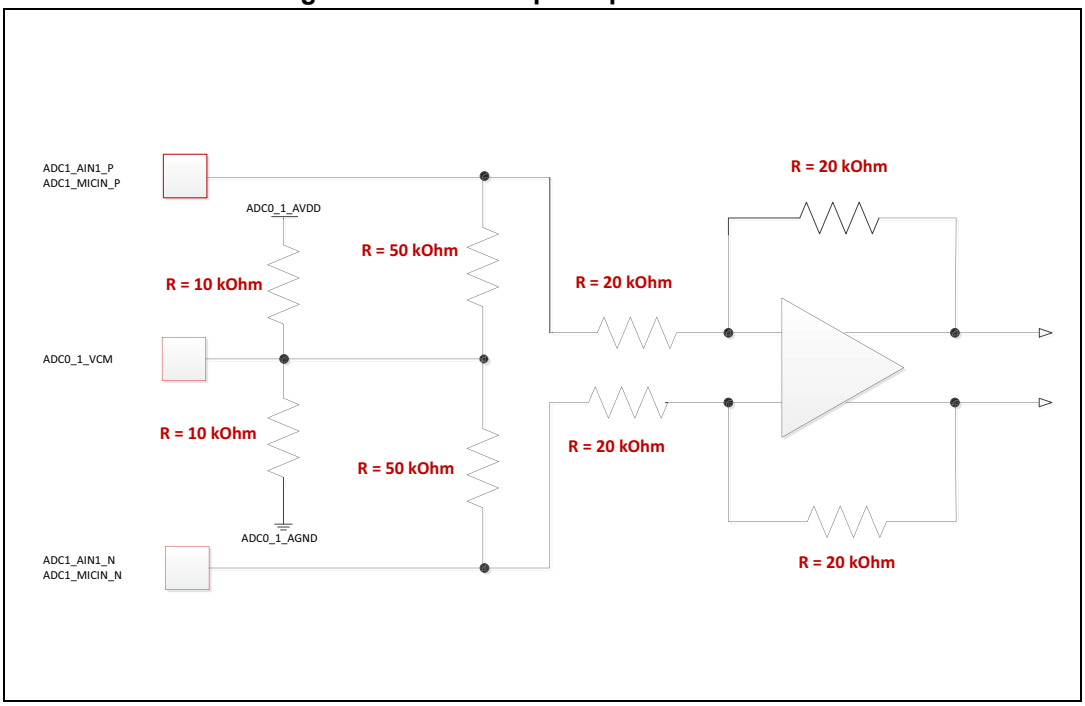
4.8.1 ADC1: Microphone ΣΔ ADC Electrical Characteristics

Table 28. MICADC electrical characteristics

Symbol		Parameter	Limit values			Unit
			Min	Typ	Max	
$V_{ASupply}$	SR	Analog Supply	3.0	3.3	3.6	V
V_{in}	S	Differential Analog Input	-	5.6(1) 2.0(1)	-	V_{p-p} V_{rms}
V_{in}	SR	Single ended Analog Input	-	2.8(1) 1.0(1)	-	V_{p-p} V_{rms}
V_{com}	P	DC coupled Input common mode AC coupled input common mode	1.5 0	1.65 1.65	1.8 3.3	V
SNR	V	Differential mode Signal to Noise ratio (A-weighted, Output rate 48 kHz, BW = 20 kHz)	86	-	-	dB
SNR	V	Differential mode Signal to Noise ratio (Unweighted, Output rate 48 kHz, BW = 3.2 kHz)	88	-	-	dB
SNR	V	Single ended mode Signal to Noise ratio (A-weighted, Output rate 48 kHz, BW = 20 kHz)	80	-	-	dB
SNR	V	Single ended mode Signal to Noise ratio (Unweighted, Output rate 48 kHz, BW = 3.2 kHz)	81	-	-	dB
THD + N	V	Differential mode Total harmonic distortion + Noise	-80	-85	-	dB
THD + N	V	Single ended mode Total harmonic distortion + Noise	-74	-79	-	dB
V_{MIC_BIAS}	P	MIC_BIAS	-	2.5(2)	-	V
I_{MIC_BIAS}	V	Current through MIC_BIAS	-	-	2	mA
$I_{DD\_AMICADC}$	C	Analog current consumption	-	6.5	-	mA

1. Max possible tolerable variation +/-5 %.
2. Max variation due to process mismatch +/- 5 %.

Figure 6. MICADC Input Equivalent Circuit



4.8.2 ADC0: ΣΔ Audio ADC Electrical Characteristics

Table 29. Audio ΣΔ ADC Electrical Characteristics

Symbol		Parameter	Limit values			Unit
			Min	Typ	Max	
$V_{ASupply}$	SR	Analog Supply	3.0	3.3	3.6	V
V_{in}	SR	Single Ended Analog Input	-	2.8(1) 1.0(1)	-	V_{p-p} V_{rms}
V_{com}	P	DC coupled Input common mode AC coupled input common mode	1.5 0	1.65 1.65	1.8 3.3	V
SNR	V	Signal to Noise ratio (A-weighted, 1kHz, 0 dBFs, BW = 20 kHz)	91	94	-	dB
THD + N	V	Total harmonic distortion + Noise	-85	-87	-	dB
I_{DD_ASDADC}	C	Analog current consumption	-	12.5	-	mA

1. Max possible tolerable variation +/-5 %.

Figure 7. Audio ADC Input Equivalent Circuit

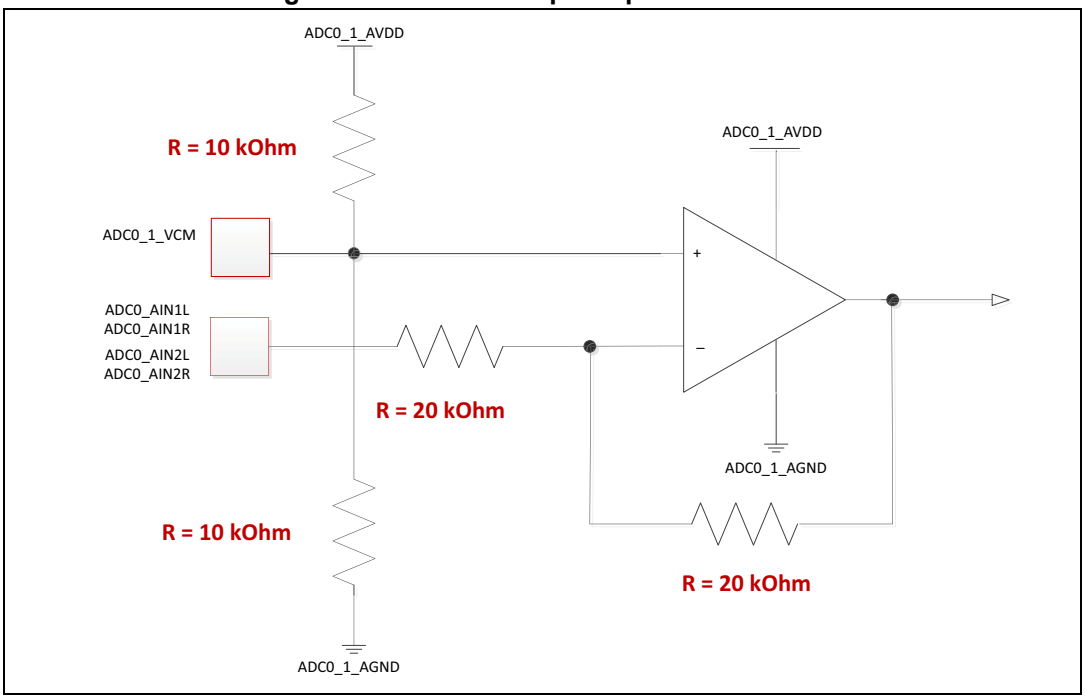
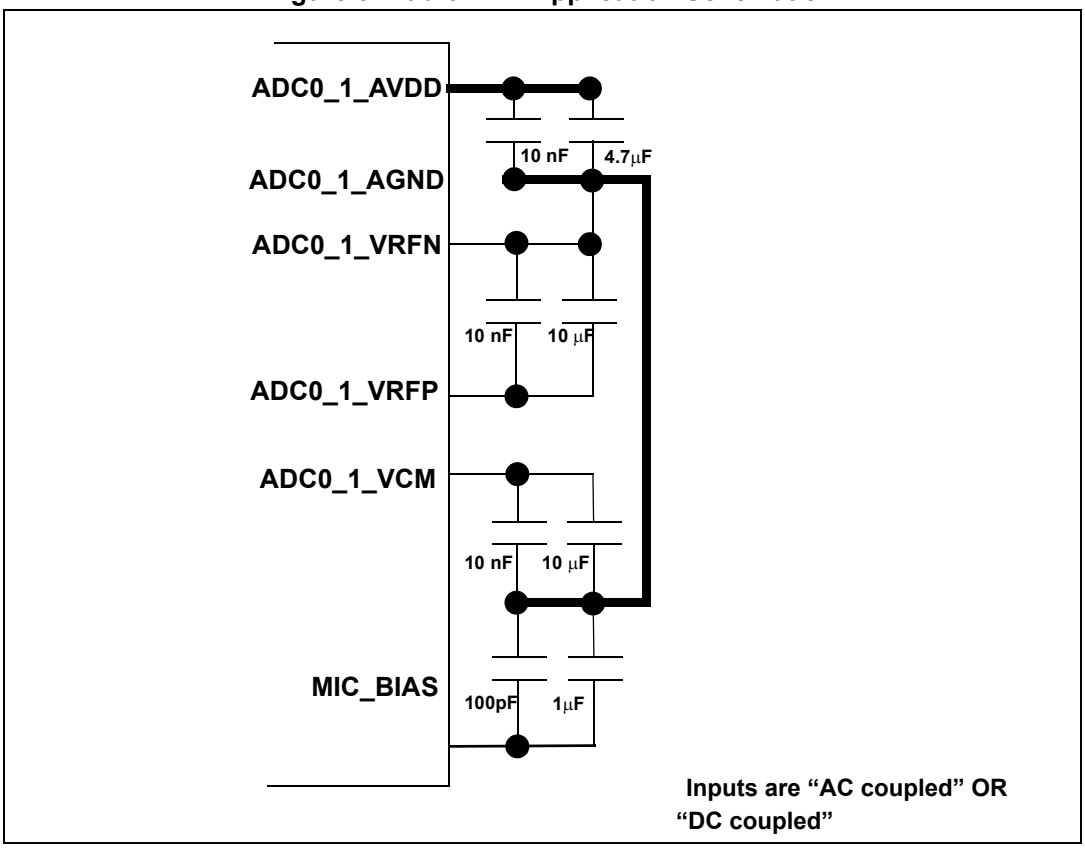


Figure 8. Audio ADC Application Schematic



4.8.3 DAC Electrical Characteristics

Table 30. DAC Electrical Characteristics

Symbol		Parameter	Limit values			Unit
			Min	Typ	Max	
$V_{ASupply}$	SR	Analog Supply	3.0	3.3	3.6	V
V_{rms}(1)	V	Analog RMS output	741	780	819	mV_{rms}
V_{rms}(2)	V	Analog RMS output	693	730	766	mV_{rms}
V_{com}	P		-	1.45(3)	-	V
C_{max}	SR	Maximum output load	-	-	10	pF
R_{min}	SR	Minimum output resistance	10	-	-	KΩ
SNR	V	Signal to Noise ratio (A-weighted, BW = 20 kHz, 1 kHz, -60 dBFs)	98	103	-	dB
THD + N	V	Total harmonic distortion + Noise (A-weighted, BW = 20 kHz, 1 kHz, 0dbFS)	-84	-90	-	dB
I_{DD_ADAC}	C	Analog current consumption of single DAC	-	-	8	mA

1. No external load resistance.
2. External load resistance: 500 Ω series on 10 kΩ next stage (10/10.5 partition).
3. Max variation due to process mismatch +/- 5 %.

Figure 9. DAC Output Equivalent Circuit

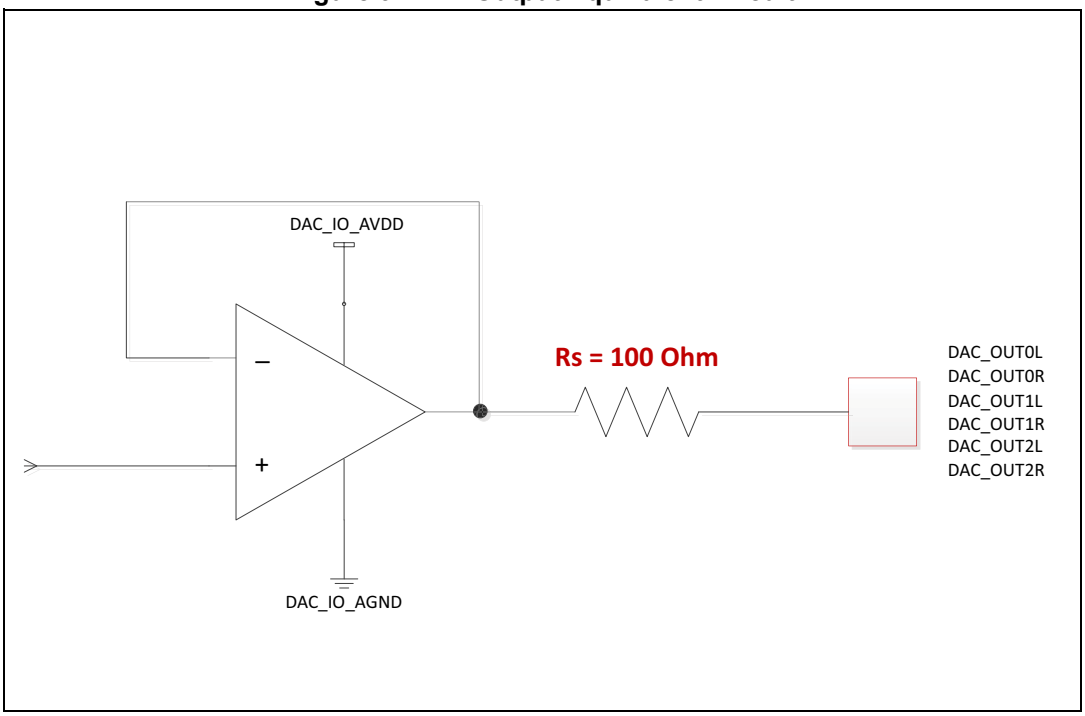


Figure 10. DAC VCOM Equivalent Circuit

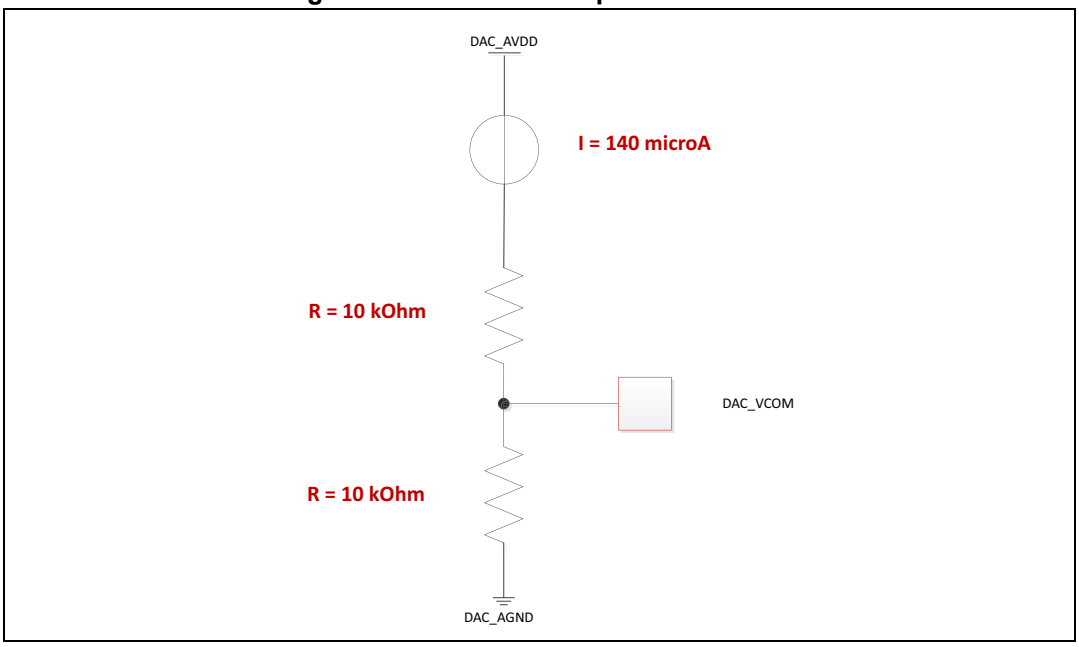
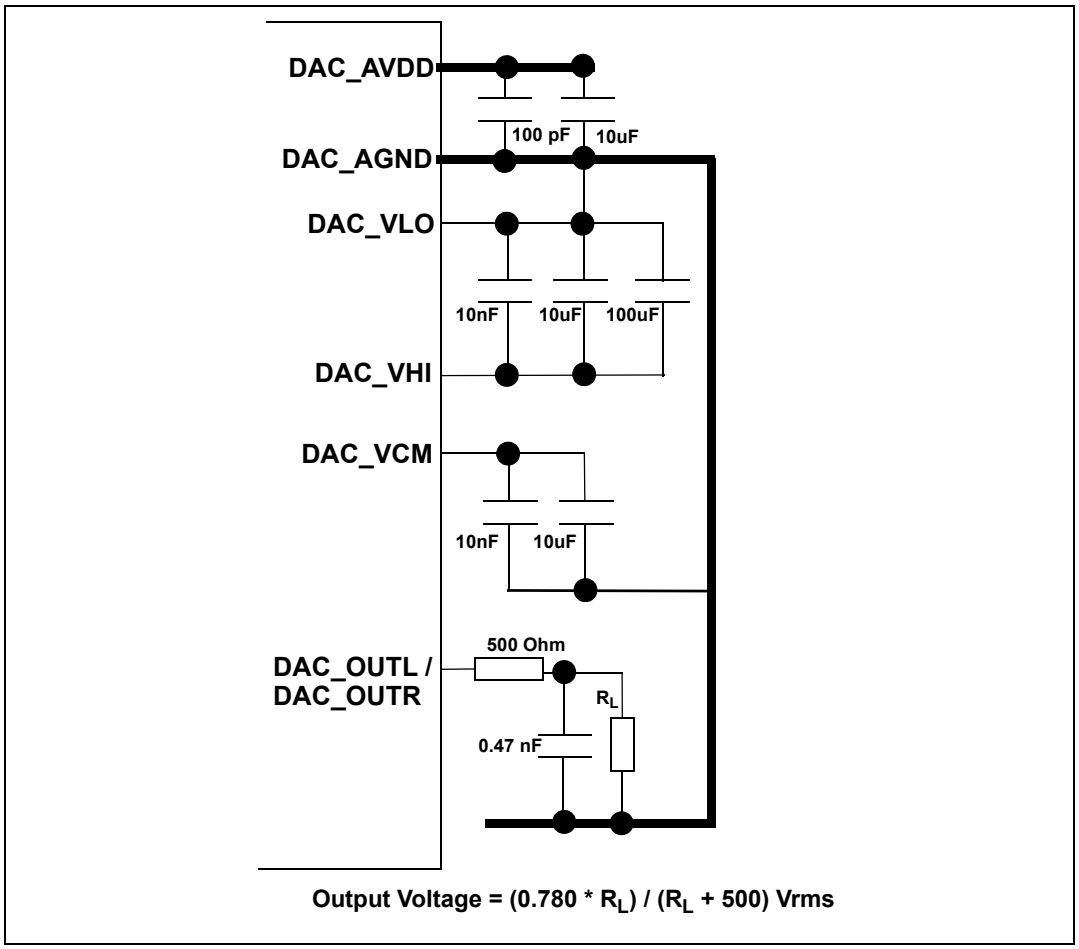


Figure 11. DAC Application Schematic



4.9 ADC2: SAR ADC Electrical Characteristics

Table 31. ADC Conversion Characteristics

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{REFE}	SR	External reference voltage[2]	-	3.0	3.3	3.6	V
R_{REFE}	S	External reference input impedance	-	75	-	-	kΩ
V_{REFI}	V	Internal reference voltage	-	1.95	2.0	2.05	V
t_{START}	S	Start-up time	From Enable to first EOC	-	-	10	µs
f_{CK}	SR	ADC Clock frequency (depends on system configuration)	-	4	-	13	MHz
f_s	SR	Sampling + conversion cycle	-	-	14	-	cycle
INL	P	Integral non linearity	-	-2	-	2	LSB
DNL	P	Differential non linearity[3]	-	-1	-	1	LSB
OFS	P	Offset error	-	-5	-	5	LSB
GNE	P	Gain error	-	-2	-	2	LSB
TUE	P	Total unadjusted error	Without current injection	-6	-	6	LSB
I_{INJ}	V	Max positive/negative injection[4]	-	–3	-	3	mA
SNR	V	Signal-to-noise ratio	-	58	-	-	dB
THD	V	Total harmonic distortion	-	63	-	-	dB
SINAD	V	Signal-to-noise and distortion	-	58	-	-	dB
ENOB	V	Effective number of bits	-	9.4	-	-	bits
I_{SAM}	S	Average sampling current drawn from input source	-	-	5	-	µA/M sps
R_{inout}	S	Input impedance of each channel	-	-	1	-	MΩ

1. V_{DD} = 3.3 V, T_J = –40 to +125 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}.
2. VREFP <= VDDA + 25 mV.
3. No missing codes.
4. Maximum current injection without ADC performance degradation.

4.10 Touch Screen Controller (TSC) Electrical Characteristics

The following table lists the electrical characteristics of the TSC.

Table 32. Touch screen controller

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{DDTSC}	SR	Full scale voltage input span(1)	-	3.0	3.3	3.6	V
C_{IN}	S	Total input capacitance(2)	-	-	-	13	pF
I_{LEAK}	S	Input leakage	-	-2	-	+2	µA
t_{SETTLE}	S	Panel settling time(3)	-	0.01	-	100	ms
t_{TOUCH}	S	Touch detect delay(3)	-	0.01	-	50	ms
R_{ON-P}	P	Y+, X+ drivers on resistance	I_{OH} = -30 mA	-	-	12	Ω
R_{ON-N}	P	Y-, X- drivers on resistance	I_{OL} = +30 mA	-	-	13	Ω
I_{PANEL}	P	Panel driver current capability	-	-	-	30	mA
V_{TOUCH}	P	Touch detect comparator threshold(4)	V_{DDTSC} = 3.0 V	2.1	-	-	V
V_{TOHYS}	S	Touch detect comparator hysteresis	-	300	-	-	mV

1. It is the same as ADC voltage reference range.
2. Equivalent to Cp1 + Cp2 + Cs in ADC section.
3. Controlled by the Touch Screen Configuration Register (TSCCONFIG).
4. Measured as VIH on X+ input.

4.11 Regulator Specifications

4.11.1 Always-on LDO (3V3 TO 1V2 Low Power Regulator)

Table 33. 3V3 TO 1V2 Low Power Regulator

Symbol		Parameter	Limit values			Unit
			Min	Typ	Max	
$V_{ASupply}$	SR	Analog Supply	3.0	3.3	3.6	V
$V_{out(@100µA)}$	P	Output Voltage @ $I_{load = max}$	1.14	1.2	1.26	V
C_{load}	SR	Total off chip capacitance value(1)	-	-	2.2	nF
PSRR	S	Power supply rejection at DC @ Full load	-	-50	-40	dB
PSRR	S	Power supply rejection at 1MHz @ Full load	-	-50	-40	dB
T_{start}	S	Start up time from power down to active	-	-	500	µs

1. This is mandatory for proper device functionality.

4.11.2 VDD Low Voltage Detector

Table 34. Digital Supply LVD

Symbol		Parameter	Limit values			Unit
			Min	Typ	Max	
V_{uthres}	P	Upper voltage threshold (Value @ 27C, 0σ), σ: 5mV	1.07	-	1.09	V
V_{lthres}	P	Lower voltage threshold (Value @ 27C, 0σ), σ: 5mV	1.01	-	1.02	V
V_{hyst}	S	Hysteresis	-	60	-	mV

4.11.3 VDDIO_IO_ON Main Voltage Detector

Table 35. VDDIO_IO_ON supply LVD

Symbol		Parameter	Limit values			Unit
			Min	Typ	Max	
V_{uthres}	P	Upper voltage threshold (Value @ 27C , 0σ), σ: 12mV	2.78	-	2.92	V
V_{lthres}	P	Lower voltage threshold (Value @ 27C , 0σ), σ: 12mV	2.69	-	2.83	V
V_{hyst}	S	Hysteresis	-	90	-	mV

4.11.4 PLL LDO (3V3 TO 2V5 Low Power Regulator)

Table 36. 3V3 TO 2V5 Regulator

Symbol		Parameter	Limit values			Unit
			Min	Typ	Max	
$V_{ASupply}$	SR	Analog Supply	3.0	3.3	3.6	V
V_{out}	P	Output Voltage @ $I_{load = max}$	2.375	2.5	2.63	V
C_{load}	SR	Total off chip capacitance values(1)	-	4.7	-	µF
		ESR of each external capacitor in frequency range of 100 kHz - 100 MHz	10	-	150	mΩ
PSRR_DC	S	Power supply rejection at DC @ NO load	-	-	-23	dB
PSRR	S	Power supply rejection at 2MHZ @ NO load	-	-	-12	dB
T_{start}	S	Start up time from power down to active after input supply stabilizes (Supply rise time of 1µs)	-	-	300	µs

1. This is mandatory for proper device functionality.

4.11.5 USB 1V8 LDO (3V3 TO 1V8 Low Power Regulator)

Table 37. 3V3 TO 1V8 regulator

Symbol		Parameter	Limit values			Unit
			Min	Typ	Max	
$V_{ASupply}$	SR	Analog Supply(1)	3.0	3.3	3.6	V
V_{out}	P	Output Voltage @ $I_{load = max}$	1.71	-	1.87	V
C_{load}	SR	Total off chip capacitance value(2)	-	4.7	-	µF
		ESR of each external capacitor in frequency range of 100 kHz - 100 MHz	10	-	150	mΩ
PSRR_DC	S	Power supply rejection at DC @ NO load	-	-	-40	dB
PSRR	S	Power supply rejection at 2 MHz @ NO load	-	-	-11	dB
T_{start}	S	Start up time from power down to active after input supply stabilizes (Supply rise time of 1µs)	-	-	300	µs

1. USB_VREG3V3_1V8, USB0_VDD3V3 & USB1_VDD3V3 are internally shorted in the device IO ring.
2. This is mandatory for proper device functionality.

4.11.6 USB 1V1 LDO (3V3 TO 1V1 Low Power Regulator)

Table 38. 3V3 TO 1V1 regulator

Symbol		Parameter	Limit values			Unit
			Min	Typ	Max	
$V_{ASupply}$	SR	Analog Supply	3.0	3.3	3.6	V
V_{out}	P	Output Voltage @ $I_{load = max}$	1.0	1.1	-	V
C_{load}	SR	Total off chip capacitance value(1)	-	4.7	-	µF
PSRR_DC	S	Power supply rejection at DC @ Full load	-	-	-30	dB
PSRR	S	Power supply rejection at 1 MHz @ Full load	-	-	-28	dB
T_{start}	S	Start up time from power down to active after input supply stabilizes (Supply rise time of 1 µs)	-	-	300	µs

1. Mandatory for proper device functionality.

4.12 Power On and Reset Timings

4.12.1 Timing Requirements for the Device Power-on Reset

The timings to power on the system have been summarized in the table below and represented in *Figure 12*.

Figure 12. Power Supply Possible Start-up Sequences

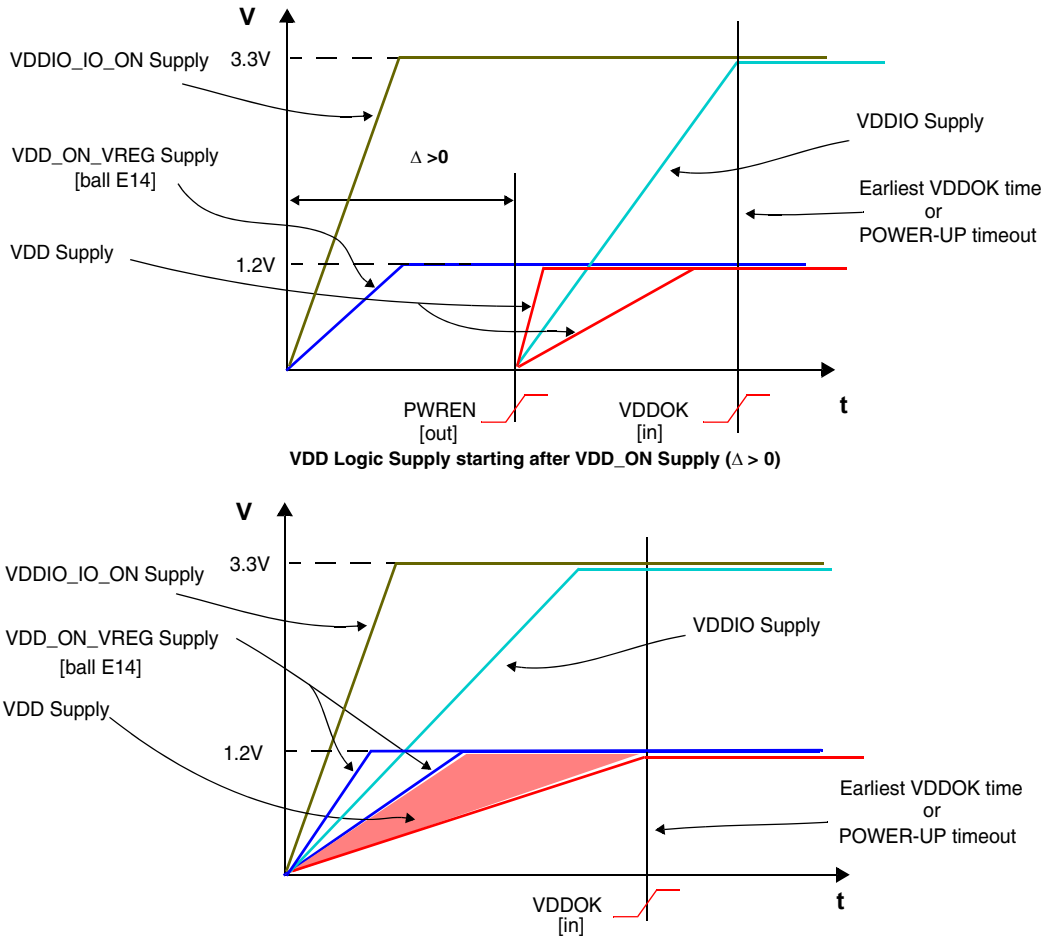


Figure 13. Initial Power-On Sequence (VDDOK timed)

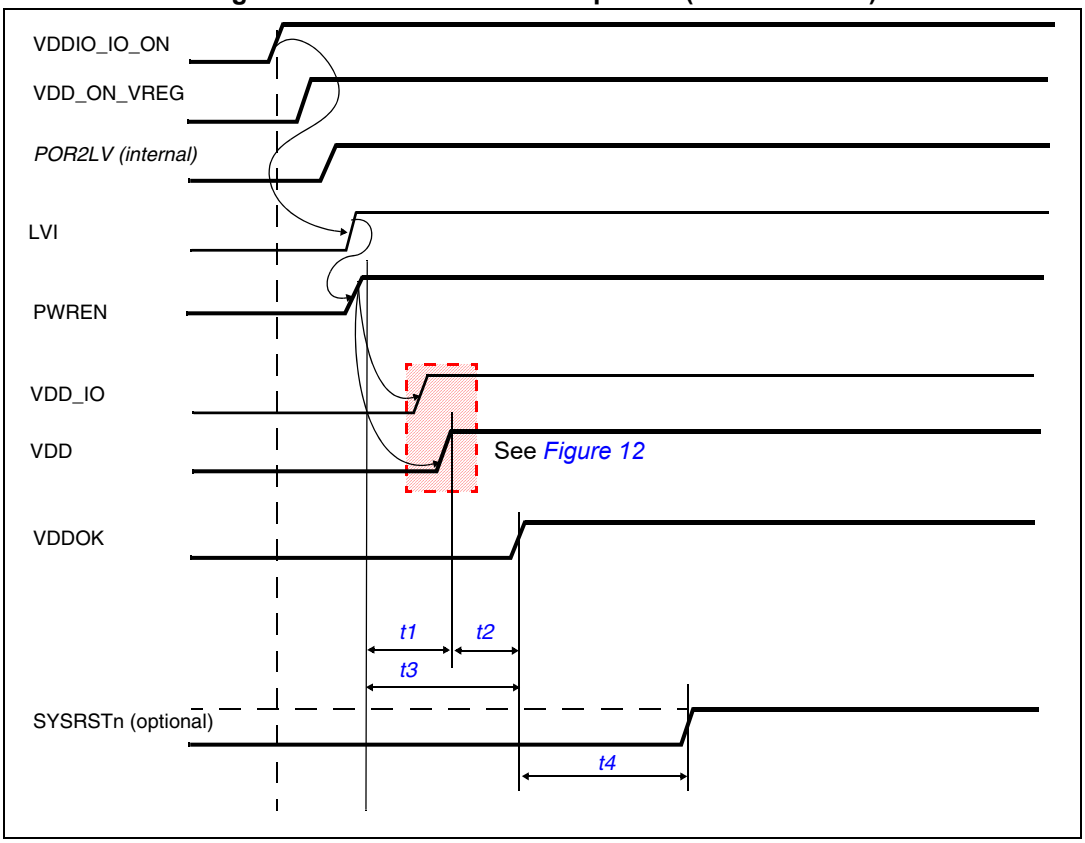


Table 39. Initial Power-up Sequence Timings (VDDOK timed)

Symbol		Parameter	Timing		Unit
			Min.	Max.	
t1	SR	PWREN to last voltage stable	-	174	ms
t2	SR	Last voltage stable to VDDOK	> 0	-	µs
t3	SR	PWREN to VDDOK	-	174	ms
t4	SR	VDDOK to SYSRSTn	10	-	µs

Note: For the Power-Up sequence VDDOK timed see Figure 13.

Figure 14. Initial Power-up Sequence (without VDDOK)

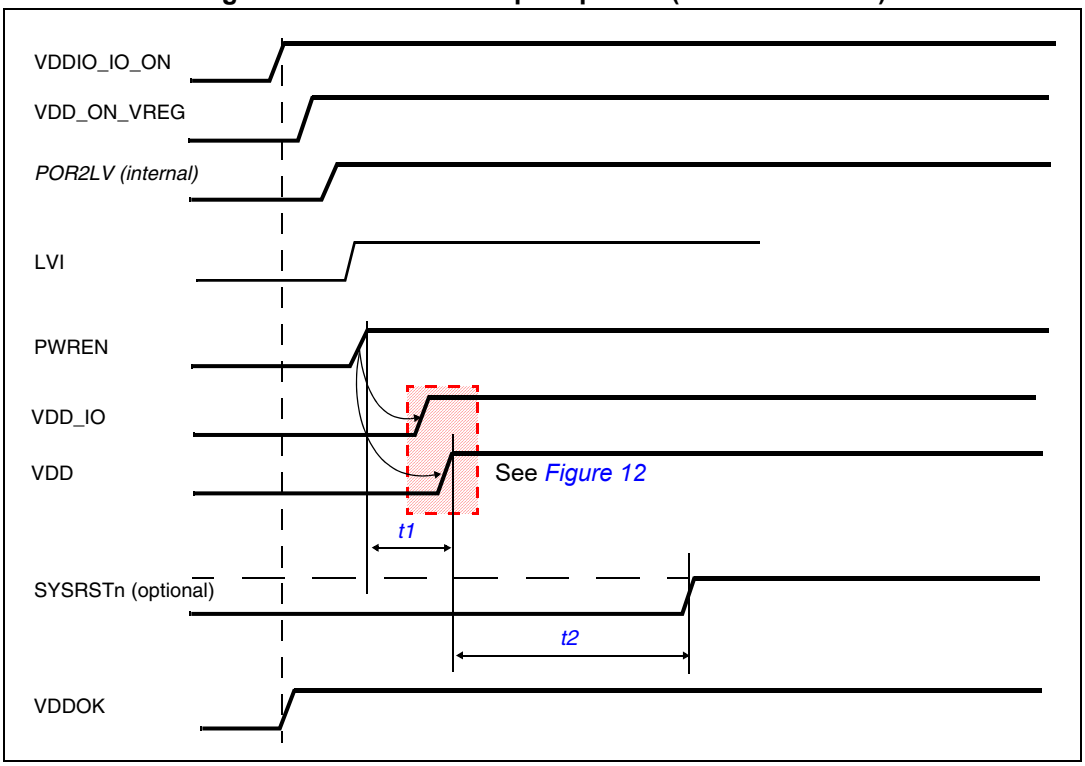


Table 40. Initial Power-up Sequence Timings (without VDDOK)

Symbol		Parameter	Timing		Unit
			Min.	Max.	
t1	SR	PWREN to last voltage stable	-	174(1)	ms
t2	SR	Last voltage stable to SYSRSTn	10	-	µs

1. This value is programmable in the Power Management Unit. By default, at POR, is set to the maximum of 174 ms.

Note: For the Power-Up sequence without VDDOK see Figure 14.

Figure 15. Wake Up (VDDOK timed)

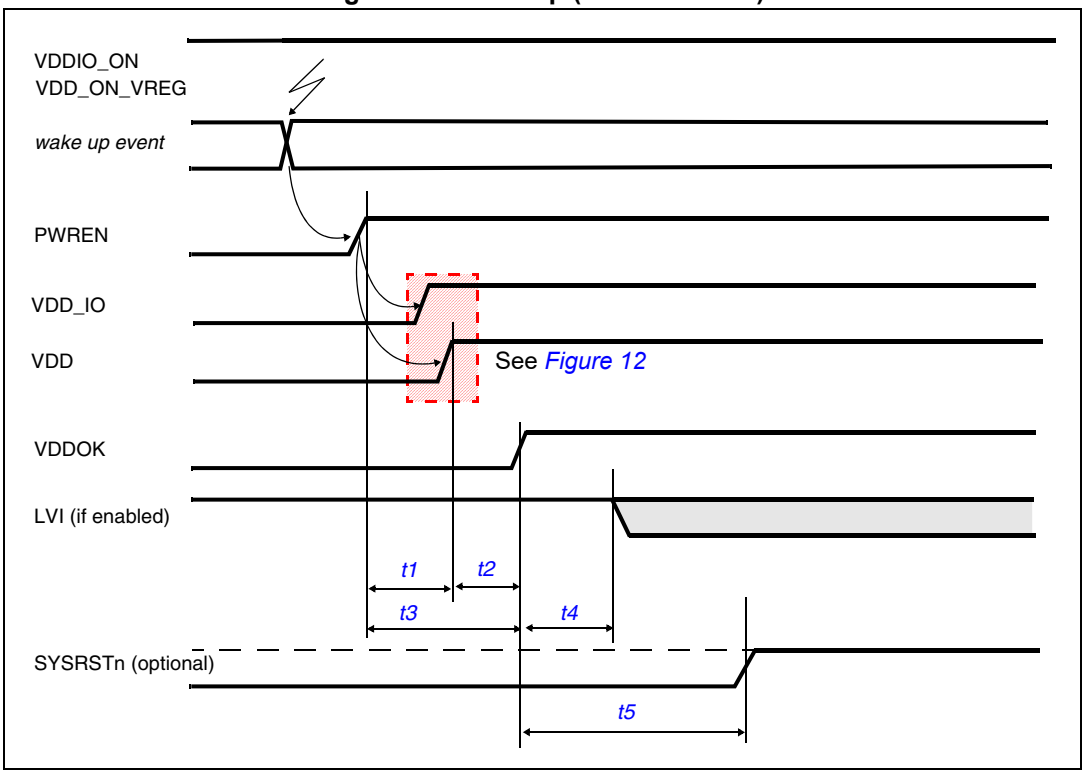


Table 41. Wake Up (VDDOK timed)

Symbol		Parameter	Timing		Unit
			Min.	Max.	
t1	SR	PWREN to last voltage stable	-	174(1)	ms
t2	SR	Last voltage stable to VDDOK	> 0	-	µs
t3	SR	PWREN to VDDOK	-	174	ms
t4	SR	VDDOK to LVI(2)	2	-	µs
t5	SR	VDDOK to SYSRSTn release	> 0	-	µs

1. This value is programmable in the Power Management Unit. By default, at POR, is set to the maximum of 174 ms.
2. The LVI signal has effect during the boot only if the LVIEn bit is set.
If the LVIEn bit is set, the t4 timing, if respected, is the minimum timing that ensures that the PMU FSM reaches the ON state.
If the LVIEn bit is set and an LVI event occurs before the timing t4, the PMU FSM directly moves back to the STAND-By state without reaching the ON state.

Note: For the Wake-Up sequence VDDOK timed see Figure 15.

Figure 16. Wake Up (without VDDOK)

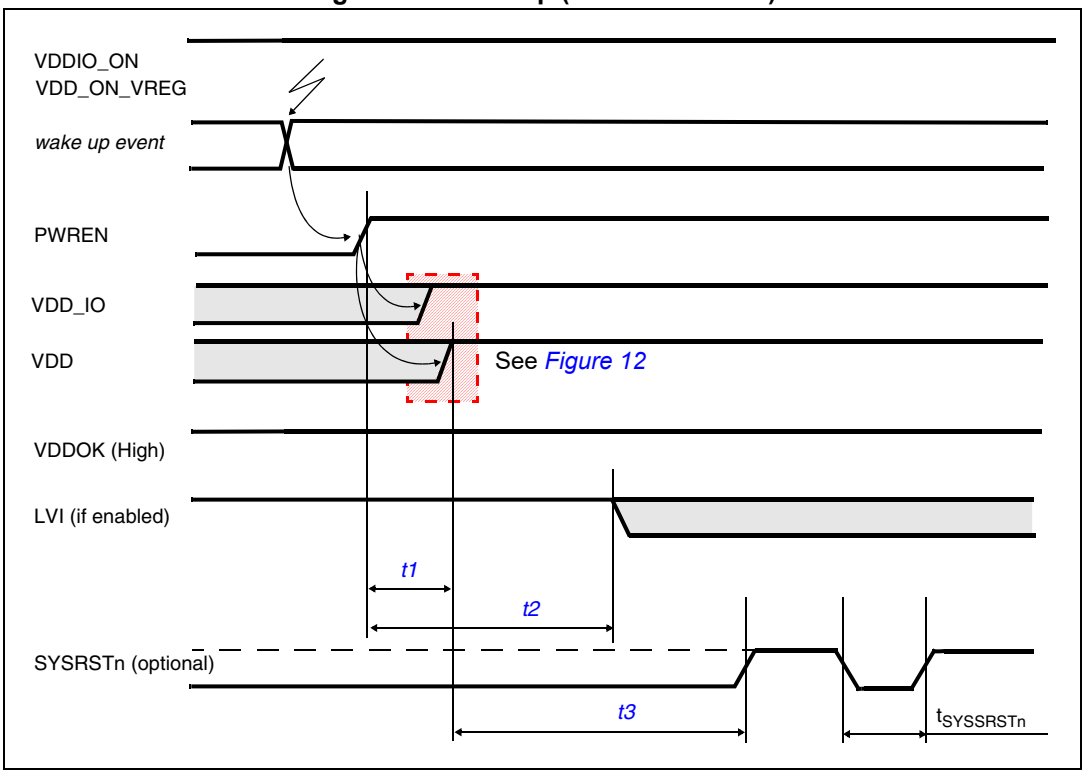


Table 42. Wake Up Timings (without VDDOK)

Symbol		Parameter	Timing		Unit
			Min.	Max.	
t1	SR	PWREN to last voltage stable	-	174(1)	ms
t2	SR	Last voltage stable to LVI(2)	8000+2	-	µs
t3	SR	Last Voltage Stable to SYSRTSn	> 0	-	µs

1. This value is programmable in the Power Management Unit. By default, at POR, is set to the maximum of 174 ms.
2. The LVI signal has effect during the boot only if the LVIEn bit is set.
If the LVIEn bit is set, the t4 timing, if respected, is the minimum timing that ensures that the PMU FSM reaches the ON state.
If the LVIEn bit is set and an LVI event occurs before the timing t2, the PMU FSM directly moves back to the STAND-By state without reaching the ON state.

Note: For the Wake-Up sequence without VDDOK see Figure 16.

4.12.2 Timing Requirements for Device Hardware Reset

The timing requirements in this section assumes stable power supplies at the assertion of SYSRSTn signal.

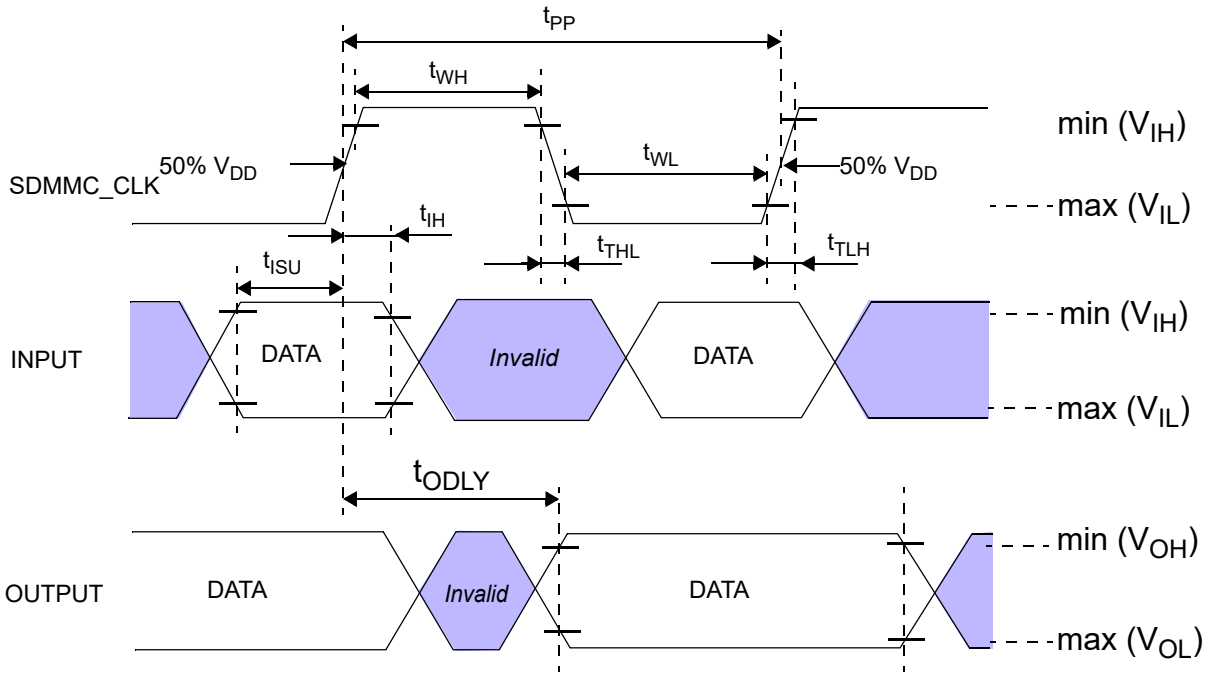
The assertion of the SYSRSTn signal resets all the device circuitry with the exception of the PMU. The reset signal generated by the PMU is actually put in logical and with the SYSRSTn input.

Table 43. Hardware reset timing

Symbol		Parameter	Timing		Unit
			Min.	Max.	
$t_{SYSRSTn}$	SR	SYSRSTn low pulse width	1000	-	ns

4.13 SD/MMC Timings

Figure 17. SD/MMC Timing Diagrams: Data input/output



Data is always sampled, by the card or the controller, on the rising edge of the clock.

Note: SD/MMC Timings
Source: JEDEC Standard No. 84-A44

4.14 Color LCD Controller (CLCD) Timings

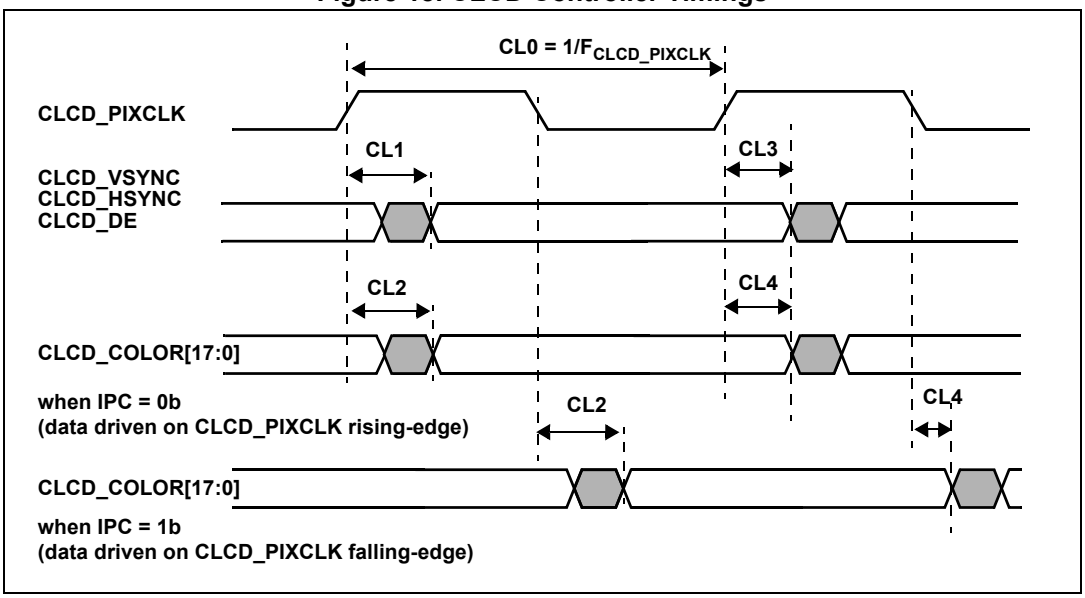
4.14.1 Switching Characteristics for CLCD controller outputs

All the switching timing characteristics are relative to CLCD_PIXCLK signal.

Table 44. Switching Characteristics for CLCD controller outputs

No.	Symbol		Parameter	Timing		Unit
				Min	Max	
CL0	F_{CLCD_PIXCLK}	S	Pixel Clock Frequency	-	78	MHz
CL1	$T1_{ODLY}$	S	Control Signals Output Delay	-	5.3	ns
CL2	$T2_{ODLY}$	S	Data Output Delay	-	8.5	ns
CL3	$T3_{HOLD}$	S	Invalid Control Signals Delay	TBD	-	ns
CL4	$T4_{HOLD}$	S	Invalid Data Delay	TBD	-	ns

Figure 18. CLCD Controller Timings



4.15 I²S and SAI Ports Timings

4.15.1 I²S (MSP) Input Timings

Table 45. I²S (MSP) Input Timings

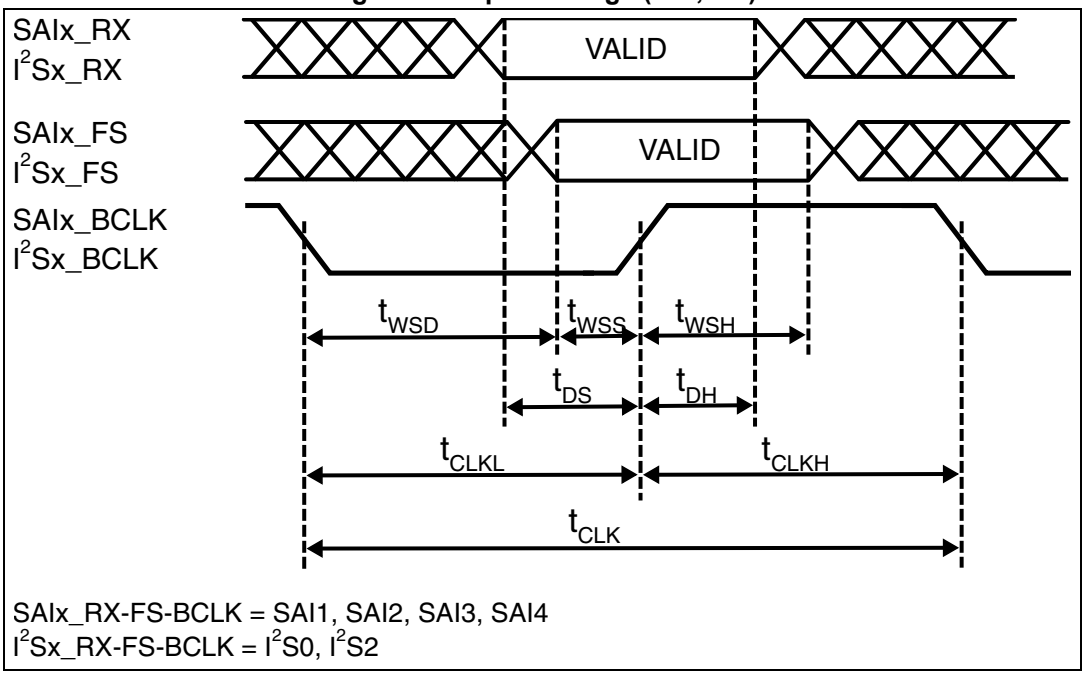
Symbol		Parameter	Timing		Unit	Cload [pF]
			Min	Max		
tc	S	Bitclock Frequency	-	25	MHz	25
tclk	S	Bitclock time period	40	-	ns	-
twss (Slave Mode)	S	Word select input setup time	4	-	ns	25
twsh (Slave Mode)	S	Word select input hold time	4	-	ns	25
Tds	S	Data input setup time	4	-	ns	25
Tdh	S	Data input hold time	4	-	ns	25

4.15.2 SAI Input Timings

Table 46. SAI Input Timings

Symbol		Parameter	Timing		Unit	Cload [pF]
			Min	Max		
t_c	S	Clock frequency	-	25	MHz	25
tclk	S	Clock time period	40	-	ns	-
twss (Slave Mode)	S	Word select input Setup time	4	-	ns	25
twsh (Slave Mode)	S	Word select input Hold time	4	-	ns	25
Tds	S	Data input setup time	4	-	ns	25
Tdh	S	Data input hold time	4	-	ns	25

Figure 19. Input Timings (SAI, I²S)



4.15.3 I²S (MSP) Output Timings

Table 47. I²S (MSP) Output Timings

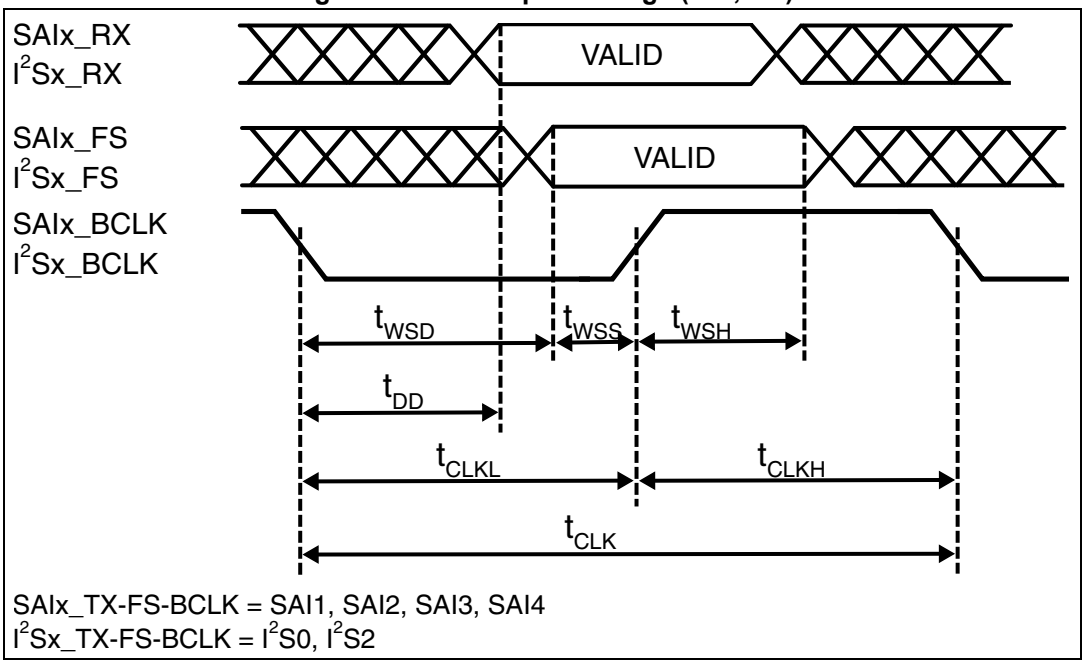
Symbol		Parameter	Timing		Unit	Cload (pf)
			Min	Max		
t_c	S	Clock Frequency	-	25	MHz	25
t_{clk}	S	Clock time period	40	-	ns	-
t_{wsd} (Master Mode)	S	Word select output delay	-	10	ns	25
t_{dd}	S	Data output delay	-	10	ns	25

4.15.4 SAI Output Timings

Table 48. SAI Output Timings

Symbol		Parameter	Timing		Unit	Cload (pf)
			Min	Max		
t_c	S	Clock Frequency	-	25	MHz	25
t_{clk}	S	Clock time period	40	-	ns	-
t_{wsd} (Master Mode)	S	Word select output delay	-	10	ns	25
t_{dd}	S	Data output delay	-	10	ns	25

Figure 20. SAI Output Timings (SAI, I^2S)



4.16 SPI (SSP) Timing Interface

4.16.1 SPI Master Mode (SPH=0)

Table 49. SPI master mode (SPH=0)

Symbol		Parameter	Timing		Unit	Cload [pF]
			Min	Max		
F_{ck}	S	Clock frequency	-	52	MHz	25
t_{SUI}	S	Input setup time	7	-	ns	25
t_{HI}	S	Input hold time	2	-	ns	15
t_{DO_Master}	S	Data output delay	-	5	ns	25
t_{HO}	S	Data hold time	0	-	ns	25

Figure 21. SPI Timings

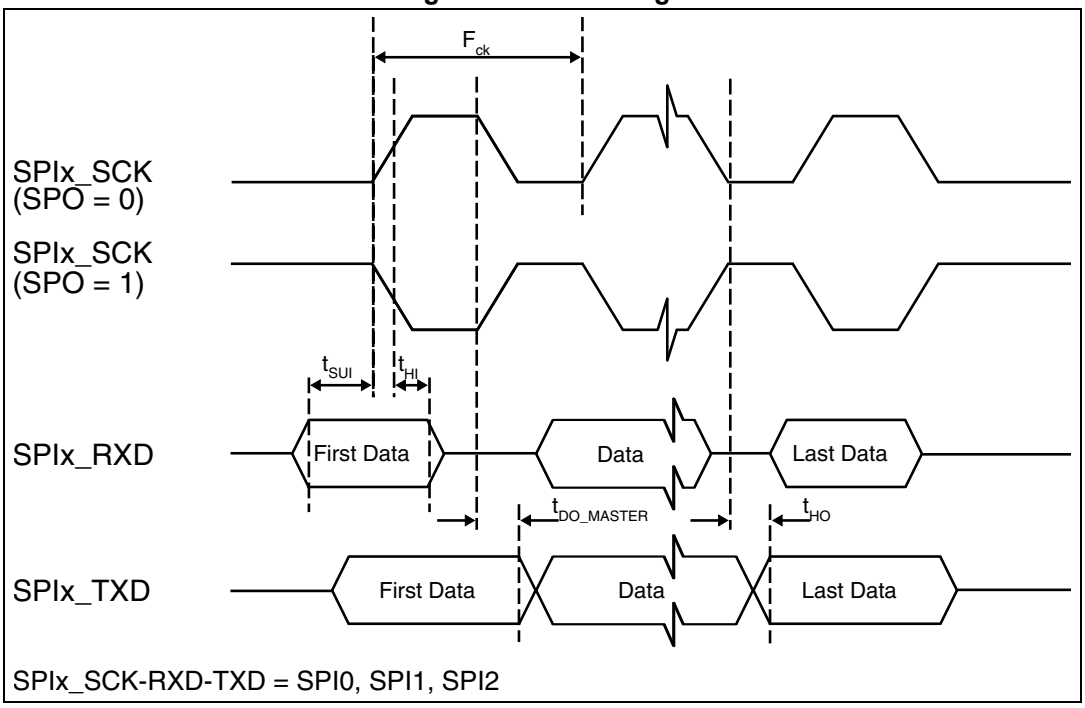


Figure 22. SPI Frame Format (Single transfer) with SPO = 0b and SPH = 0b

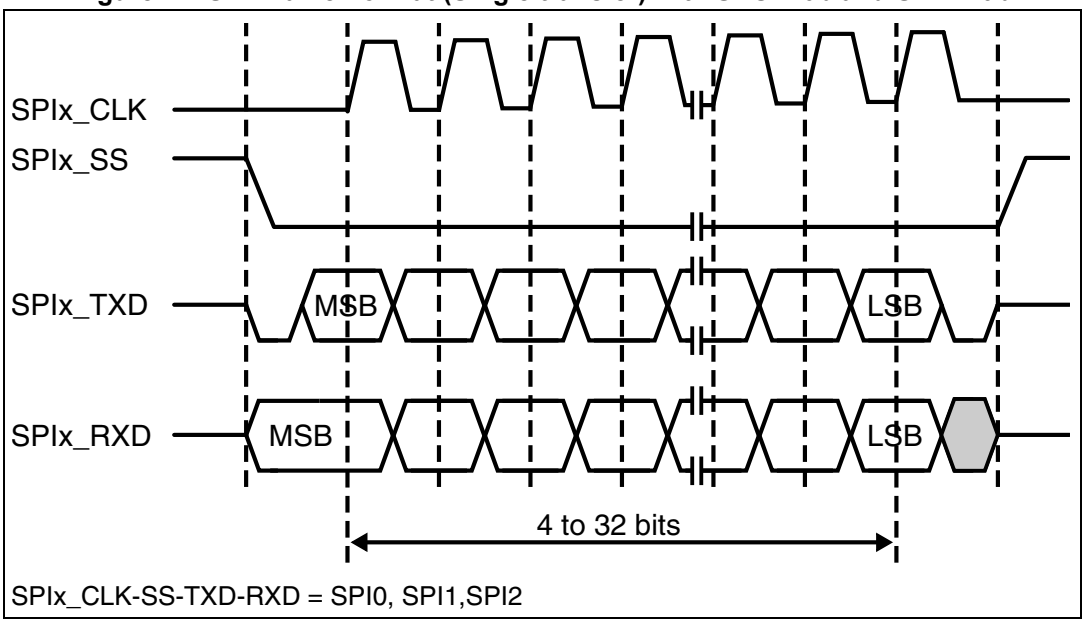
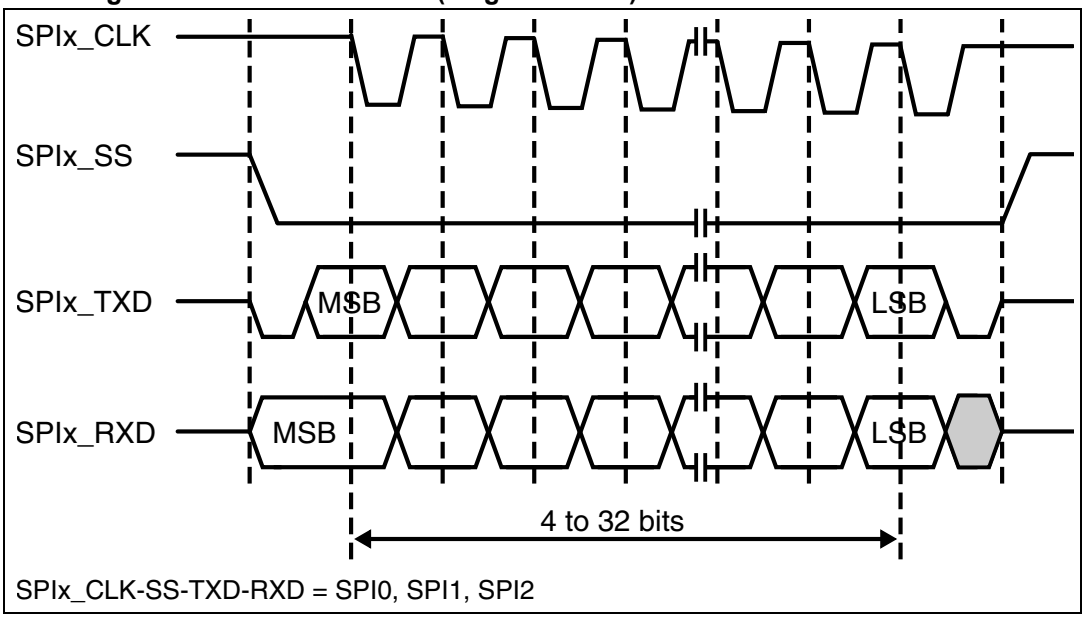


Figure 23. SPI frame format (single transfer) with SPO = 1b and SPH = 0b

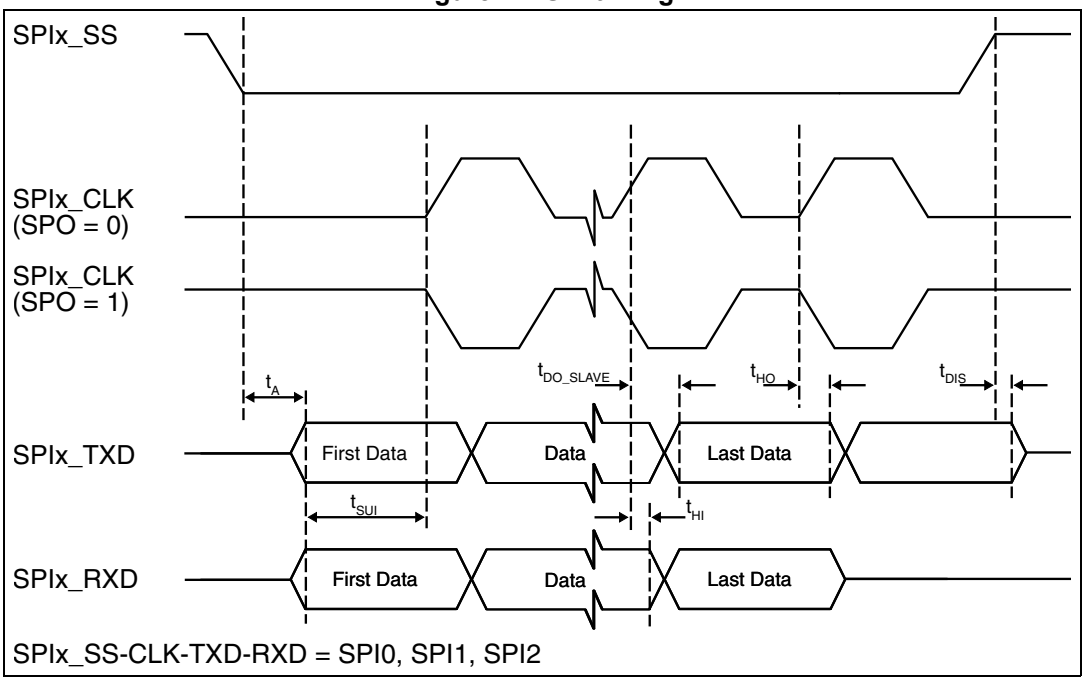


4.16.2 SPI Slave Mode (SPH=0)

Table 50. SPI slave mode (SPH=0)

Symbol		Parameter	Timing		Unit	Cload [pF]
			Min	Max		
F_{ck}	S	Clock frequency	-	8.68	MHz	25
t_{SUI}	S	Input setup time	4	-	ns	25
t_{HI}	S	Input hold time	-	2	ns	15
t_{DO_Slave}	S	Data output delay	-	12	ns	25
t_{HO}	S	Data hold time	-	4	ns	25
t_A	S	Data valid after start of frame	12	-	ns	25
t_{DIS}	S	Data valid after end of frame	0	12	ns	25

Figure 24. SPI timing



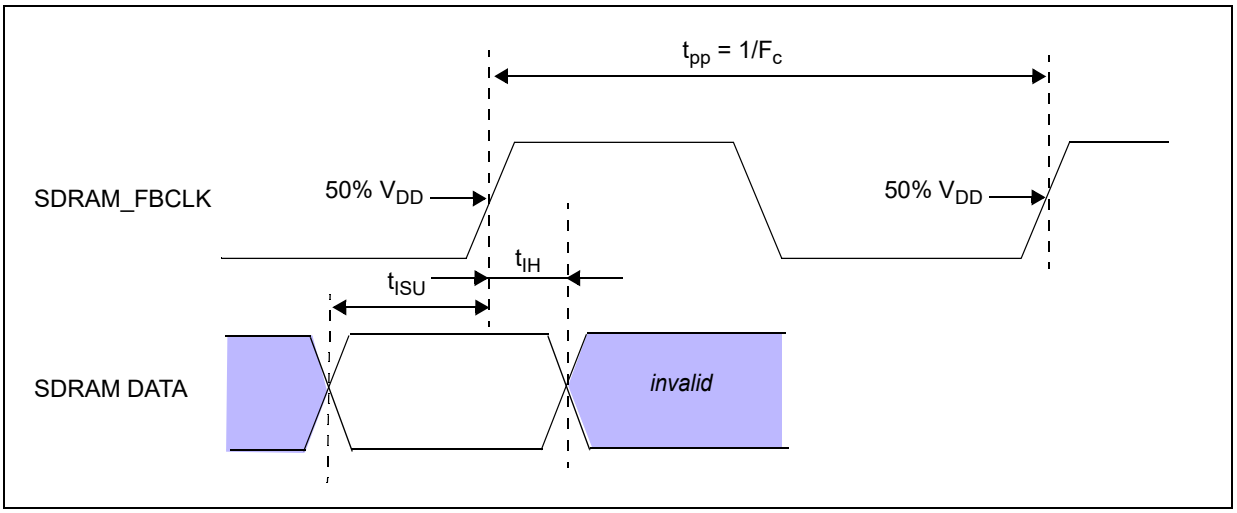
4.17 SDRAM Interface Timing

4.17.1 SDRAM Interface Input Timings

Table 51. SDRAM Input Timings

Symbol		Parameter	Timing		Unit	Cload [pF]
			Min	Max		
F_c	S	Clock frequency	-	166	MHz	10
t_{ISU}	S	Input setup time	0.3	-	ns	-
t_{IH}	S	Input hold time	1.5	-	ns	-

Figure 25. SDRAM Input Timings



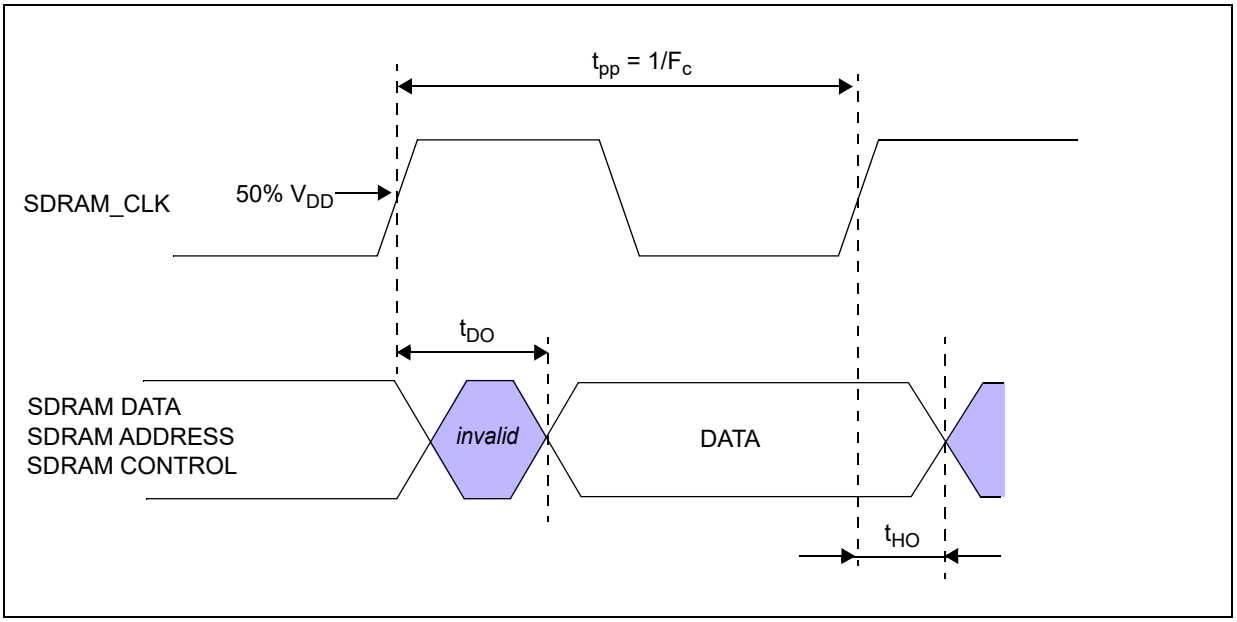
4.17.2 SDRAM Interface Output Timings

Table 52. SDRAM Output Timings

Symbol		Parameter	Timing		Unit	Cload [pF]
			Min	Max		
F_c	S	Clock frequency		166	MHz	10
t_{DO}	S	Data output delay@166MHZ(1)		3.6	ns	10
t_{HO}	S	Data hold time	1		ns	10

1. Internally data is launched at the negative edge of the clock. The output delay can be expressed as 1/Fc*0.55+.3. The multiplication factor 0f 0.55 is used to represent the duty cycle variation of the clock due to IO pads. 0.3 ns is the data travel time from the flop to the IO pad. At 112 MHz the max data output delay is 5.19 ns.

Figure 26. SDRAM Output Timings



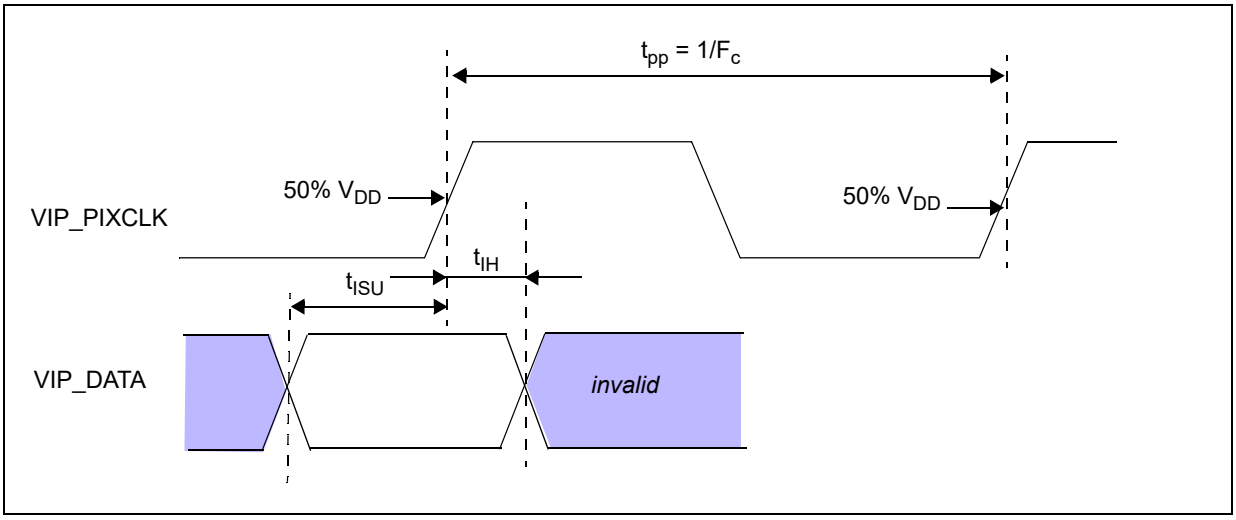
Note: Input timings referred to SDRAM_FBCLK input.
Output timings referred to SDRAM_CLK output.

4.18 VIP Timings

Table 53. VIP Input Timings

Symbol		Parameter	Timing		Unit	Cload [pF]
			Min	Max		
F_c	S	Clock frequency	-	60	MHz	25
t_{ISU}	S	Input setup time	3	-	ns	
t_{IH}	S	Input hold time	0.4	-	ns	

Figure 27. VIP Input Timings

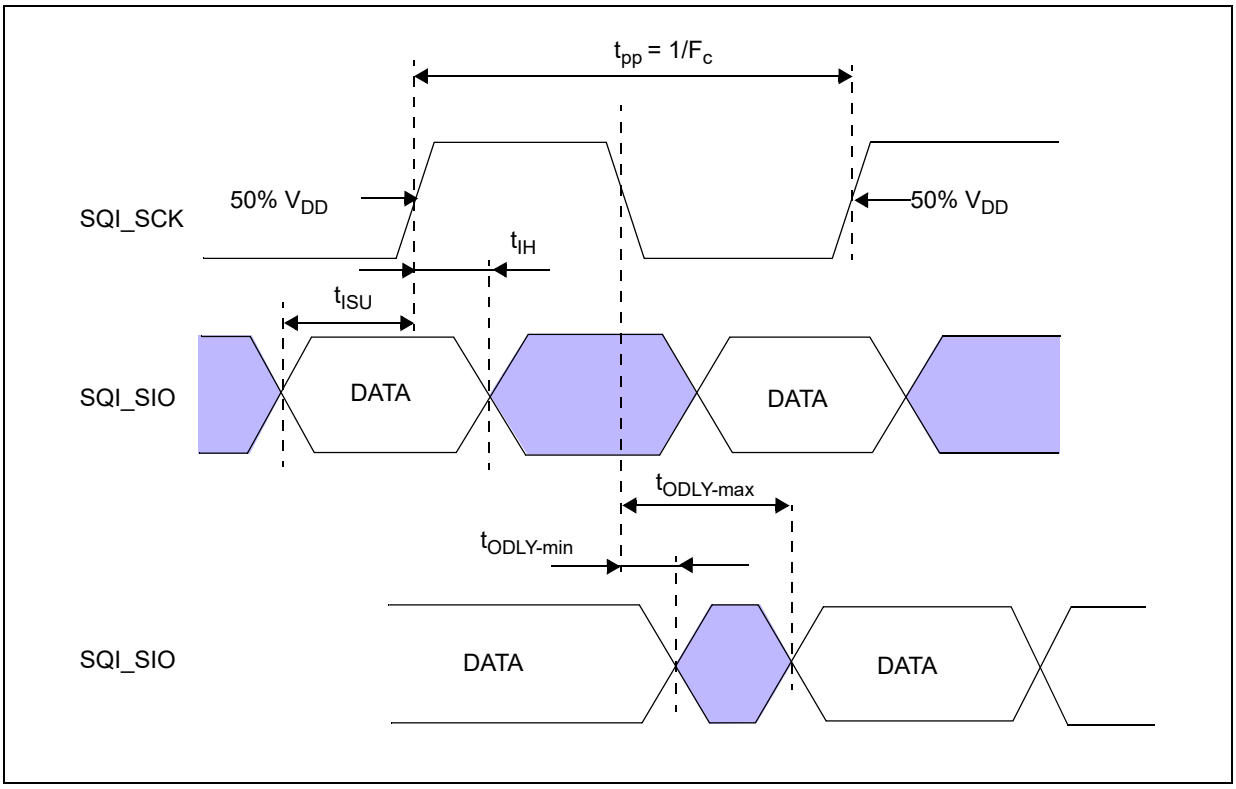


4.19 SQI Timings

Table 54. SQI Timings

Symbol		Parameter	Timing		Unit	Cload [pF]
			Min	Max		
F_c	S	Clock frequency	-	125	MHz	20
t_{ISU}	S	Input setup time	0	-	ns	20
t_{IH}	S	Input hold time	2.5	-	ns	20
$t_{ODLY-max}$	S	Data output delay	-	1	ns	20
$t_{ODLY-min}$	S	Data hold time	0	-	ns	20

Figure 28. SQI Timings



4.19.1 SQI Bit Clock Generation

The SQI serial bitclock (SQI_SCK) is generated dividing the peripheral input master clock SQI_CLK.

The division factor is controlled by the bits [7:0] of the SQI_CONF_REG1 of the SQI controller:

Bit 7:0 SPI_CLK_DIV (SQI master clock divider)

0x00, 0x01 = divide by 2

0x02, 0x03 = divide by 4

0x04, 0x05 = divide by 6

…

0xFE, 0xFF = divide by 256

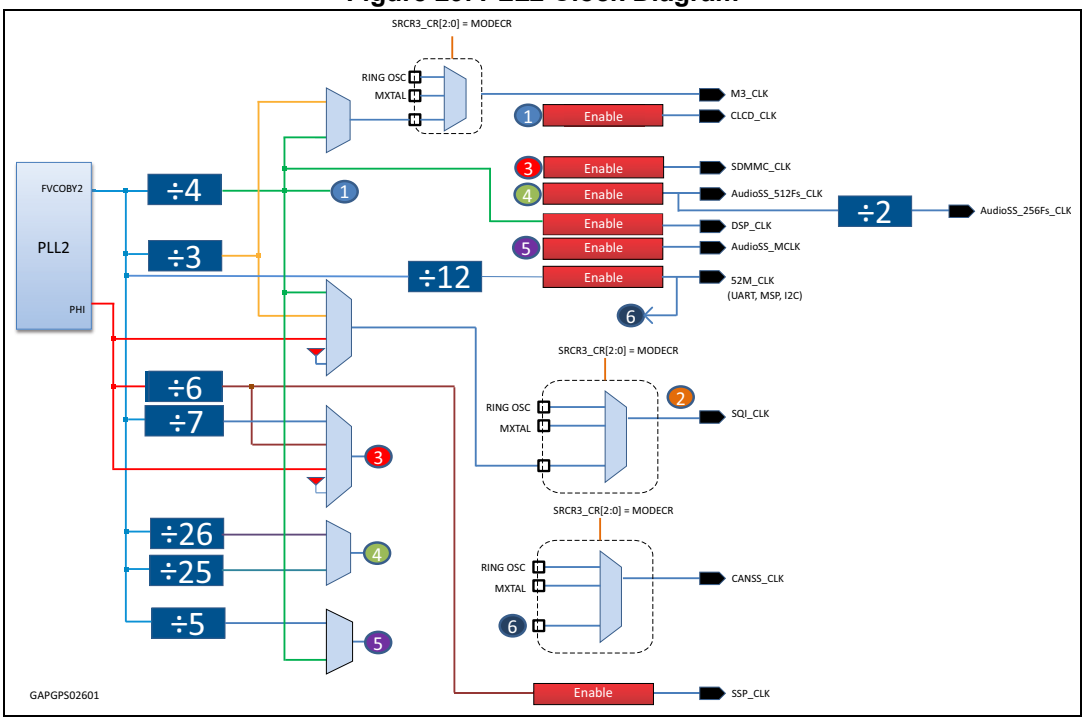
The SQI peripheral is accessed by the system bus masters through the bus matrix. The clock of the bus matrix is HCLK.

A frequency clock relationship must be respected in the configuration of the SQI clock between SQI_CLK and HCLK, as reported in the *Chapter 4.19.2: Clock Constraint*. This condition must be respected to ensure that the system works correctly in all voltage, temperature and process conditions.

SQI_CLK Clock Generation

The SQI master clock SQI_CLK is generated dividing the PLL2 output clock, according to the following picture:

Figure 29. PLL2 Clock Diagram



The SQI_CLK generation is controlled by the bits [2:1] of SRCM3_CLKDIV register of the SRC-M3 peripheral. The field SRCM3_CLKDIV[2:1] = SQI_CLK_SEL decodes as follows:

Bit 2:1 SQI_CLK_SEL

0b00 = PLL2.FVCOBY2 divide by 4 is selected

0b01 = PLL2.FVCOBY2 divide by 3 is selected

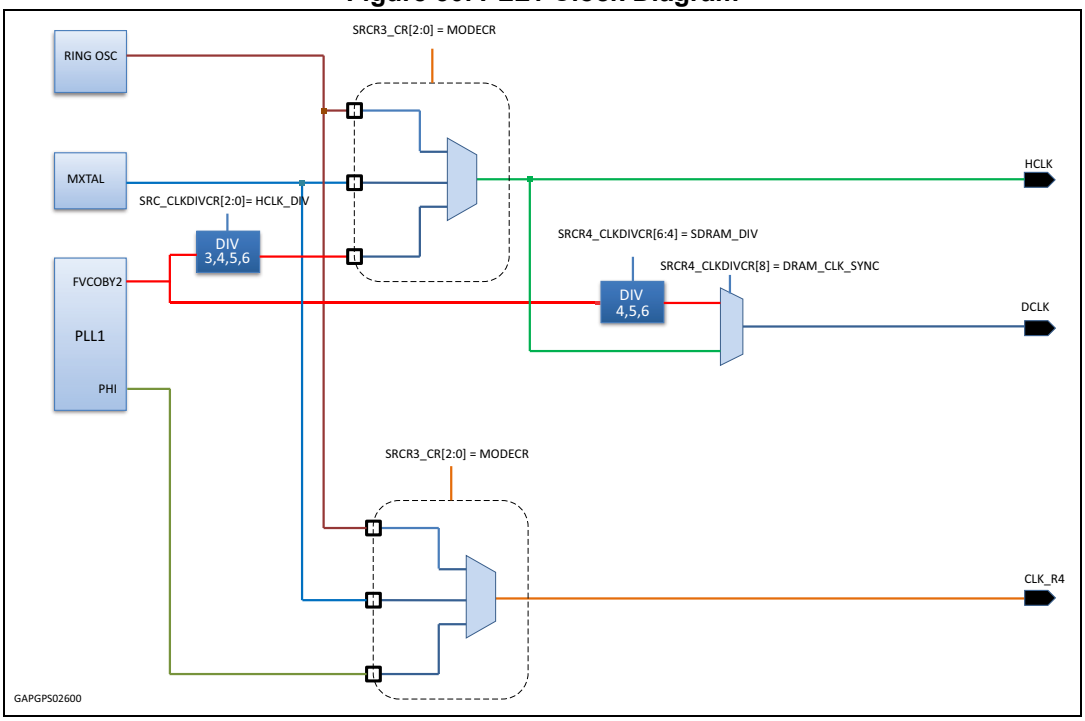
0b10 = PLL2.PHI is selected

0b11 = Reserved

HCLK Clock Generation

The HCLK clock is the main clock of the system. This is the clock used by the bus matrix and the AHB or APB bridges, for the VIC, for the system timers (MTU0 and MTU1), the watchdog and the embedded static RAM (eSRAM). HCLK is generated dividing the PLL1 output clock according to the following picture:

Figure 30. PLL1 Clock Diagram



The clock selected for HCLK is controlled by bits [2:0] of the SRCM3_CR registers:

Bit 2:0 Mode Control

Bit [0]: Internal Oscillator

Bit [1]: External Oscillator

Bit [3]: Normal

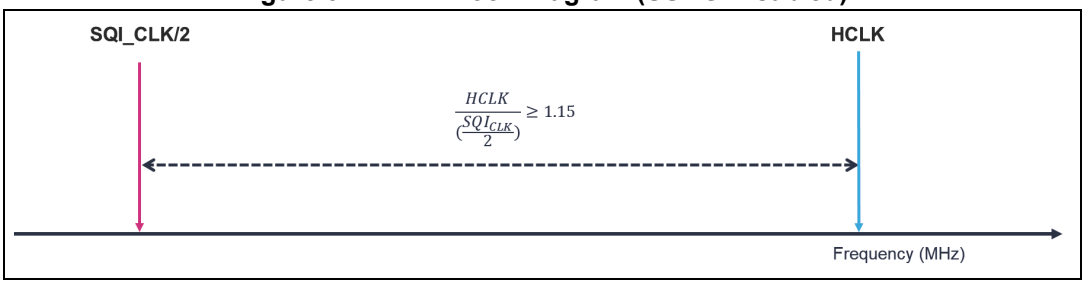
When the system is running in Normal mode, Bit [3] is set and HCLK is generated by the output of PLL1. HCLK can run up to 208 MHz.

4.19.2 Clock Constraint

A frequency clock relationship must be always respected in the configuration of HCLK and SQI_CLK. This condition must be respected to ensure that the system works correctly in all voltage, temperature and process conditions.

PLL1 SSCG (Spread Spectrum Clock Generation) Disabled

Figure 31. PLL1 Clock Diagram (SSCG Disabled)

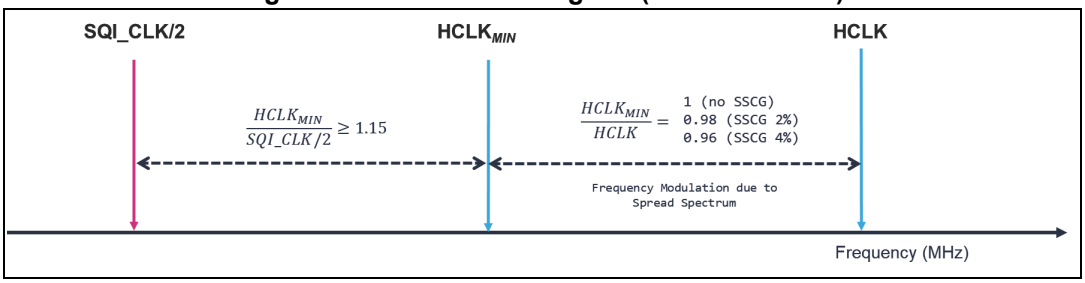


The constraint to be respected is:

$$HCLK \geq \left(\frac{SQI\_CLK}{2}\right) \bullet 1.15$$

PLL1 SSCG (Spread Spectrum Clock Generation) Enabled

Figure 32. PLL1 Clock Diagram (SSCG Enabled)



The constraint to be respected is:

$$HCLK_{MIN} \geq \left(\frac{SQI\_CLK}{2}\right) \bullet 1.15$$

If the Spread Spectrum clock modulation is applied in the configuration of PLL1, the real clock will be modulated between HCLK and $HCLK_{MIN}$, so the minimum frequency of HCLK ($HCLK_{MIN}$) will be lower than HCLK by 2 % or 4 % depending on the configured modulation width. With respect to HCLK, the constraint is expressed as:

$$HCLK \geq \left(\frac{SQI\_CLK}{2}\right) \bullet \frac{1.15}{1 - SSCG}$$

where SSCG = 0, 0.02, 0.04

5 Ball list

Legenda:

- PU: under reset and out of reset, until software different programming, defaults to pull-up.
- PD: under reset and out of reset, until software different programming, defaults to pull-down.
- Disabled: under reset and out of reset, until software different programming, pull is disabled.
- - : pull (up or down) is not implemented.
- RESET DIR: direction under reset and out of reset, until software different programming.

5.1 STA1080, STA1085 Ball list

Table 55. STA108x Ball list

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
A1	OTP_FUSE_HV	-	NA	NA
A2	GPIO41	PU	GPIO Input	GPIO Input
A3	GPIO42	PU	GPIO Input	GPIO Input
A4	GPIO43	PU	GPIO Input	GPIO Input
A5	S_GPIO3	PU	GPIO Input	GPIO Input
A6	GPIO15	PU	GPIO Input	GPIO Input
A7	GPIO14	PU	GPIO Input	GPIO Input
A8	GPIO9	PU	GPIO Input	GPIO Input
A9	GPIO8	PU	GPIO Input	GPIO Input
A10	GPIO21	PU	GPIO Input	GPIO Input
A11	GPIO0	PU	GPIO Input	GPIO Input
A12	M3_GPIO13	PU	GPIO Input	GPIO Input
A13	M3_ONOFF	Disabled	Input	Input
A14	M3_VDDOK	Disabled	Input	Input
A15	M3_IGNKEY	Disabled	Input	Input
A16	M3_GPIO5	PD	GPIO Input	GPIO Input
A17	M3_GPIO6	PD	GPIO Input	GPIO Input
A18	M3_GPIO7	PD	GPIO Input	GPIO Input
A19	GND	-	NA	NA
B1	GPIO40	PU	GPIO Input	GPIO Input
B2	M3_GPIO15	PU	GPIO Input	GPIO Input

Table 55. STA108x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
B3	GPIO35	PU	GPIO Input	GPIO Input
B4	GPIO34	PU	GPIO Input	GPIO Input
B5	GPIO44	PU	GPIO Input	GPIO Input
B6	SYSRSTn	PU	Input	Input
B7	M3_GPIO8	PU	GPIO Input	GPIO Input
B8	GPIO13	PU	GPIO Input	GPIO Input
B9	GPIO12	PU	GPIO Input	GPIO Input
B10	GPIO7	PU	GPIO Input	GPIO Input
B11	GPIO20	PU	GPIO Input	GPIO Input
B12	GPIO1	PU	GPIO Input	GPIO Input
B13	GPIO5	PU	GPIO Input	GPIO Input
B14	M3_LVI	Disabled	Input	Input
B15	M3_PWREN	-	Output	Output
B16	M3_GPIO2	PD	GPIO Input	GPIO Input
B17	DAC_VHI	-	NA	NA
B18	DAC_OUT1L	-	Output	Output
B19	DAC_OUT2R	-	Output	Output
C1	M3_GPIO11	PU	GPIO Input	GPIO Input
C2	SQI_SIO3	PU	Input	Input
C3	M3_GPIO14	PU	GPIO Input	GPIO Input
C4	GPIO45	PU	GPIO Input	GPIO Input
C5	S_GPIO2	PU	GPIO Input	GPIO Input
C6	M3_GPIO9	PU	GPIO Input	GPIO Input
C7	I2C0_SCL	PU	Input	Input
C8	GPIO10	PU	GPIO Input	GPIO Input
C9	GPIO16	PU	GPIO Input	GPIO Input
C10	GPIO19	PU	GPIO Input	GPIO Input
C11	M3_GPIO12	PU	GPIO Input	GPIO Input
C12	GPIO2	PU	GPIO Input	GPIO Input
C13	GPIO4	PU	GPIO Input	GPIO Input
C14	M3_SXTALI	-	Input	Input
C15	M3_GPIO0	PD	GPIO Input	GPIO Input
C16	M3_GPIO3	PD	GPIO Input	GPIO Input
C17	DAC_VLO	-	NA	NA

Table 55. STA108x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
C18	DAC_OUT0L	-	Output	Output
C19	DAC_OUT2L	-	Output	Output
D1	SQI_SCK	-	Output	Input
D2	SQI_SIO1	PU	Input	Input
D3	SQI_CE0n	-	Output	Input
D4	SQI_SIO0	-	Output	Input
D5	GPIO46	PU	GPIO Input	GPIO Input
D6	S_GPIO0	PU	GPIO Input	GPIO Input
D7	S_GPIO1	PU	GPIO Input	GPIO Input
D8	I2C0_SDA	PU	Input	Input
D9	GPIO11	PU	GPIO Input	GPIO Input
D10	GPIO17	PU	GPIO Input	GPIO Input
D11	GPIO18	PU	GPIO Input	GPIO Input
D12	GPIO3	PU	GPIO Input	GPIO Input
D13	M3_CLK32KOUT	-	Output	Output
D14	M3_SXTALO	-	Output	Output
D15	M3_GPIO1	PD	GPIO Input	GPIO Input
D16	M3_GPIO4	PD	GPIO Input	GPIO Input
D17	DAC_VCOM	-	NA	NA
D18	DAC_OUT0R	-	Output	Output
D19	DAC_OUT1R	-	Output	Output
E1	SQI_SIO2	PU	Input	Input
E2	GPIO6	PU	GPIO Input	GPIO Input
E3	GPIO47	PU	GPIO Input	GPIO Input
E4	GPIO48	PU	GPIO Input	GPIO Input
E5	M3_GPIO10	PU	GPIO Input	GPIO Input
E6	VDD_IO	-	NA	NA
E7	VDD_IO	-	NA	NA
E8	VDD_IO	-	NA	NA
E9	VDD	-	NA	NA
E10	VDD	-	NA	NA
E11	JTAGSEL	PD	Input	Input
E12	ADC2_VREFN	-	NA	NA
E13	VDD_IO_ON	-	NA	NA

Table 55. STA108x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
E14	VDD_ON_VREG	-	NA	NA
E15	MIC_BIAS	-	NA	NA
E16	ADC2_AIN9	-	Input	Input
E17	ADC2_AIN6	-	Input	Input
E18	ADC2_AIN7	-	Input	Input
E19	ADC2_AIN4	-	Input	Input
F1	GPIO90	PU	GPIO Input	GPIO Input
F2	GPIO91	PU	GPIO Input	GPIO Input
F3	GPIO92	PU	GPIO Input	GPIO Input
F4	GPIO93	PU	GPIO Input	GPIO Input
F5	GPIO49	PU	GPIO Input	GPIO Input
F6	VDD	-	NA	NA
F7	VDD_IO	-	NA	NA
F8	VDD_IO	-	NA	NA
F9	VDD	-	NA	NA
F10	OSC32K_GND	-	NA	NA
F11	GND	-	NA	NA
F12	GND	-	NA	NA
F13	ADC2_AGND	-	NA	NA
F14	DAC_AGND	-	NA	NA
F15	ADC2_VREFP	-	NA	NA
F16	ADC0_AIN2_L	-	Input	Input
F17	ADC0_AIN2_R	-	Input	Input
F18	ADC0_AIN1_L	-	Input	Input
F19	ADC0_AIN1_R	-	Input	Input
G1	GPIO94	PU	GPIO Input	GPIO Input
G2	GPIO95	PU	GPIO Input	GPIO Input
G3	GPIO96	Disabled	ALTB Output. Low.	ALTB Output. Low.
G4	GPIO97	Disabled	ALTB Output. Low.	ALTB Output. Low.
G5	VDD	-	NA	NA
G6	VDD_IO	-	NA	NA
G7	GND	-	NA	NA
G8	GND	-	NA	NA
G9	GND	-	NA	NA

Table 55. STA108x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
G10	GND	-	NA	NA
G11	GND	-	NA	NA
G12	GND	-	NA	NA
G13	ADC2_AVDD	-	NA	NA
G14	DAC_I/O_AGND	-	NA	NA
G15	DAC_AVDD	-	NA	NA
G16	ADC2_AIN3_YN	-	HighZ	HighZ
G17	ADC2_AIN2_YP	-	HighZ	HighZ
G18	ADC1_MICIN_P	-	Input	Input
G19	ADC1_MICIN_N	-	Input	Input
H1	GPIO98	Disabled	ALTB Output. Low.	ALTB Output. Low.
H2	GPIO99	PU	GPIO Input	GPIO Input
H3	GPIO100	Disabled	ALTB Output. Low.	ALTB Output. Low.
H4	GPIO101	Disabled	ALTB Output. Low.	ALTB Output. Low.
H5	VDD	-	NA	NA
H6	VDD_IO	-	NA	NA
H7	GND	-	NA	NA
H8	GND	-	NA	NA
H9	GND	-	NA	NA
H10	GND	-	NA	NA
H11	GND	-	NA	NA
H12	GND	-	NA	NA
H13	USB_VREG3V3_1V1	-	NA	NA
H14	ADC0_1_AVDD	-	NA	NA
H15	DAC_I/O_AVDD	-	NA	NA
H16	ADC2_AIN5	-	Input	Input
H17	ADC2_AIN0_XP	-	HighZ	HighZ
H18	ADC1_AIN1_P	-	Input	Input
H19	ADC1_AIN1_N	-	Input	Input
J1	GPIO102	Disabled	ALTB Output. Low.	ALTB Output. Low.
J2	GPIO103	Disabled	ALTB Output. Low.	ALTB Output. Low.
J3	GPIO104	Disabled	ALTB Output. Low.	ALTB Output. Low.
J4	GPIO105	Disabled	ALTB Output. High.	ALTB Output. High.
J5	VDD	-	NA	NA

Table 55. STA108x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
J6	VDD_IO	-	NA	NA
J7	GND	-	NA	NA
J8	GND	-	NA	NA
J9	GND	-	NA	NA
J10	GND	-	NA	NA
J11	GND	-	NA	NA
J12	GND	-	NA	NA
J13	USB_VREG3V3_1V8	-	NA	NA
J14	ADC0_1_AGND	-	NA	NA
J15	ADC0_1_VRFP	-	NA	NA
J16	ADC0_1_VRFN	-	NA	NA
J17	ADC0_1_VCM	-	NA	NA
J18	ADC2_AIN8	-	Input	Input
J19	ADC2_AIN1_XN	-	HighZ	HighZ
K1	I2S0_TX	PU	Input	Input
K2	I2S0_RX	PU	Input	Input
K3	UART0_RX	PU	Input	Input
K4	UART0_TX	-	Output	Output
K5	VDD	-	NA	NA
K6	VDD_IO	-	NA	NA
K7	GND	-	NA	NA
K8	GND	-	NA	NA
K9	GND	-	NA	NA
K10	GND	-	NA	NA
K11	GND	-	NA	NA
K12	GND	-	NA	NA
K13	USB1_VDD3V3	-	NA	NA
K14	USB_BGEXT	-	NA	NA
K15	USB_1.8VREG	-	NA	NA
K16	USB_1.1VREG	-	NA	NA
K17	USB0_AGND	-	NA	NA
K18	USB1_DN	-	NA	NA
K19	USB1_DP	-	NA	NA
L1	I2S0_BCLK	PU	Input	Input

Table 55. STA108x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
L2	I2S0_FS	PU	Input	Input
L3	UART0_CTS	PU	Input	Input
L4	UART0_RTS	-	Output	Output
L5	VDD	-	NA	NA
L6	VDD_IO	-	NA	NA
L7	GND	-	NA	NA
L8	GND	-	NA	NA
L9	GND	-	NA	NA
L10	GND	-	NA	NA
L11	GND	-	NA	NA
L12	GND	-	NA	NA
L13	VDD_IO	-	NA	NA
L14	USB0_VDD3V3	-	NA	NA
L15	USB_KELVIN_TERM	-	NA	NA
L16	COMP0	-	NA	NA
L17	USB1_AGND	-	NA	NA
L18	USB0_DN	-	NA	NA
L19	USB0_DP	-	NA	NA
M1	GPIO30	PU	GPIO Input	GPIO Input
M2	GPIO33	PU	GPIO Input	GPIO Input
M3	GPIO32	PU	GPIO Input	GPIO Input
M4	GPIO31	PU	GPIO Input	GPIO Input
M5	VDD	-	NA	NA
M6	VDD_IO	-	NA	NA
M7	VDD_IO	-	NA	NA
M8	VDD_IO	-	NA	NA
M9	VDD_IO	-	NA	NA
M10	VDD_IO	-	NA	NA
M11	VDD_IO	-	NA	NA
M12	VDD_IO	-	NA	NA
M13	VDD_IO	-	NA	NA
M14	VDD_IO	-	NA	NA
M15	PLL_GND	-	NA	NA
M16	XOSC_VDD	-	NA	NA

Table 55. STA108x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
M17	VREG_BYPASS	-	Input	Input
M18	USB_REXT	-	NA	NA
M19	GPIO28	PU	GPIO Input	GPIO Input
N1	SPI0_SCK	-	Output	Output
N2	SPI0_SS	PU	Input	Input
N3	SPI0_RXD	PU	Input	Input
N4	SPI0_TXD	PU	Input	Input
N5	VDD	-	NA	NA
N6	VDD	-	NA	NA
N7	VDD_IO	-	NA	NA
N8	VDD_IO	-	NA	NA
N9	VDD_IO	-	NA	NA
N10	VDD	-	NA	NA
N11	VDD	-	NA	NA
N12	VDD	-	NA	NA
N13	VDD	-	NA	NA
N14	NC	-	-	-
N15	PLL_VREG3.3V	-	NA	NA
N16	GPIO26	PU	GPIO Input	GPIO Input
N17	GPIO27	PU	GPIO Input	GPIO Input
N18	MXTALO	-	Output	Output
N19	MXTALI	-	Input	Input
P1	S_GPIO7	PU	GPIO Input	GPIO Input
P2	S_GPIO6	PU	GPIO Input	GPIO Input
P3	S_GPIO5	PU	GPIO Input	GPIO Input
P4	S_GPIO4	PU	GPIO Input	GPIO Input
P5	NC	-	-	-
P6	NC	-	-	-
P7	NC	-	-	-
P8	NC	-	-	-
P9	NC	-	-	-
P10	NC	-	-	-
P11	NC	-	-	-
P12	NC	-	-	-

Table 55. STA108x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
P13	NC	-	-	-
P14	NC	-	-	-
P15	NC	-	-	-
P16	SDMMC0_DATA_1	PU	Input	Input
P17	SDMMC0_DATA_2	-	Output	Output
P18	SDMMC0_CMD	PU	Input	Input
P19	GPIO29	PU	GPIO Input	GPIO Input
R1	GPIO22	PU	GPIO Input	GPIO Input
R2	GPIO23	PU	GPIO Input	GPIO Input
R3	GPIO24	PU	GPIO Input	GPIO Input
R4	GPIO25	PU	GPIO Input	GPIO Input
R5	NC	-	-	-
R6	NC	-	-	-
R7	NC	-	-	-
R8	NC	-	-	-
R9	NC	-	-	-
R10	NC	-	-	-
R11	NC	-	-	-
R12	NC	-	-	-
R13	NC	-	-	-
R14	NC	-	-	-
R15	NC	-	-	-
R16	SDMMC0_DATA_0	-	Output	Output
R17	SDMMC0_DATA_3	PU	Input	Input
R18	SDMMC0_CLK	-	Output	Output
R19	GPIO39	PU	GPIO Input	GPIO Input
T1	JTAG_TDI	PU	Input	Input
T2	JTAG_TDO	-	Output	Output
T3	JTAG_TCK	-	Input	Input
T4	JTAG_TMS	PU	Input	Input
T5	NC	-	-	-
T6	NC	-	-	-
T7	NC	-	-	-
T8	NC	-	-	-

Table 55. STA108x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
T9	NC	-	-	-
T10	NC	-	-	-
T11	NC	-	-	-
T12	NC	-	-	-
T13	NC	-	-	-
T14	NC	-	-	-
T15	NC	-	-	-
T16	GPIO37	PU	GPIO Input	GPIO Input
T17	GPIO36	PD	GPIO Input	GPIO Input
T18	GPIO38	PU	GPIO Input	GPIO Input
T19	GPIO70	Disabled	ALTB Output. High.	ALTB Output. High.
U1	GPIO76	PU	ALTB Input	ALTB Input
U2	JTAG_TRSTn	PD	Input	Input
U3	NC	-	-	-
U4	NC	-	-	-
U5	NC	-	-	-
U6	NC	-	-	-
U7	NC	-	-	-
U8	NC	-	-	-
U9	NC	-	-	-
U10	NC	-	-	-
U11	NC	-	-	-
U12	NC	-	-	-
U13	NC	-	-	-
U14	NC	-	-	-
U15	NC	-	-	-
U16	NC	-	-	-
U17	NC	-	-	-
U18	GPIO68	Disabled	ALTB Output. Low.	ALTB Output. Low.
U19	GPIO69	Disabled	ALTB Output. High.	ALTB Output. High.
V1	GPIO77	Disabled	ALTB Output. Low.	ALTB Output. Low.
V2	GPIO78	Disabled	ALTB Output. Low.	ALTB Output. Low.
V3	GPIO80	Disabled	ALTB Output. Low.	ALTB Output. Low.
V4	GPIO74	Disabled	ALTB Output. Low.	ALTB Output. Low.

Table 55. STA108x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
V5	GPIO84	Disabled	ALTB Output. High.	ALTB Output. High.
V6	GPIO82	Disabled	ALTB Output. Low.	ALTB Output. Low.
V7	GPIO86	Disabled	ALTB Output. High.	ALTB Output. High.
V8	GPIO50	Disabled	ALTB Output. Low.	ALTB Output. Low.
V9	GPIO64	Disabled	ALTB Output. Low.	ALTB Output. Low.
V10	GPIO62	Disabled	ALTB Output. Low.	ALTB Output. Low.
V11	GPIO60	Disabled	ALTB Output. Low.	ALTB Output. Low.
V12	GPIO58	Disabled	ALTB Output. Low.	ALTB Output. Low.
V13	GPIO56	PU	ALTB Input	ALTB Input
V14	GPIO53	PU	ALTB Input	ALTB Input
V15	GPIO87	PU	ALTB Input	ALTB Input
V16	GPIO85	PU	ALTB Input	ALTB Input
V17	GPIO71	PU	ALTB Input	ALTB Input
V18	GPIO65	Disabled	ALTB Output. Low.	ALTB Output. Low.
V19	GPIO66	Disabled	ALTB Output. Low.	ALTB Output. Low.
W1	GND	-	NA	NA
W2	GPIO79	PU	ALTB Input	ALTB Input
W3	GPIO75	Disabled	ALTB Output. High.	ALTB Output. High.
W4	GPIO73	Disabled	ALTB Output. High.	ALTB Output. High.
W5	GPIO81	Disabled	ALTB Output. Low.	ALTB Output. Low.
W6	GPIO83	Disabled	ALTB Output. Low.	ALTB Output. Low.
W7	GPIO51	Disabled	ALTB Output. Low.	ALTB Output. Low.
W8	GPIO54	Disabled	ALTB Output. Low.	ALTB Output. Low.
W9	GPIO63	Disabled	ALTB Output. Low.	ALTB Output. Low.
W10	GPIO61	Disabled	ALTB Output. Low.	ALTB Output. Low.
W11	GPIO59	Disabled	ALTB Output. Low.	ALTB Output. Low.
W12	GPIO57	PU	ALTB Input	ALTB Input
W13	GPIO55	PU	ALTB Input	ALTB Input
W14	GPIO52	PU	ALTB Input	ALTB Input
W15	GPIO89	PU	ALTB Input	ALTB Input
W16	GPIO88	Disabled	ALTB Output. Low.	ALTB Output. Low.
W17	GPIO72	PU	ALTB Input	ALTB Input
W18	GPIO67	Disabled	ALTB Output. Low.	ALTB Output. Low.
W19	GND	-	NA	NA

5.2 STA1090, STA1095 Ball list

Table 56. STA109x Ball list

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
A1	OTP_FUSE_HV	-	NA	NA
A2	GPIO41	PU	GPIO Input	GPIO Input
A3	GPIO42	PU	GPIO Input	GPIO Input
A4	GPIO43	PU	GPIO Input	GPIO Input
A5	S_GPIO3	PU	GPIO Input	GPIO Input
A6	GPIO15	PU	GPIO Input	GPIO Input
A7	GPIO14	PU	GPIO Input	GPIO Input
A8	GPIO9	PU	GPIO Input	GPIO Input
A9	GPIO8	PU	GPIO Input	GPIO Input
A10	GPIO21	PU	GPIO Input	GPIO Input
A11	GPIO0	PU	GPIO Input	GPIO Input
A12	M3_GPIO13	PU	GPIO Input	GPIO Input
A13	M3_ONOFF	Disabled	Input	Input
A14	M3_VDDOK	Disabled	Input	Input
A15	M3_IGNKEY	Disabled	Input	Input
A16	M3_GPIO5	PD	GPIO Input	GPIO Input
A17	M3_GPIO6	PD	GPIO Input	GPIO Input
A18	M3_GPIO7	PD	GPIO Input	GPIO Input
A19	GND	-	NA	NA
B1	GPIO40	PU	GPIO Input	GPIO Input
B2	M3_GPIO15	PU	GPIO Input	GPIO Input
B3	GPIO35	PU	GPIO Input	GPIO Input
B4	GPIO34	PU	GPIO Input	GPIO Input
B5	GPIO44	PU	GPIO Input	GPIO Input
B6	SYSRSTn	PU	Input	Input
B7	M3_GPIO8	PU	GPIO Input	GPIO Input
B8	GPIO13	PU	GPIO Input	GPIO Input
B9	GPIO12	PU	GPIO Input	GPIO Input
B10	GPIO7	PU	GPIO Input	GPIO Input
B11	GPIO20	PU	GPIO Input	GPIO Input
B12	GPIO1	PU	GPIO Input	GPIO Input
B13	GPIO5	PU	GPIO Input	GPIO Input

Table 56. STA109x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
B14	M3_LVI	Disabled	Input	Input
B15	M3_PWREN	-	Output	Output
B16	M3_GPIO2	PD	GPIO Input	GPIO Input
B17	DAC_VHI	-	NA	NA
B18	DAC_OUT1L	-	Output	Output
B19	DAC_OUT2R	-	Output	Output
C1	M3_GPIO11	PU	GPIO Input	GPIO Input
C2	SQI_SIO3	PU	Input	Input
C3	M3_GPIO14	PU	GPIO Input	GPIO Input
C4	GPIO45	PU	GPIO Input	GPIO Input
C5	S_GPIO2	PU	GPIO Input	GPIO Input
C6	M3_GPIO9	PU	GPIO Input	GPIO Input
C7	I2C0_SCL	PU	Input	Input
C8	GPIO10	PU	GPIO Input	GPIO Input
C9	GPIO16	PU	GPIO Input	GPIO Input
C10	GPIO19	PU	GPIO Input	GPIO Input
C11	M3_GPIO12	PU	GPIO Input	GPIO Input
C12	GPIO2	PU	GPIO Input	GPIO Input
C13	GPIO4	PU	GPIO Input	GPIO Input
C14	M3_SXTALI	-	Input	Input
C15	M3_GPIO0	PD	GPIO Input	GPIO Input
C16	M3_GPIO3	PD	GPIO Input	GPIO Input
C17	DAC_VLO	-	NA	NA
C18	DAC_OUT0L	-	Output	Output
C19	DAC_OUT2L	-	Output	Output
D1	SQI_SCK	-	Output	Output
D2	SQI_SIO1	PU	Input	Input
D3	SQI_CE0n	-	Output	Output
D4	SQI_SIO0	-	Output	Output
D5	GPIO46	PU	GPIO Input	GPIO Input
D6	S_GPIO0	PU	GPIO Input	GPIO Input
D7	S_GPIO1	PU	GPIO Input	GPIO Input
D8	I2C0_SDA	PU	Input	Input
D9	GPIO11	PU	GPIO Input	GPIO Input

Table 56. STA109x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
D10	GPIO17	PU	GPIO Input	GPIO Input
D11	GPIO18	PU	GPIO Input	GPIO Input
D12	GPIO3	PU	GPIO Input	GPIO Input
D13	M3_CLK32KOUT	-	Output	Output
D14	M3_SXTALO	-	Output	Output
D15	M3_GPIO1	PD	GPIO Input	GPIO Input
D16	M3_GPIO4	PD	GPIO Input	GPIO Input
D17	DAC_VCOM	-	NA	NA
D18	DAC_OUT0R	-	Output	Output
D19	DAC_OUT1R	-	Output	Output
E1	SQI_SIO2	PU	Input	Input
E2	GPIO6	PU	GPIO Input	GPIO Input
E3	GPIO47	PU	GPIO Input	GPIO Input
E4	GPIO48	PU	GPIO Input	GPIO Input
E5	M3_GPIO10	PU	GPIO Input	GPIO Input
E6	VDD_IO	-	NA	NA
E7	VDD_IO	-	NA	NA
E8	VDD_IO	-	NA	NA
E9	VDD	-	NA	NA
E10	VDD	-	NA	NA
E11	JTAGSEL	PD	Input	Input
E12	ADC2_VREFN	-	NA	NA
E13	VDD_IO_ON	-	NA	NA
E14	VDD_ON_VREG	-	NA	NA
E15	MIC_BIAS	-	NA	NA
E16	ADC2_AIN9	-	Input	Input
E17	ADC2_AIN6	-	Input	Input
E18	ADC2_AIN7	-	Input	Input
E19	ADC2_AIN4	-	Input	Input
F1	GPIO90	PU	GPIO Input	GPIO Input
F2	GPIO91	PU	GPIO Input	GPIO Input
F3	GPIO92	PU	GPIO Input	GPIO Input
F4	GPIO93	PU	GPIO Input	GPIO Input
F5	GPIO49	PU	GPIO Input	GPIO Input

Table 56. STA109x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
F6	VDD	-	NA	NA
F7	VDD_IO	-	NA	NA
F8	VDD_IO	-	NA	NA
F9	VDD	-	NA	NA
F10	OSC32K_GND	-	NA	NA
F11	GND	-	NA	NA
F12	GND	-	NA	NA
F13	ADC2_AGND	-	NA	NA
F14	DAC_AGND	-	NA	NA
F15	ADC2_VREFP	-	NA	NA
F16	ADC0_AIN2_L	-	Input	Input
F17	ADC0_AIN2_R	-	Input	Input
F18	ADC0_AIN1_L	-	Input	Input
F19	ADC0_AIN1_R	-	Input	Input
G1	GPIO94	PU	GPIO Input	GPIO Input
G2	GPIO95	PU	GPIO Input	GPIO Input
G3	GPIO96	Disabled	ALTB Output. Low.	ALTB Output. Low.
G4	GPIO97	Disabled	ALTB Output. Low.	ALTB Output. Low.
G5	VDD	-	NA	NA
G6	VDD_IO	-	NA	NA
G7	GND	-	NA	NA
G8	GND	-	NA	NA
G9	GND	-	NA	NA
G10	GND	-	NA	NA
G11	GND	-	NA	NA
G12	GND	-	NA	NA
G13	ADC2_AVDD	-	NA	NA
G14	DAC_I/O_AGND	-	NA	NA
G15	DAC_AVDD	-	NA	NA
G16	ADC2_AIN3_YN	-	HighZ	HighZ
G17	ADC2_AIN2_YP	-	HighZ	HighZ
G18	ADC1_MICIN_P	-	Input	Input
G19	ADC1_MICIN_N	-	Input	Input
H1	GPIO98	Disabled	ALTB Output. Low.	ALTB Output. Low.

Table 56. STA109x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
H2	GPIO99	PU	GPIO Input	GPIO Input
H3	GPIO100	Disabled	ALTB Output. Low.	ALTB Output. Low.
H4	GPIO101	Disabled	ALTB Output. Low.	ALTB Output. Low.
H5	VDD	-	NA	NA
H6	VDD_IO	-	NA	NA
H7	GND	-	NA	NA
H8	GND	-	NA	NA
H9	GND	-	NA	NA
H10	GND	-	NA	NA
H11	GND	-	NA	NA
H12	GND	-	NA	NA
H13	USB_VREG3V3_1V1	-	NA	NA
H14	ADC0_1_AVDD	-	NA	NA
H15	DAC_I/O_AVDD	-	NA	NA
H16	ADC2_AIN5	-	Input	Input
H17	ADC2_AIN0_XP	-	HighZ	HighZ
H18	ADC1_AIN1_P	-	Input	Input
H19	ADC1_AIN1_N	-	Input	Input
J1	GPIO102	Disabled	ALTB Output. Low.	ALTB Output. Low.
J2	GPIO103	Disabled	ALTB Output. Low.	ALTB Output. Low.
J3	GPIO104	Disabled	ALTB Output. Low.	ALTB Output. Low.
J4	GPIO105	Disabled	ALTB Output. High.	ALTB Output. High.
J5	VDD	-	NA	NA
J6	VDD_IO	-	NA	NA
J7	GND	-	NA	NA
J8	GND	-	NA	NA
J9	GND	-	NA	NA
J10	GND	-	NA	NA
J11	GND	-	NA	NA
J12	GND	-	NA	NA
J13	USB_VREG3V3_1V8	-	NA	NA
J14	ADC0_1_AGND	-	NA	NA
J15	ADC0_1_VRFP	-	NA	NA
J16	ADC0_1_VRFN	-	NA	NA

Table 56. STA109x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
J17	ADC0_1_VCM	-	NA	NA
J18	ADC2_AIN8	-	Input	Input
J19	ADC2_AIN1_XN	-	HighZ	HighZ
K1	I2S0_TX	PU	Input	Input
K2	I2S0_RX	PU	Input	Input
K3	UART0_RX	PU	Input	Input
K4	UART0_TX	-	Output	Output
K5	VDD	-	NA	NA
K6	VDD_IO	-	NA	NA
K7	GND	-	NA	NA
K8	GND	-	NA	NA
K9	GND	-	NA	NA
K10	GND	-	NA	NA
K11	GND	-	NA	NA
K12	GND	-	NA	NA
K13	USB1_VDD3V3	-	NA	NA
K14	USB_BGEXT	-	NA	NA
K15	USB_1.8VREG	-	NA	NA
K16	USB_1.1VREG	-	NA	NA
K17	USB0_AGND	-	NA	NA
K18	USB1_DN	-	NA	NA
K19	USB1_DP	-	NA	NA
L1	I2S0_BCLK	PU	Input	Input
L2	I2S0_FS	PU	Input	Input
L3	UART0_CTS	PU	Input	Input
L4	UART0_RTS	-	Output	Output
L5	VDD	-	NA	NA
L6	VDD_IO	-	NA	NA
L7	GND	-	NA	NA
L8	GND	-	NA	NA
L9	GND	-	NA	NA
L10	GND	-	NA	NA
L11	GND	-	NA	NA
L12	GND	-	NA	NA

Table 56. STA109x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
L13	VDD_IO	-	NA	NA
L14	USB0_VDD3V3	-	NA	NA
L15	USB_KELVIN_TERM	-	NA	NA
L16	COMP0	-	NA	NA
L17	USB1_AGND	-	NA	NA
L18	USB0_DN	-	NA	NA
L19	USB0_DP	-	NA	NA
M1	GPIO30	PU	GPIO Input	GPIO Input
M2	GPIO33	PU	GPIO Input	GPIO Input
M3	GPIO32	PU	GPIO Input	GPIO Input
M4	GPIO31	PU	GPIO Input	GPIO Input
M5	VDD	-	NA	NA
M6	VDD_IO	-	NA	NA
M7	VDD_IO	-	NA	NA
M8	VDD_IO	-	NA	NA
M9	VDD_IO	-	NA	NA
M10	VDD_IO	-	NA	NA
M11	VDD_IO	-	NA	NA
M12	VDD_IO	-	NA	NA
M13	VDD_IO	-	NA	NA
M14	VDD_IO	-	NA	NA
M15	PLL_GND	-	NA	NA
M16	XOSC_VDD	-	NA	NA
M17	VREG_BYPASS	-	Input	Input
M18	USB_REXT	-	NA	NA
M19	GPIO28	PU	GPIO Input	GPIO Input
N1	SPI0_SCK	-	Output	Output
N2	SPI0_SS	PU	Input	Input
N3	SPI0_RXD	PU	Input	Input
N4	SPI0_TXD	PU	Input	Input
N5	VDD	-	NA	NA
N6	VDD	-	NA	NA
N7	VDD_IO	-	NA	NA
N8	VDD_IO	-	NA	NA

Table 56. STA109x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
N9	VDD_IO	-	NA	NA
N10	VDD	-	NA	NA
N11	VDD	-	NA	NA
N12	VDD	-	NA	NA
N13	VDD	-	NA	NA
N14	GPIO130	PU	GPIO Input	GPIO Input
N15	PLL_VREG3.3V	-	NA	NA
N16	GPIO26	PU	GPIO Input	GPIO Input
N17	GPIO27	PU	GPIO Input	GPIO Input
N18	MXTALO	-	Output	Output
N19	MXTALI	-	Input	Input
P1	S_GPIO7	PU	GPIO Input	GPIO Input
P2	S_GPIO6	PU	GPIO Input	GPIO Input
P3	S_GPIO5	PU	GPIO Input	GPIO Input
P4	S_GPIO4	PU	GPIO Input	GPIO Input
P5	GPIO147	PU	GPIO Input	GPIO Input
P6	GPIO149	PU	GPIO Input	GPIO Input
P7	GPIO151	PU	GPIO Input	GPIO Input
P8	GPIO153	PU	GPIO Input	GPIO Input
P9	GPIO114	PU	GPIO Input	GPIO Input
P10	GPIO110	PU	GPIO Input	GPIO Input
P11	GPIO117	PU	GPIO Input	GPIO Input
P12	GPIO121	PU	GPIO Input	GPIO Input
P13	GPIO125	PU	GPIO Input	GPIO Input
P14	GPIO129	PU	GPIO Input	GPIO Input
P15	GPIO134	PU	GPIO Input	GPIO Input
P16	SDMMC0_DATA_1	PU	Input	Input
P17	SDMMC0_DATA_2	-	Output	Output
P18	SDMMC0_CMD	PU	Input	Input
P19	GPIO29	PU	GPIO Input	GPIO Input
R1	GPIO22	PU	GPIO Input	GPIO Input
R2	GPIO23	PU	GPIO Input	GPIO Input
R3	GPIO24	PU	GPIO Input	GPIO Input
R4	GPIO25	PU	GPIO Input	GPIO Input

Table 56. STA109x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
R5	GPIO148	PU	GPIO Input	GPIO Input
R6	GPIO142	PU	GPIO Input	GPIO Input
R7	GPIO152	PU	GPIO Input	GPIO Input
R8	GPIO154	PU	GPIO Input	GPIO Input
R9	GPIO115	PU	GPIO Input	GPIO Input
R10	GPIO111	PU	GPIO Input	GPIO Input
R11	GPIO108	PU	GPIO Input	GPIO Input
R12	GPIO120	PU	GPIO Input	GPIO Input
R13	GPIO124	PU	GPIO Input	GPIO Input
R14	GPIO128	PU	GPIO Input	GPIO Input
R15	GPIO132	PU	GPIO Input	GPIO Input
R16	SDMMC0_DATA_0	-	Output	Output
R17	SDMMC0_DATA_3	PU	Input	Input
R18	SDMMC0_CLK	-	Output	Output
R19	GPIO39	PU	GPIO Input	GPIO Input
T1	JTAG_TDI	PU	Input	Input
T2	JTAG_TDO	-	Output	Output
T3	JTAG_TCK	-	Input	Input
T4	JTAG_TMS	PU	Input	Input
T5	GPIO141	PU	GPIO Input	GPIO Input
T6	GPIO139	PU	GPIO Input	GPIO Input
T7	GPIO137	PU	GPIO Input	GPIO Input
T8	GPIO145	PU	GPIO Input	GPIO Input
T9	GPIO116	PU	GPIO Input	GPIO Input
T10	GPIO112	PU	GPIO Input	GPIO Input
T11	GPIO107	PU	GPIO Input	GPIO Input
T12	GPIO119	PU	GPIO Input	GPIO Input
T13	GPIO123	PU	GPIO Input	GPIO Input
T14	GPIO127	PU	GPIO Input	GPIO Input
T15	GPIO133	PU	GPIO Input	GPIO Input
T16	GPIO37	PU	GPIO Input	GPIO Input
T17	GPIO36	PD	GPIO Input	GPIO Input
T18	GPIO38	PU	GPIO Input	GPIO Input
T19	GPIO70	Disabled	ALTB Output. High.	ALTB Output. High.

Table 56. STA109x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
U1	GPIO76	PU	ALTB Input	ALTB Input
U2	JTAG_TRSTn	PD	Input	Input
U3	GPIO144	PU	GPIO Input	GPIO Input
U4	GPIO143	PU	GPIO Input	GPIO Input
U5	GPIO150	PU	GPIO Input	GPIO Input
U6	GPIO140	PU	GPIO Input	GPIO Input
U7	GPIO138	PU	GPIO Input	GPIO Input
U8	GPIO146	PU	GPIO Input	GPIO Input
U9	GPIO106	PU	GPIO Input	GPIO Input
U10	GPIO113	PU	GPIO Input	GPIO Input
U11	GPIO109	PU	GPIO Input	GPIO Input
U12	GPIO118	PU	GPIO Input	GPIO Input
U13	GPIO122	PU	GPIO Input	GPIO Input
U14	GPIO126	PU	GPIO Input	GPIO Input
U15	GPIO131	PU	GPIO Input	GPIO Input
U16	GPIO135	PU	GPIO Input	GPIO Input
U17	GPIO136	PU	GPIO Input	GPIO Input
U18	GPIO68	Disabled	ALTB Output. Low.	ALTB Output. Low.
U19	GPIO69	Disabled	ALTB Output. High.	ALTB Output. High.
V1	GPIO77	Disabled	ALTB Output. Low.	ALTB Output. Low.
V2	GPIO78	Disabled	ALTB Output. Low.	ALTB Output. Low.
V3	GPIO80	Disabled	ALTB Output. Low.	ALTB Output. Low.
V4	GPIO74	Disabled	ALTB Output. Low.	ALTB Output. Low.
V5	GPIO84	Disabled	ALTB Output. High.	ALTB Output. High.
V6	GPIO82	Disabled	ALTB Output. Low.	ALTB Output. Low.
V7	GPIO86	Disabled	ALTB Output. High.	ALTB Output. High.
V8	GPIO50	Disabled	ALTB Output. Low.	ALTB Output. Low.
V9	GPIO64	Disabled	ALTB Output. Low.	ALTB Output. Low.
V10	GPIO62	Disabled	ALTB Output. Low.	ALTB Output. Low.
V11	GPIO60	Disabled	ALTB Output. Low.	ALTB Output. Low.
V12	GPIO58	Disabled	ALTB Output. Low.	ALTB Output. Low.
V13	GPIO56	PU	ALTB Input	ALTB Input
V14	GPIO53	PU	ALTB Input	ALTB Input
V15	GPIO87	PU	ALTB Input	ALTB Input

Table 56. STA109x Ball list (continued)

Ball	Ball name	Pull up/down	RESET DIR (REMAP[1:0]=00,01,10)	RESET DIR (REMAP[1:0]=11)
V16	GPIO85	PU	ALTB Input	ALTB Input
V17	GPIO71	PU	ALTB Input	ALTB Input
V18	GPIO65	Disabled	ALTB Output. Low.	ALTB Output. Low.
V19	GPIO66	Disabled	ALTB Output. Low.	ALTB Output. Low.
W1	GND	-	NA	NA
W2	GPIO79	PU	ALTB Input	ALTB Input
W3	GPIO75	Disabled	ALTB Output. High.	ALTB Output. High.
W4	GPIO73	Disabled	ALTB Output. High.	ALTB Output. High.
W5	GPIO81	Disabled	ALTB Output. Low.	ALTB Output. Low.
W6	GPIO83	Disabled	ALTB Output. Low.	ALTB Output. Low.
W7	GPIO51	Disabled	ALTB Output. Low.	ALTB Output. Low.
W8	GPIO54	Disabled	ALTB Output. Low.	ALTB Output. Low.
W9	GPIO63	Disabled	ALTB Output. Low.	ALTB Output. Low.
W10	GPIO61	Disabled	ALTB Output. Low.	ALTB Output. Low.
W11	GPIO59	Disabled	ALTB Output. Low.	ALTB Output. Low.
W12	GPIO57	PU	ALTB Input	ALTB Input
W13	GPIO55	PU	ALTB Input	ALTB Input
W14	GPIO52	PU	ALTB Input	ALTB Input
W15	GPIO89	PU	ALTB Input	ALTB Input
W16	GPIO88	Disabled	ALTB Output. Low.	ALTB Output. Low.
W17	GPIO72	PU	ALTB Input	ALTB Input
W18	GPIO67	Disabled	ALTB Output. Low.	ALTB Output. Low.
W19	GND	-	NA	NA

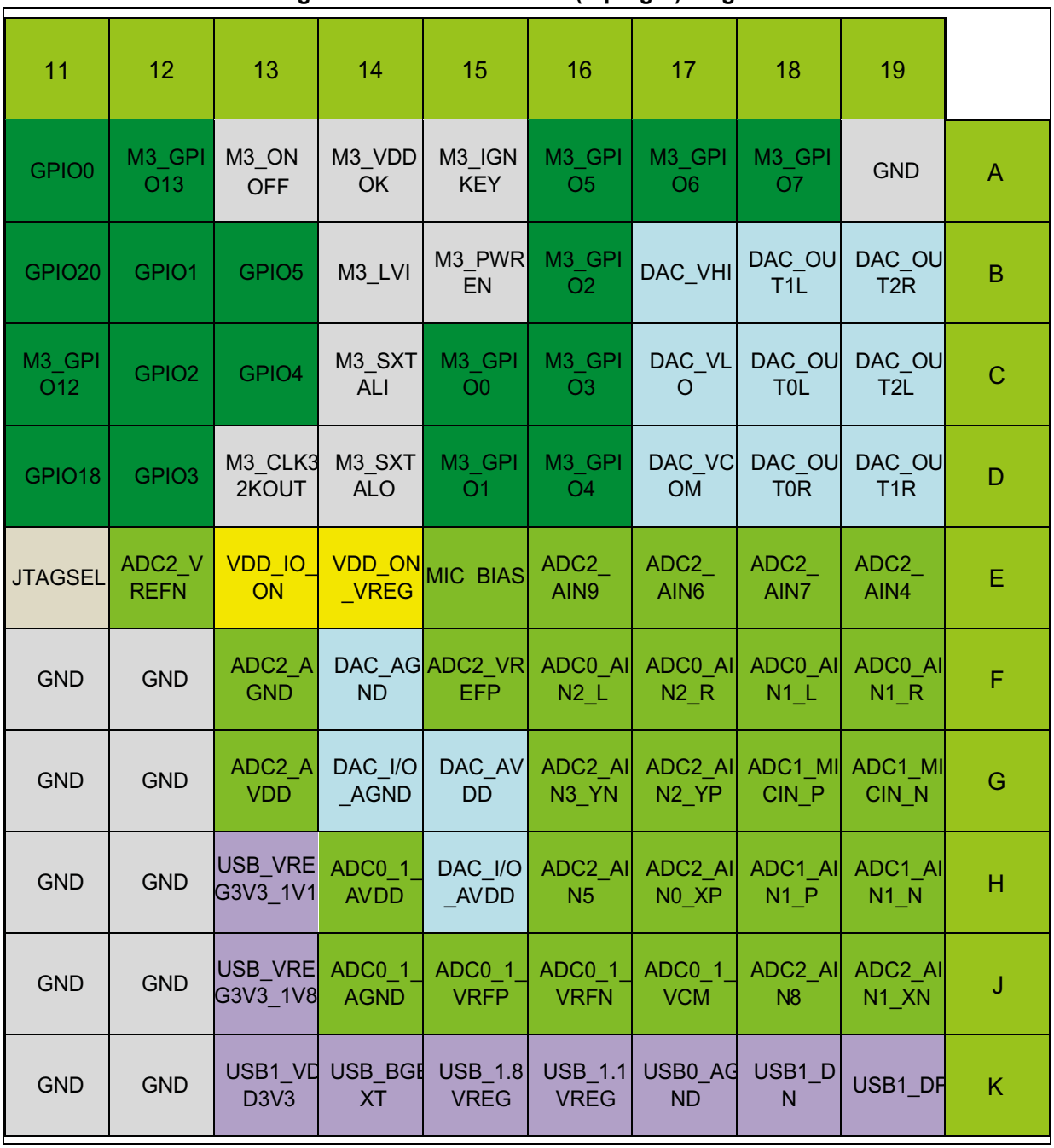
6 Ballout

6.1 STA1080, STA1085 Ballout

Figure 33. STA108x Ballout (top left) diagram

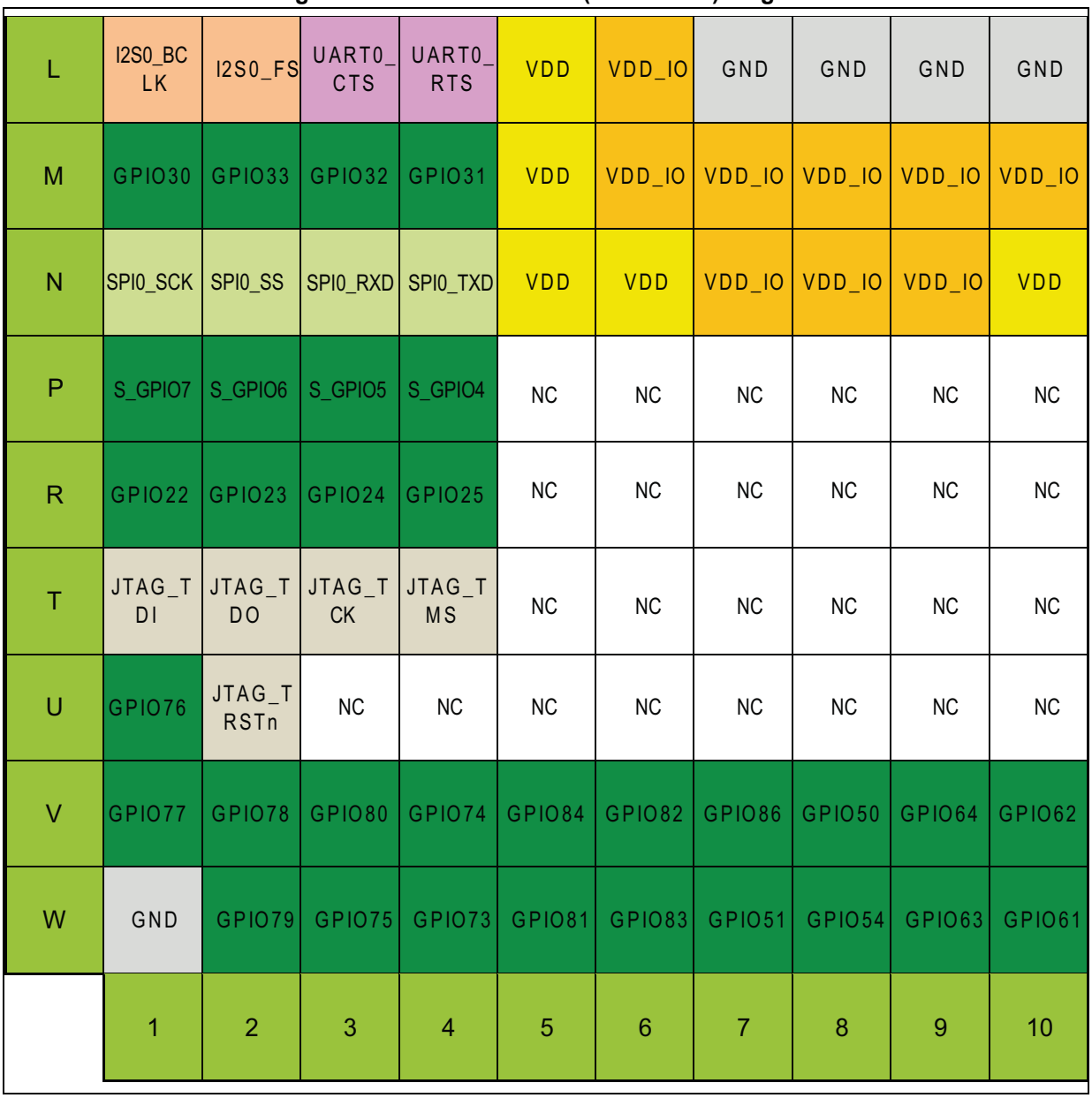
	1	2	3	4	5	6	7	8	9	10
A	OTP_FUSE_HV	GPIO41	GPIO42	GPIO43	S_GPIO3	GPIO15	GPIO14	GPIO9	GPIO8	GPIO21
B	GPIO40	M3_GPIO15	GPIO35	GPIO34	GPIO44	SYSRSTn	M3_GPIO8	GPIO13	GPIO12	GPIO7
C	M3_GPIO11	SQI_SIO3	M3_GPIO14	GPIO45	S_GPIO2	M3_GPIO9	I2C0_SCL	GPIO10	GPIO16	GPIO19
D	SQI_SCK	SQI_SIO1	SQI_CE0n	SQI_SIO0	GPIO46	S_GPIO0	S_GPIO1	I2C0_SDA	GPIO11	GPIO17
E	SQI_SIO2	GPIO6	GPIO47	GPIO48	M3_GPIO10	VDD_IO	VDD_IO	VDD_IO	VDD	VDD
F	GPIO90	GPIO91	GPIO92	GPIO93	GPIO49	VDD	VDD_IO	VDD_IO	VDD	OSC32K_GND
G	GPIO94	GPIO95	GPIO96	GPIO97	VDD	VDD_IO	GND	GND	GND	GND
H	GPIO98	GPIO99	GPIO100	GPIO101	VDD	VDD_IO	GND	GND	GND	GND
J	GPIO102	GPIO103	GPIO104	GPIO105	VDD	VDD_IO	GND	GND	GND	GND
K	I2S0_TX	I2S0_RX	UART0_RX	UART0_TX	VDD	VDD_IO	GND	GND	GND	GND

Figure 34. STA108x Ballout (top right) diagram



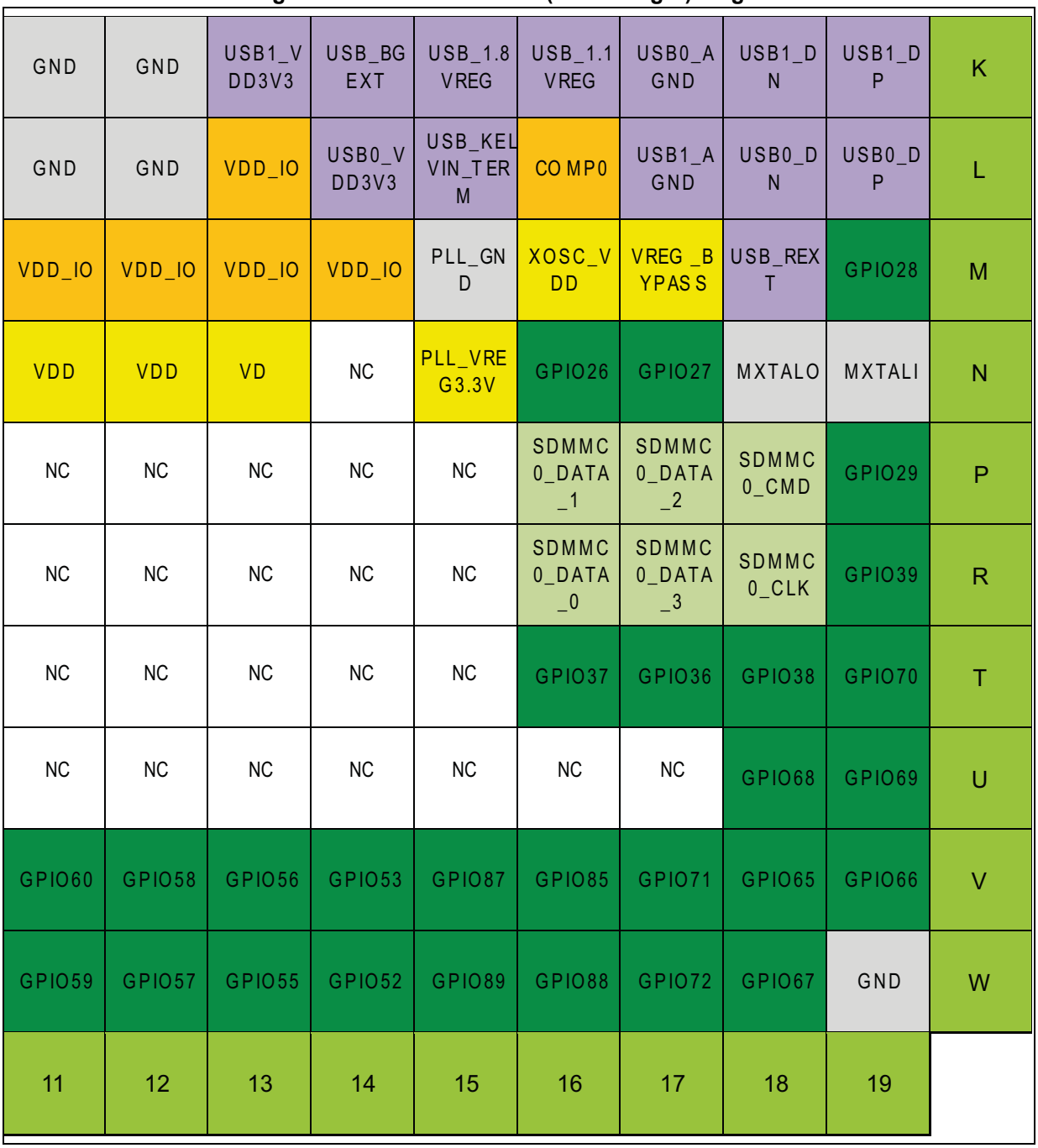
11	12	13	14	15	16	17	18	19	
GPIO0	M3_GPIO13	M3_ONOFF	M3_VDDOK	M3_IGNKEY	M3_GPIO5	M3_GPIO6	M3_GPIO7	GND	A
GPIO20	GPIO1	GPIO5	M3_LVI	M3_PWREN	M3_GPIO2	DAC_VHI	DAC_OUT1L	DAC_OUT2R	B
M3_GPIO12	GPIO2	GPIO4	M3_SXTALI	M3_GPIO0	M3_GPIO3	DAC_VLO	DAC_OUT0L	DAC_OUT2L	C
GPIO18	GPIO3	M3_CLK32KOUT	M3_SXTALO	M3_GPIO1	M3_GPIO4	DAC_VCOM	DAC_OUT0R	DAC_OUT1R	D
JTAGSEL	ADC2_VREFN	VDD_IO_ON	VDD_ON_VREG	MIC BIAS	ADC2_AIN9	ADC2_AIN6	ADC2_AIN7	ADC2_AIN4	E
GND	GND	ADC2_AGND	DAC_AGND	ADC2_VREFP	ADC0_AIN2_L	ADC0_AIN2_R	ADC0_AIN1_L	ADC0_AIN1_R	F
GND	GND	ADC2_AVDD	DAC_I/O_AGND	DAC_AVDD	ADC2_AIN3_YN	ADC2_AIN2_YP	ADC1_MICIN_P	ADC1_MICIN_N	G
GND	GND	USB_VREG3V3_1V1	ADC0_1_AVDD	DAC_I/O_AVDD	ADC2_AIN5	ADC2_AIN0_XP	ADC1_AIN1_P	ADC1_AIN1_N	H
GND	GND	USB_VREG3V3_1V8	ADC0_1_AGND	ADC0_1_VRFP	ADC0_1_VRFN	ADC0_1_VCM	ADC2_AIN8	ADC2_AIN1_XN	J
GND	GND	USB1_VDD3V3	USB_BGEXT	USB_1.8VREG	USB_1.1VREG	USB0_AGND	USB1_DN	USB1_DP	K

Figure 35. STA108x Ballout (bottom left) diagram



L	I2S0_BCLK	I2S0_FS	UART0_CTS	UART0_RTS	VDD	VDD_IO	GND	GND	GND	GND
M	GPIO30	GPIO33	GPIO32	GPIO31	VDD	VDD_IO	VDD_IO	VDD_IO	VDD_IO	VDD_IO
N	SPI0_SCK	SPI0_SS	SPI0_RXD	SPI0_TXD	VDD	VDD	VDD_IO	VDD_IO	VDD_IO	VDD
P	S_GPIO7	S_GPIO6	S_GPIO5	S_GPIO4	NC	NC	NC	NC	NC	NC
R	GPIO22	GPIO23	GPIO24	GPIO25	NC	NC	NC	NC	NC	NC
T	JTAG_TDI	JTAG_TDO	JTAG_TCK	JTAG_TMS	NC	NC	NC	NC	NC	NC
U	GPIO76	JTAG_TRSTn	NC	NC	NC	NC	NC	NC	NC	NC
V	GPIO77	GPIO78	GPIO80	GPIO74	GPIO84	GPIO82	GPIO86	GPIO50	GPIO64	GPIO62
W	GND	GPIO79	GPIO75	GPIO73	GPIO81	GPIO83	GPIO51	GPIO54	GPIO63	GPIO61
	1	2	3	4	5	6	7	8	9	10

Figure 36. STA108x Ballout (bottom right) diagram

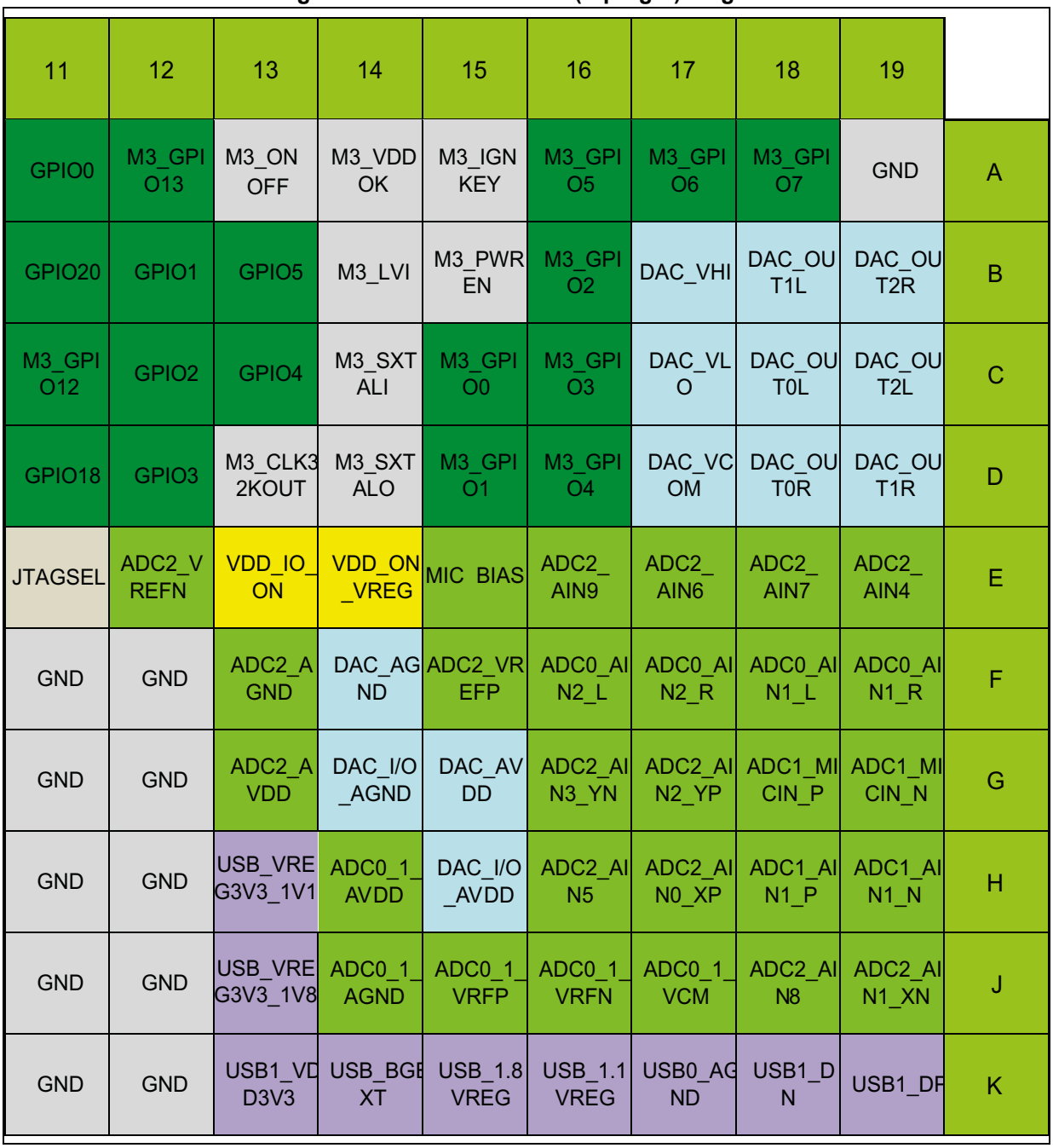


6.2 STA1090, STA1095 Ballout

Figure 37. STA109x Ballout (top left) diagram

	1	2	3	4	5	6	7	8	9	10
A	OTP_FUSE_HV	GPIO41	GPIO42	GPIO43	S_GPIO3	GPIO15	GPIO14	GPIO9	GPIO8	GPIO21
B	GPIO40	M3_GPIO15	GPIO35	GPIO34	GPIO44	SYSRSTn	M3_GPIO8	GPIO13	GPIO12	GPIO7
C	M3_GPIO11	SQI_SIO3	M3_GPIO14	GPIO45	S_GPIO2	M3_GPIO9	I2C0_SCL	GPIO10	GPIO16	GPIO19
D	SQI_SCK	SQI_SIO1	SQI_CE0n	SQI_SIO0	GPIO46	S_GPIO0	S_GPIO1	I2C0_SDA	GPIO11	GPIO17
E	SQI_SIO2	GPIO6	GPIO47	GPIO48	M3_GPIO10	VDD_IO	VDD_IO	VDD_IO	VDD	VDD
F	GPIO90	GPIO91	GPIO92	GPIO93	GPIO49	VDD	VDD_IO	VDD_IO	VDD	OSC32K_GND
G	GPIO94	GPIO95	GPIO96	GPIO97	VDD	VDD_IO	GND	GND	GND	GND
H	GPIO98	GPIO99	GPIO100	GPIO101	VDD	VDD_IO	GND	GND	GND	GND
J	GPIO102	GPIO103	GPIO104	GPIO105	VDD	VDD_IO	GND	GND	GND	GND
K	I2S0_TX	I2S0_RX	UART0_RX	UART0_TX	VDD	VDD_IO	GND	GND	GND	GND

Figure 38. STA109x Ballout (top right) diagram



11	12	13	14	15	16	17	18	19	
GPIO0	M3_GPIO13	M3_ONOFF	M3_VDDOK	M3_IGNKEY	M3_GPIO5	M3_GPIO6	M3_GPIO7	GND	A
GPIO20	GPIO1	GPIO5	M3_LVI	M3_PWREN	M3_GPIO2	DAC_VHI	DAC_OUT1L	DAC_OUT2R	B
M3_GPIO12	GPIO2	GPIO4	M3_SXTALI	M3_GPIO0	M3_GPIO3	DAC_VLO	DAC_OUT0L	DAC_OUT2L	C
GPIO18	GPIO3	M3_CLK32KOUT	M3_SXTALO	M3_GPIO1	M3_GPIO4	DAC_VCOM	DAC_OUT0R	DAC_OUT1R	D
JTAGSEL	ADC2_VREFN	VDD_IO_ON	VDD_ON_VREG	MIC BIAS	ADC2_AIN9	ADC2_AIN6	ADC2_AIN7	ADC2_AIN4	E
GND	GND	ADC2_AGND	DAC_AGND	ADC2_VREFP	ADC0_AIN2_L	ADC0_AIN2_R	ADC0_AIN1_L	ADC0_AIN1_R	F
GND	GND	ADC2_AVDD	DAC_I/O_AGND	DAC_AVDD	ADC2_AIN3_YN	ADC2_AIN2_YP	ADC1_MICIN_P	ADC1_MICIN_N	G
GND	GND	USB_VREG3V3_1V1	ADC0_1_AVDD	DAC_I/O_AVDD	ADC2_AIN5	ADC2_AIN0_XP	ADC1_AIN1_P	ADC1_AIN1_N	H
GND	GND	USB_VREG3V3_1V8	ADC0_1_AGND	ADC0_1_VRFP	ADC0_1_VRFN	ADC0_1_VCM	ADC2_AIN8	ADC2_AIN1_XN	J
GND	GND	USB1_VDD3V3	USB_BGEXT	USB_1.8VREG	USB_1.1VREG	USB0_AGND	USB1_DN	USB1_DP	K

Figure 39. STA109x Ballout (bottom left) diagram

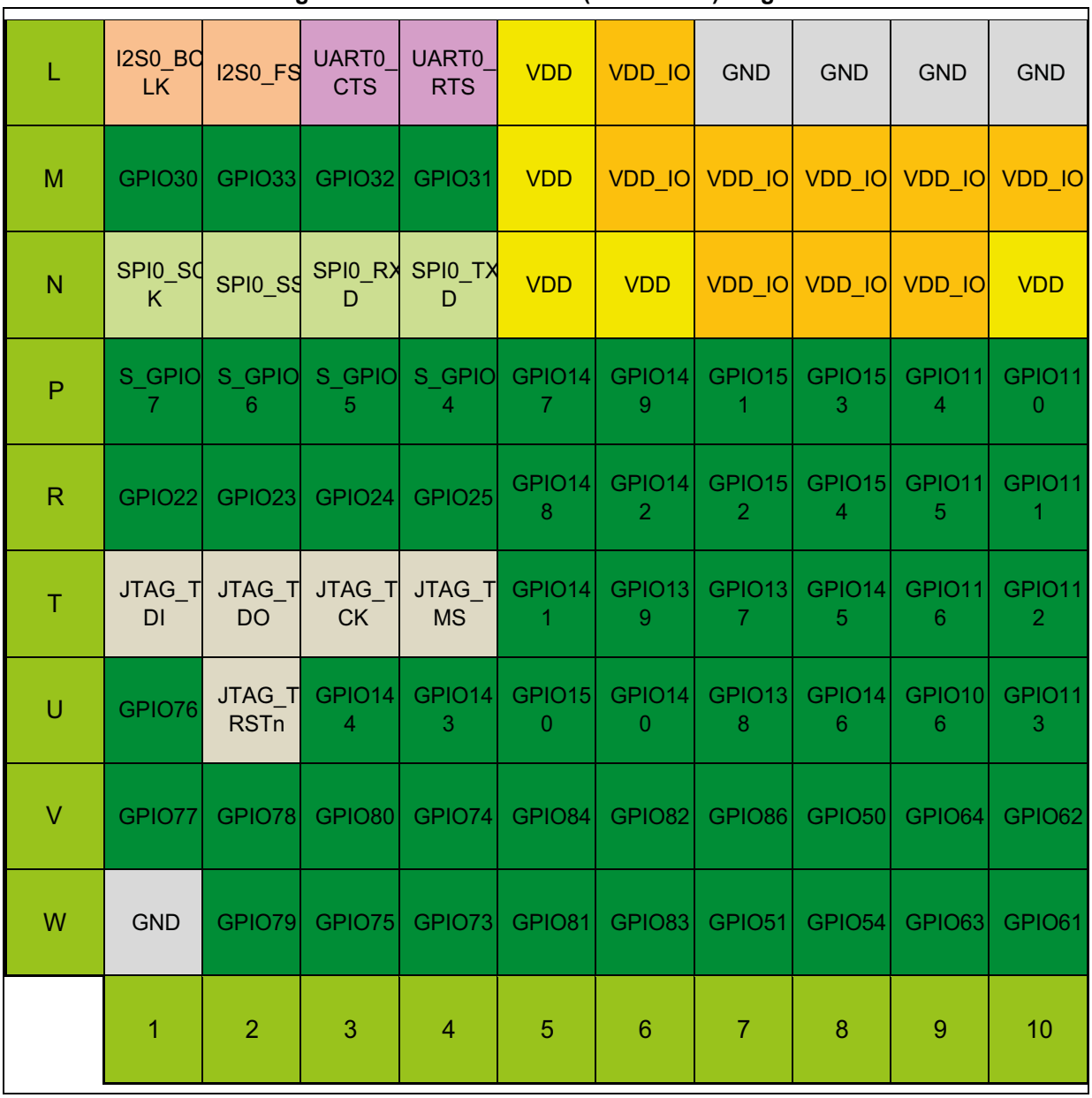
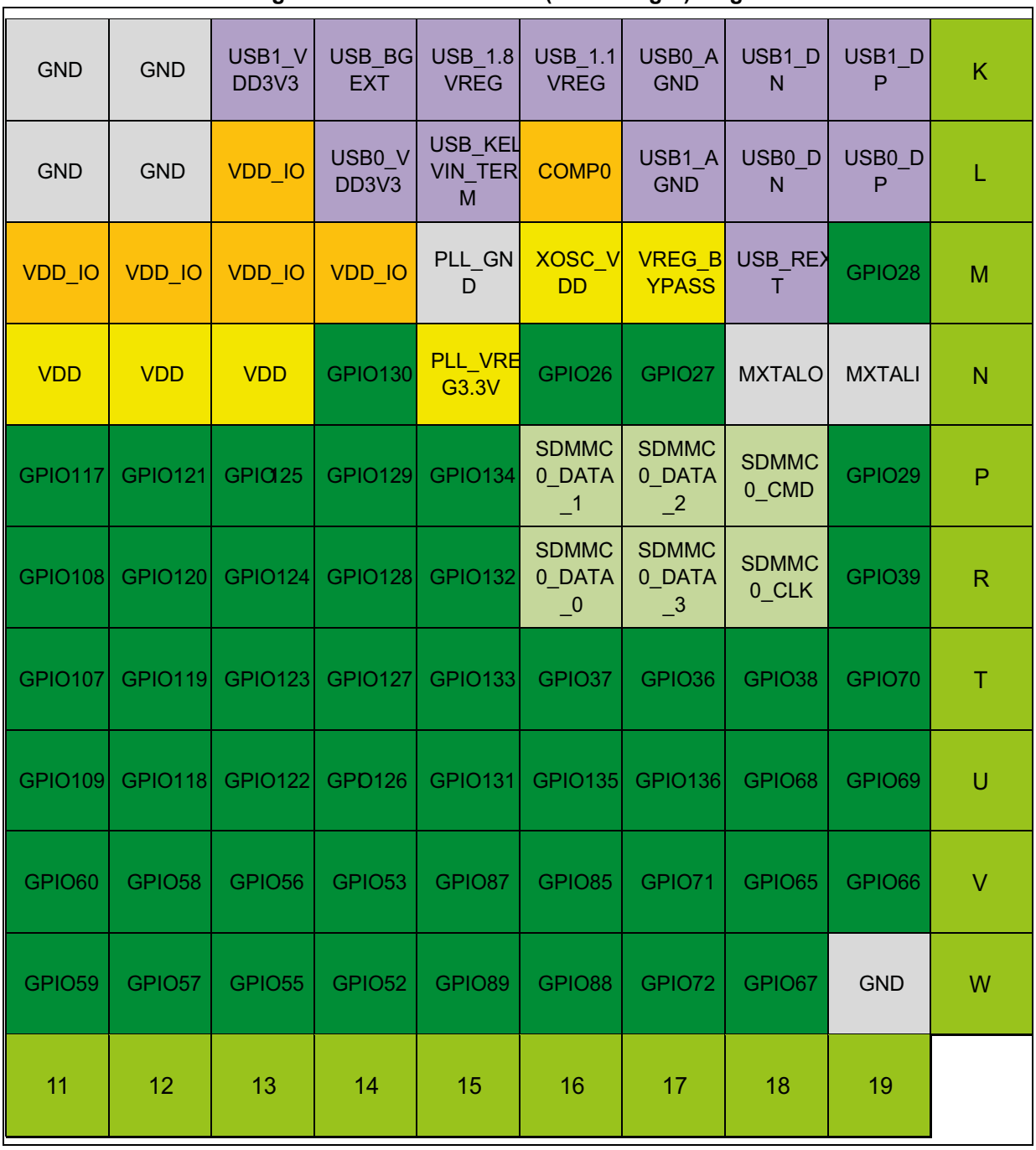


Figure 40. STA109x Ballout (bottom right) diagram



GND	GND	USB1_VDD3V3	USB_BGEXT	USB_1.8VREG	USB_1.1VREG	USB0_AGND	USB1_DN	USB1_DP	K
GND	GND	VDD_IO	USB0_VDD3V3	USB_KELVIN_TERM	COMP0	USB1_AGND	USB0_DN	USB0_DP	L
VDD_IO	VDD_IO	VDD_IO	VDD_IO	PLL_GND	XOSC_VDD	VREG_BYPASS	USB_REXT	GPIO28	M
VDD	VDD	VDD	GPIO130	PLL_VREG3.3V	GPIO26	GPIO27	MXTALO	MXTALI	N
GPIO117	GPIO121	GPIO125	GPIO129	GPIO134	SDMMC0_DATA_1	SDMMC0_DATA_2	SDMMC0_CMD	GPIO29	P
GPIO108	GPIO120	GPIO124	GPIO128	GPIO132	SDMMC0_DATA_0	SDMMC0_DATA_3	SDMMC0_CLK	GPIO39	R
GPIO107	GPIO119	GPIO123	GPIO127	GPIO133	GPIO37	GPIO36	GPIO38	GPIO70	T
GPIO109	GPIO118	GPIO122	GPIO126	GPIO131	GPIO135	GPIO136	GPIO68	GPIO69	U
GPIO60	GPIO58	GPIO56	GPIO53	GPIO87	GPIO85	GPIO71	GPIO65	GPIO66	V
GPIO59	GPIO57	GPIO55	GPIO52	GPIO89	GPIO88	GPIO72	GPIO67	GND	W
11	12	13	14	15	16	17	18	19	

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of *ECOPACK* packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 LFBGA361 (16x16x1.7 mm) package information

Figure 41. LFBGA361 (16x16x1.7 mm) package outline

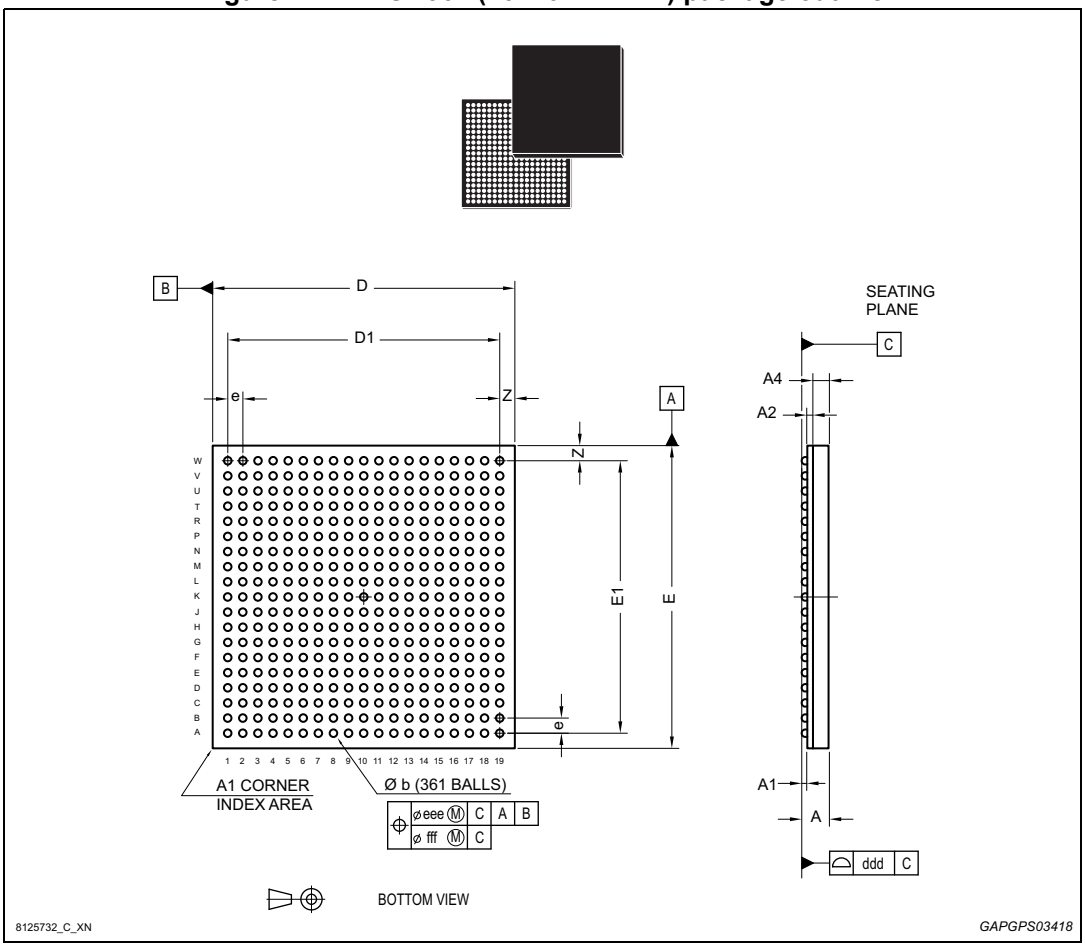


Table 57. LFBGA361 (16x16x1.7 mm) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.7	-	-	0.0669
A1	0.25	-	-	0.0098	-	-
A2	-	0.3	-	-	0.0118	-
A4	-	-	0.8	-	-	0.0315
b	0.35	0.4	0.48	0.0138	0.0157	0.0189
D	15.85	16	16.15	0.624	0.6299	0.6358
D1	-	14.4	-	-	0.5669	-
E	15.85	16	16.15	0.624	0.6299	0.6358
E1	-	14.4	-	-	0.5669	-
e	-	0.8	-	-	0.0315	-
Z	-	0.8	-	-	0.0315	-
ddd	-	-	0.1	-	-	0.0039
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

8 Order codes

Part numbers / sales codes are composed as follows:

STA	Root	Freq	Sec	Grade	Sil. Ver.	SW Pkg	Pack

Each field is described below:

Table 58. Part number coding

[Root] Root Code	**[Freq]** CortexR4 Frequency	**[Sec]** Security	**[Grade]** Qualification Grade	**[Sil. Ver.]** Silicon Version	**[SW Pkg]** Software Package	**[Pack]** Packing
108x 109x	**E** = *Eco (450MHz)*	**L** = *Locked* *(JTAG locked; secure boot enabled)*	**A** = *Automotive*	*[empty]* = cut2.2	*[empty]* = default	*[empty]* = *Tray*
	H = *High (533MHz)*	**O** = *Open* *(JTAG open; secure boot disabled)*				**TR** = *Tape&Reel*
	P = *Premium (600MHz)*	**U** = *Unsecured* *(JTAG locked; secure boot disabled)*		**3** = cut2.3	**S1** = custom	
Part number example: **STA1080EOA3**						
1080	**E** = *Eco (450MHz)*	**O** = *Open*	**A** = *Automotive*	**3** = cut2.3	*[empty]* = default	*[empty]* = *Tray*

9 Revision history

Table 59. Document revision history

Date	Revision	Changes
25-May-2020	1	Initial release.
20-Apr-2021	2	Removed watermark Restricted. Updated *Table 18: Voltage Characteristics*.

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