STB170NF04

N-channel 40 V, 4.4 mΩ typ., 80 A STripFET™ II Power MOSFET in a D^{2}PAK package

Datasheet — production data

Features

Order code	V_{DSS} @T_J max.	$R_{DS(on)}$ max.	I_D	P_{TOT}
STB170NF04	40 V	< 5 mΩ	80 A	300 W

■ Standard threshold drive

Applications

■ Automotive switching applications

Description

This N-channel enhancement mode Power MOSFET benefits from the latest refinement of STMicroelectronics' unique "single feature size" strip-based process, which decreases the critical alignment steps to offer exceptional manufacturing reproducibility. The result is a transistor with extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.
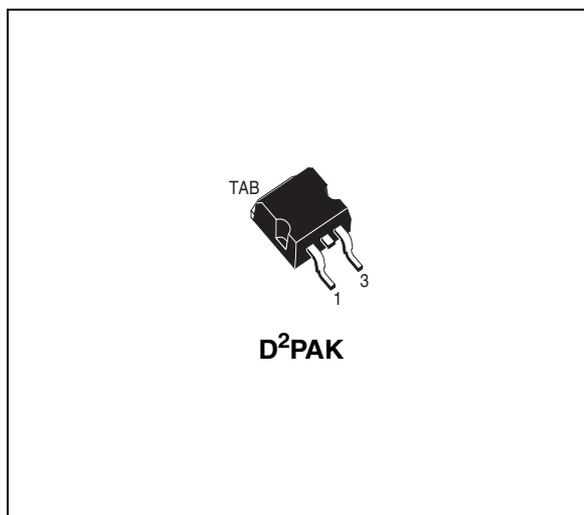

D^{2}PAK

Figure 1. Internal schematic diagram

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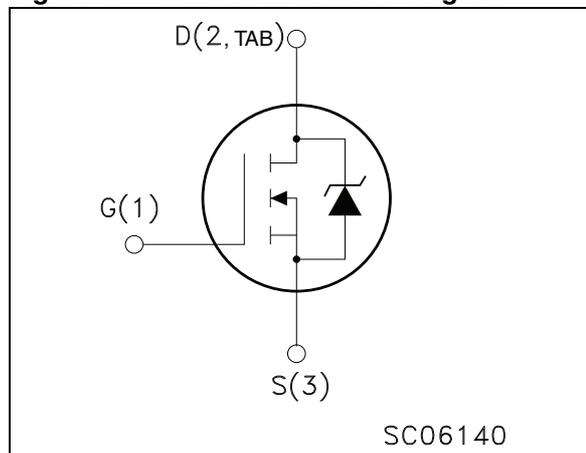
Table 1. Device summary

Order code	Marking	Package	Packaging
STB170NF04	B170NF04	D^{2}PAK	Tape and reel

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Contents

1 Electrical ratings

Table 2.   Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D [1]	Drain current (continuous) at T_C = 25 °C	80	A
I_D [1]	Drain current (continuous) at T_C = 100 °C	80	A
I_{DM} [2]	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	300	W
	Derating factor	2	W/°C
dv/dt [3]	Peak diode recovery voltage slope	8	V/ns
E_{AS} [4]	Single pulse avalanche energy	1.5	J
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Current limited by package

2. Pulse width limited by safe operating area

3. $I_{SD} \leq$ 80 A, di/dt $\leq$ 300 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$

4. Starting Tj = 25 °C, I_D = 40 A, V_{DD} = 30 V

Table 3.   Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.5	°C/W
Rthj-pcb[1]	Thermal resistance junction-pcb max	35	°C/W

1. When mounted on 1 inch² FR4 2 oz Cu

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified).

Table 4. On/off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	40			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 40 V, V_{DS} = 40 V, Tc=125 °C			10 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 40 A		4.4	5	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} [1]	Forward transconductance	V_{DS} =15 V, I_D = 40 A	-	90		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	5345 1400 430	9000	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=20 V, I_D = 80 A V_{GS} =10 V *(see Figure 14)*	-	117 27 41	170	nC nC nC

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}= 20 V, I_D= 40 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 13)*	-	26 57	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}= 20 V, I_D= 40 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 13)*	-	100 66	-	ns ns

Table 7.   Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} [1]	Source-drain current Source-drain current (pulsed)		-		80 320	A A
V_{SD} [2]	Forward on voltage	I_{SD}= 80 A, V_{GS}=0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 80 A, di/dt = 100 A/µs, V_{DD}=20 V, Tj=150 °C *(see Figure 18)*	-	70 180 4		ns nC A

1.   Pulse width limited by safe operating area

2.   Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area
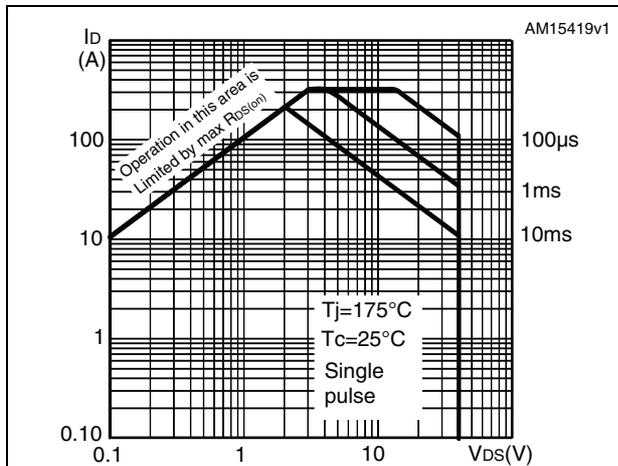
Figure 3. Thermal impedance
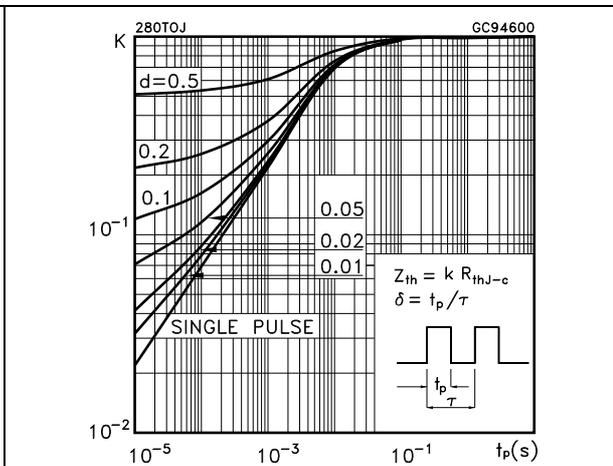
Figure 4. Output characteristics
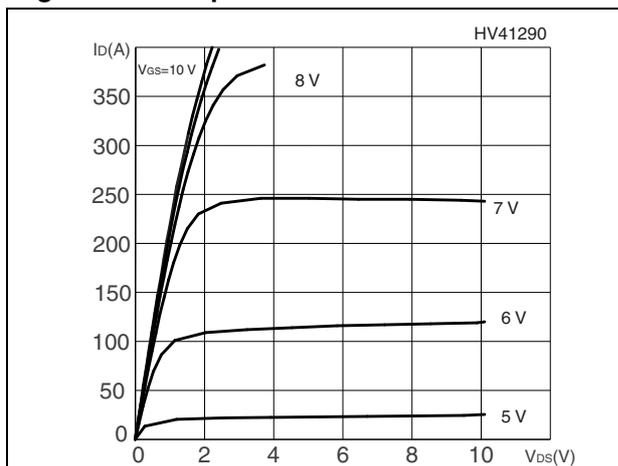

Figure 5. Transfer characteristics
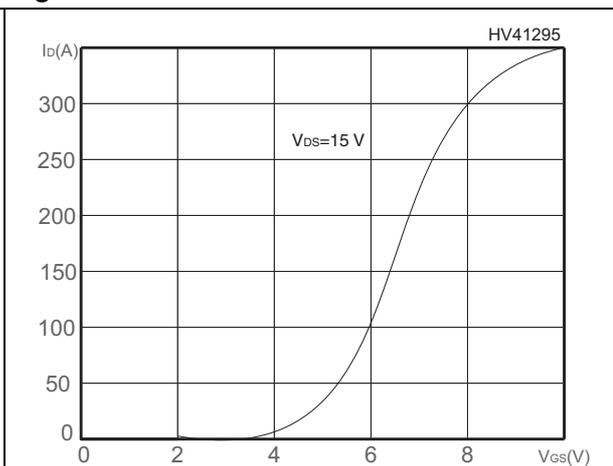
Figure 6. Normalized BV$_{DSS}$ vs temperature
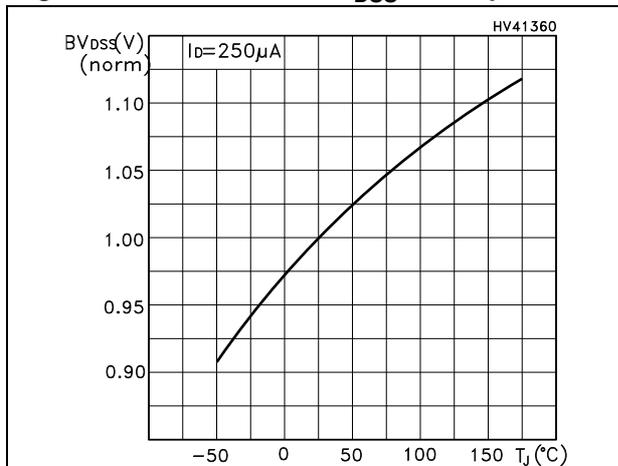

**Figure 7. Static drain-source on-resistance**
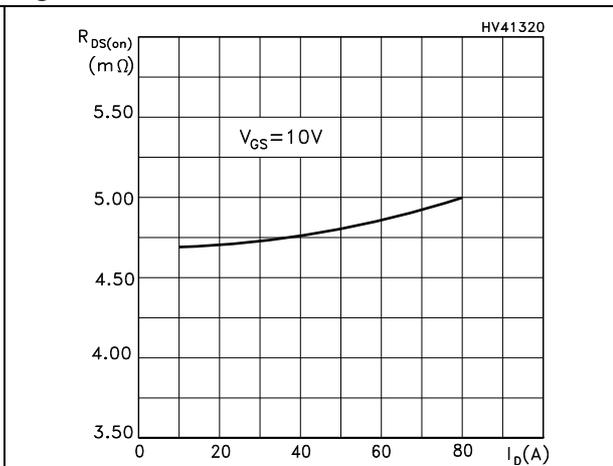
Figure 8.   Gate charge vs gate-source voltage


Figure 9.   Capacitance variations
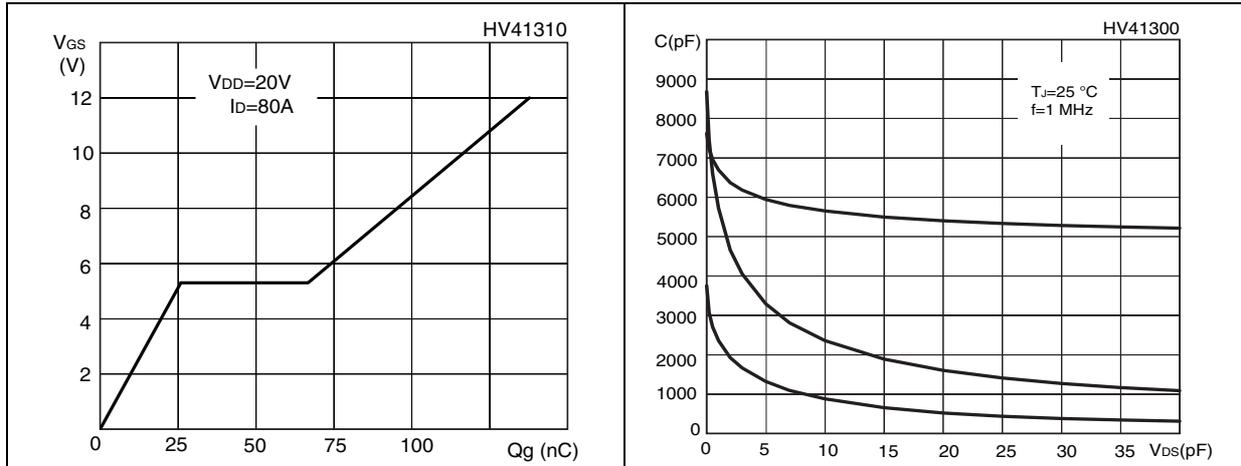
Figure 10.   Normalized gate threshold voltage vs temperature

**Figure 11.   Normalized on-resistance vs temperature**
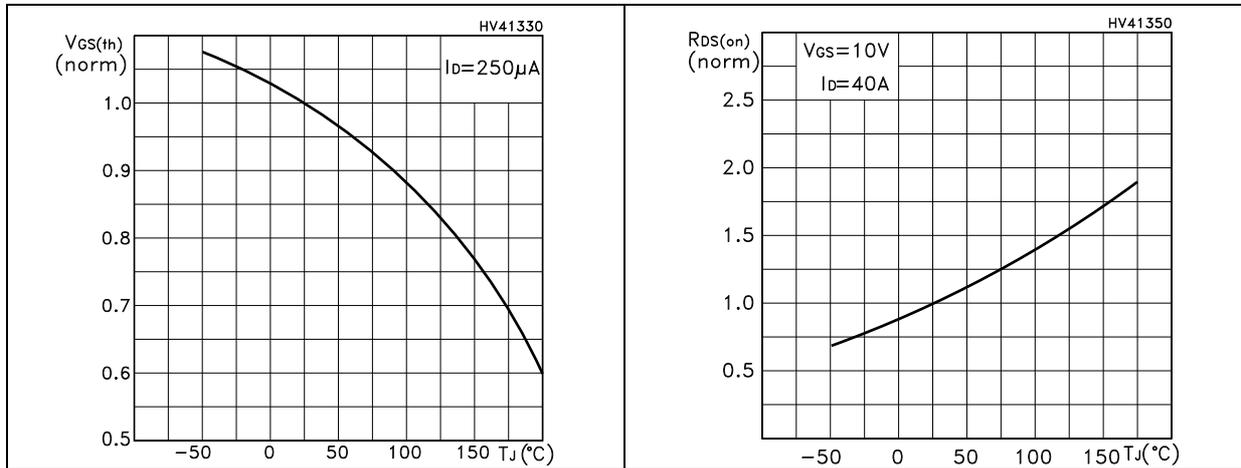
Figure 12.   Source-drain diode forward characteristics
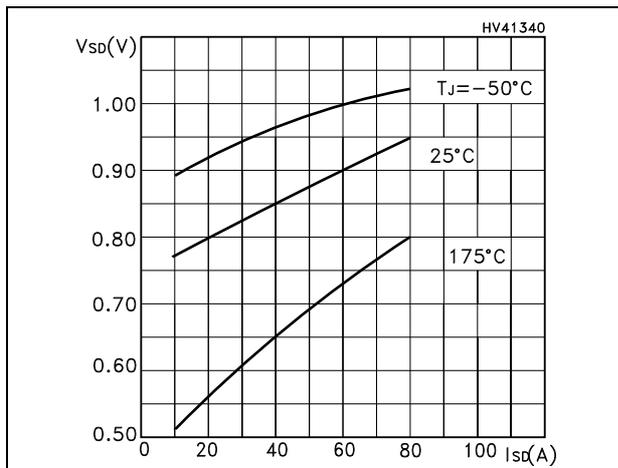
3   Test circuits

Figure 13.   **Switching times test circuit for**
   **resistive load**
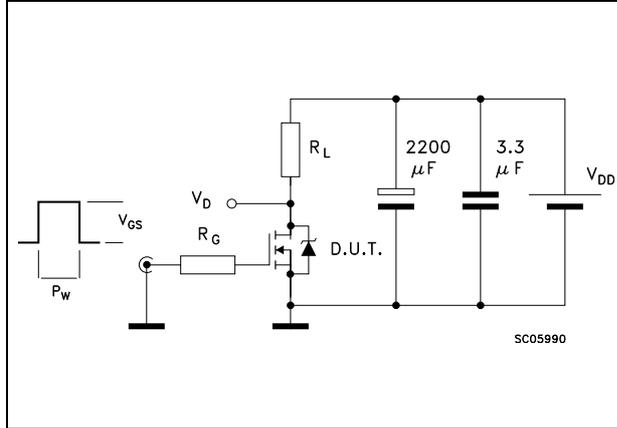
Figure 14.   **Gate charge test circuit**
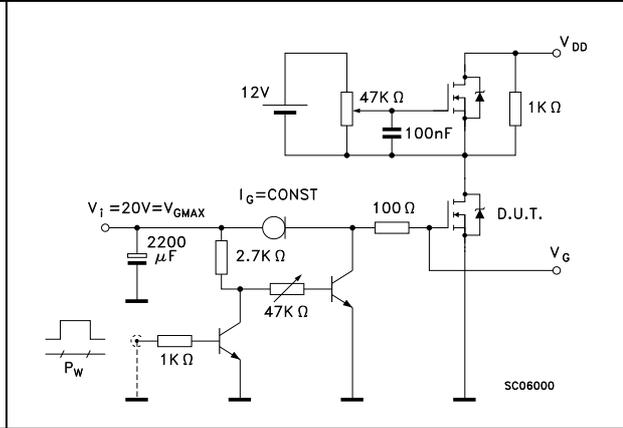
Figure 15.   **Test circuit for inductive load**
   **switching and diode recovery times**
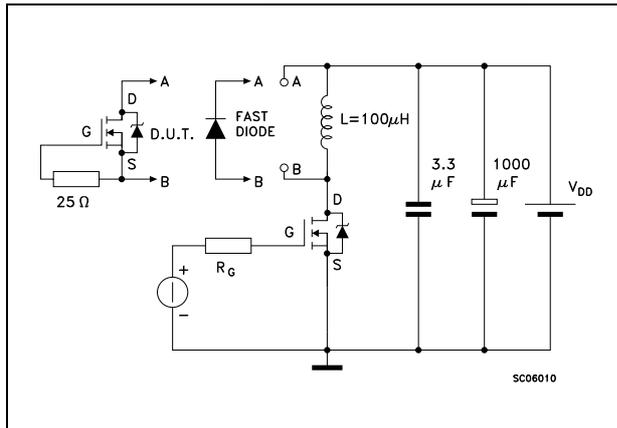
Figure 16.   **Unclamped inductive load test**
   **circuit**
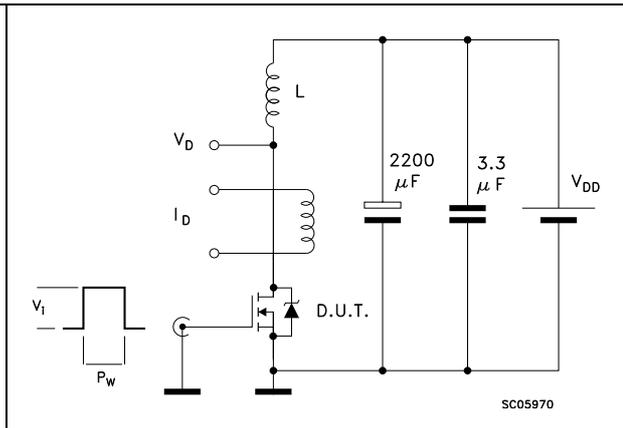
Figure 17.   **Unclamped inductive waveform**
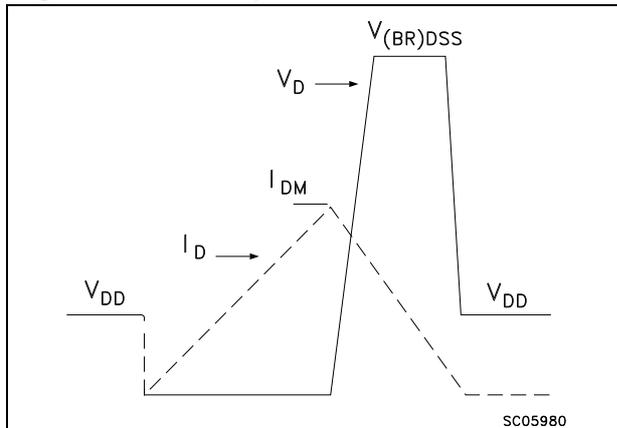
Figure 18.   **Switching time waveform**
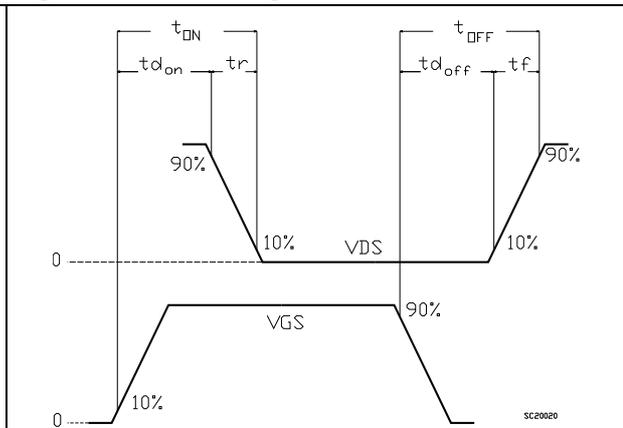
4 Package mechanical data

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Table 8.   D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 19.   D²PAK (TO-263) drawing


0079457_T
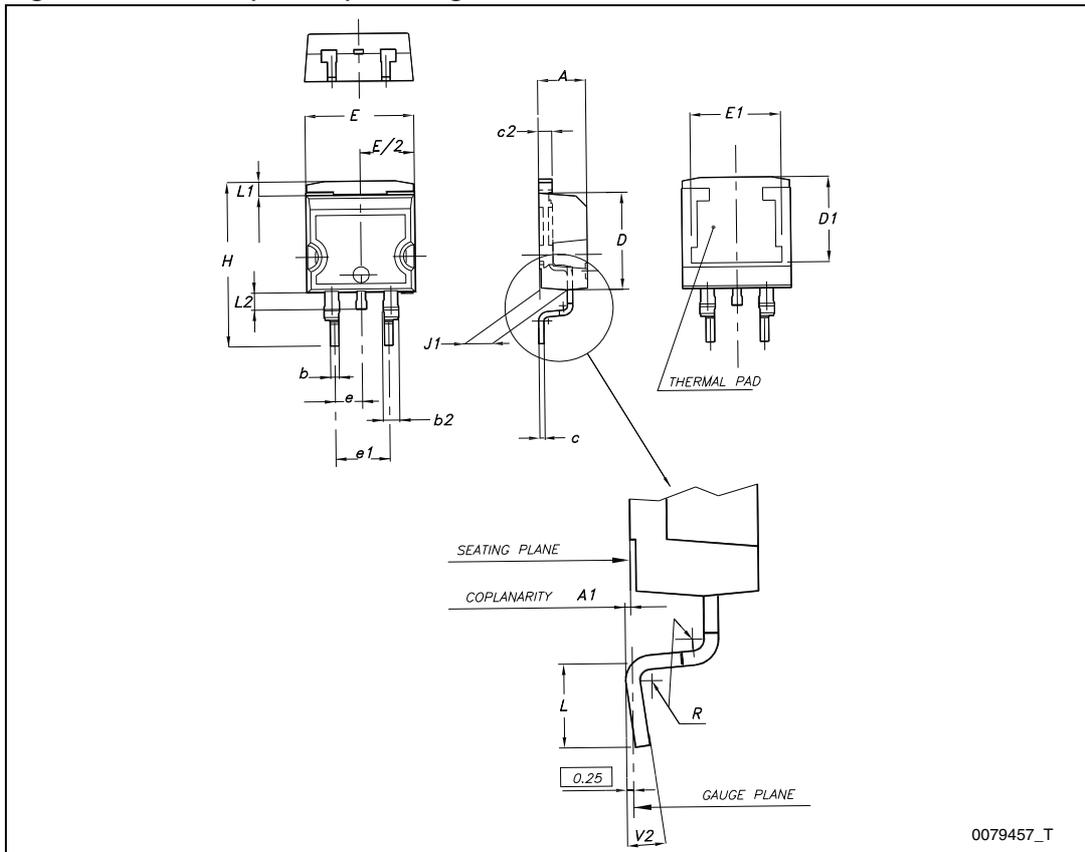
Figure 20.   D²PAK footprint[a]

Footprint
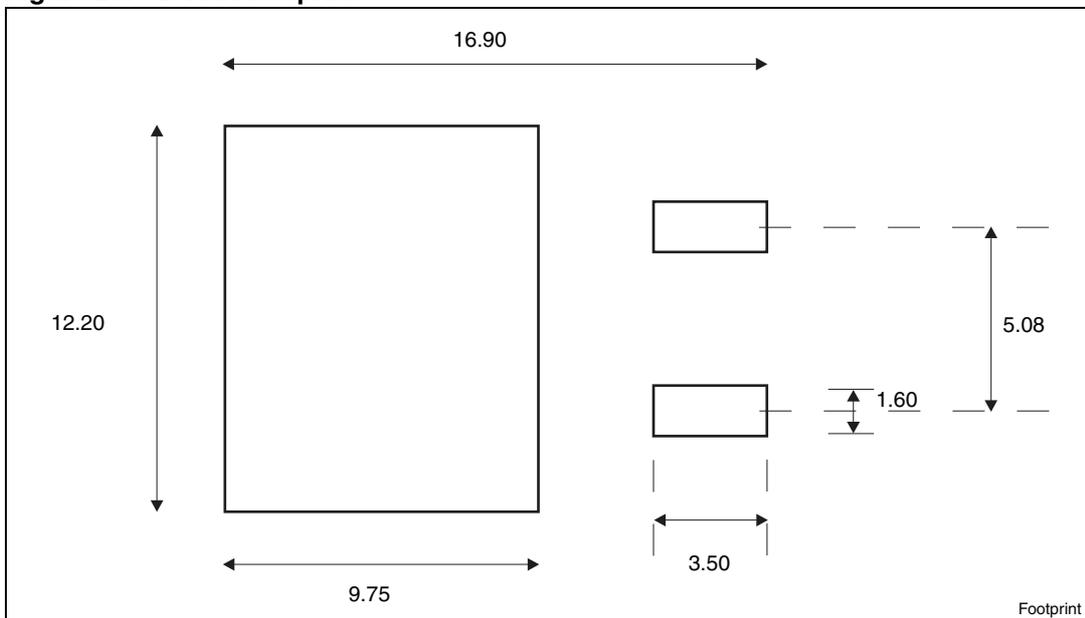
a.   All dimension are in millimeters

5 Packaging mechanical data

Table 9.   D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	**mm**		**Dim.**	**mm**	
	Min.	**Max.**		**Min.**	**Max.**
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 21. Tape
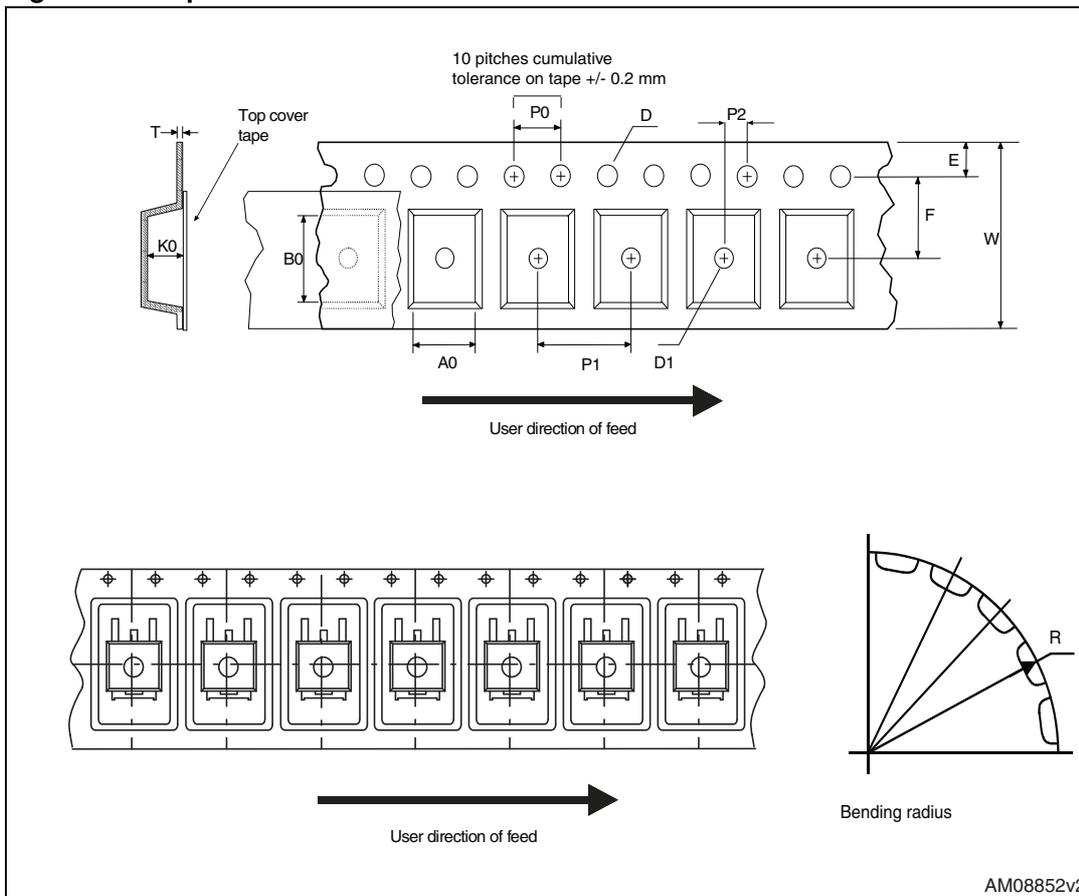
Figure 22. Reel
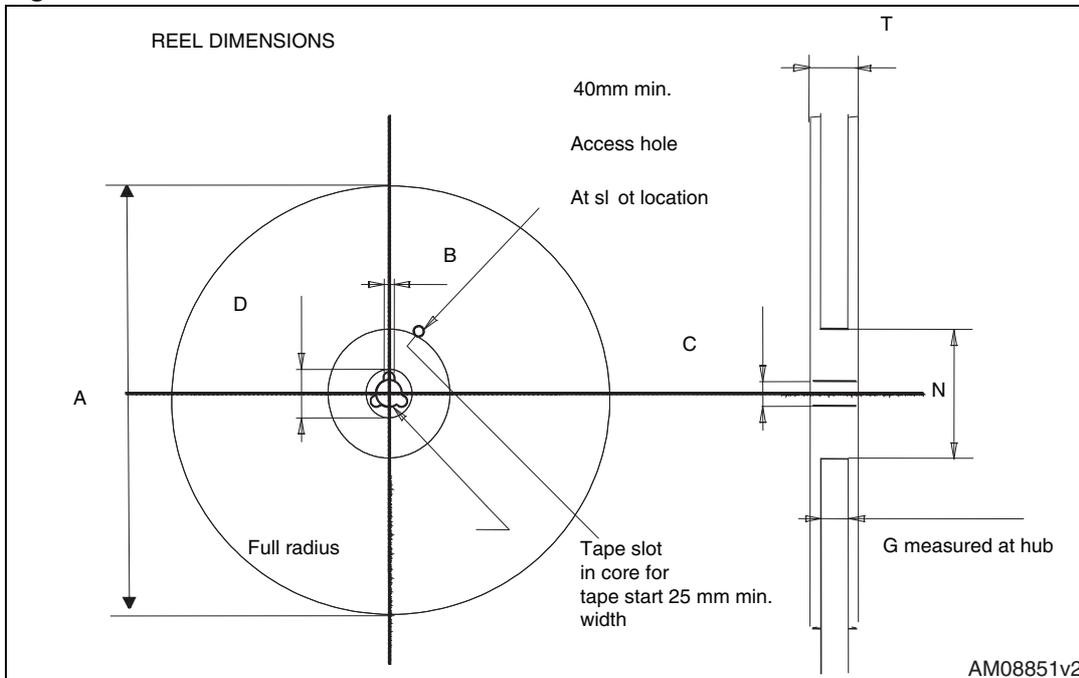
6   Revision history

Table 10.   Document revision history

Date	Revision	Changes
16-Apr-2009	1	Initial release
31-Oct-2012	2	Modified: *Figure 2*, *3* and *Section 4: Package mechanical data* and *Section 5: Packaging mechanical data*

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