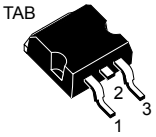
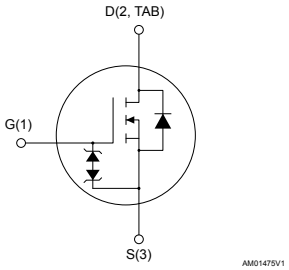
Datasheet

N-channel 600 V, 230 mΩ typ., 13 A, MDmesh M6 Power MOSFET in a D²PAK package



D²PAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB18N60M6	600 V	280 mΩ	13 A

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters
- Boost PFC converters

Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

Product status link
STB18N60M6

Product summary	
Order code	STB18N60M6
Marking	18N60M6
Package	D²PAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	13	A
	Drain current (continuous) at T_{case} = 100 °C	8.2	
I_{DM}(1)	Drain current (pulsed)	38	A
P_{TOT}	Total power dissipation at T_{case} = 25 °C	110	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	100	
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 13 A, di/dt ≤ 400 A/µs, $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V*
3. *V_{DS} ≤ 480 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.14	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	30	°C/W

1. *When mounted on 1 inch^2 FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_{Jmax})	2.7	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	210	mJ

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_{case} = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	I_D = 6.5 A, V_{GS} = 10 V		230	280	mΩ

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	650	-	pF
C_{oss}	Output capacitance		-	45	-	
C_{rss}	Reverse transfer capacitance		-	2	-	
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	123	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	4.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 13 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	16.8	-	nC
Q_{gs}	Gate-source charge		-	4.5	-	
Q_{gd}	Gate-drain charge		-	8.4	-	

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 6.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	16	-	ns
t_r	Rise time		-	7	-	
$t_{d(off)}$	Turn-off delay time		-	28	-	
t_f	Fall time		-	9	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		13	A
I_{SDM} (1)	Source-drain current (pulsed)		-		38	A
V_{SD} (2)	Forward on voltage	I_{SD} = 13 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 13 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	208		ns
Q_{rr}	Reverse recovery charge		-	1.9		µC
I_{RRM}	Reverse recovery current		-	18		A
t_{rr}	Reverse recovery time	I_{SD} = 13 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	290		ns
Q_{rr}	Reverse recovery charge		-	2.9		µC
I_{RRM}	Reverse recovery current		-	20		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

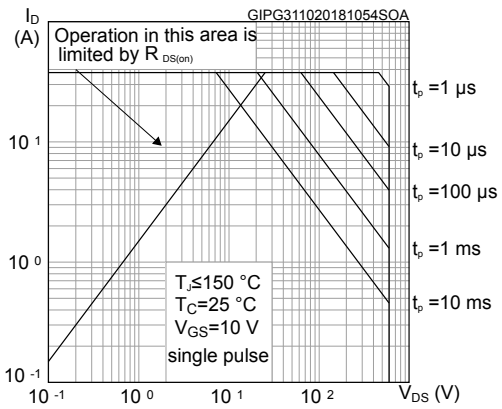


Figure 2. Thermal impedance

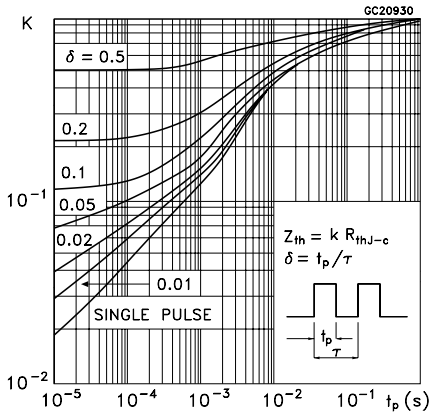


Figure 3. Output characteristics

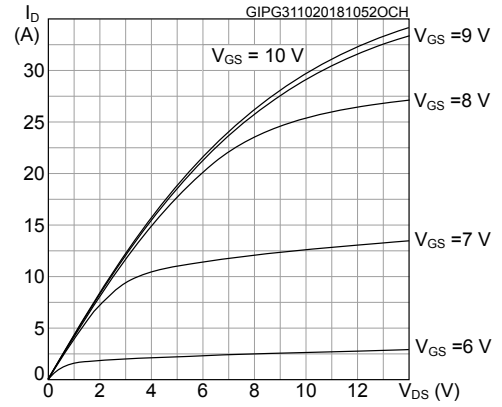


Figure 4. Transfer characteristics

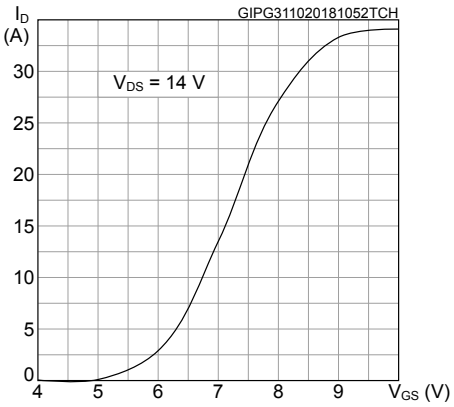


Figure 5. Gate charge vs gate-source voltage

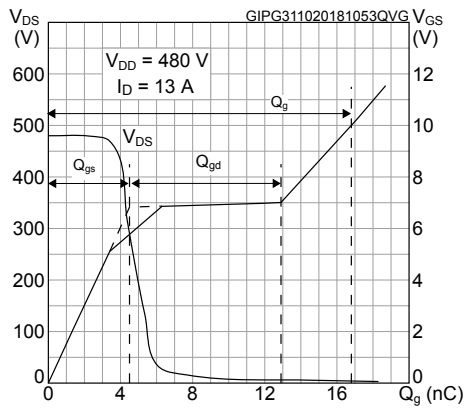


Figure 6. Static drain-source on-resistance

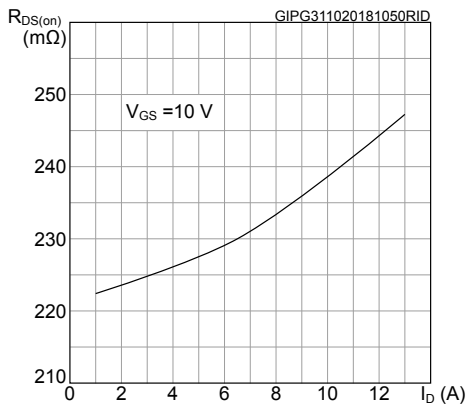


Figure 7. Capacitance variations

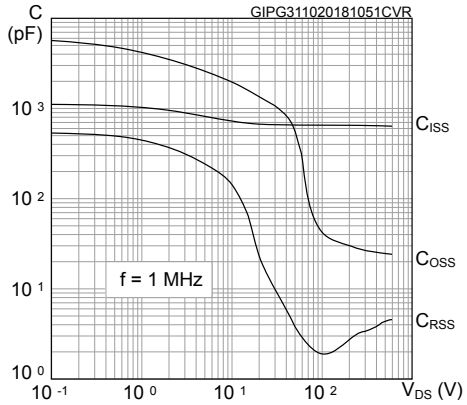


Figure 8. Output capacitance stored energy

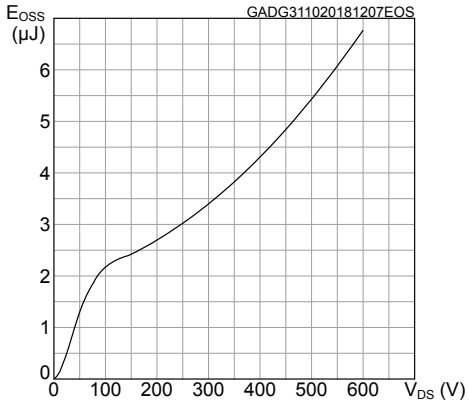


Figure 9. Normalized gate threshold voltage vs temperature

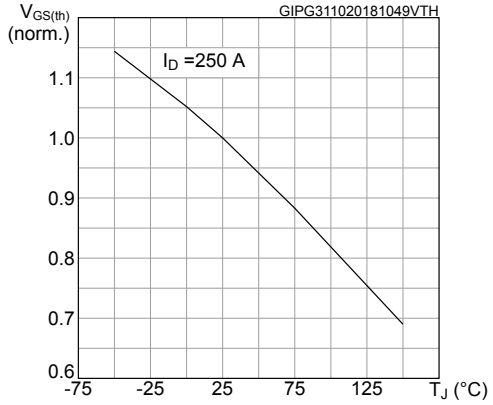


Figure 10. Normalized on-resistance vs temperature

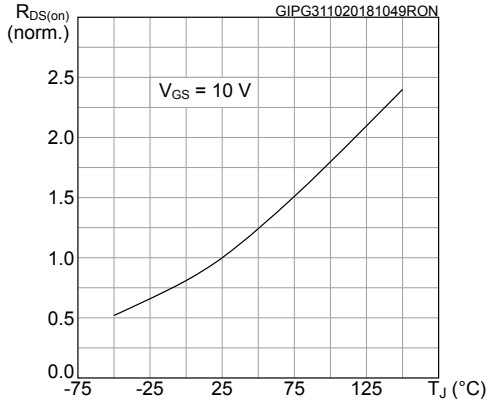


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

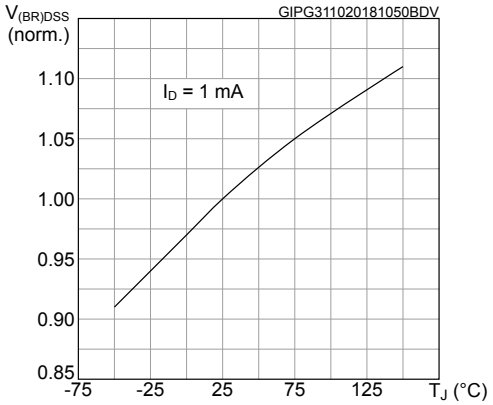
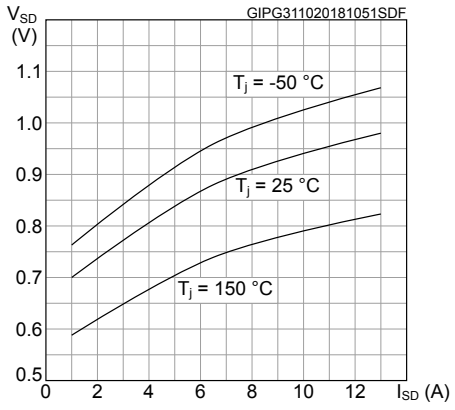


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

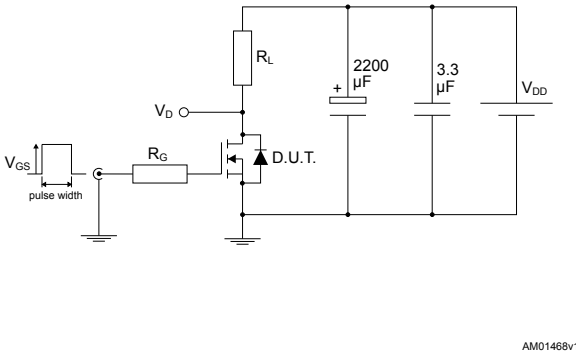


Figure 14. Test circuit for gate charge behavior

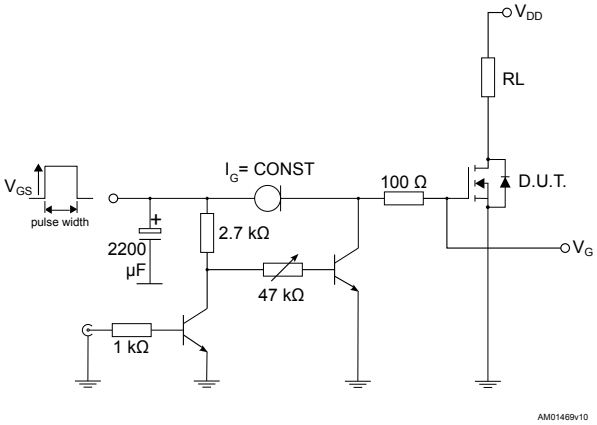


Figure 15. Test circuit for inductive load switching and diode recovery times

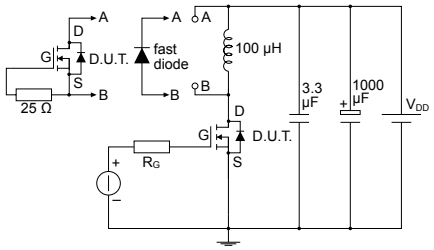


Figure 16. Unclamped inductive load test circuit

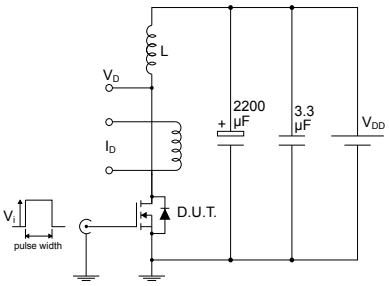


Figure 17. Unclamped inductive waveform

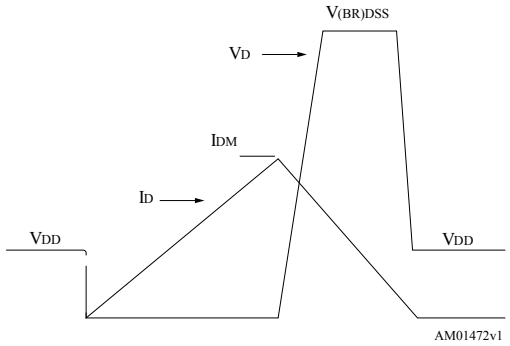
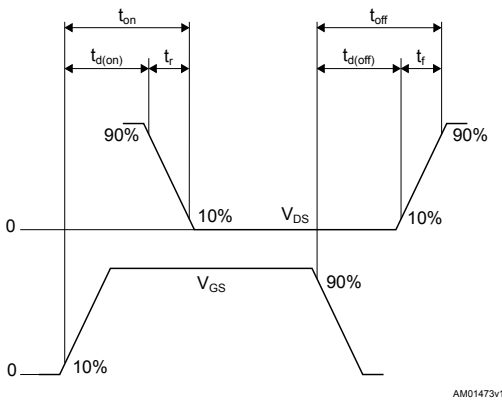


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 19. D²PAK (TO-263) type A package outline

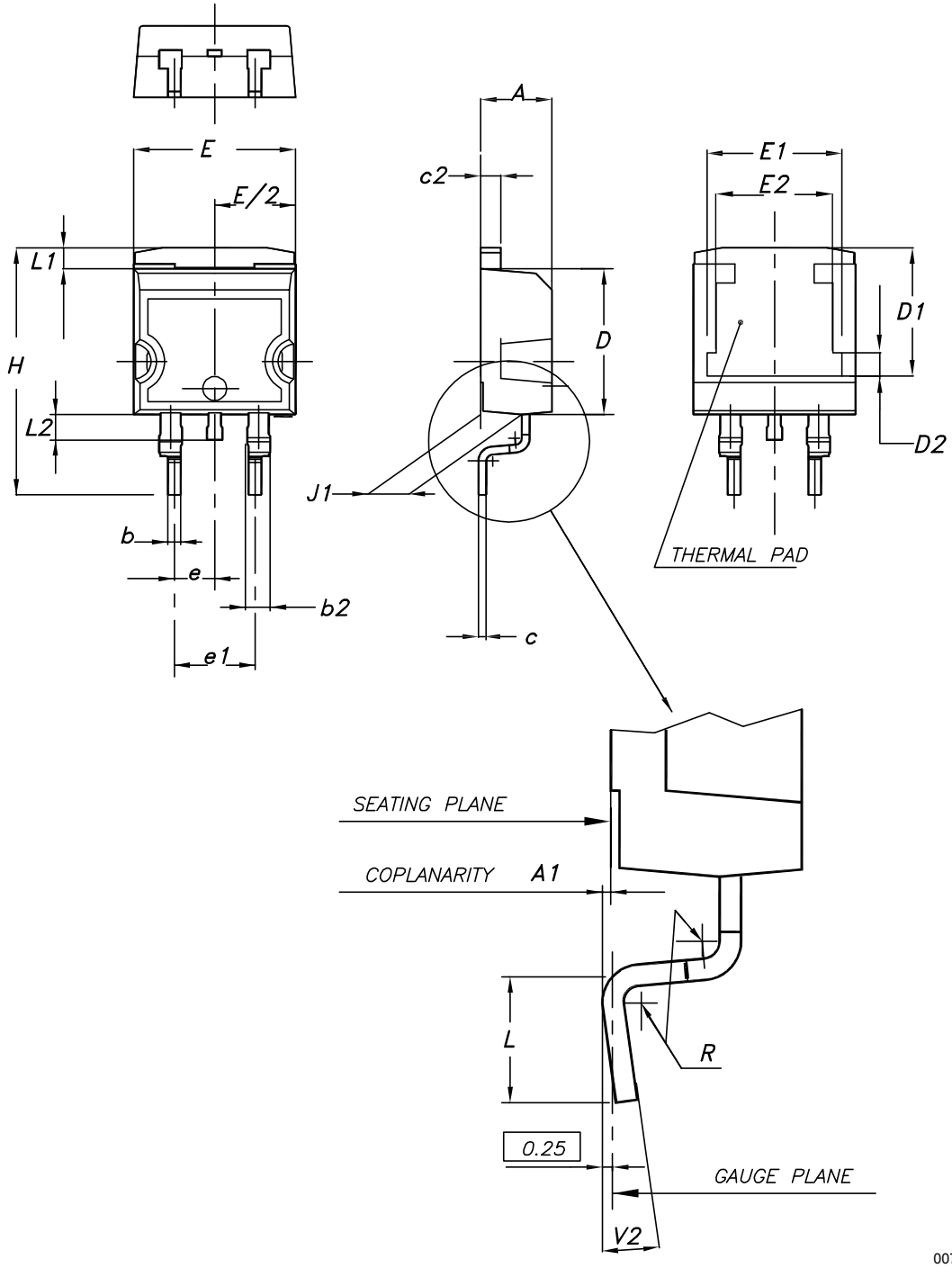
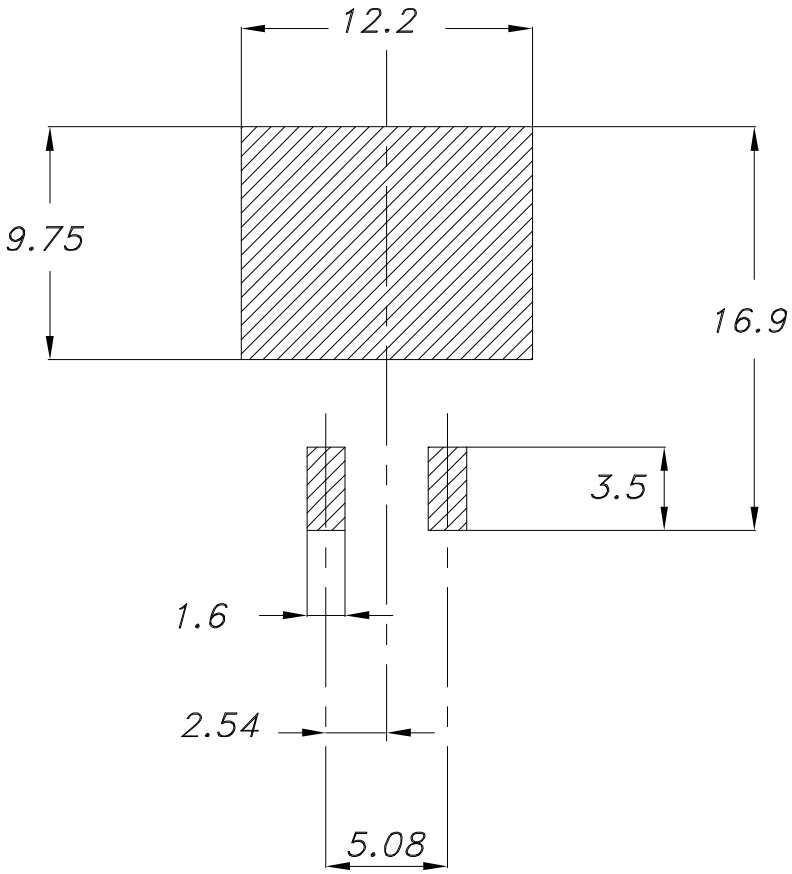


Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 20. D²PAK (TO-263) recommended footprint (dimensions are in mm)



Footprint

4.2 D²PAK packing information

Figure 21. D²PAK tape outline

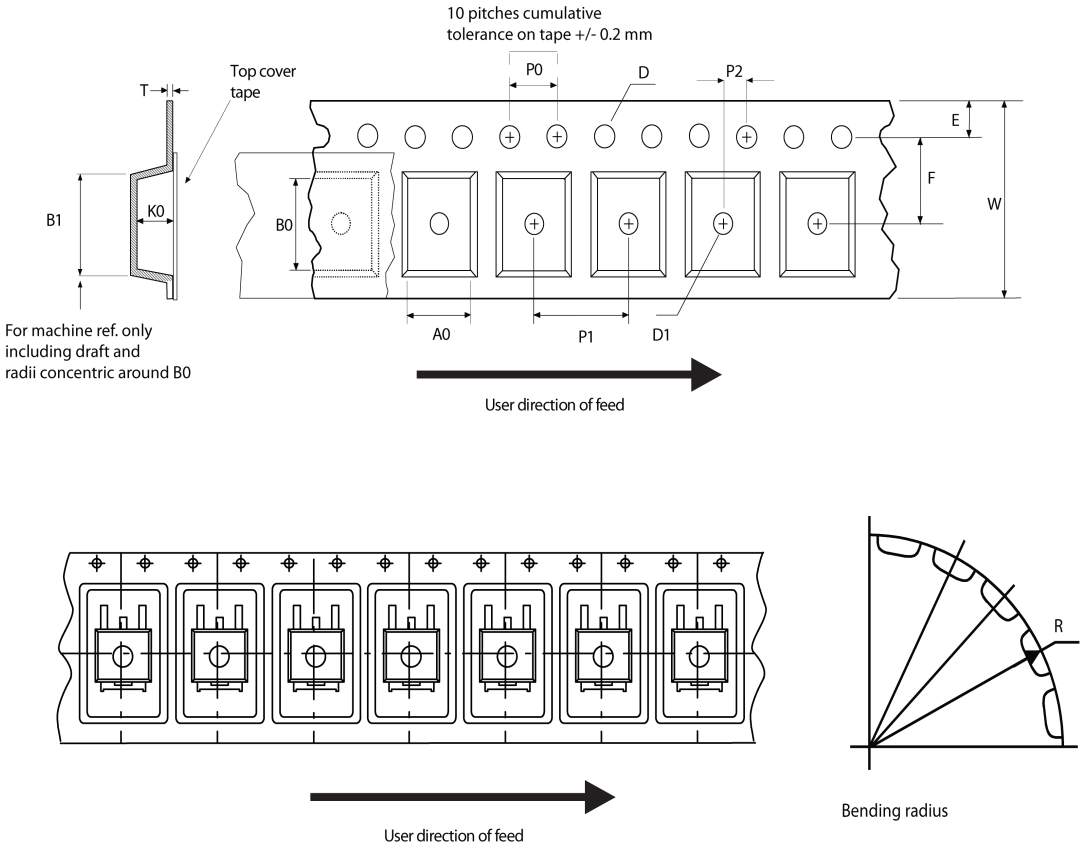
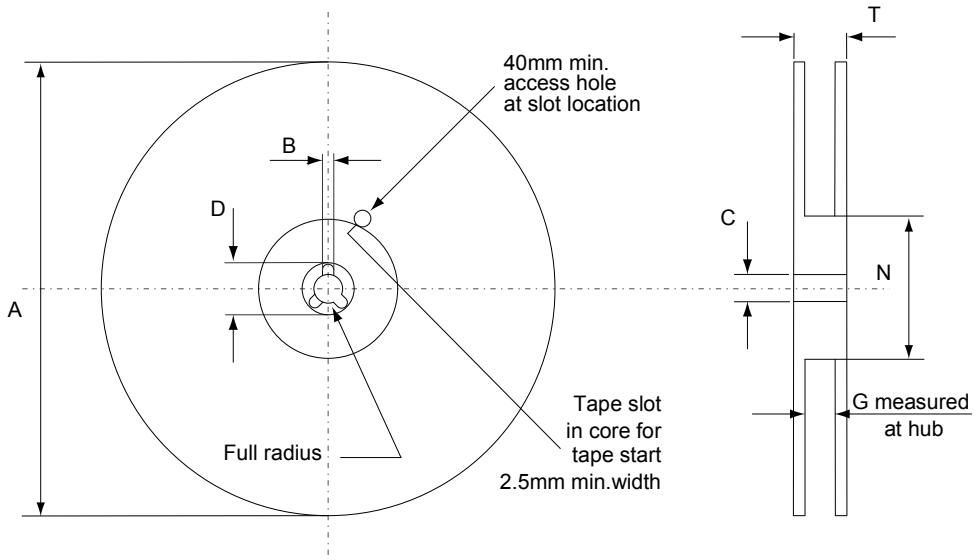


Figure 22. **D²PAK reel outline**



AM06038v1

Table 9. **D²PAK tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Revision history

Table 10. **Document revision history**

Date	Version	Changes
15-Nov-2018	1	First release.
19-Apr-2019	2	Updated product status link table in cover page.

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