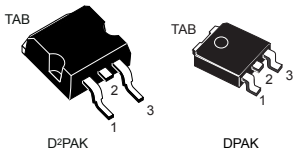
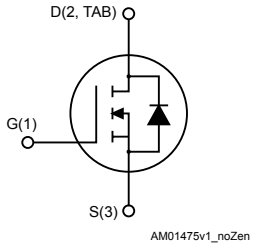
Automotive-grade N-channel 250 V, 0.140 Ω typ., 17 A STripFET™ II Power MOSFETs in D²PAK and DPAK packages





Features

Order codes	V_{DS}	$R_{DS(on)}$max.	I_D	P_{TOT}
STB18NF25	250 V	0.165 Ω	17 A	110 W
STD18NF25				

- AEC-Q101 qualified
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

These Power MOSFETs have been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the devices suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Product status
STB18NF25
STD18NF25

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	250	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	17	A
I_D	Drain current (continuous) at T_C = 100 °C	12	A
I_{DM} (1)	Drain current (pulsed)	68	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
dv/dt (2)	Peak diode recovery voltage slope	10	V/ns
T_j	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 17 A, di/dt ≤ 200 A/µs, V_{DSpeak} ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		D^2PAK	DPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.36		°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	30	50	°C/W

1. *When mounted on 1 inch² FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_{jmax})	17	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	170	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	250			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 250 V			1	µA
		V_{GS} = 0 V, V_{DS} = 250 V, T_C = 125 °C (1)			10	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 8.5 A		0.140	0.165	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1000	-	pF
C_{oss}	Output capacitance			178		
C_{rss}	Reverse transfer capacitance			28		
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{DS} = 0 to 200 V, V_{GS} = 0 V	-	106	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related			79	-	
R_g	Gate input resistance	f = 1 MHz, I_D=0 A	-	2	-	Ω
Q_g	Total gate charge	V_{DD} = 200 V, I_D = 17 A, V_{GS} = 0 to 10 V (see Figure 16. Test circuit for gate charge behavior)	-	29.3	-	nC
Q_{gs}	Gate-source charge			4.5	-	
Q_{gd}	Gate-drain charge			14.4		

1. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 125 V, I_D = 8.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	10.2	-	ns
t_r	Rise time			16.5		
$t_{d(off)}$	Turn-off delay time			31.5		
t_f	Fall time			9.8		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17	A
I_{SDM} (1)	Source-drain current (pulsed)				68	
V_{SD} (2)	Forward on voltage	I_{SD} = 17 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/µs	-	147		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V		0.8		µC
I_{RRM}	Reverse recovery current	(see Figure 17. Test circuit for inductive load switching and diode recovery times)		10.6		A
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/µs	-	180		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_j = 150 °C		1.1		µC
I_{RRM}	Reverse recovery current	(see Figure 17. Test circuit for inductive load switching and diode recovery times)		12		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics curves

Figure 1. Safe operating area for D²PAK

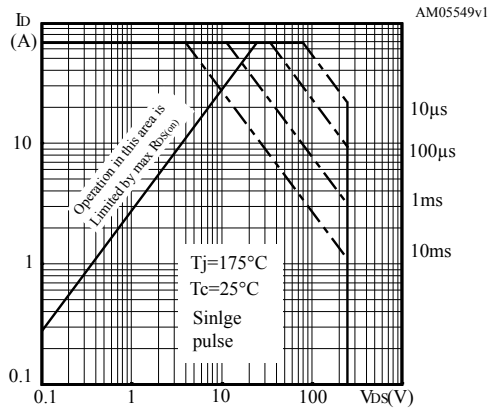


Figure 2. Thermal impedance for D²PAK

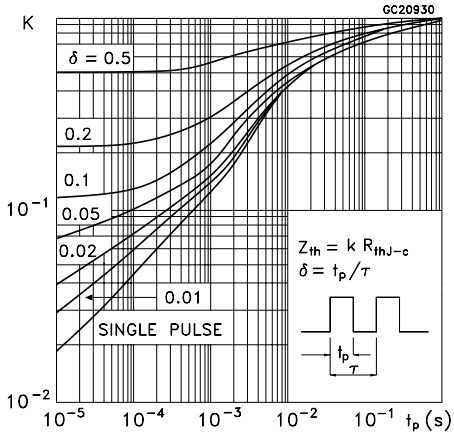


Figure 3. Safe operating area for DPAK

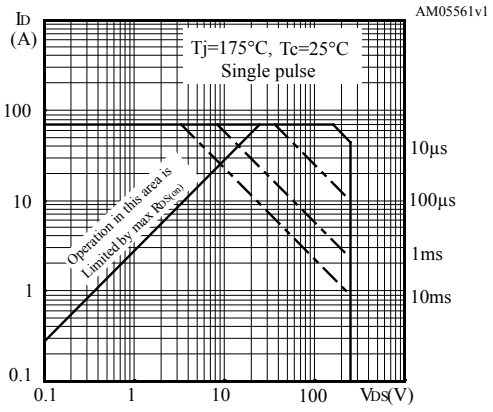


Figure 4. Thermal impedance for DPAK

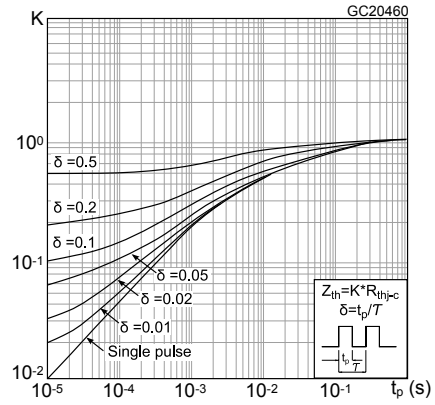


Figure 5. Output characterisics

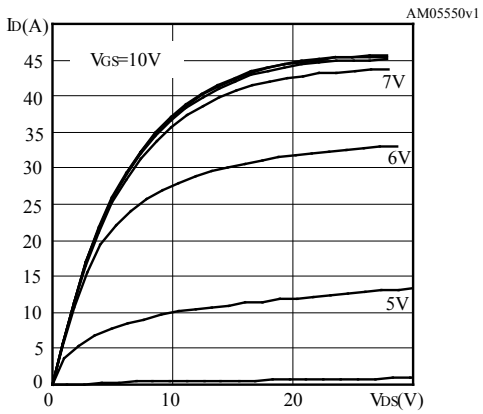


Figure 6. Transfer characteristics

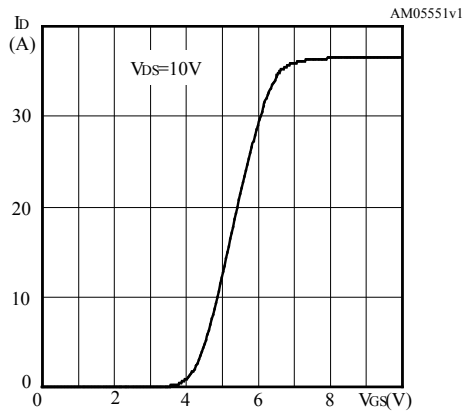


Figure 7. Gate charge vs gate-source voltage

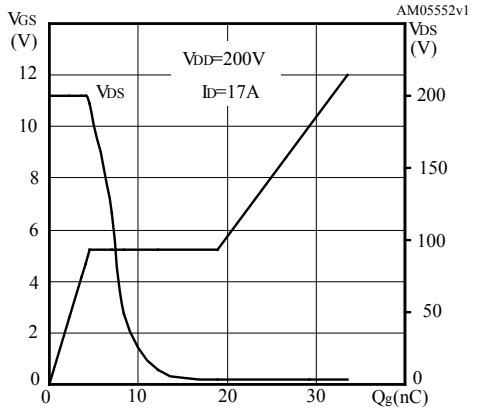


Figure 8. Static drain-source on resistance

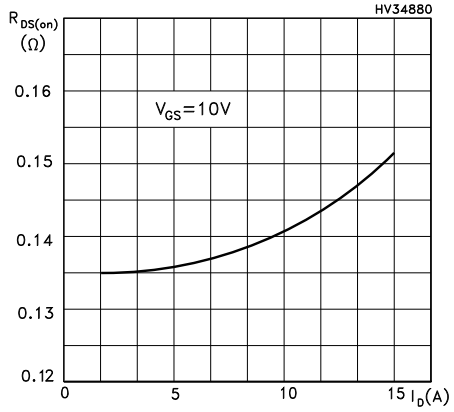


Figure 9. Output capacitance stored energy

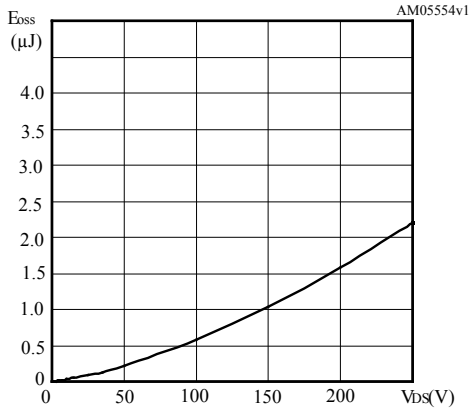


Figure 10. Capacitance variations

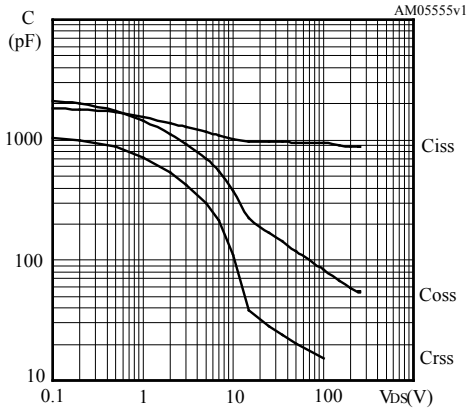


Figure 11. Normalized gate threshold voltage vs temperature

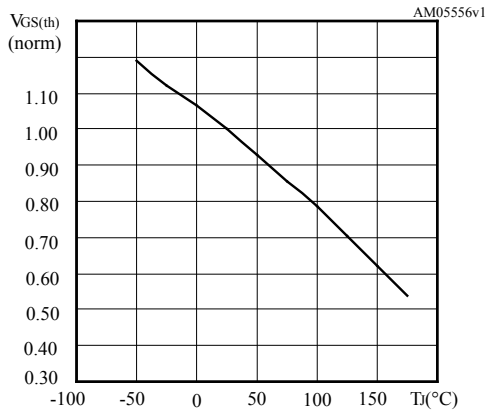


Figure 12. Normalized on-resistance vs temperature

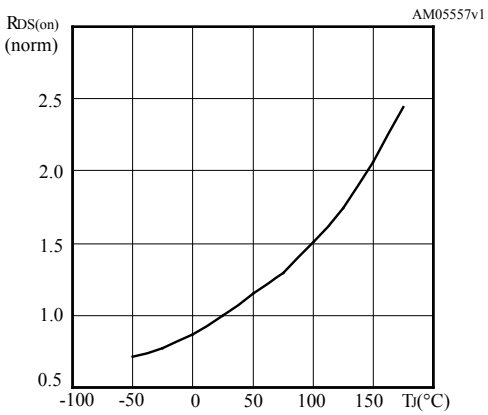


Figure 13. Source-drain diode forward characteristics

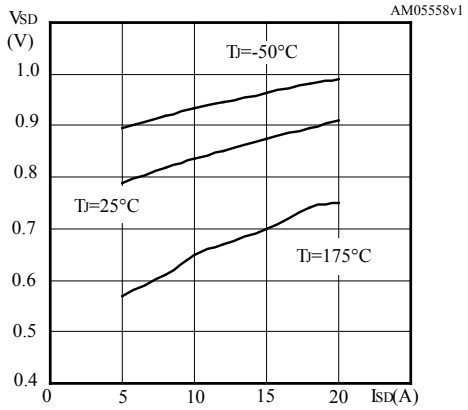
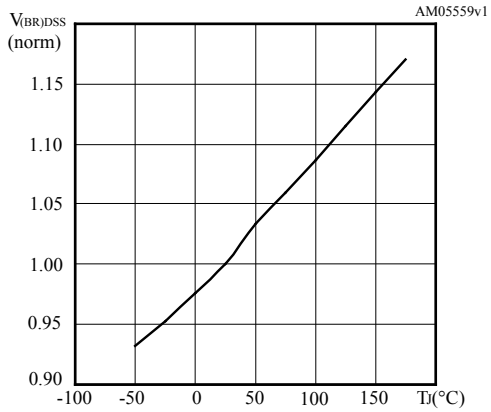


Figure 14. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 15. Test circuit for resistive load switching times

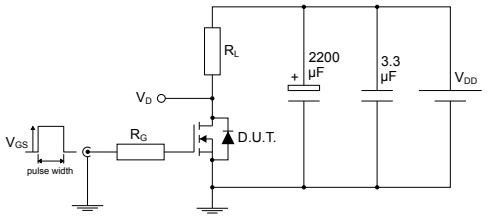


Figure 16. Test circuit for gate charge behavior

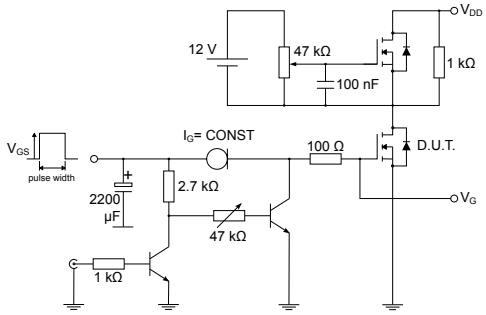


Figure 17. Test circuit for inductive load switching and diode recovery times

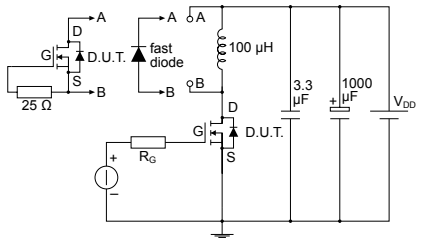


Figure 18. Unclamped inductive load test circuit

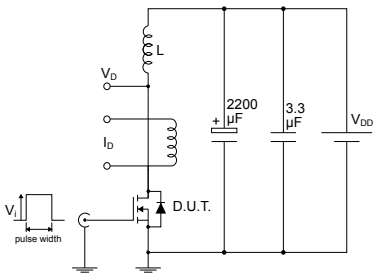


Figure 19. Unclamped inductive waveform

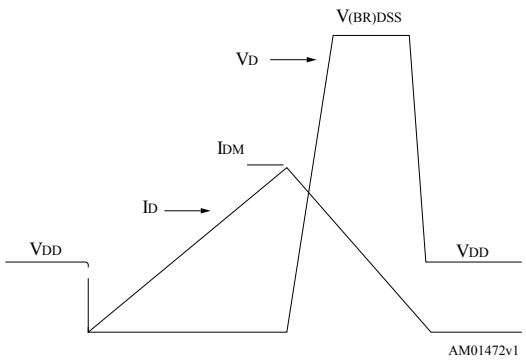
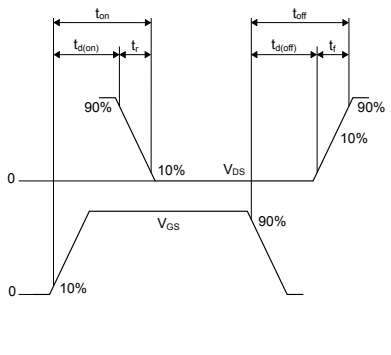


Figure 20. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 21. D²PAK (TO-263) type A package outline

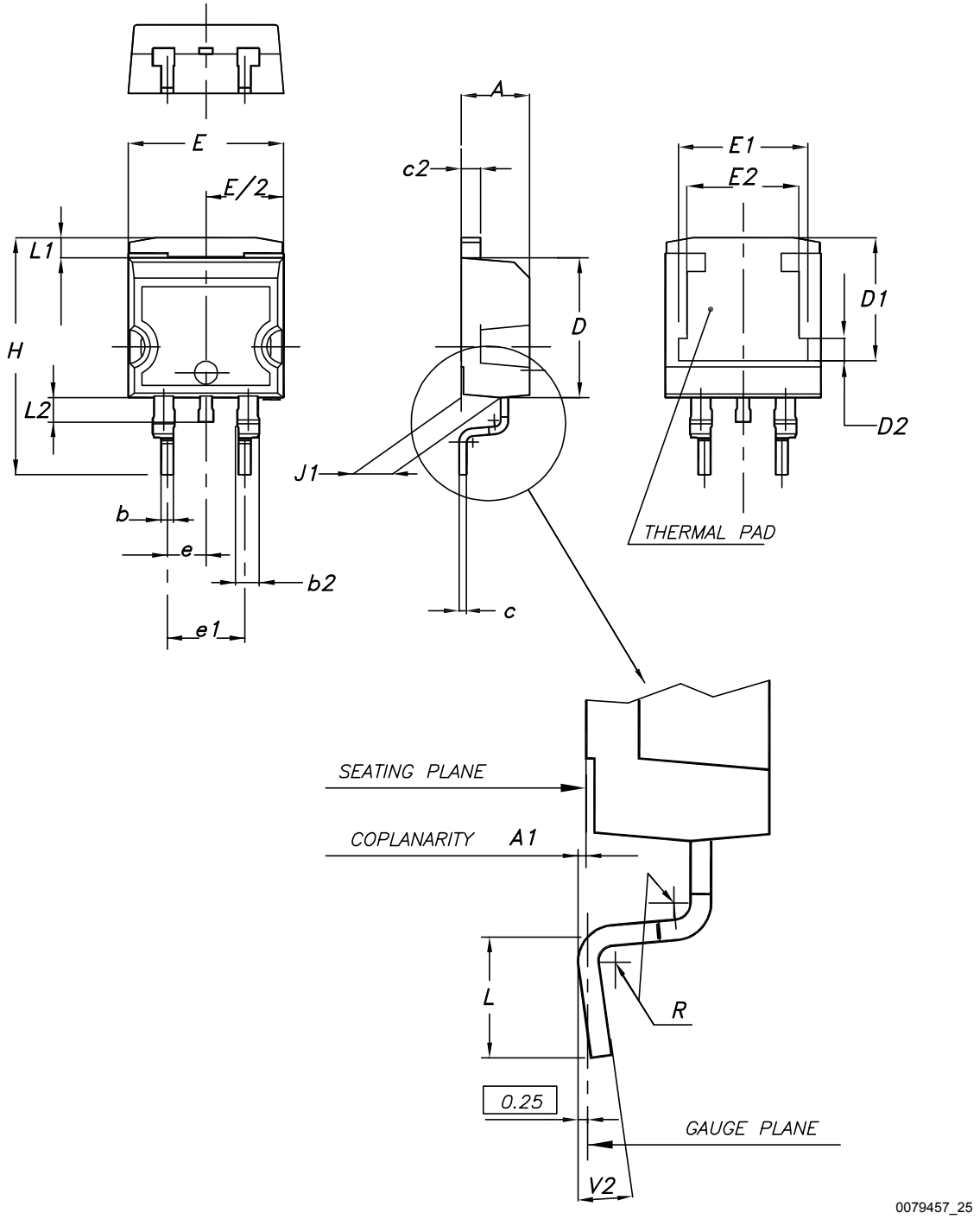
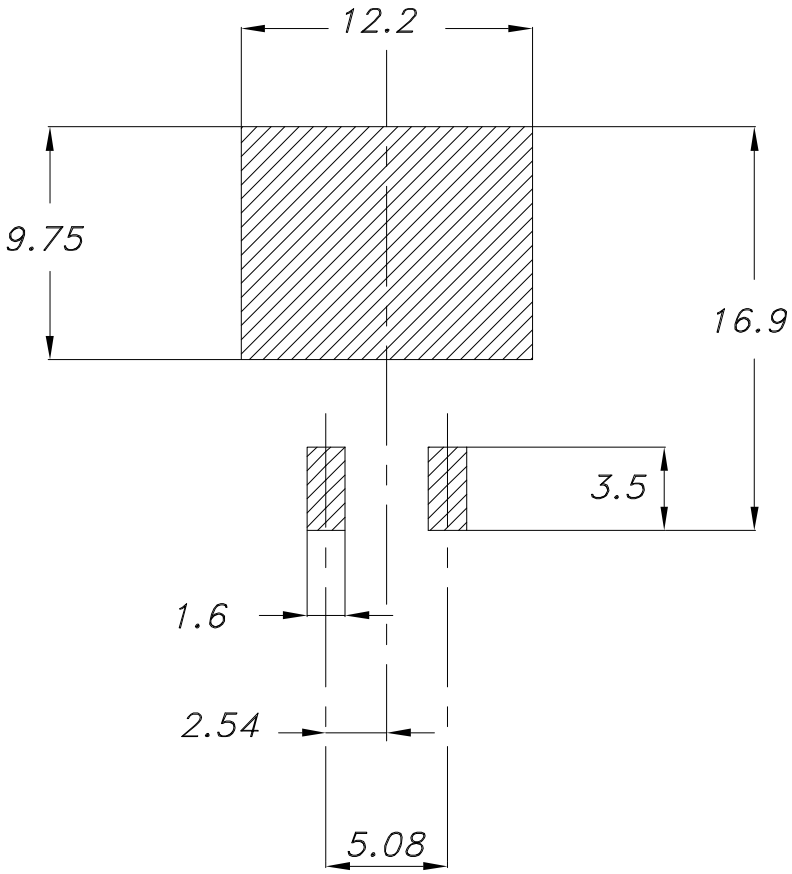


Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 22. D²PAK (TO-263) recommended footprint (dimensions are in mm)



Footprint

4.2 DPAK (TO-252) type A2 package information

Figure 23. **DPAK (TO-252) type A2 package outline**

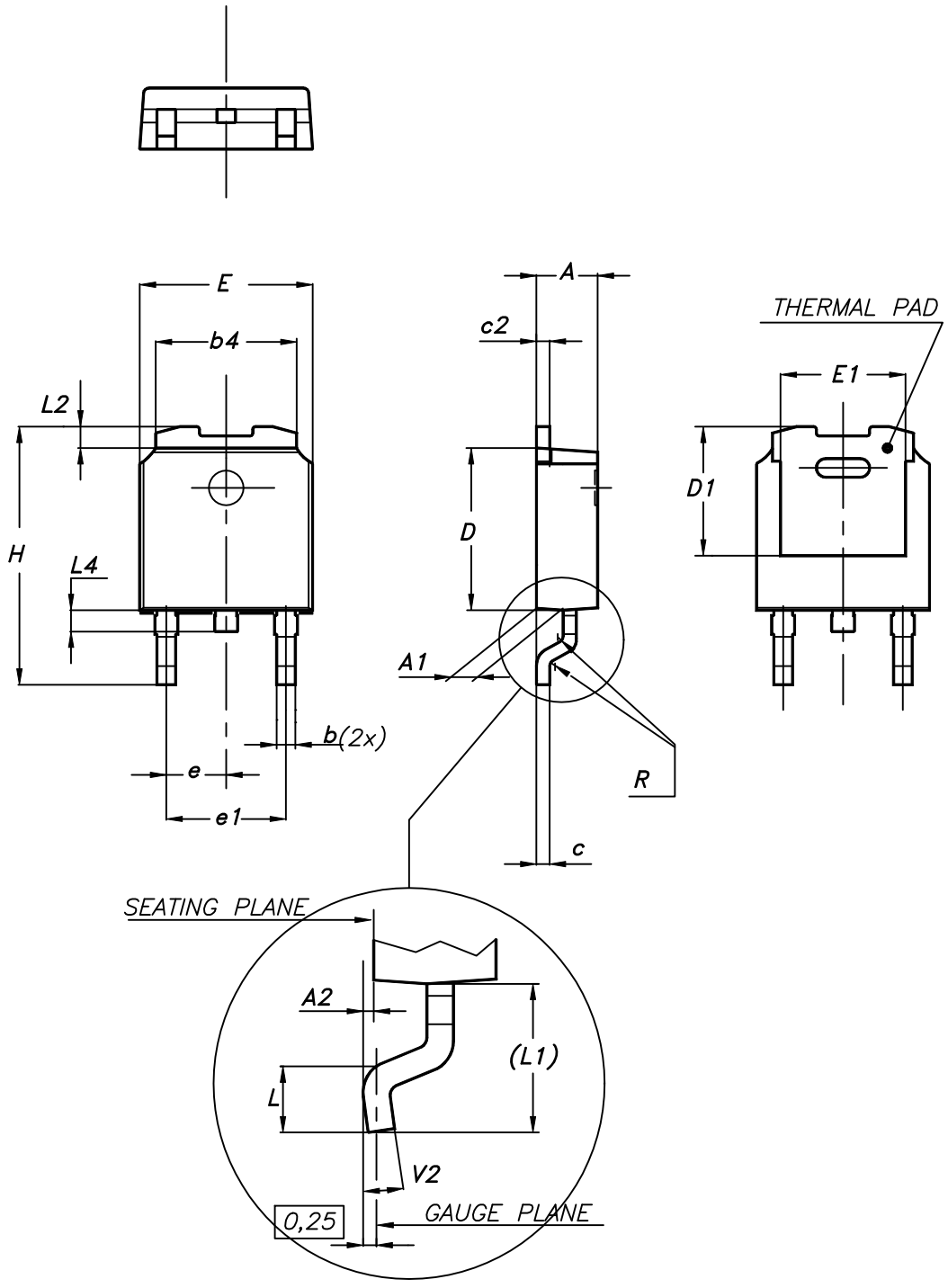
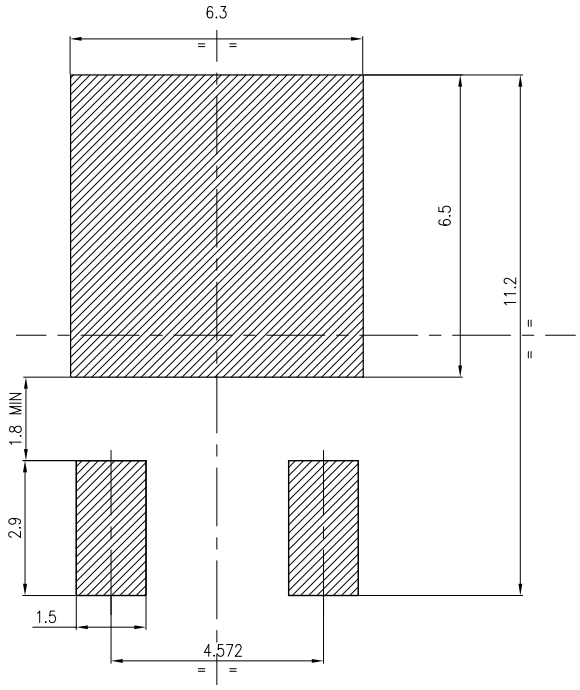


Table 9. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 24. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



4.3 D²PAK and DPAK packing information

Figure 25. Tape outline

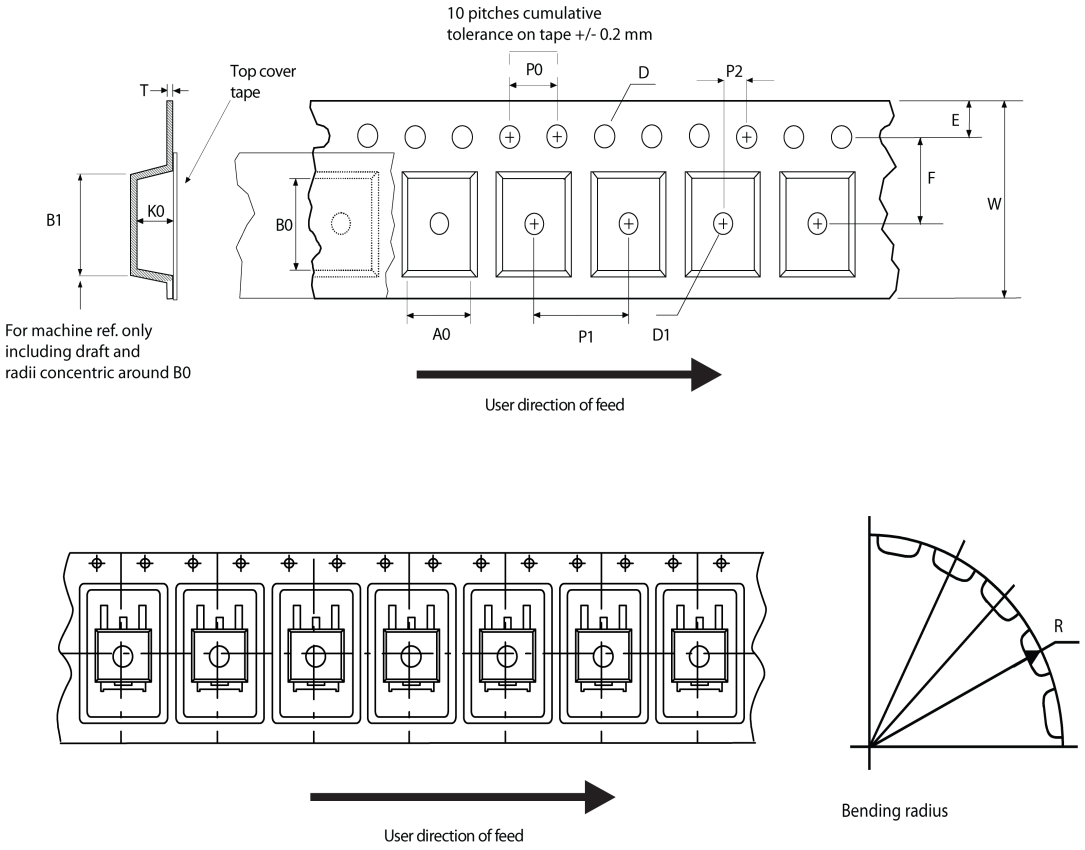
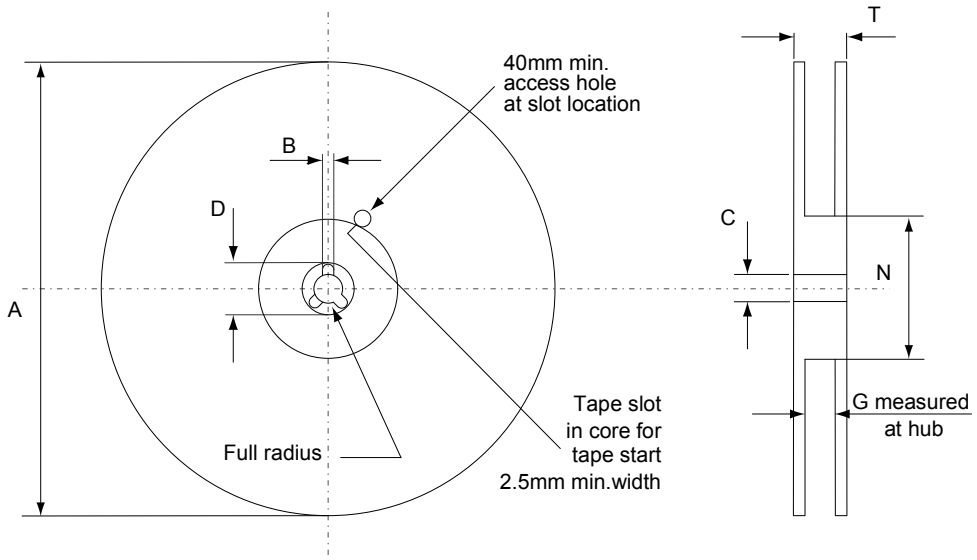


Figure 26. **Reel outline**



AM06038v1

Table 10. **D²PAK tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 11. **DPAK tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Ordering information

Table 12. **Order codes**

Order code	Marking	Package	Packing
STB18NF25	18NF25	D^2PAK	Tape and reel
STD18NF25		DPAK	

Revision history

Table 13. **Document revision history**

Date	Version	Changes
16-Nov-2009	1	First release.
19-Feb-2010	2	V_{DS} value in *Table 8* has been corrected.
26-Apr-2012	3	Updated E_{AS} in *Table 4: Avalanche data, Section 4: Package information* and *Section 4.3: Packing information.* Minor text changes.
10-Sep-2015	4	Updated *4.2: DPAK (TO-252) package information* Minor text changes.
07-May-2018	5	Removed maturity status indication from cover page. Modified title and features on cover page. Modified Table 5. Dynamic, Table 6. Switching times and Table 7. Source drain diode. Modified Figure 8. Static drain-source on resistance. Updated Section 4 Package information. Minor text changes.

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