



# STB18NM80, STF18NM80, STP18NM80, STW18NM80

N-channel 800 V, 0.25  $\Omega$ , 17 A, MDmesh™ Power MOSFET  
in D<sup>2</sup>PAK, TO-220FP, TO-220 and TO-247 packages

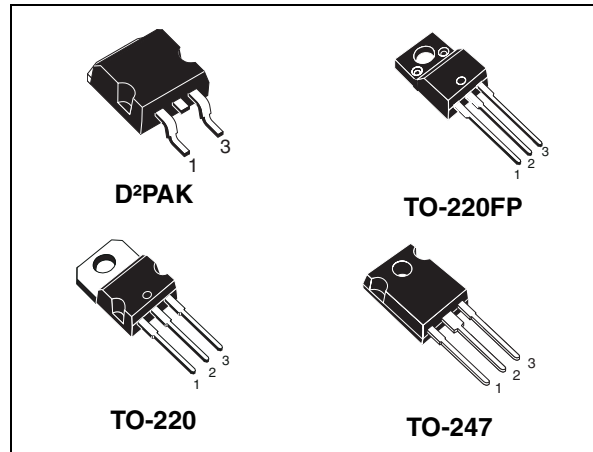
Datasheet — production data

## Features

Order codes	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>
STB18NM80	800 V	< 0.295 $\Omega$	17 A
STF18NM80	800 V	< 0.295 $\Omega$	17 A <sup>(1)</sup>
STP18NM80	800 V	< 0.295 $\Omega$	17 A
STW18NM80	800 V	< 0.295 $\Omega$	17 A

1. Limited only by maximum temperature allowed

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



## Application

- Switching applications

## Description

These N-channel Power MOSFETs are developed using STMicroelectronics' revolutionary MDmesh™ technology, which associates the multiple drain process with the company's PowerMESH™ horizontal layout. These devices offer extremely low on-resistance, high dv/dt and excellent avalanche characteristics. Utilizing ST's proprietary strip technique, these Power MOSFETs boast an overall dynamic performance which is superior to similar products on the market.

Figure 1. Internal schematic diagram

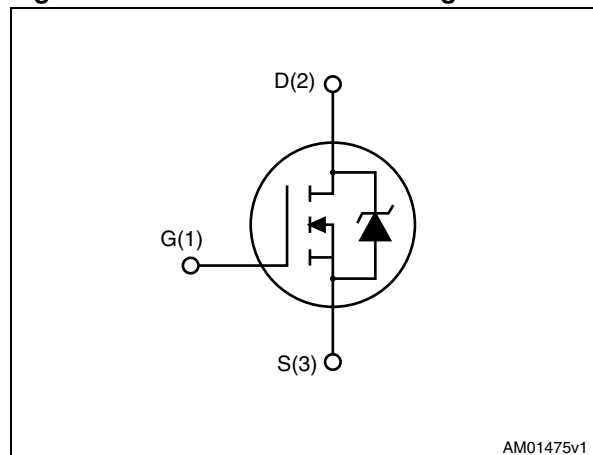


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB18NM80	18NM80	D <sup>2</sup> PAK	Tape and reel
STF18NM80		TO-220FP	Tube
STP18NM80		TO-220	
STW18NM80		TO-247	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value				Unit
		TO-220	D <sup>2</sup> PAK	TO-247	TO-220FP	
V <sub>DS</sub>	Drain-source voltage	800				V
V <sub>GS</sub>	Gate-source voltage	± 30				V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	17		17 <sup>(1)</sup>		A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	10.71		10.71 <sup>(1)</sup>		A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	68		68 <sup>(1)</sup>		A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	190		40		W
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)	2500				V
T <sub>stg</sub>	Storage temperature	-65 to 150				°C
T <sub>j</sub>	Max. operating junction temperature	150				°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area

**Table 3. Thermal data**

Symbol	Parameter	Value				Unit
		TO-220	D <sup>2</sup> PAK	TO-247	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case	0.66		3.13		°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-amb	62.5		50	62.5	°C/W
R <sub>thj-pcb</sub>	Thermal resistance junction-pcb		30			°C/W
T <sub>l</sub>	Maximum lead temperature for soldering purpose	300				°C

**Table 4. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
I <sub>AS</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>j</sub> max)	4	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AS</sub> , V <sub>DD</sub> = 50 V)	600	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	800			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 800\text{ V}$ , $V_{DS} = 800\text{ V}$ , $T_C = 125\text{ °C}$			10 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 30\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 8.5\text{ A}$		0.25	0.295	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$ , $I_D = 8.5\text{ A}$	-	14	-	S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	2070 210 29	-	pF pF pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }640\text{ V}$	-	316	-	pF
$R_G$	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain	-	4	-	$\Omega$
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 640\text{ V}$ , $I_D = 17\text{ A}$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17</a> )	-	70 13 40	-	nC nC nC

1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%
2.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$ , $I_D = 8.5\text{ A}$ ,		18		ns
$t_r$	Rise time	$R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$	-	28	-	ns
$t_{d(off)}$	Turn-off delay time	(see <a href="#">Figure 16</a> and		96		ns
$t_f$	Fall time	<a href="#">Figure 21</a> )		50		ns

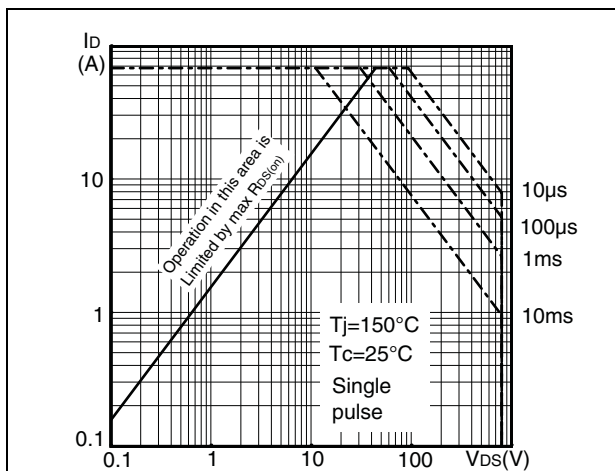
**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}$ , $di/dt = 100$		618		ns
$Q_{rr}$	Reverse recovery charge	$A/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ ,	-	9.6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 18</a> )		31.2		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}$ ,		822		ns
$Q_{rr}$	Reverse recovery charge	$di/dt = 100\text{ A}/\mu\text{s}$ ,	-	13		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	$V_{DD} = 100\text{ V}$ , $T_j = 150^\circ\text{C}$		31.8		A
		(see <a href="#">Figure 18</a> )				

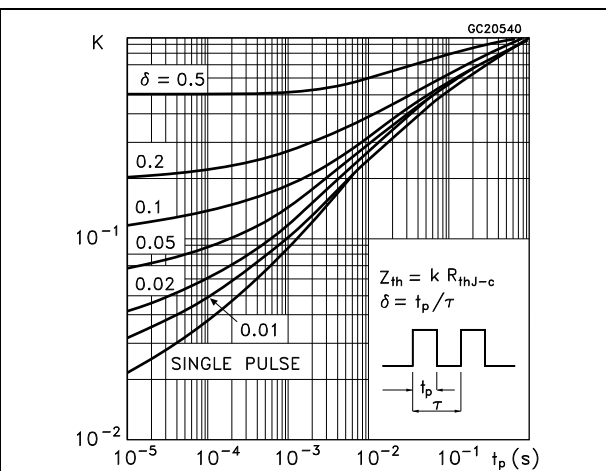
1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

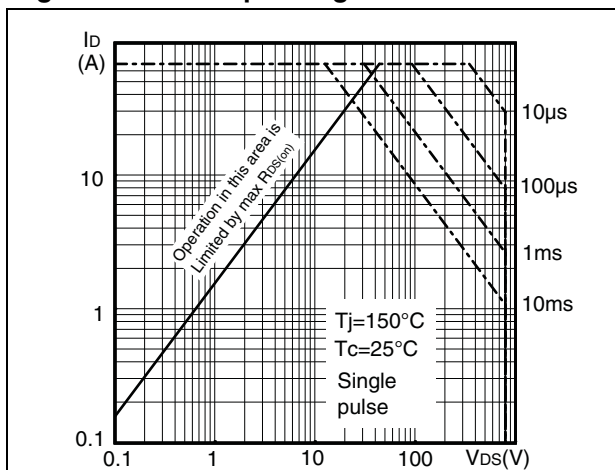
**Figure 2. Safe operating area for TO-220, D<sup>2</sup>PAK**



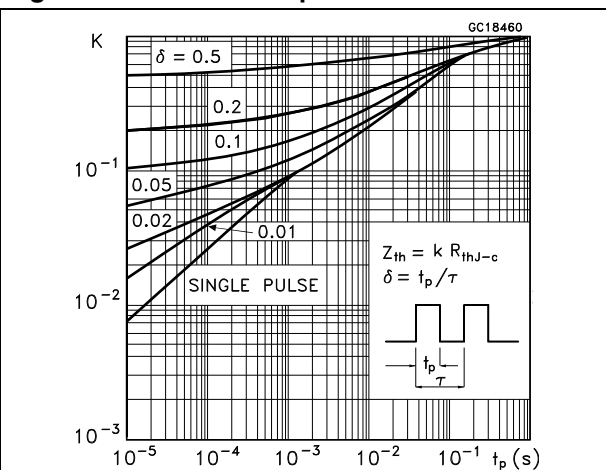
**Figure 3. Thermal impedance for TO-220, D<sup>2</sup>PAK**



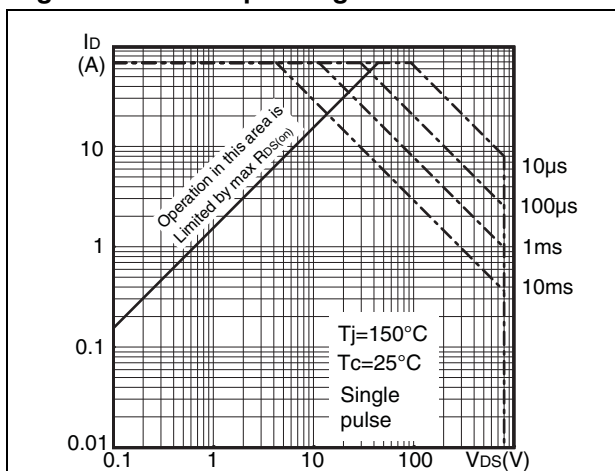
**Figure 4. Safe operating area for TO-247**



**Figure 5. Thermal impedance for TO-247**



**Figure 6. Safe operating area for TO-220FP**



**Figure 7. Thermal impedance for TO-220FP**

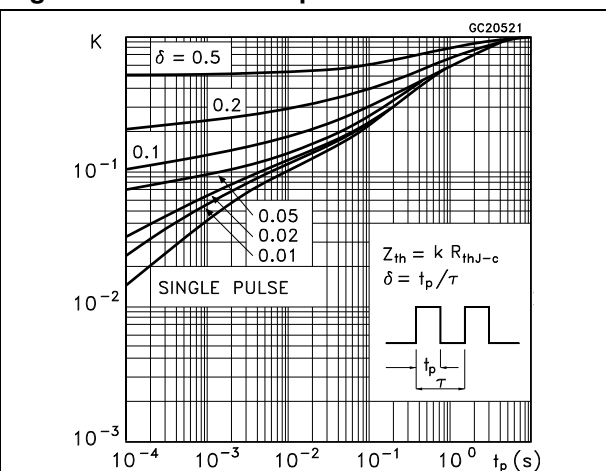


Figure 8. Output characteristics

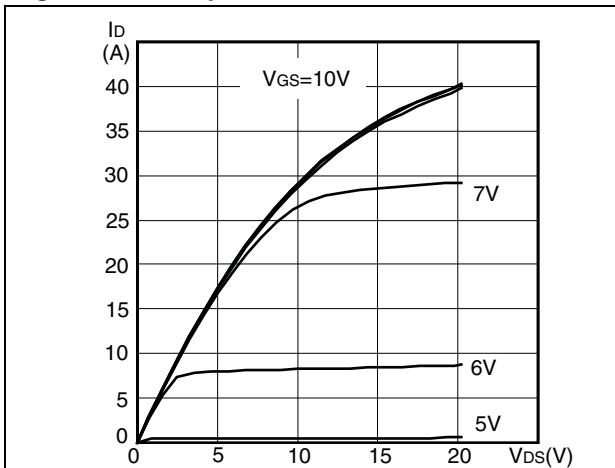


Figure 9. Transfer characteristics

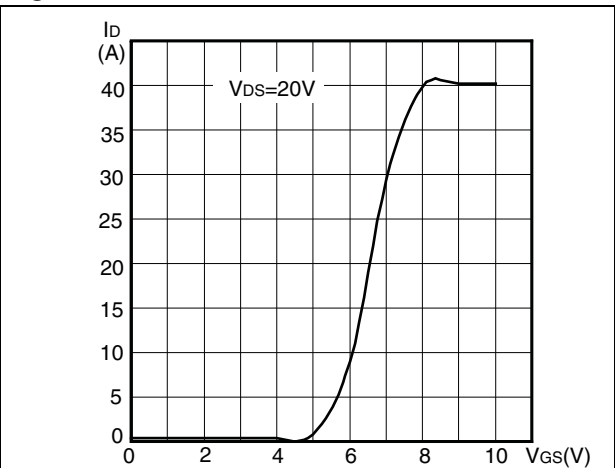


Figure 10. Normalized  $B_{V_{DSS}}$  vs temperature

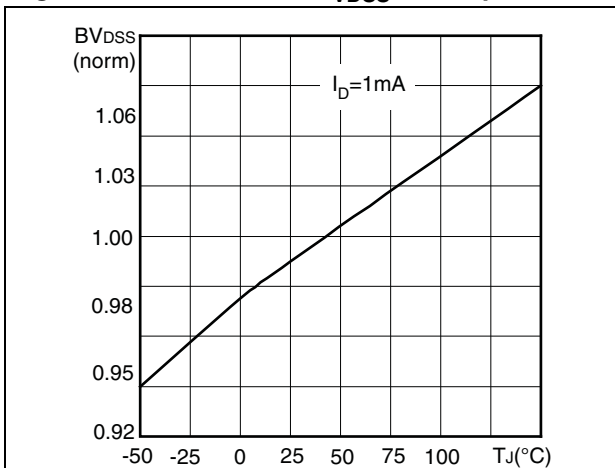


Figure 11. Static drain-source on-resistance

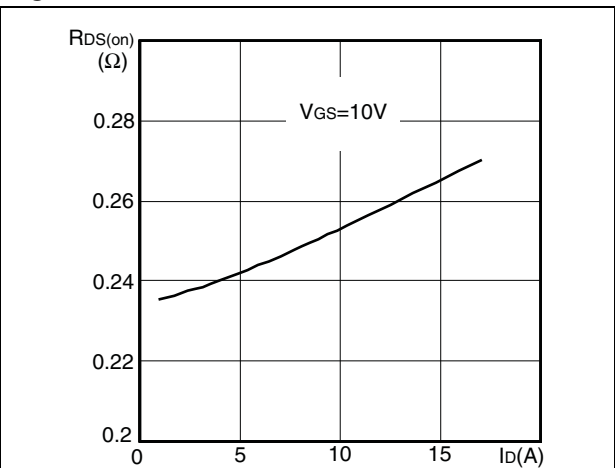


Figure 12. Gate charge vs gate-source voltage

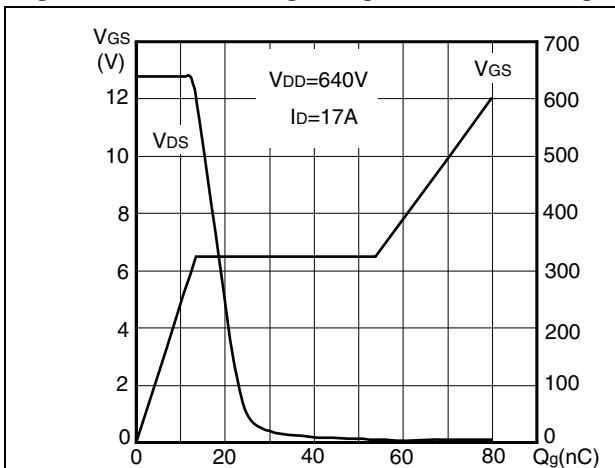


Figure 13. Capacitance variations

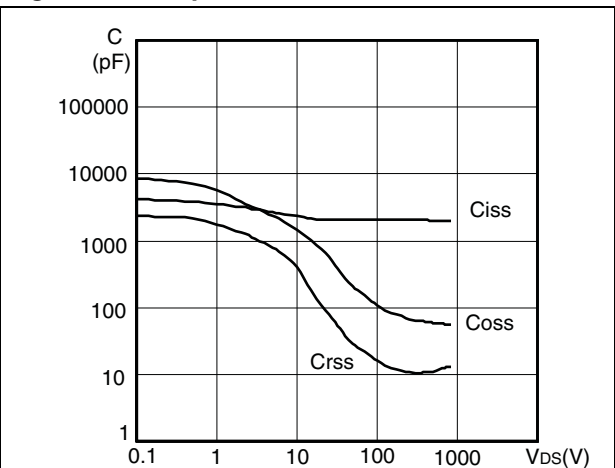


Figure 14. Normalized gate threshold voltage vs temperature

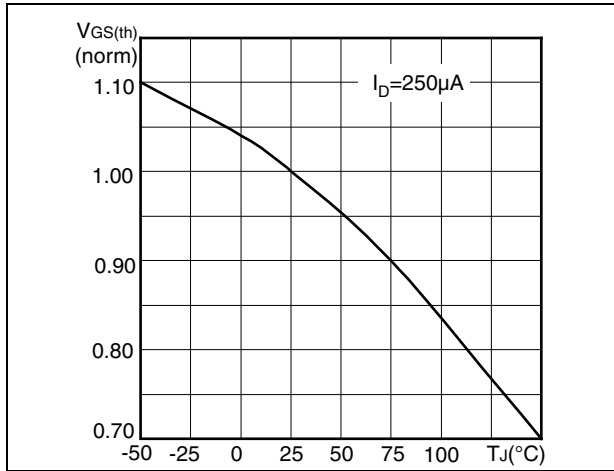
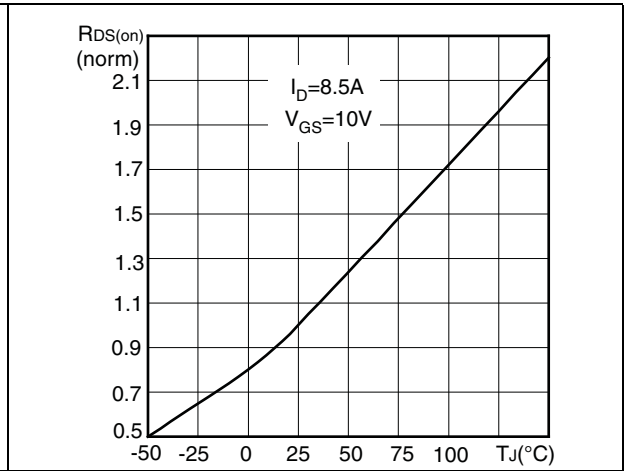


Figure 15. Normalized on-resistance vs temperature





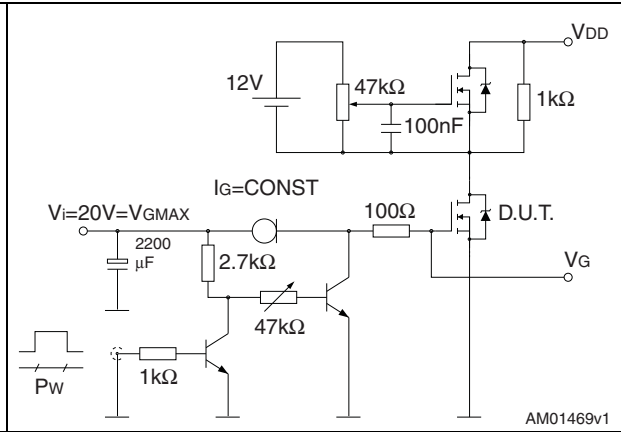
### 3 Test circuits

**Figure 16. Switching times test circuit for resistive load**



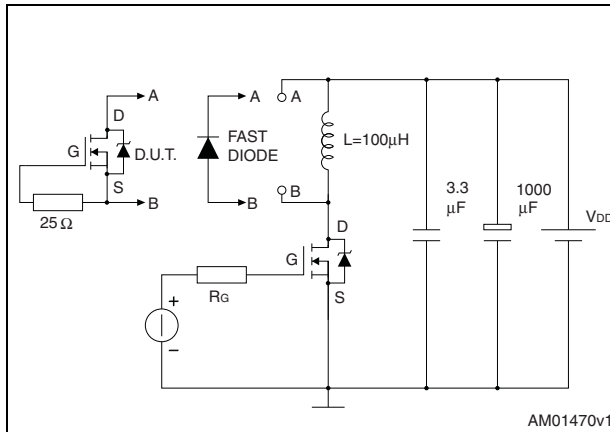
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**Figure 17. Gate charge test circuit**



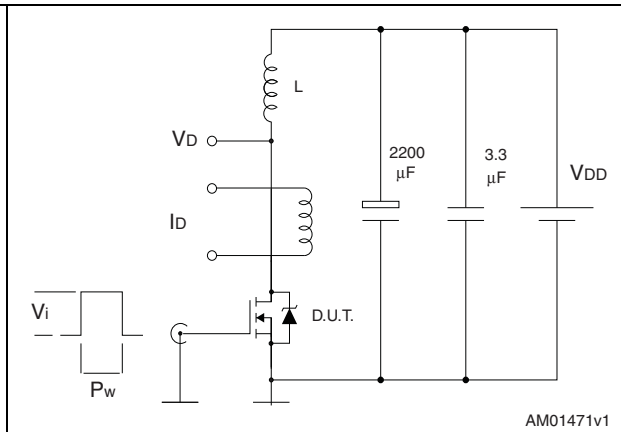
AM01469v1

**Figure 18. Test circuit for inductive load switching and diode recovery times**



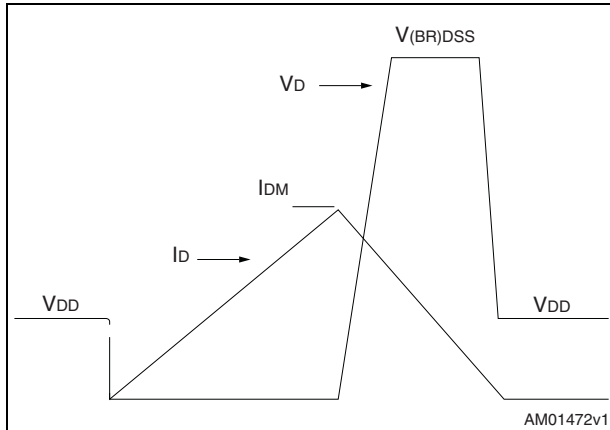
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**Figure 19. Unclamped inductive load test circuit**



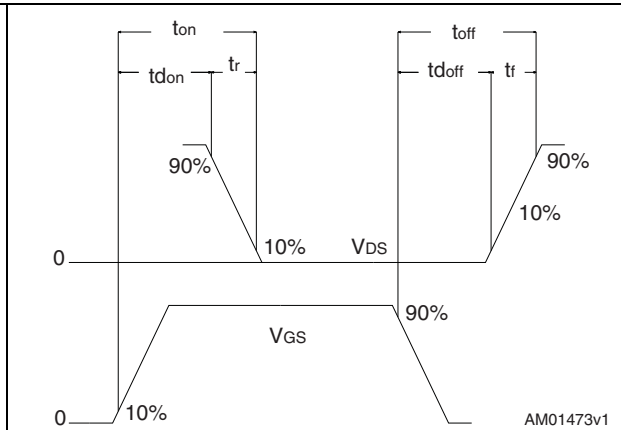
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**Figure 20. Unclamped inductive waveform**



AM01472v1

**Figure 21. Switching time waveform**



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 9. D<sup>2</sup>PAK (TO-263) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 22. D<sup>2</sup>PAK (TO-263) drawing



Figure 23. D<sup>2</sup>PAK footprint<sup>(a)</sup>



a. All dimensions are in millimeters

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 24. TO-220FP drawing



7012510\_Rev\_K\_B

Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 25. TO-220 type A drawing

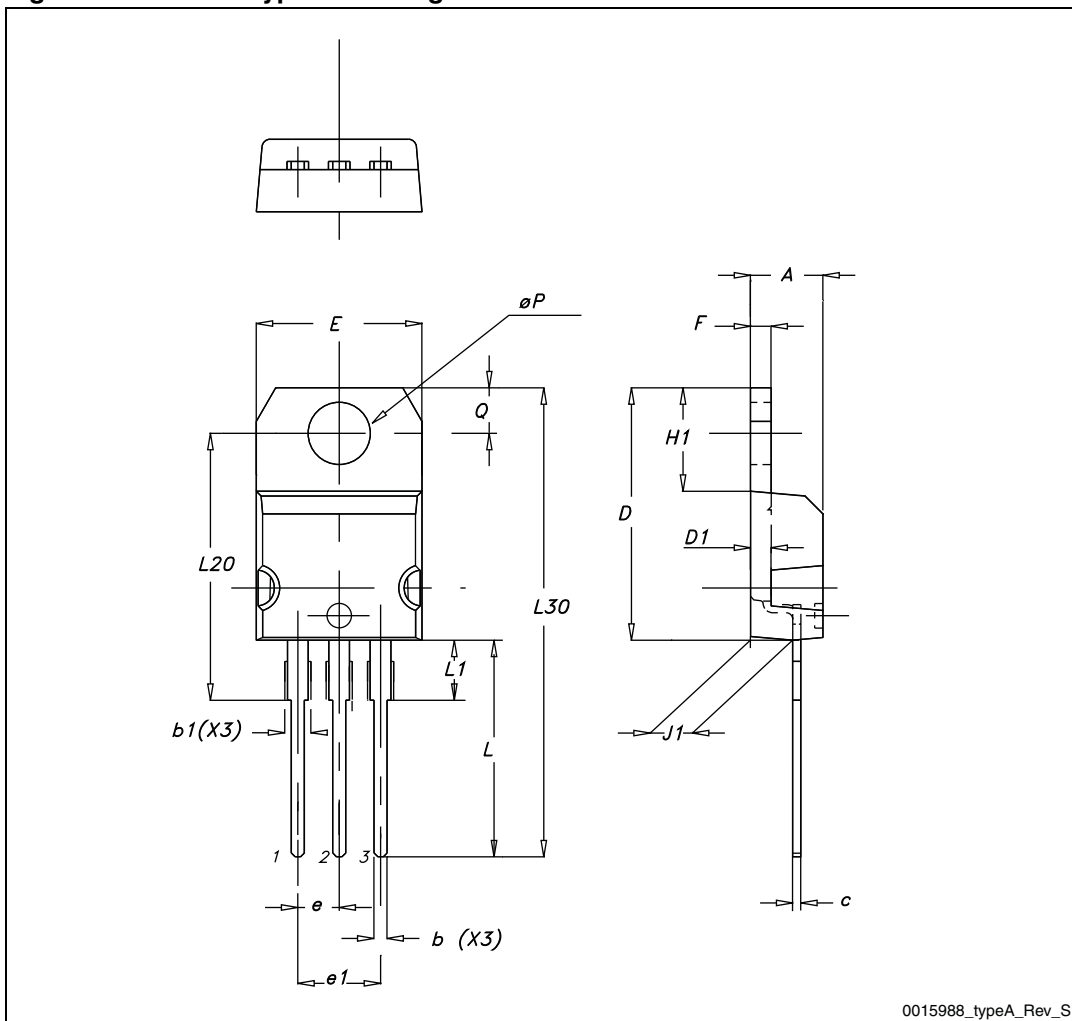


Table 12. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70



Figure 26. TO-247 drawing



0075325\_G

## 5 Packaging mechanical data

Table 13. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

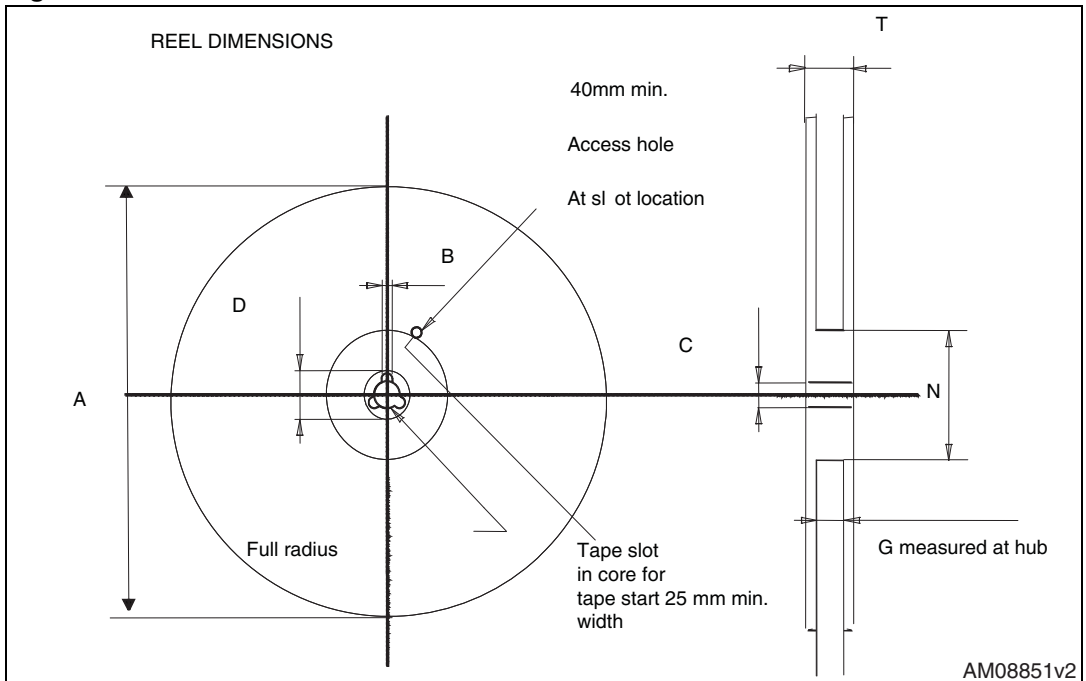
Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 27. Tape



AM08852v2

Figure 28. Reel



AM08851v2

## 6 Revision history

Table 14. Document revision history

Date	Revision	Changes
25-Feb-2009	1	First release.
07-Apr-2009	2	<a href="#">Section 4: Package mechanical data</a> has been modified.
20-Apr-2009	3	$R_{DS(on)}$ max value has been corrected.
09-Sep-2009	4	Document status promoted from preliminary data to datasheet.
25-May-2012	5	<a href="#">Figure 12: Gate charge vs gate-source voltage</a> has been updated. Minor text changes.

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