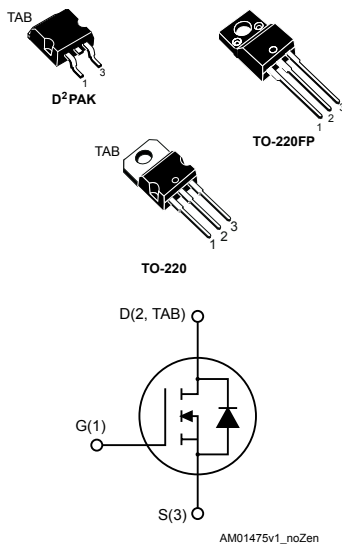


N-channel 600 V, 0.20 Ω typ., 16 A MDmesh™ II Power MOSFETs in D²PAK, TO-220FP and TO-220 packages



Features

Order code	V_{DS} @ $T_{jmax.}$	$R_{DS(on)max.}$	I_D
STB22NM60N	650 V	0.22 Ω	16 A
STF22NM60N			
STP22NM60N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Product status

STB22NM60N

STF22NM60N

STP22NM60N

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		D ² PAK	TO-220	TO-220FP	
V _{GS}	Gate-source voltage	± 30			V
I _D	Drain current (continuous) at T _C = 25 °C	16		16 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	10		10 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	64		64 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	125		30	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15			V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)			2500	V
T _j	Operating junction temperature range	-55 to 150			°C
T _{stg}	Storage temperature range				

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- $I_{SD} \leq 16$ A, $di/dt \leq 400$ A/ μ s, $V_{DSpeak} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		D ² PAK	TO-220	TO-220FP	
R _{thj-case}	Thermal resistance junction-case	1		4.17	°C/W
R _{thj-amb}	Thermal resistance junction-ambient			62.5	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	30			°C/W

- When mounted on 1inch² FR-4 board, 2 oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _j Max)	6	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	300	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			100	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 8\text{ A}$		0.20	0.22	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1330	-	μF
C_{oss}	Output capacitance			84		
C_{rss}	Reverse transfer capacitance			4.6		
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	181	-	μF
R_g	Gate input resistance	$f = 1\text{ MHz}$ open drain	-	4.7	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 16\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	44	-	nC
Q_{gs}	Gate-source charge			6		
Q_{gd}	Gate-drain charge			25		

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 8\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	11	-	ns
$t_{r(v)}$	Voltage rise time			18		
$t_{d(off)}$	Turn-off delay time			74		
$t_{f(i)}$	Fall time			38		

Table 7. Source drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				16	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		64	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 16\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 16\text{ A}$, $di/dt = 100\text{ V}$		296		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	4		μC
I_{RRM}	Reverse recovery current			26.8		A
t_{rr}	Reverse recovery time	$I_{SD} = 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		350		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	4.7		μC
I_{RRM}	Reverse recovery current			27		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

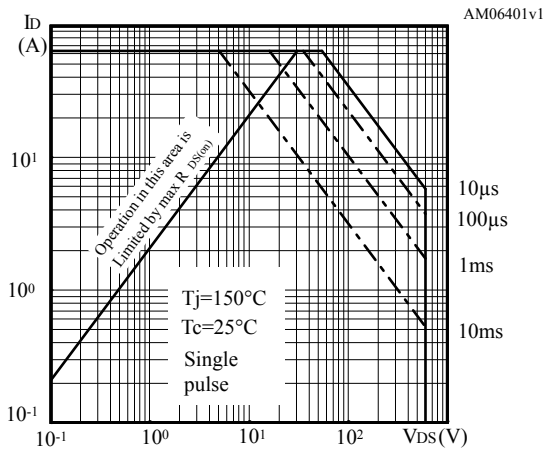
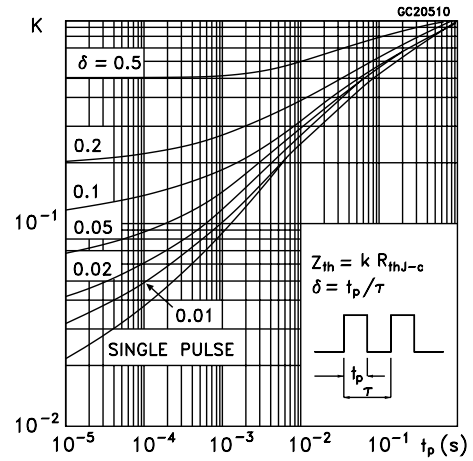
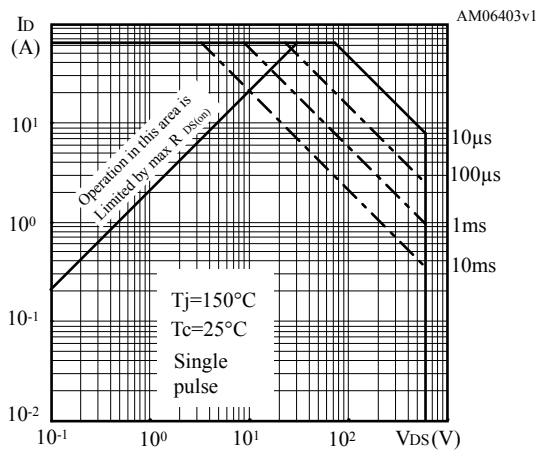
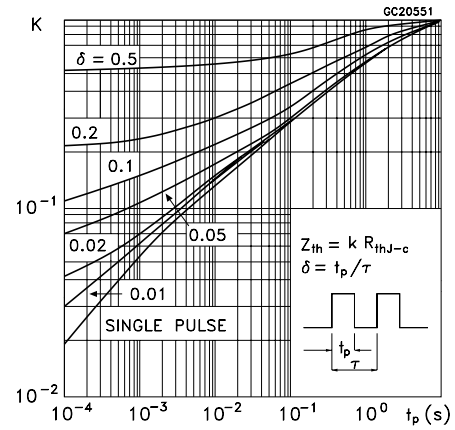
2.1 Electrical characteristics curves
Figure 1. Safe operating area for TO-220, D²PAK

Figure 2. Thermal impedance for TO-220, D²PAK

Figure 3. Safe operating area for TO-220FP

Figure 4. Thermal impedance for TO-220FP


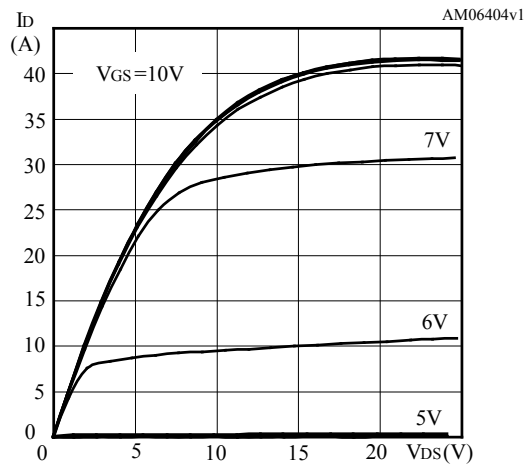
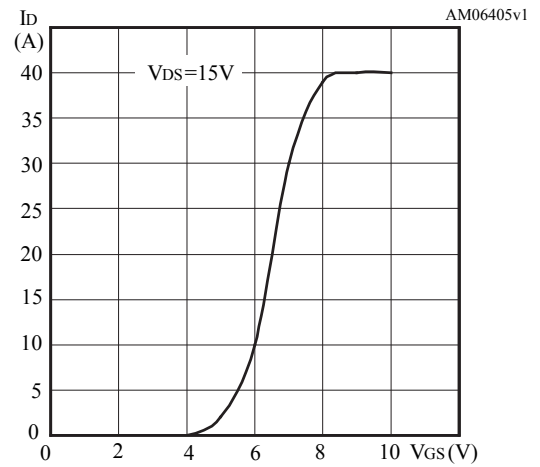
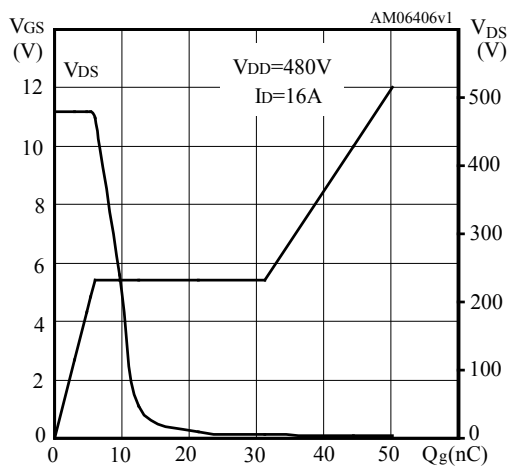
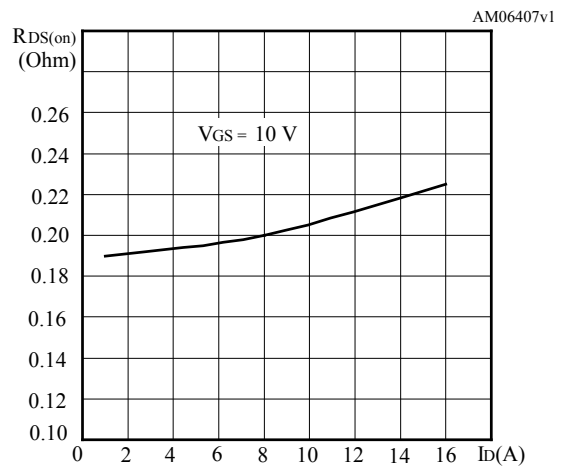
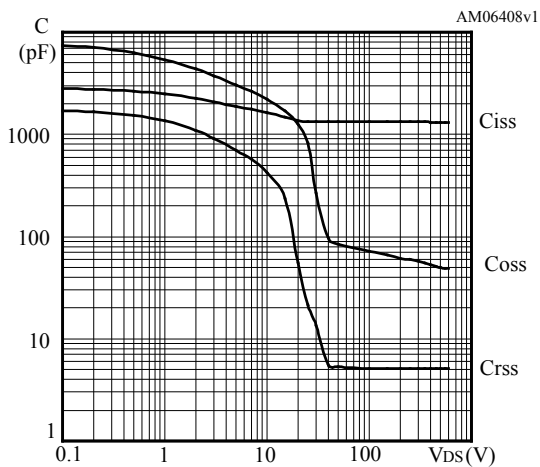
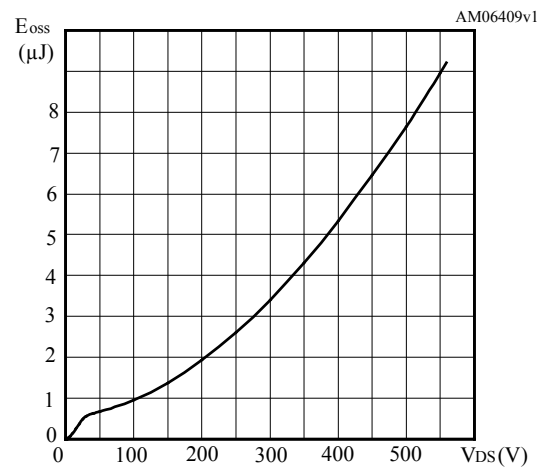
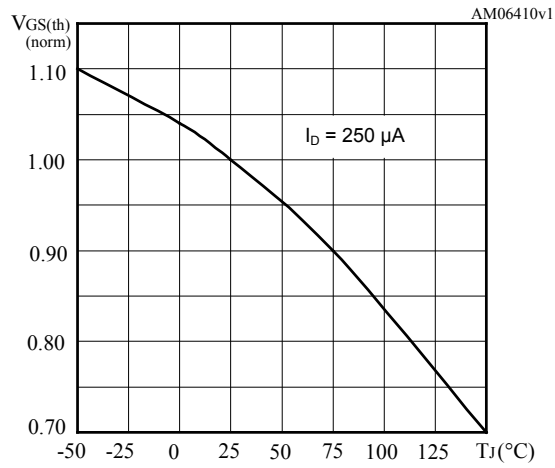
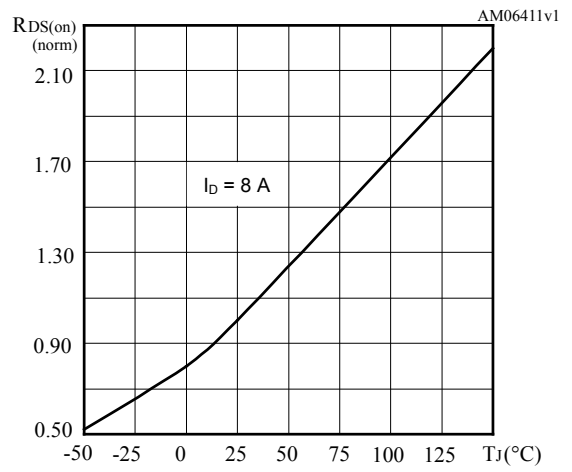
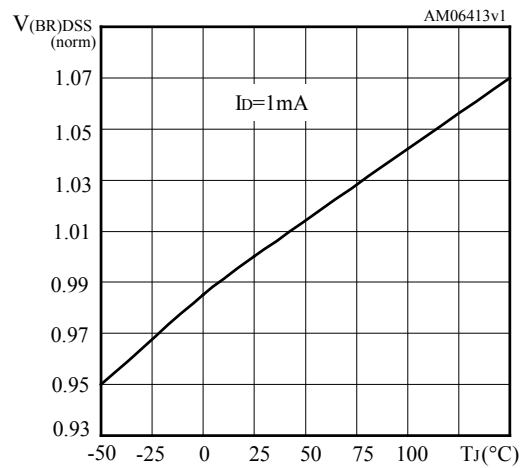
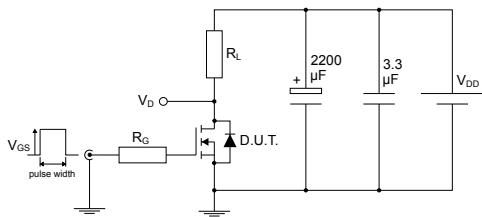
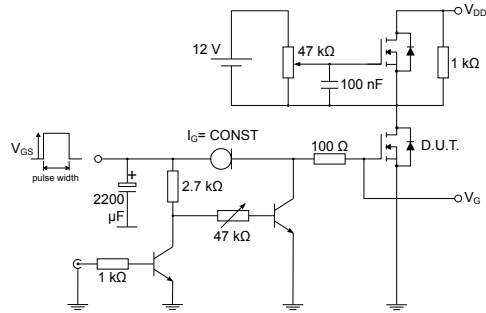
Figure 5. Output characteristics

Figure 6. Transfer characteristics

Figure 7. Gate charge vs gate-source voltage

Figure 8. Static drain-source on resistance

Figure 9. Capacitance variations

Figure 10. Output capacitance stored energy


Figure 11. Normalized gate threshold voltage vs temperature

Figure 12. Normalized on resistance vs temperature

Figure 13. Normalized $V_{(BR)DSS}$ vs temperature


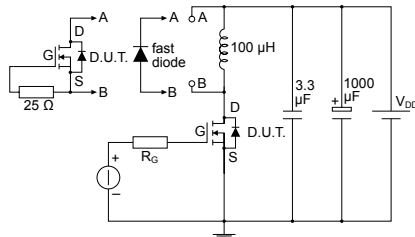
3 Test circuits

Figure 14. Test circuit for resistive load switching times


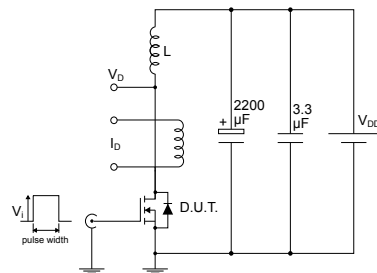
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Figure 15. Test circuit for gate charge behavior


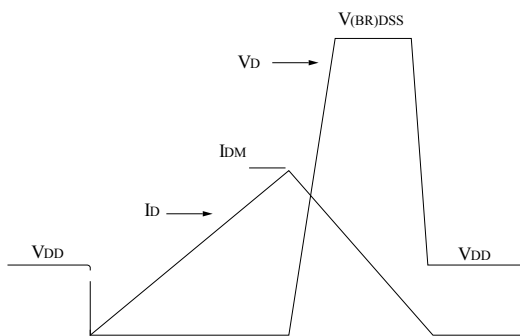
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Figure 16. Test circuit for inductive load switching and diode recovery times


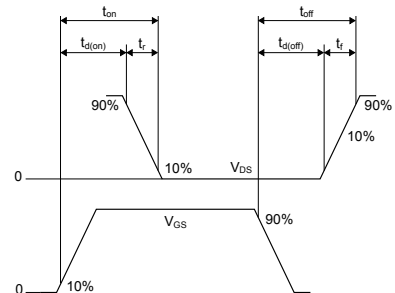
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Figure 17. Unclamped inductive load test circuit


AM01471v1

Figure 18. Unclamped inductive waveform


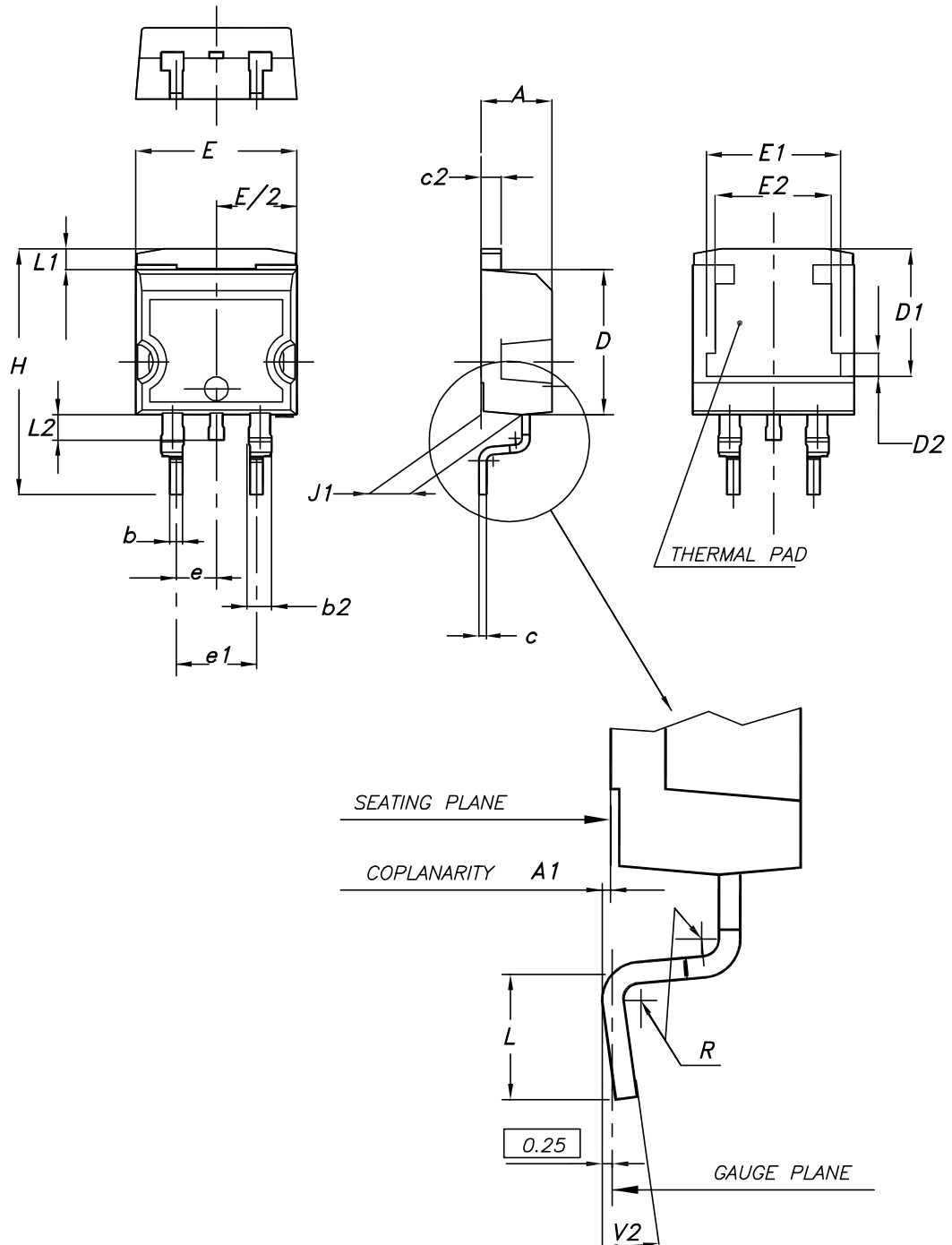
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Figure 19. Switching time waveform


AM01473v1

4 Package information

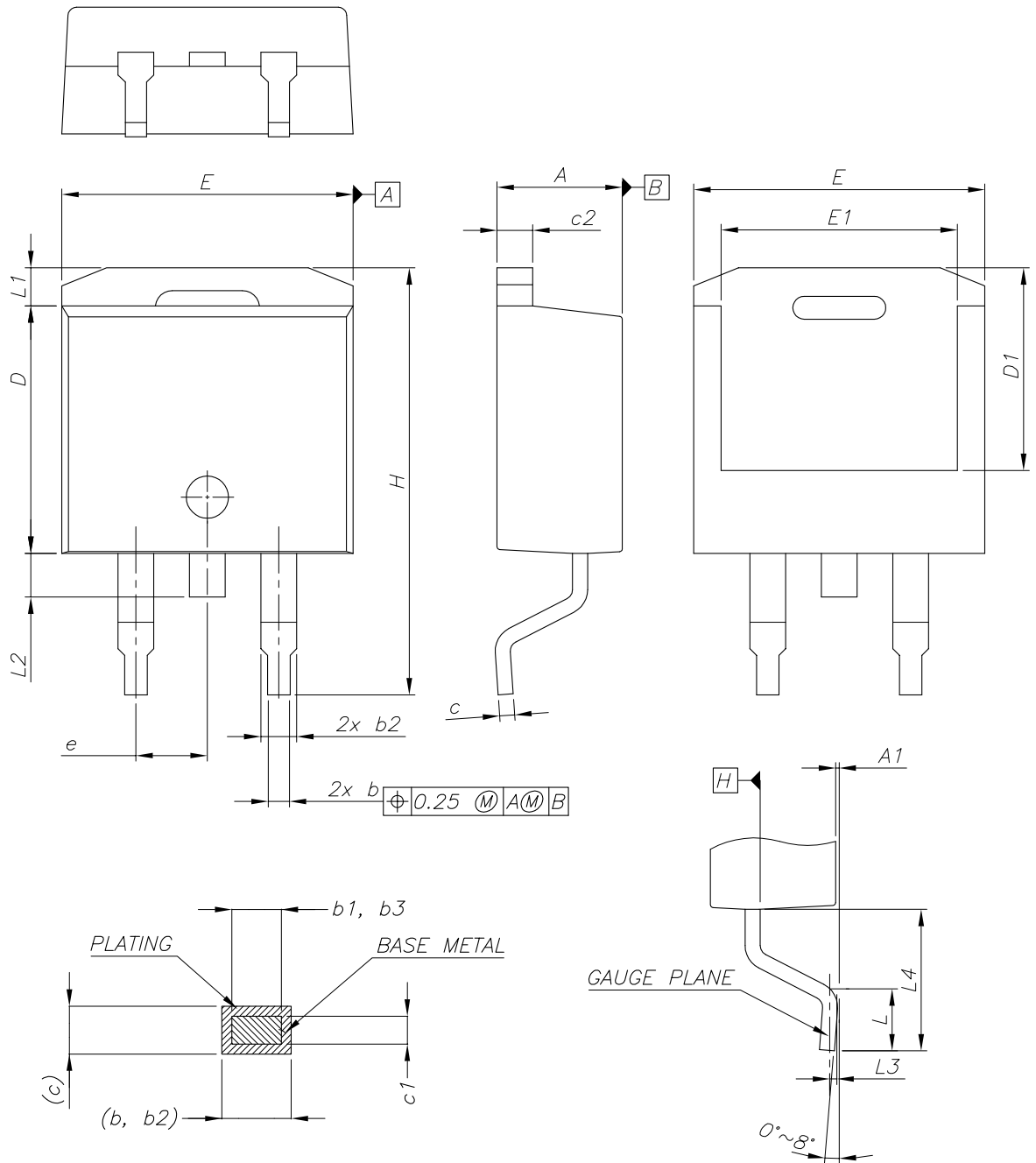
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4.1 D²PAK (TO-263) type A package information
Figure 20. D²PAK (TO-263) type A package outline


0079457_25

Table 8. D²PAK (TO-263) type A package mechanical data

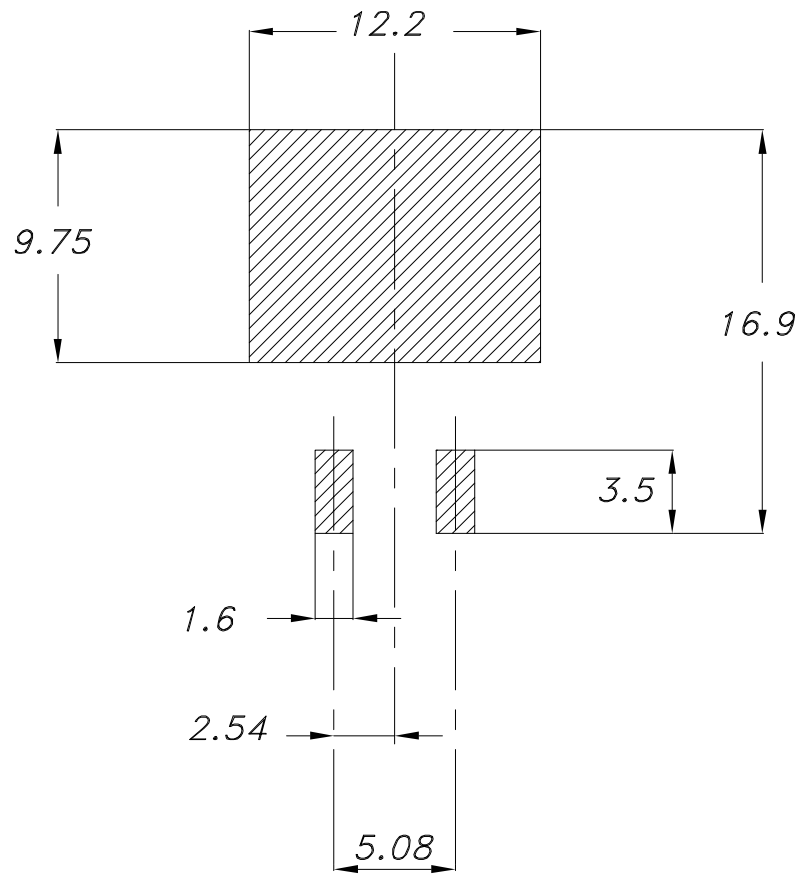
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

4.2 D²PAK (TO-263) type B package information
Figure 21. D²PAK (TO-263) type B package outline


0079457_25_B

Table 9. D²PAK (TO-263) type B mechanical data

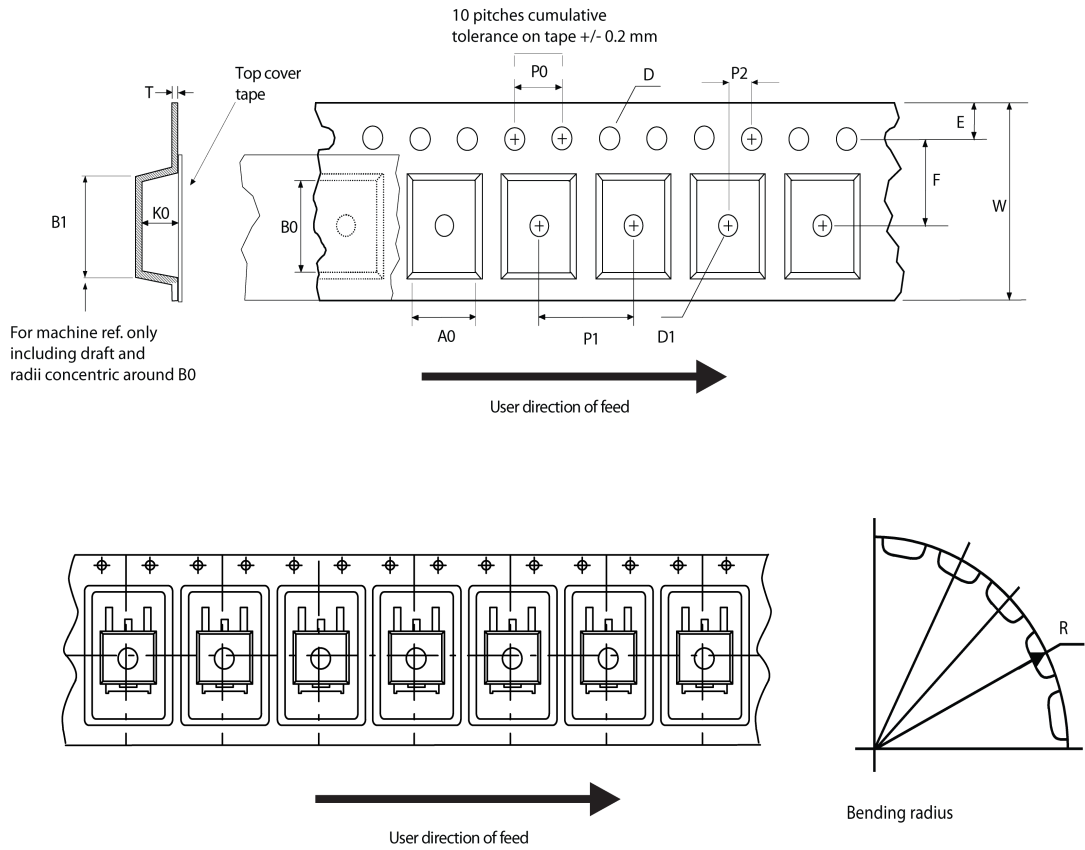
Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
b3	1.36		1.46
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

Figure 22. D²PAK (TO-263) recommended footprint (dimensions are in mm)


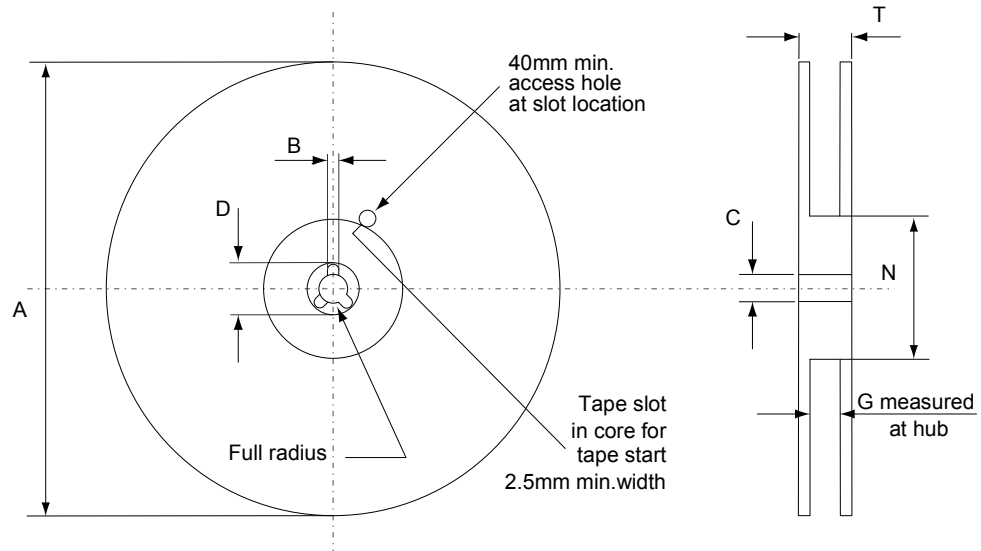
Footprint

4.3 D²PAK packing information

Figure 23. D²PAK tape outline



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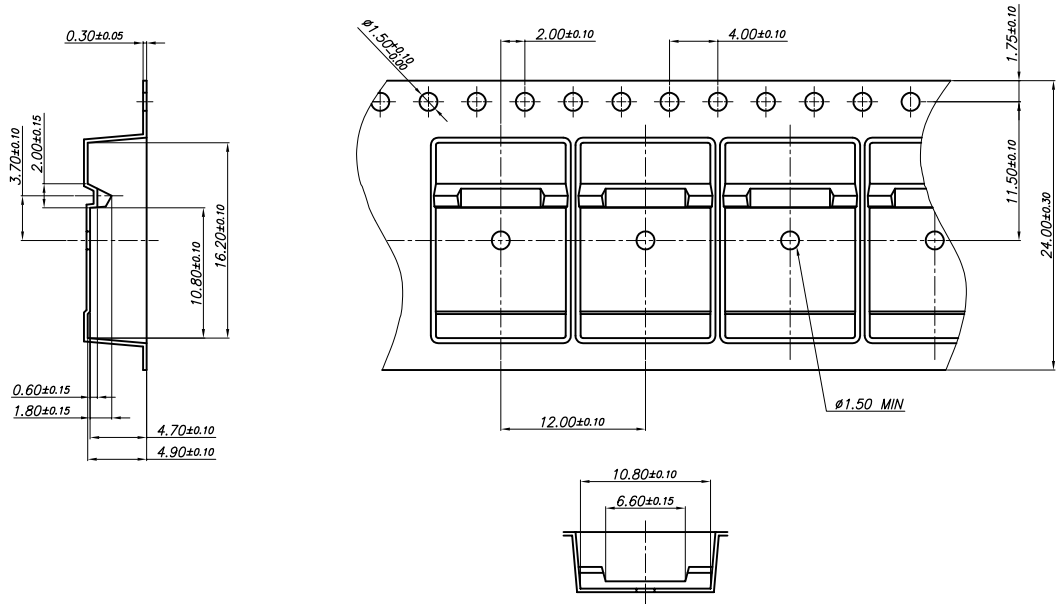
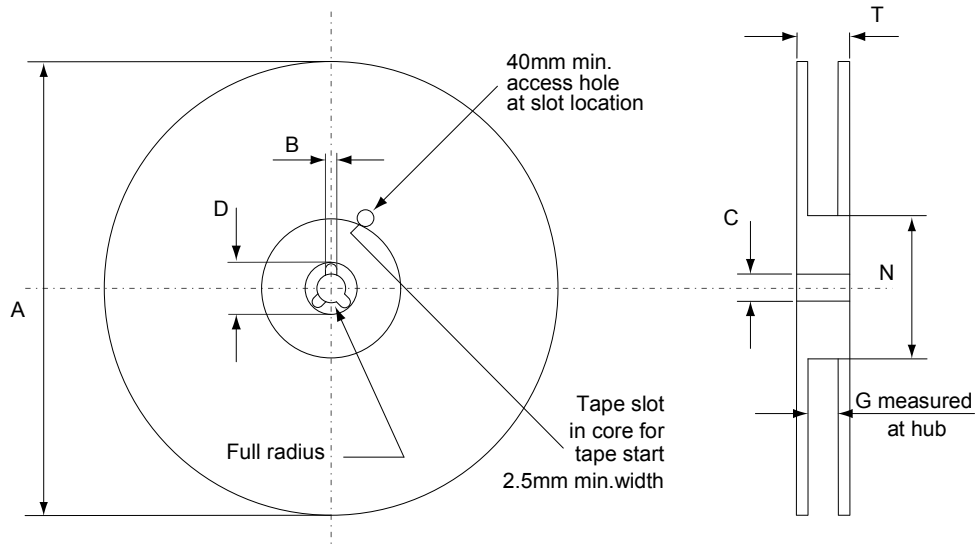
Figure 24. D²PAK reel outline


AM06038v1

Table 10. D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

4.4 D²PAK type B packing information

Figure 25. D²PAK type B tape outline

Figure 26. D²PAK type B reel outline


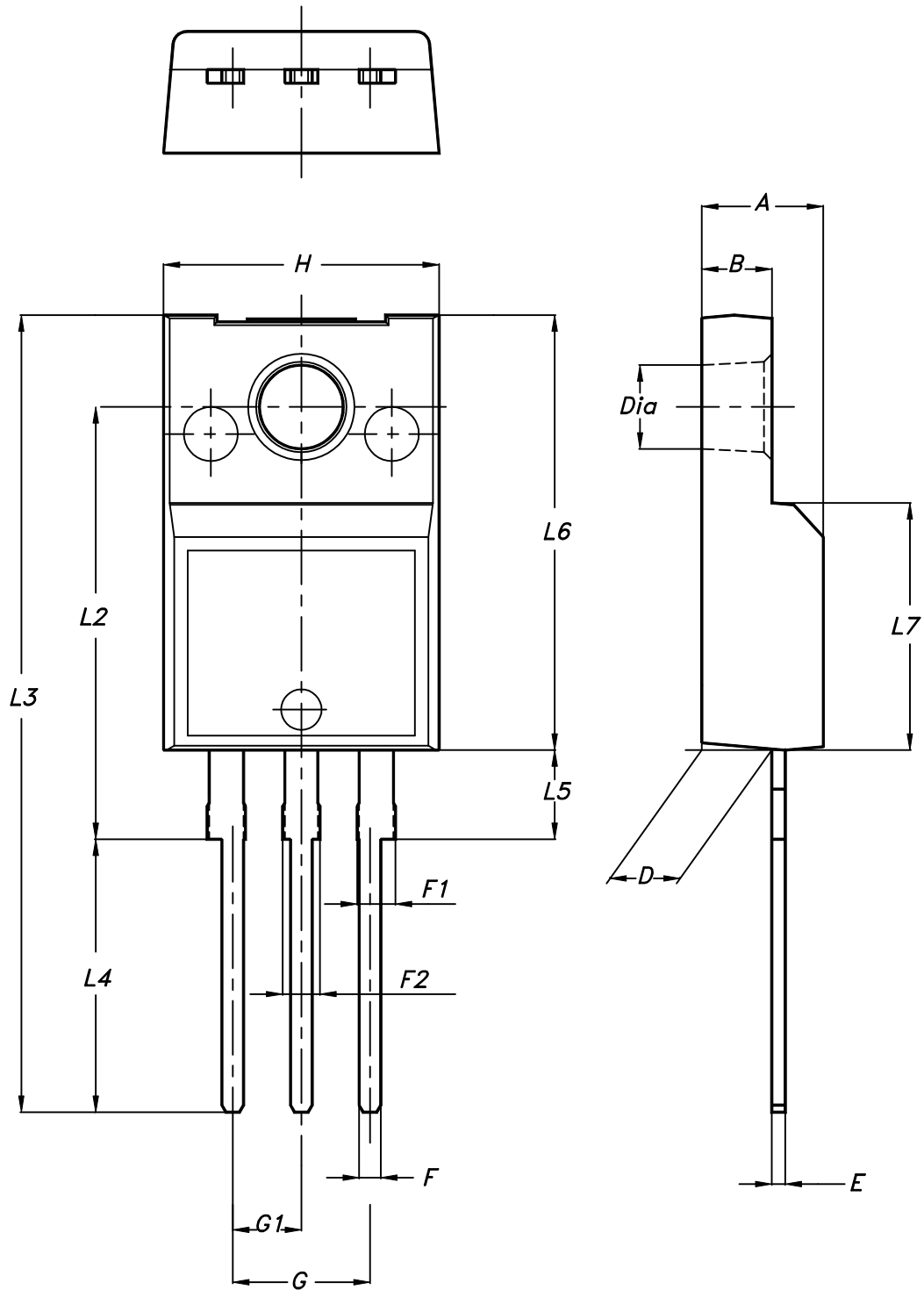
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Table 11. D²PAK type B reel mechanical data

Dim.	mm	
	Min.	Max.
A		330
B	1.5	
C	12.8	13.2
D	20.2	
G	24.4	26.4
N	100	
T		30.4

4.5 TO-220FP package information

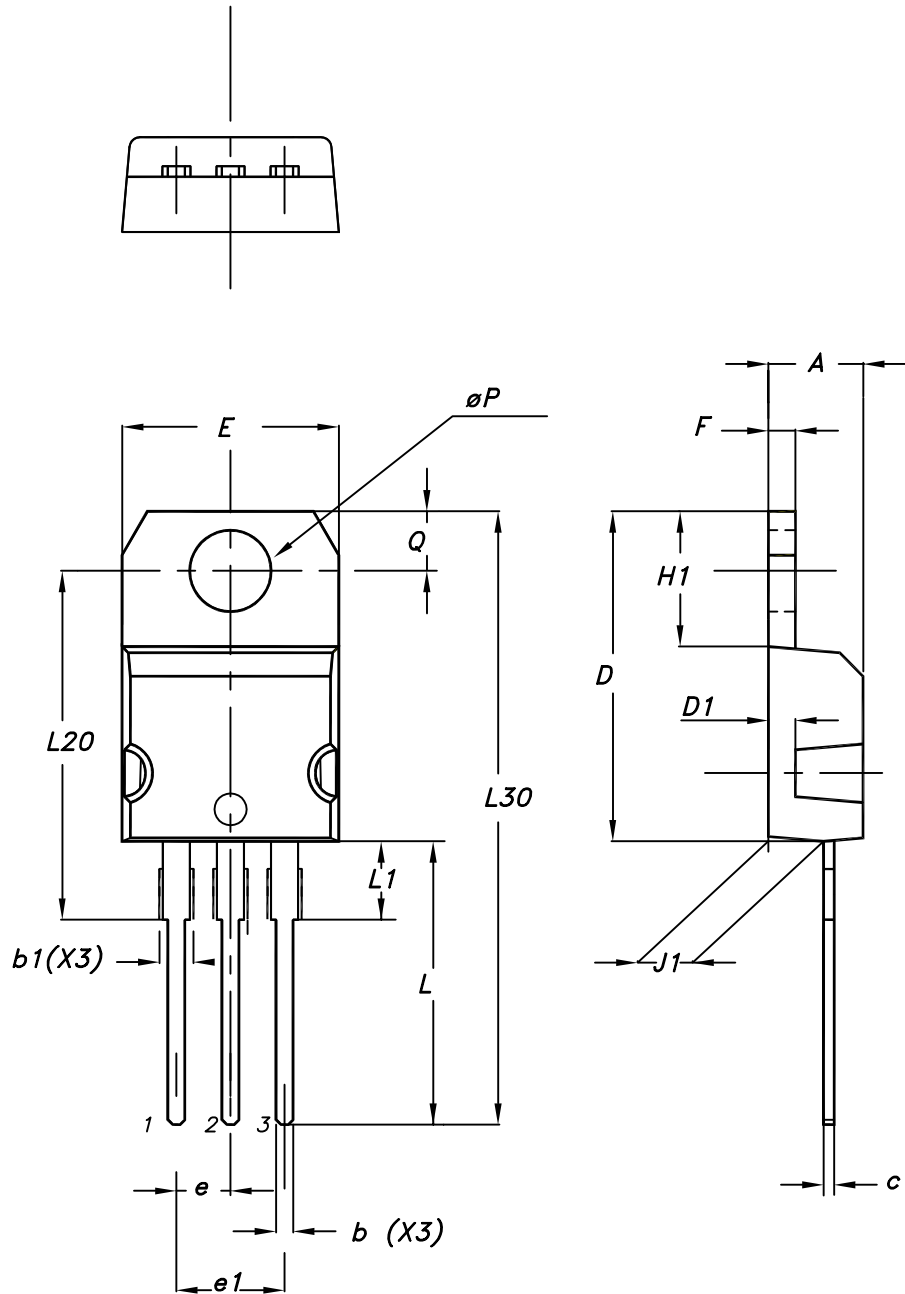
Figure 27. TO-220FP package outline



7012510_Rev_12_B

Table 12. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.6 TO-220 type A package information
Figure 28. TO-220 type A package outline


0015988_typeA_Rev_21

Table 13. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Ordering information

Table 14. Order codes

Order code	Marking	Package	Packing
STB22NM60N	22NM60N	D ² PAK	Tape and reel
STF22NM60N		TO-220FP	Tube
STP22NM60N		TO-220	

Revision history

Table 15. Document revision history

Date	Version	Changes
02-Jul-2009	1	First release.
18-Feb-2010	2	Document status promoted from preliminary data to datasheet.
27-Aug-2010	3	New package, mechanical data has been inserted: I ² PAK.
05-Nov-2011	4	Some value changed in <i>Table 5: On /off states</i> .
02-May-2018	5	<p>The part numbers STI22NM60N and STW22NM60N have been moved to a separate datasheet.</p> <p>Removed maturity status indication from cover page. The document status is production data</p> <p>Updated title and features in cover page.</p> <p>Updated Section 1 Electrical ratings, Section 2 Electrical characteristics, Section 2.1 Electrical characteristics curves and Section 4 Package information.</p> <p>Minor text changes.</p>

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[SSM6P69NU,LF](#) [DMP22D4UFO-7B](#)