STB24NM60N

N-channel 600 V, 0.168 Ω typ., 17 A MDmesh™ II Power MOSFET in a D²PAK package

**Datasheet − production data**

D²PAK
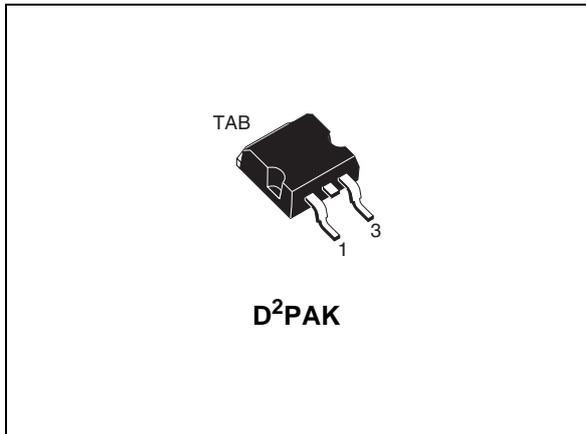
Figure 1. Internal schematic diagram

AM01475v1
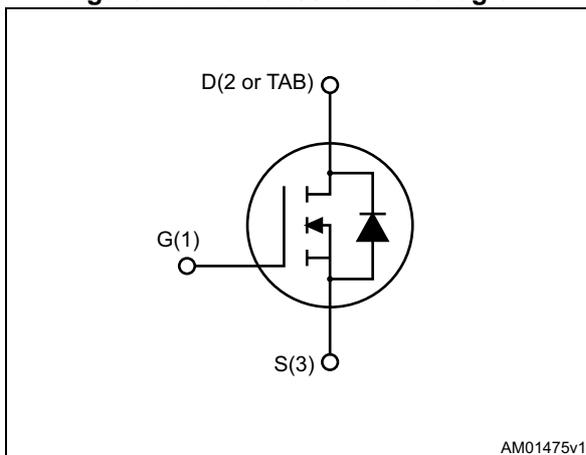
Features

Order code	V$_{DS}$ @Tjmax	R$_{DS(on)}$ max.	I$_D$
STB24NM60N	650 V	0.19 Ω	17 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STB24NM60N	24NM60N	D²PAK	Tape and reel

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Contents

1   Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	17	A
I_D	Drain current (continuous) at T_C = 100 °C	11	A
I_{DM} [1]	Drain current (pulsed)	68	A
P_{TOT}	Total dissipation at T_C = 25 °C	125	W
dv/dt[2]	Peak diode recovery voltage slope	15	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area.

2. I_{SD} ≤ 17 A, di/dt ≤ 400 A/µs, peak V_{DS} ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	1	°C/W
$R_{thj-pcb}$ [1]	Thermal resistance junction-pcb max	30	°C/W

1. When mounted on 1 inch² FR-4, 2 oz Cu

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	6	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	300	mJ

2 Electrical characteristics

(Tcase = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$, $I_D = 1$ mA	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0$, $V_{DS} = 600$ V			1	μA
		$V_{GS} = 0$, $V_{DS} = 600$ V, T_C=125 °C			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0$, $V_{GS} = \pm 25$ V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250$ μA	2	3	4	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10$ V, $I_D = 8$ A		0.168	0.19	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50$ V, f = 1 MHz, $V_{GS} = 0$	-	1330	-	pF
C_{oss}	Output capacitance		-	80	-	pF
C_{rss}	Reverse transfer capacitance		-	3.2	-	pF
$C_{oss\ eq.}$[1]	Equivalent output capacitance	$V_{DS} = 0$ to 480 V, $V_{GS} = 0$	-	182	-	pF
R_g	Gate input resistance	f=1 MHz open drain	-	5	-	Ω
Q_g	Total gate charge	$V_{DD} = 480$ V, $I_D = 17$ A, $V_{GS} = 10$ V *(see Figure 15)*	-	44	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain charge		-	24	-	nC

1. $C_{o(eff).}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}.

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 8.5 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 14)*	-	11.5	-	ns
$t_{r(v)}$	Voltage rise time		-	16.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	73	-	ns
$t_{f(i)}$	Fall time		-	37	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		17	A
I_{SDM} [1]	Source-drain current (pulsed)		-		68	A
V_{SD} [2]	Forward on voltage	I_{SD} = 17 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/μs V_{DD}= 60 V *(see Figure 16)*	-	340		ns
Q_{rr}	Reverse recovery charge		-	4.6		μC
I_{RRM}	Reverse recovery current		-	27		A
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/μs V_{DD}= 60 V T_J = 150 °C *(see Figure 16)*	-	404		ns
Q_{rr}	Reverse recovery charge		-	5.7		μC
I_{RRM}	Reverse recovery current		-	28		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**
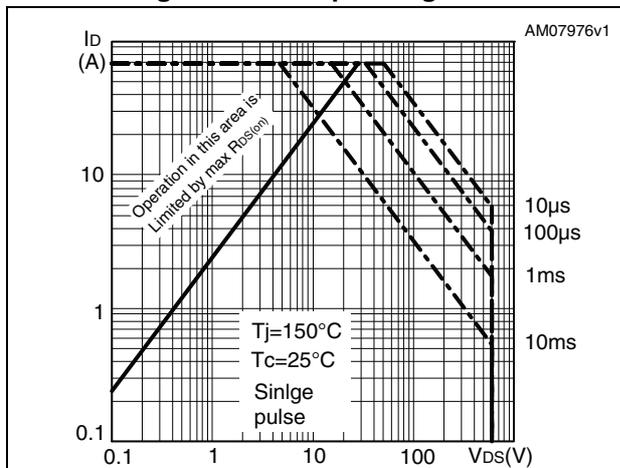
Figure 3. Thermal impedance
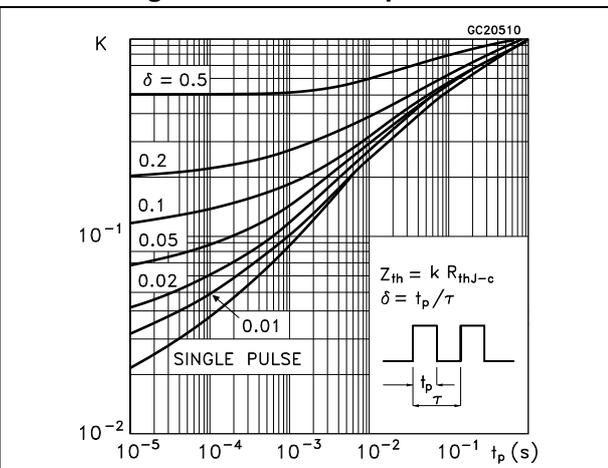

Figure 4. Output characteristics
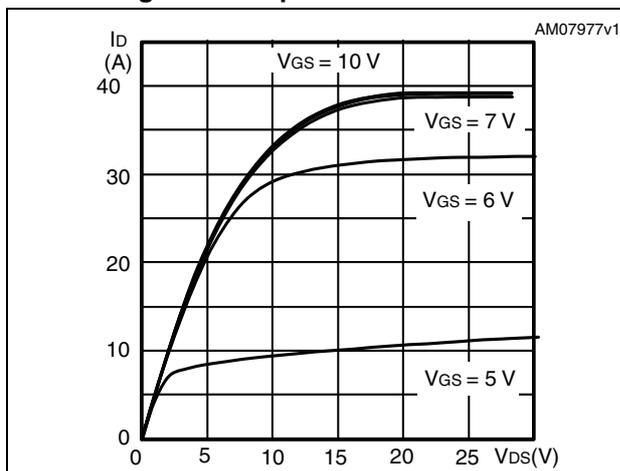
**Figure 5. Transfer characteristics**
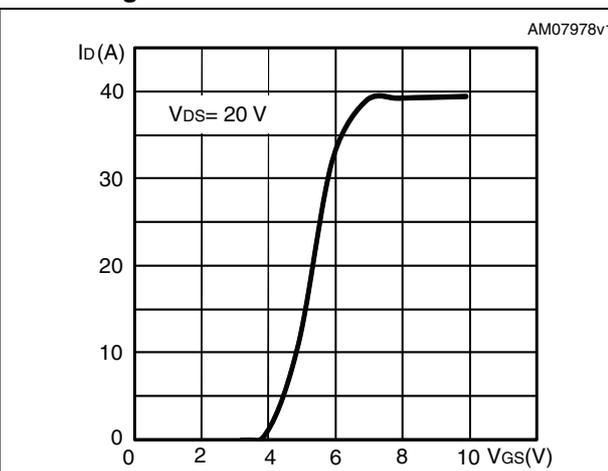
**Figure 6. Gate charge vs gate-source voltage**
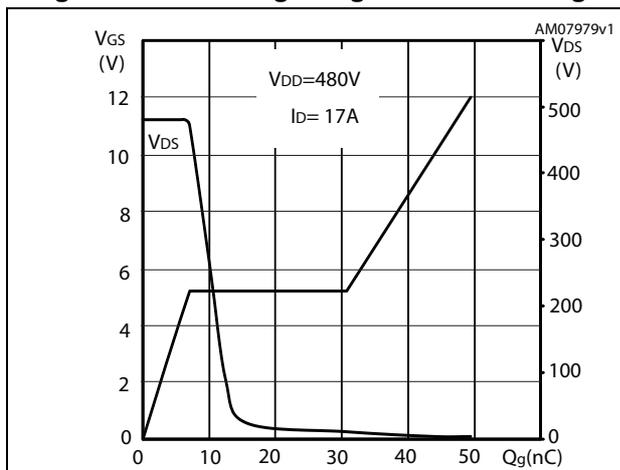
**Figure 7. Static drain-source on-resistance**
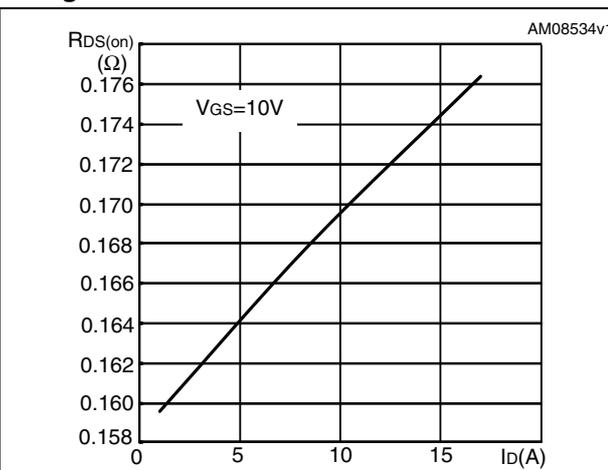
Figure 8. Capacitance variations
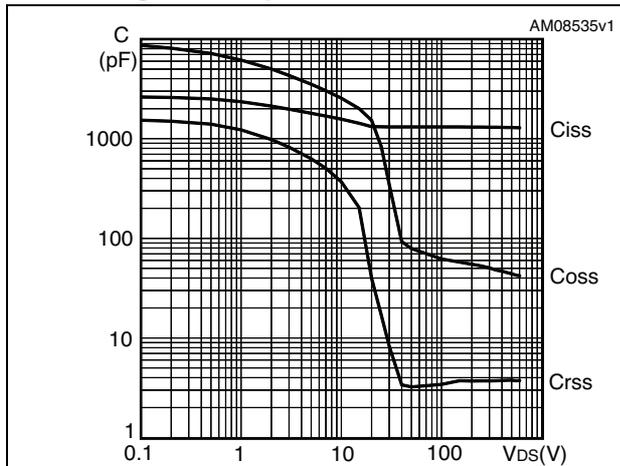
**Figure 9. Output capacitance stored energy**
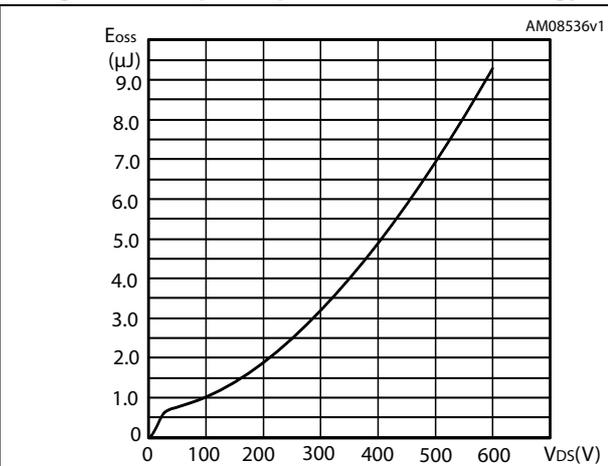
**Figure 10. Normalized gate threshold voltage vs temperature**
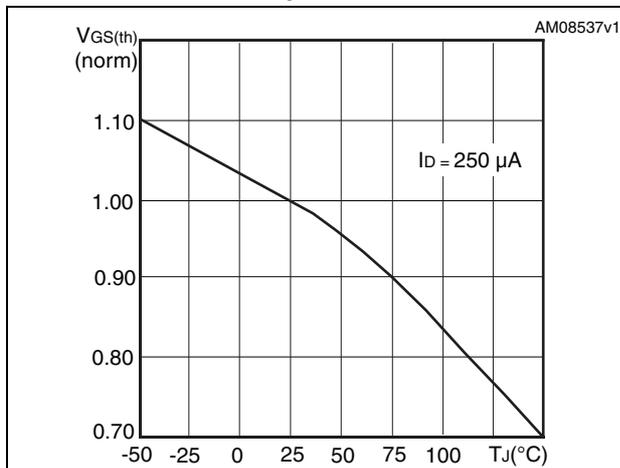
Figure 11. Normalized on-resistance vs temperature
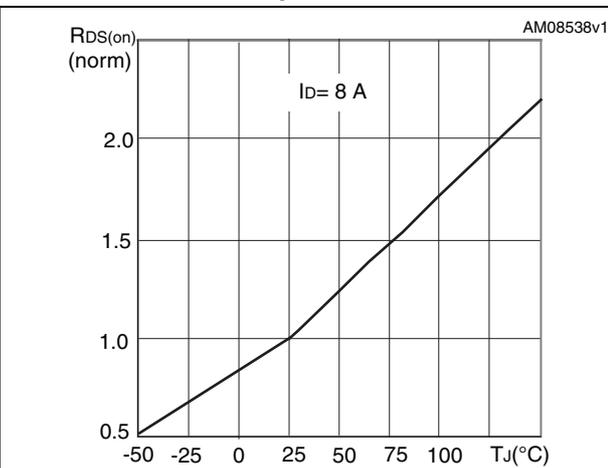

Figure 12. Normalized V$_{(BR)DSS}$ vs temperature
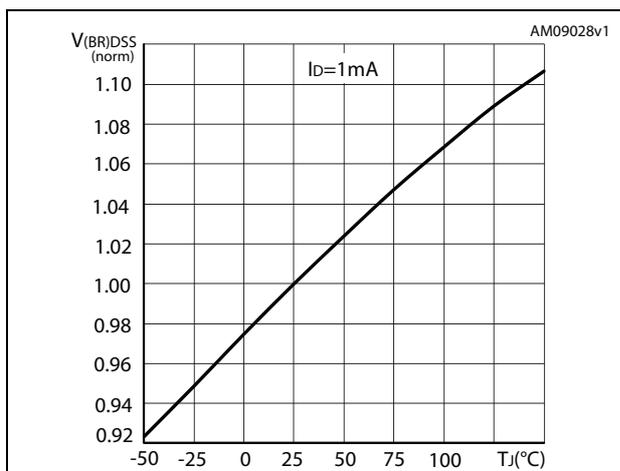
Figure 13. Source-drain diode forward characteristics
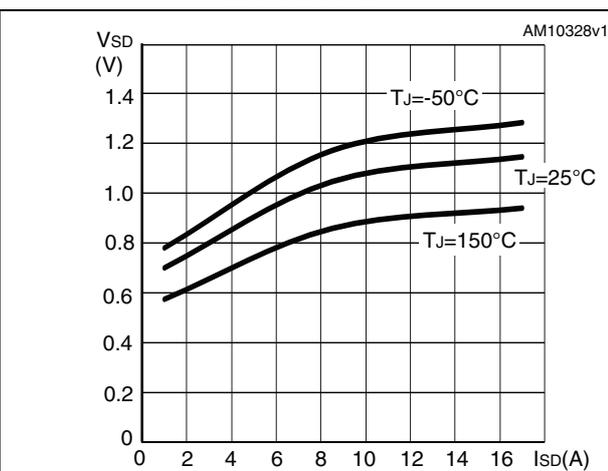
3 Test circuits

Figure 14. Switching times test circuit for resistive load

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Figure 15. Gate charge test circuit

AM01469v1
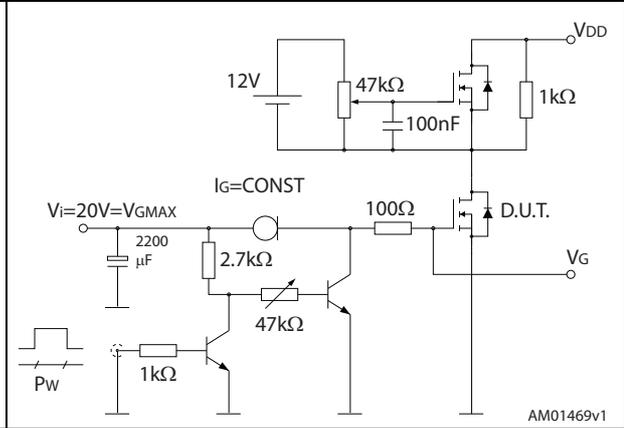
Figure 16. Test circuit for inductive load switching and diode recovery times

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Figure 17. Unclamped inductive load test circuit

AM01471v1
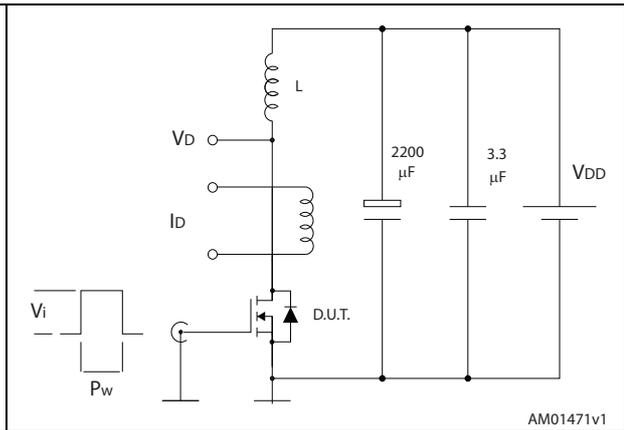
Figure 18. Unclamped inductive waveform


AM01472v1
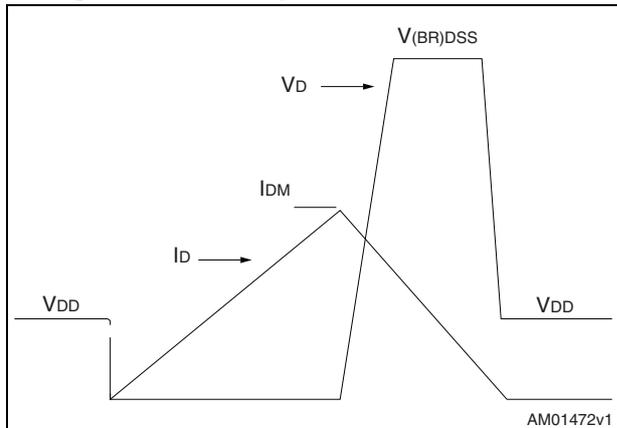
Figure 19. Switching time waveform

AM01473v1
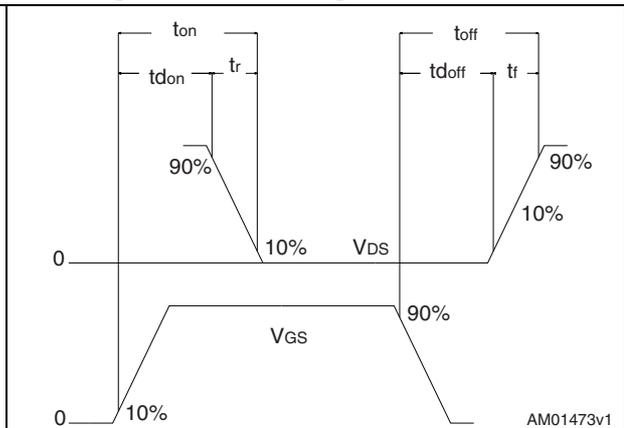
4   Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 20. D²PAK (TO-263) drawing
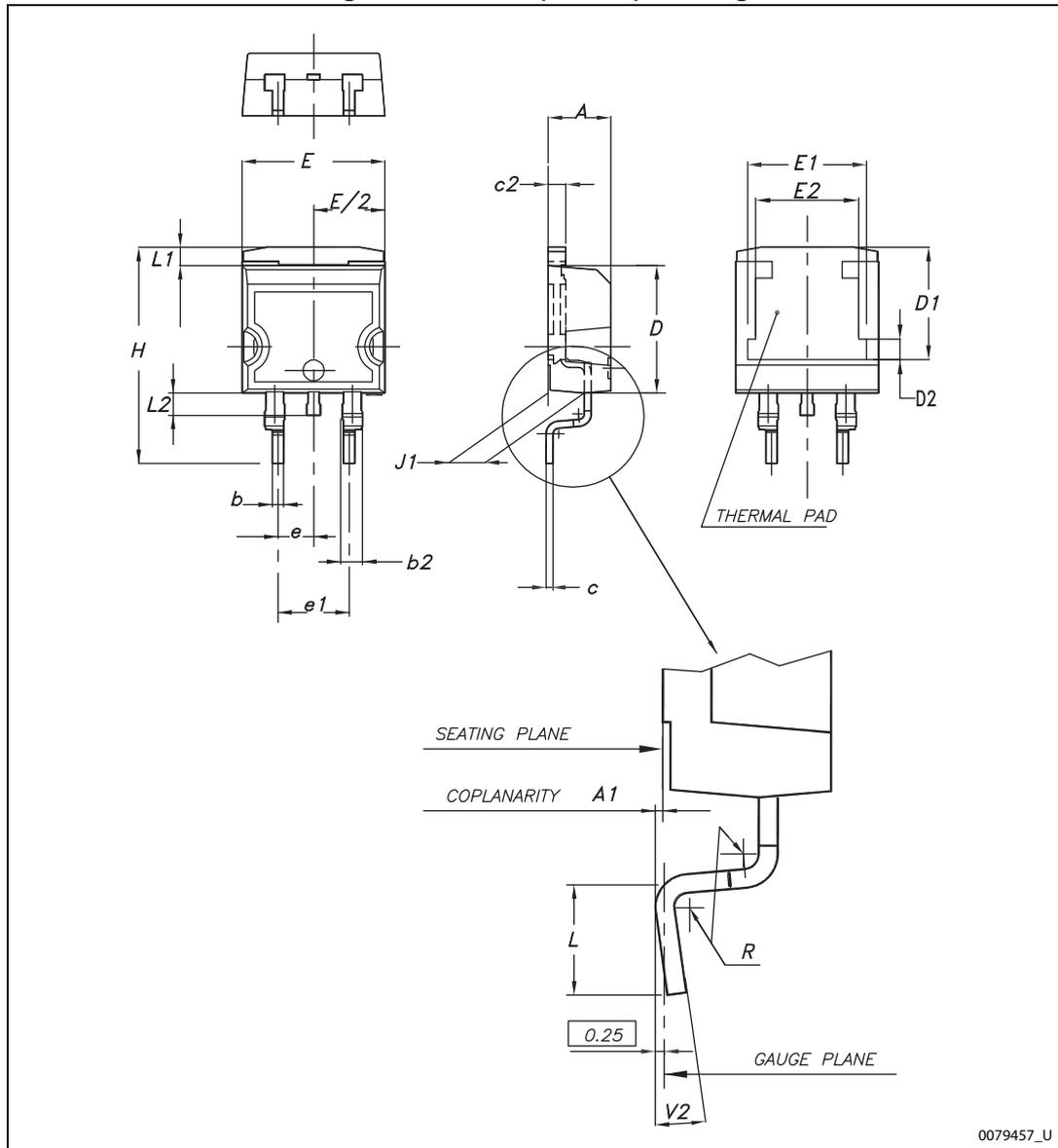
Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 21. D²PAK footprint[a]
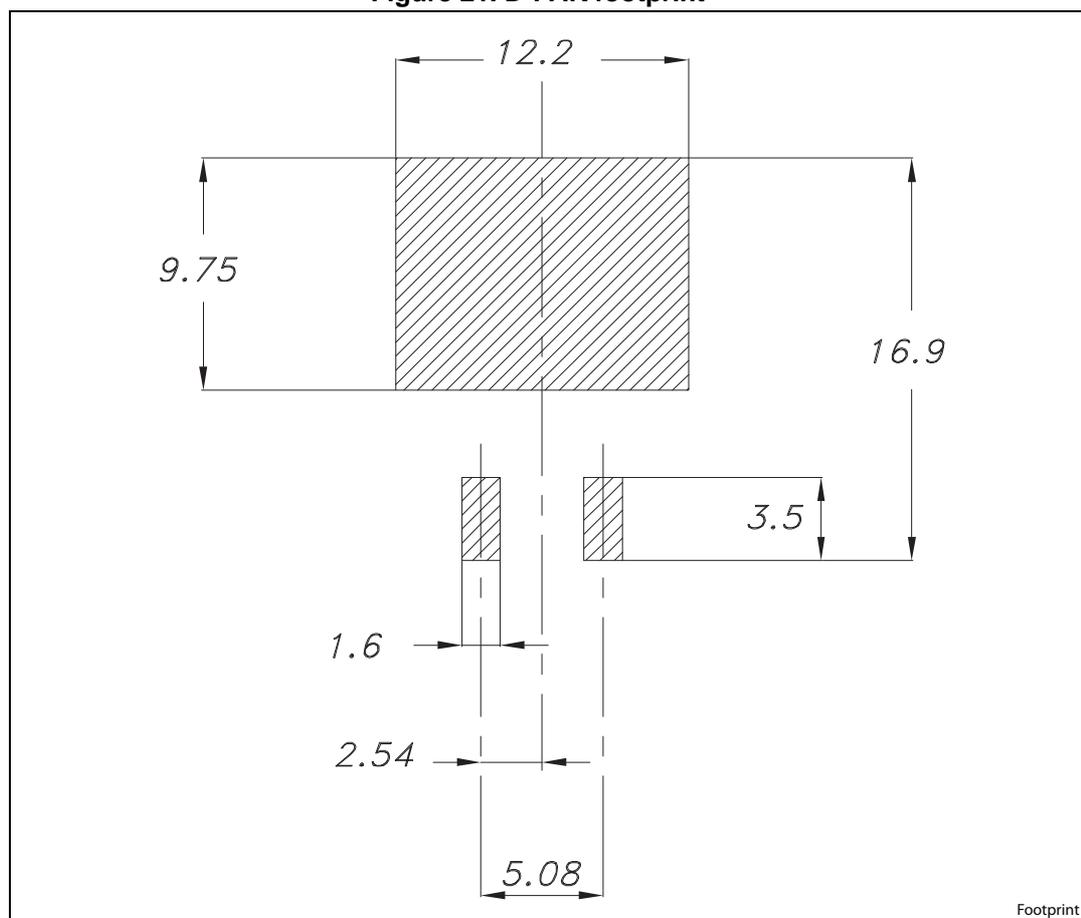
a. All dimension are in millimeters

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
05-Jan-2011	1	First release.
24-Jul-2014	2	– Modified: the entire typical values in *Table 6* – Updated: *Section 4: Package mechanical data* – Minor text changes

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