

Automotive-grade N-channel 60 V, 53 mΩ typ., 20 A STripFET™ II Power MOSFET in a D²PAK package

Datasheet - production data

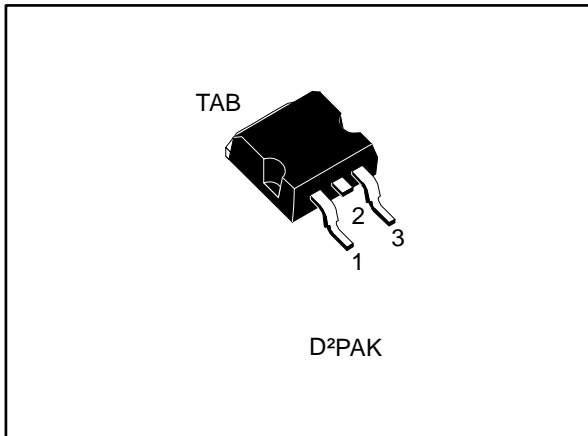
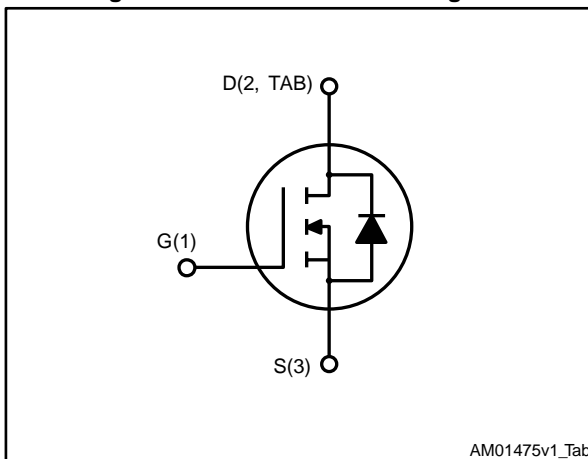


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STB25NF06LAG	60 V	70 mΩ	20 A	60 W

- AEC-Q101 qualified
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge



Applications

- Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process is specifically designed to minimize input capacitance and gate charge. It is therefore ideal as a primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer applications. It is also suitable for any application with low gate charge drive requirements.

Table 1: Device summary

Order code	Marking	Package	Packing
STB25NF06LAG	25NF06L	D ² PAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 18	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	20	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	14	
$I_{DM}^{(1)}$	Drain current (pulsed)	77	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	60	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	180	mJ
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$
T_j	Operating junction temperature range		

Notes:

(1) Pulse width is limited by safe operating area.

(2) starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 10\text{ A}$, $V_{DD} = 40\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.5	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	

Notes:

(1) When mounted on a 1-inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	60			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 60\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 60\text{ V}$, $T_{\text{case}} = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 18\text{ V}$			± 100	nA
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 10\text{ A}$		53	70	m Ω
		$V_{\text{GS}} = 5\text{ V}$, $I_{\text{D}} = 10\text{ A}$		62	85	

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iSS}	Input capacitance	$V_{\text{DS}} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	370	-	pF
C_{oSS}	Output capacitance		-	102	-	
C_{rSS}	Reverse transfer capacitance		-	44	-	
Q_{g}	Total gate charge	$V_{\text{DD}} = 30\text{ V}$, $I_{\text{D}} = 20\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	13	-	nC
Q_{gs}	Gate-source charge		-	2	-	
Q_{gd}	Gate-drain charge		-	5	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$, $I_D = 10\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	7	-	ns
t_r	Rise time		-	11	-	
$t_{d(off)}$	Turn-off delay time		-	22	-	
t_f	Fall time		-	5	-	

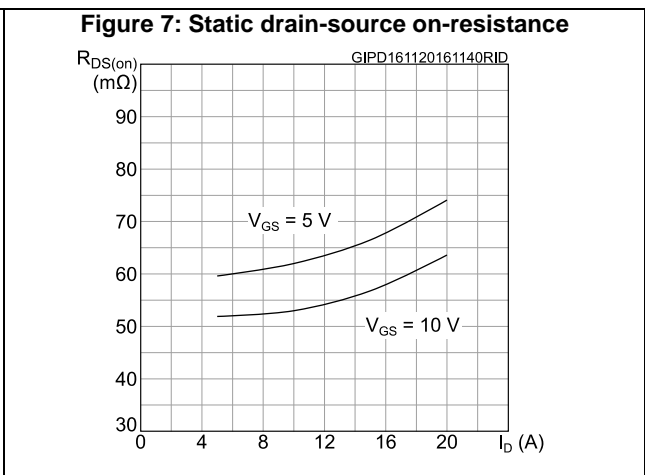
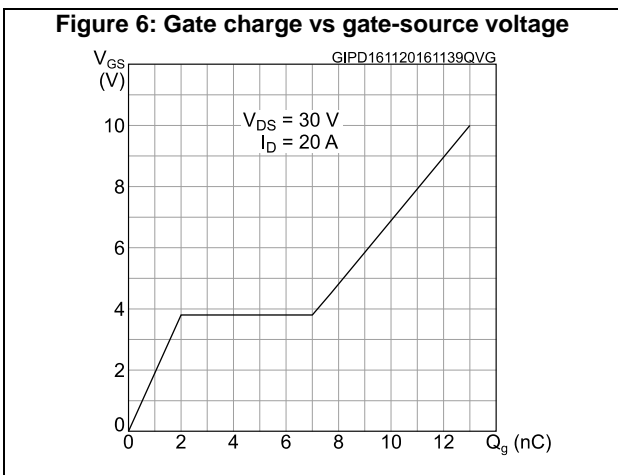
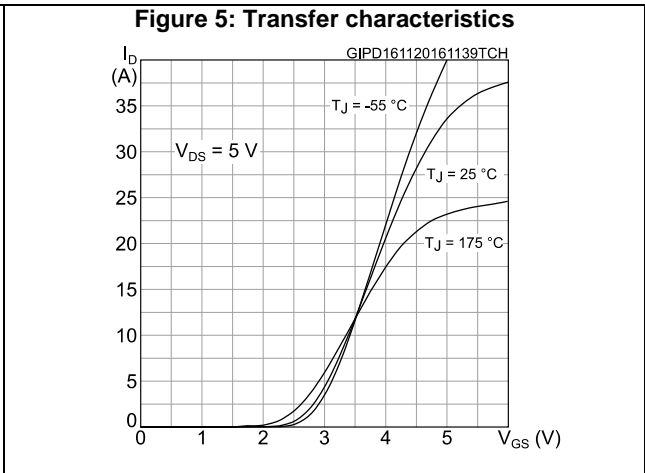
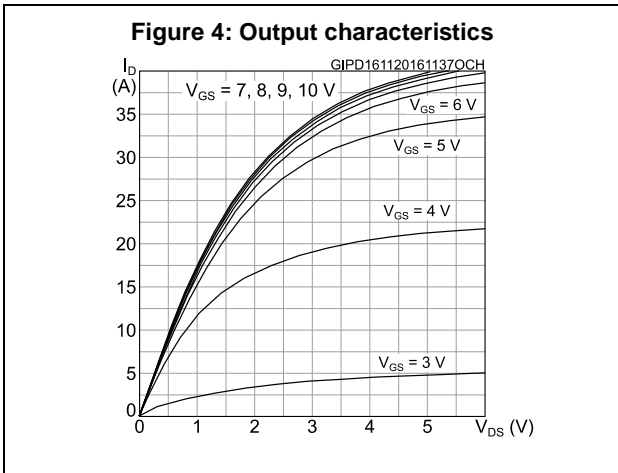
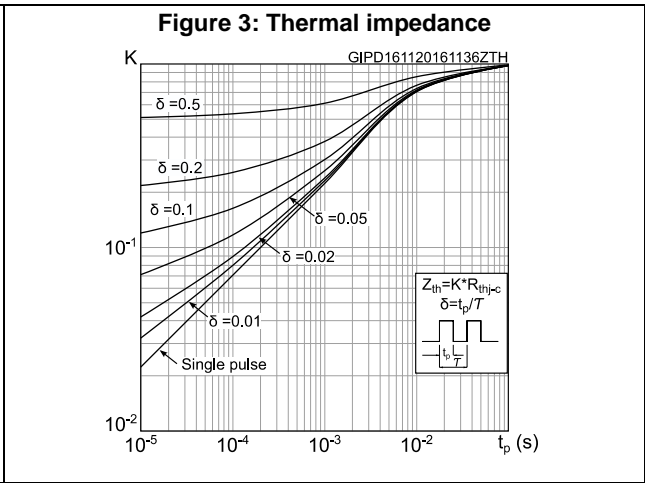
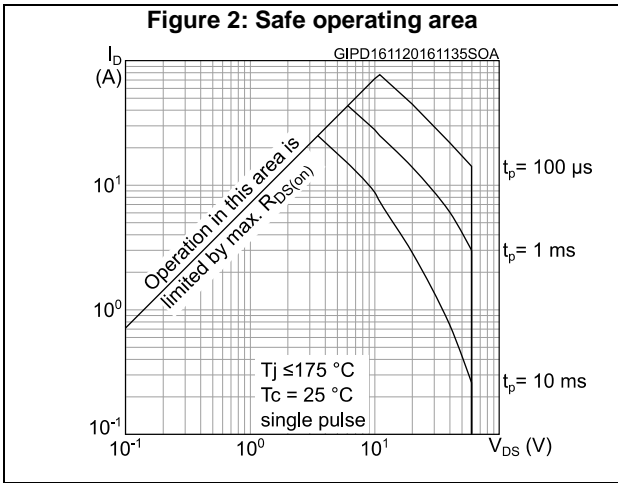
Table 7: Source-drain diode

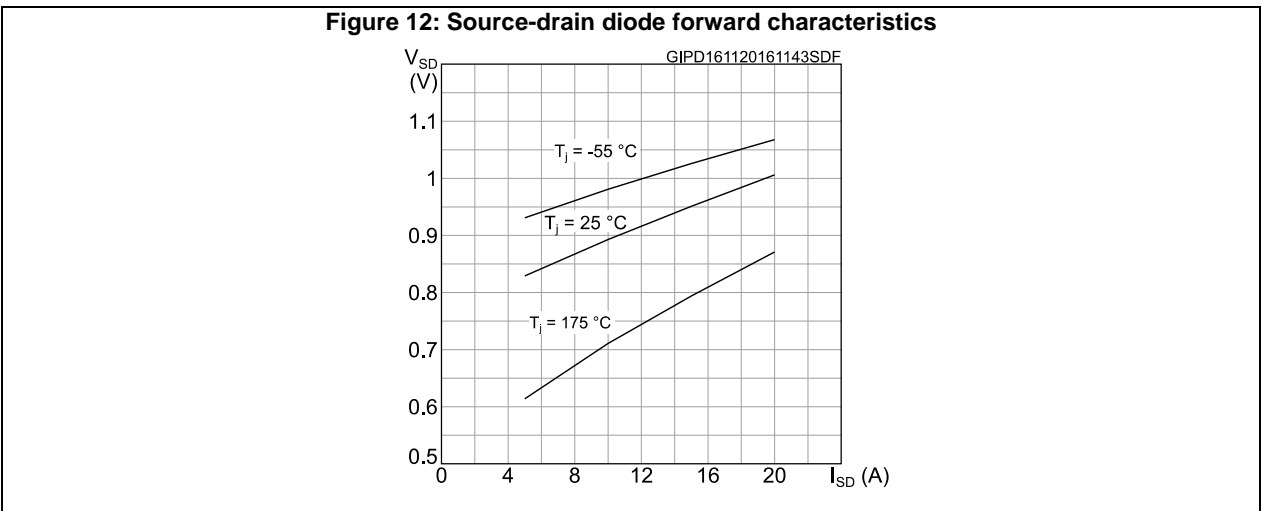
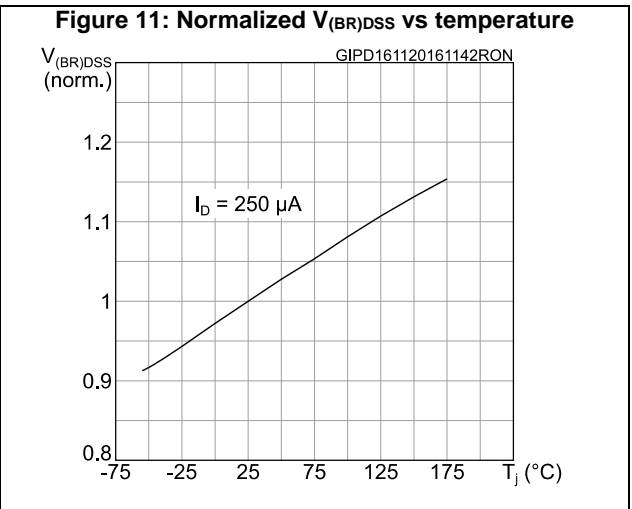
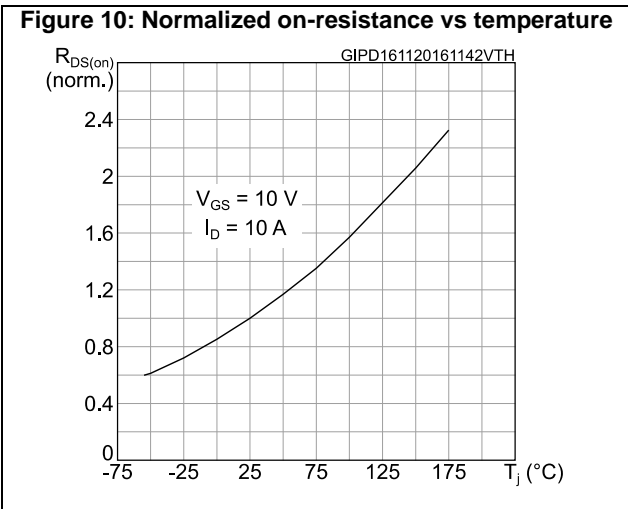
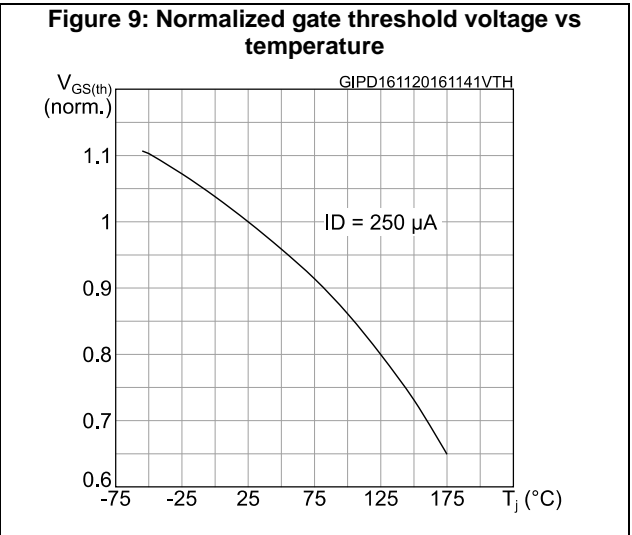
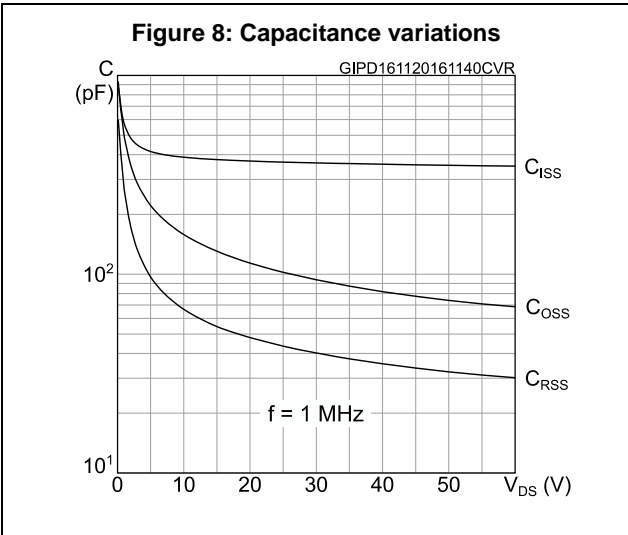
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		77	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 20\text{ A}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 48\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	49		ns
Q_{rr}	Reverse recovery charge		-	61		nC
I_{RRM}	Reverse recovery current		-	2.5		A

Notes:

- (1) Pulse width limited by safe operating area .
(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5 %.

2.1 Electrical characteristics (curves)





3 Test circuits

Figure 13: Test circuit for resistive load switching times



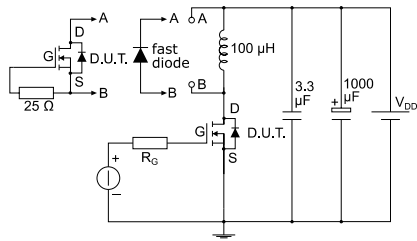
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Figure 14: Test circuit for gate charge behavior



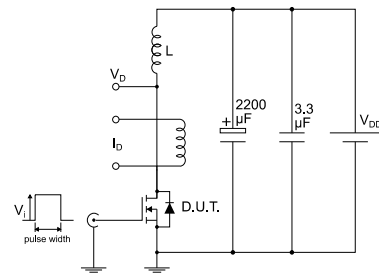
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Figure 15: Test circuit for inductive load switching and diode recovery times



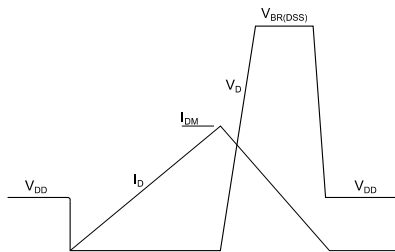
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Figure 16: Unclamped inductive load test circuit



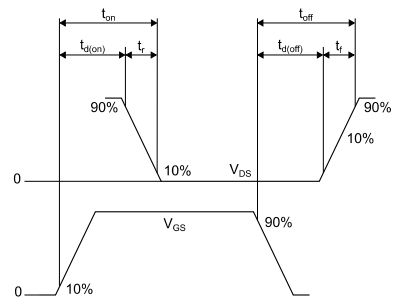
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



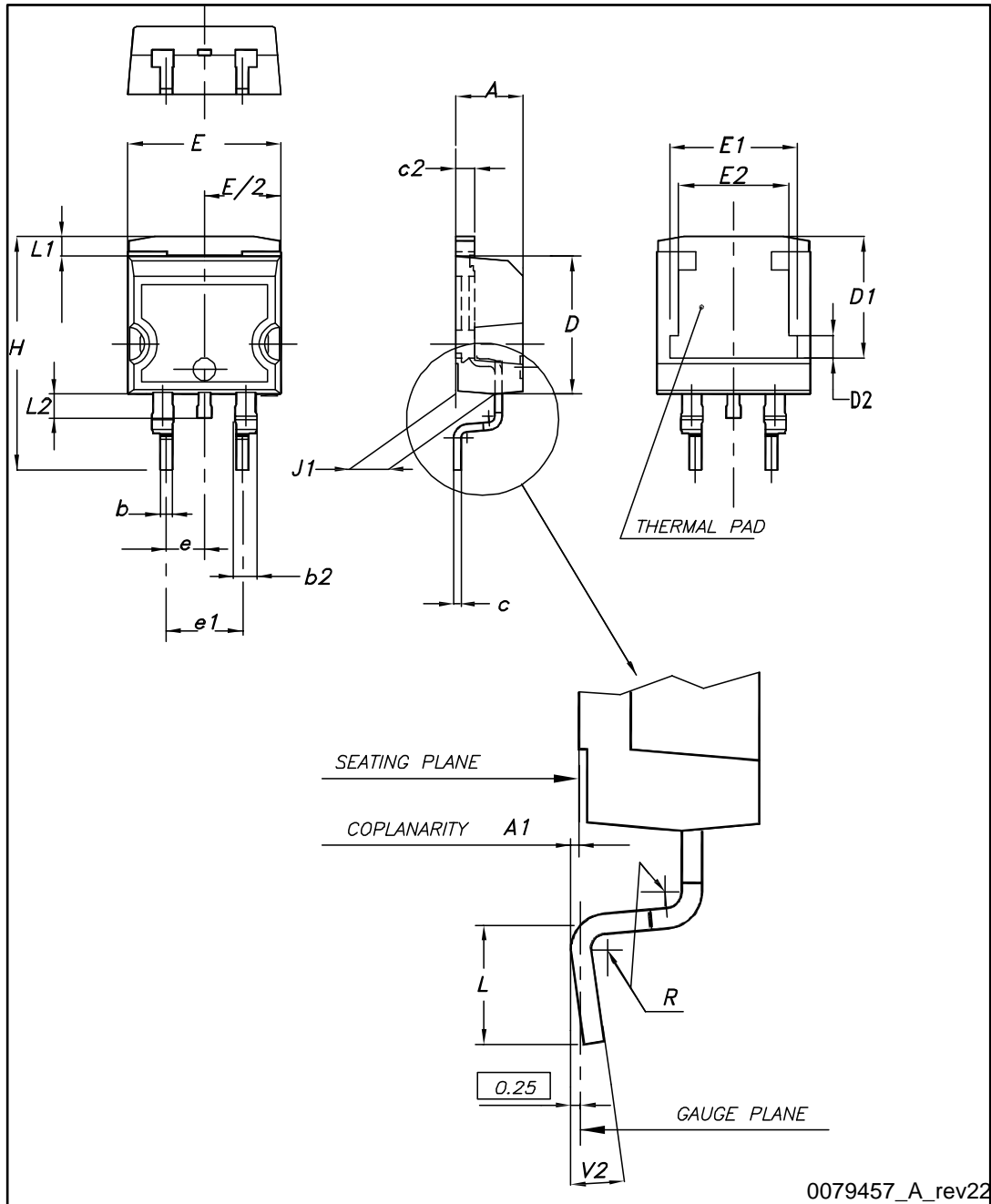
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK package information

Figure 19: D²PAK (TO-263) type A package outline

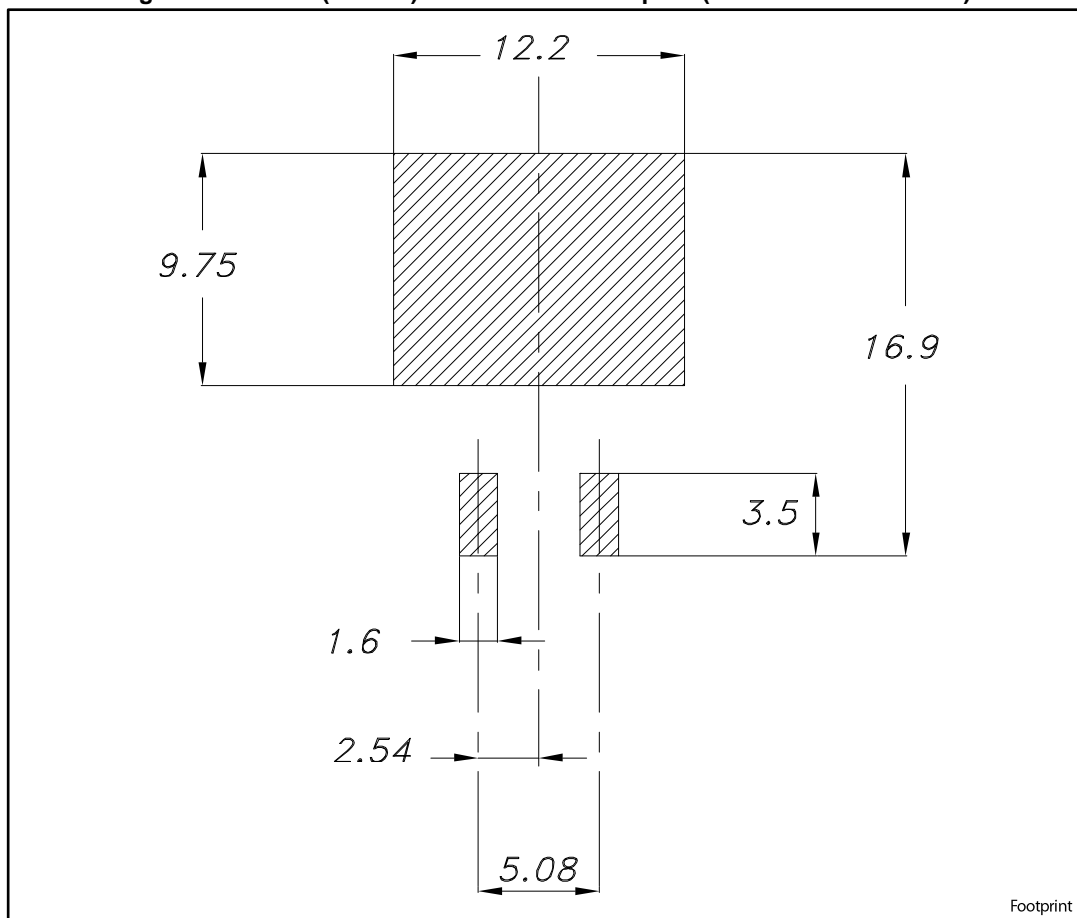


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Table 8: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20: D²PAK (TO-263) recommended footprint (dimensions are in mm)



Footprint

4.2 D²PAK packing information

Figure 21: Tape outline

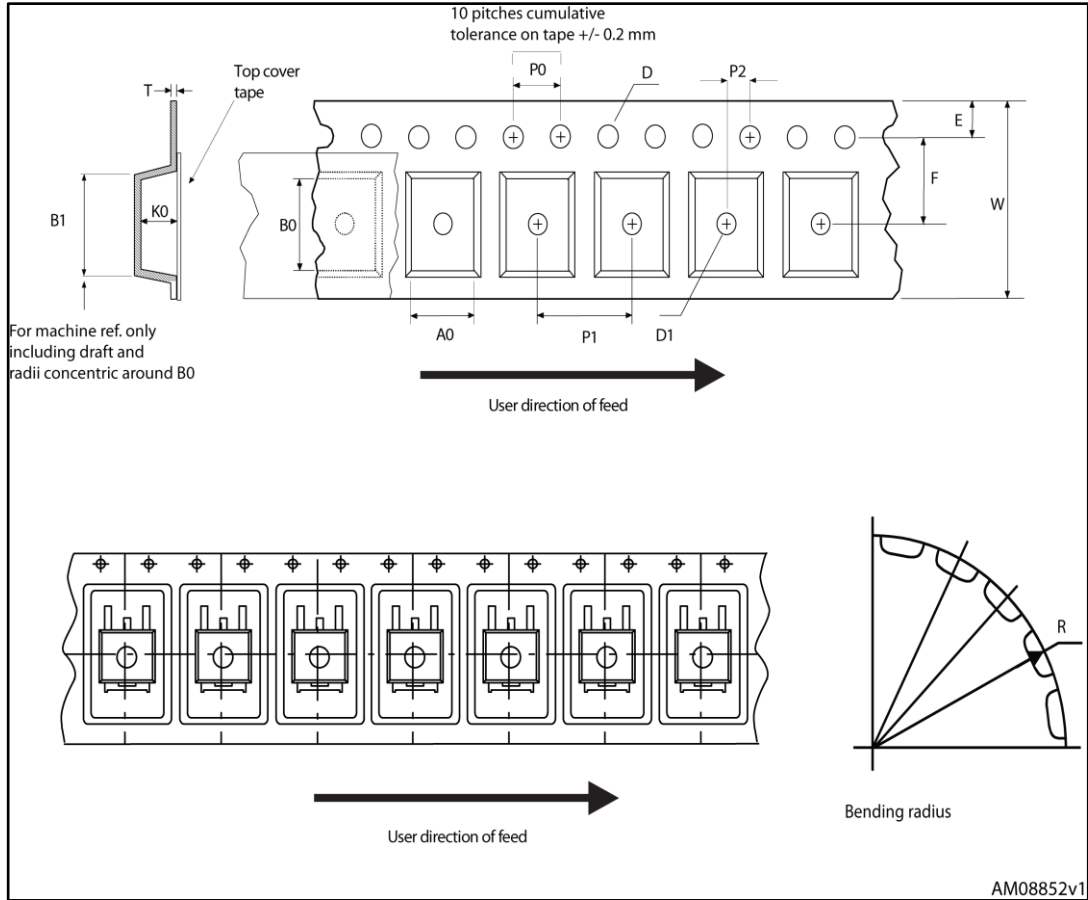


Figure 22: Reel outline

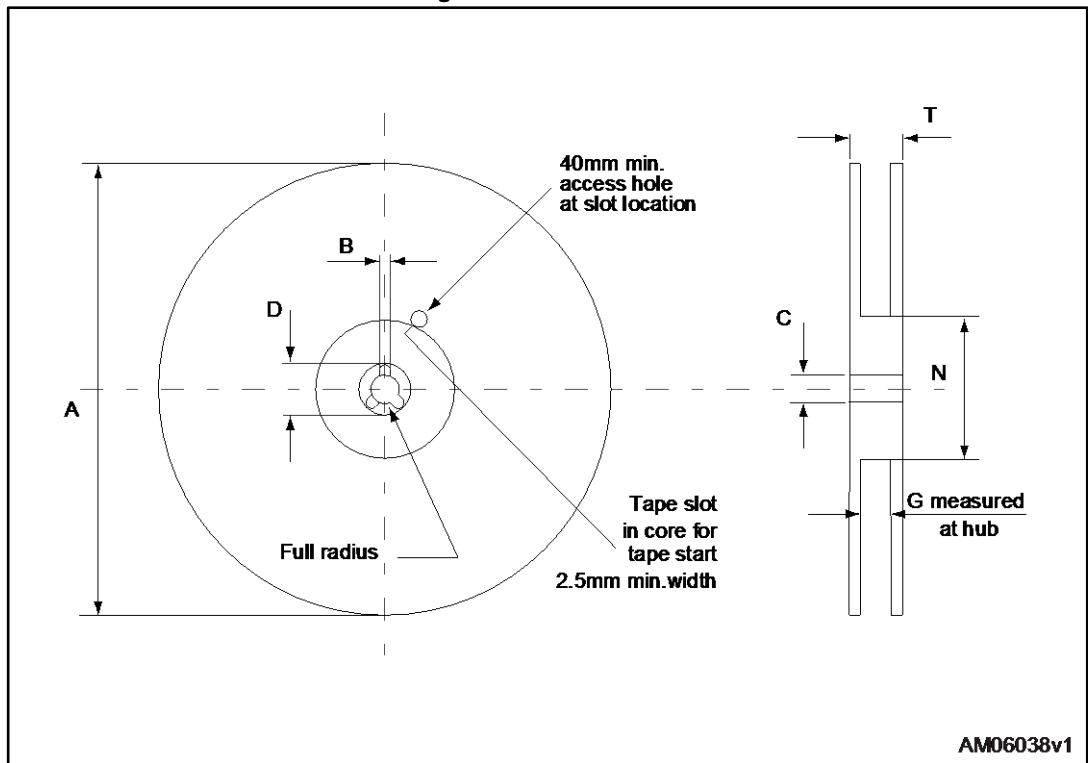


Table 9: D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
24-Nov-2016	1	First release.

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