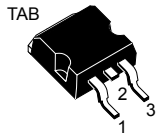
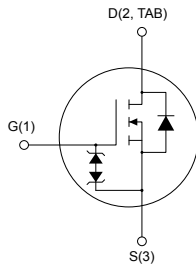


## N-channel 600 V, 0.108 $\Omega$ typ., 26 A MDmesh M2 Power MOSFET in a D<sup>2</sup>PAK package


 D<sup>2</sup>PAK


AM01475V1



### Features

Order code	V <sub>DS</sub> @ T <sub>J</sub> max.	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB33N60M2	650 V	0.125 $\Omega$	26 A

- Extremely low gate charge
- Excellent output capacitance (C<sub>OSS</sub>) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- LLC converters, resonant converters

### Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

#### Product status link

[STB33N60M2](#)

#### Product summary

<b>Order code</b>	STB33N60M2
<b>Marking</b>	33N60M2
<b>Package</b>	D <sup>2</sup> PAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	26	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	16	A
$I_{DM}^{(1)}$	Drain current (pulsed)	104	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	190	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 26\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .
3.  $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.66	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	450	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V},$ $T_C = 125\text{ °C}^{(1)}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 13\text{ A}$		0.108	0.125	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0\text{ V}$	-	1781	-	pF
$C_{oss}$	Output capacitance		-	85	-	pF
$C_{riss}$	Reverse transfer capacitance		-	2.5	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}, V_{GS} = 0\text{ V}$	-	135	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0\text{ A}$	-	5.2	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 26\text{ A},$ $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	45.5	-	nC
$Q_{gs}$	Gate-source charge		-	9.9	-	nC
$Q_{gd}$	Gate-drain charge		-	18.5	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 13\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$	-	16	-	ns
$t_r$	Rise time		-	9.6	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	109	-	ns
$t_f$	Fall time		-	9	-	ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		26	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		104	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 26\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 26\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	375		ns
$Q_{rr}$	Reverse recovery charge		-	5.6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	30		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 26\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	478		ns
$Q_{rr}$	Reverse recovery charge		-	7.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	32.5		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

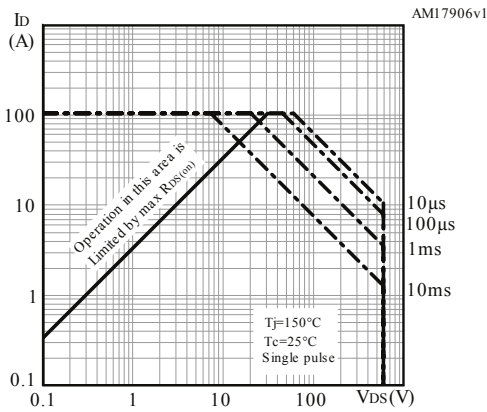


Figure 2. Normalized thermal impedance

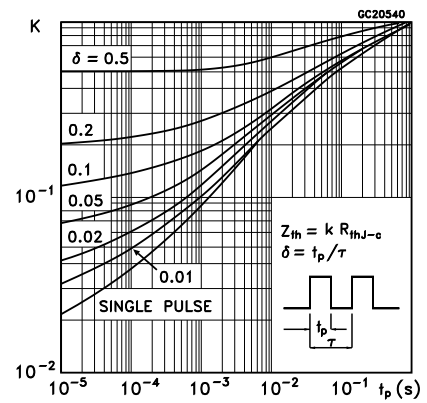


Figure 3. Output characteristics

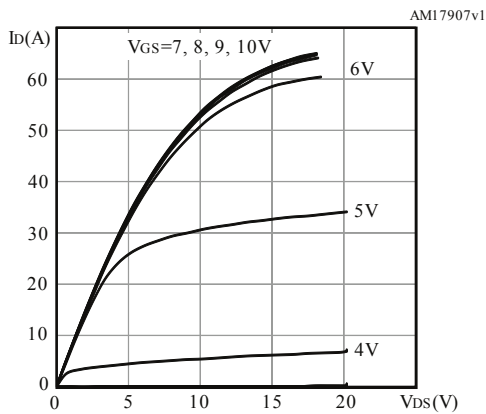


Figure 4. Transfer characteristics

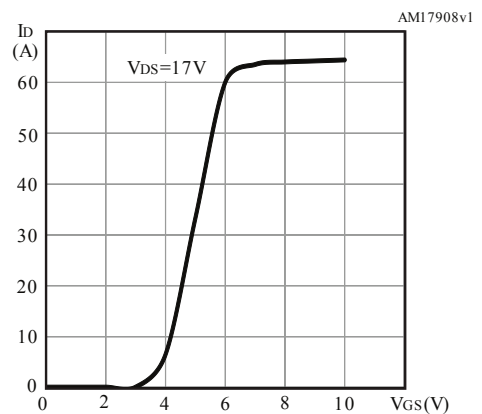


Figure 5. Gate charge vs gate-source voltage

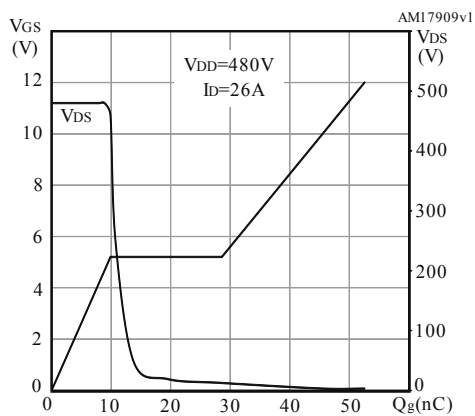
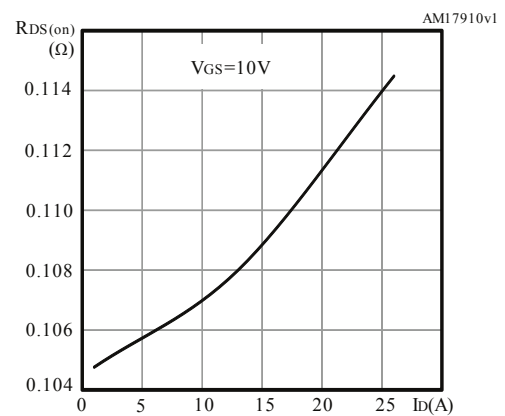
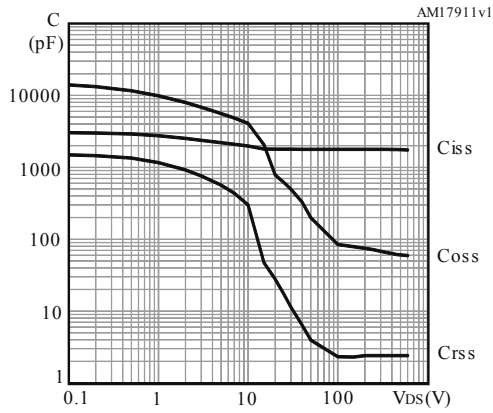


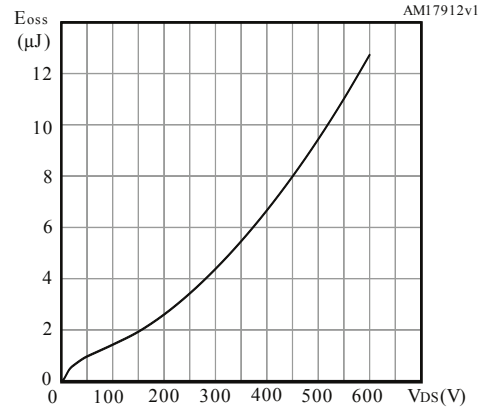
Figure 6. Static drain-source on-resistance



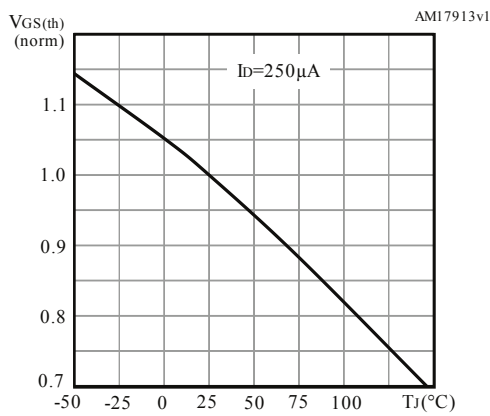
**Figure 7. Capacitance variations**



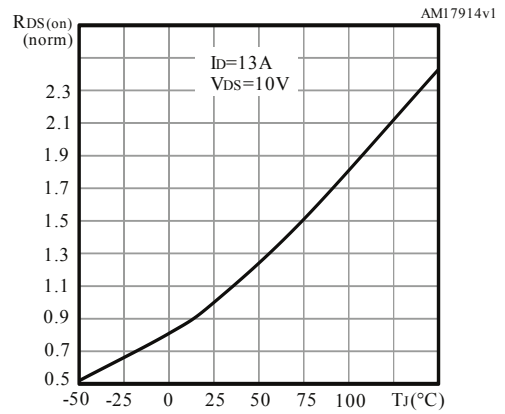
**Figure 8. Output capacitance stored energy**



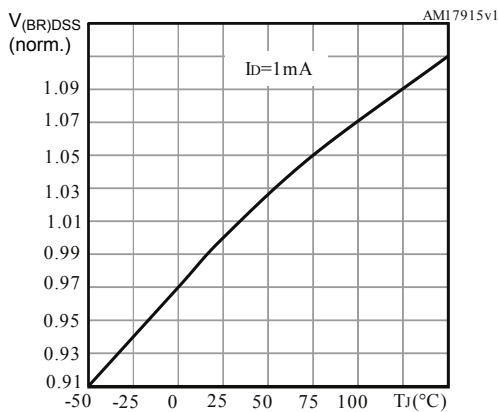
**Figure 9. Normalized gate threshold voltage vs temperature**



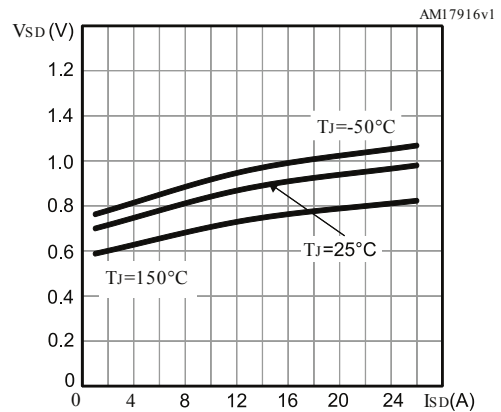
**Figure 10. Normalized on-resistance vs temperature**



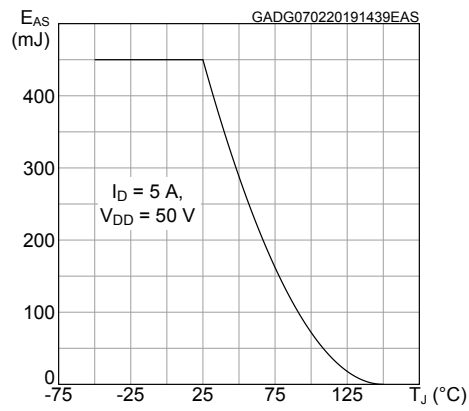
**Figure 11. Normalized VDS vs temperature**



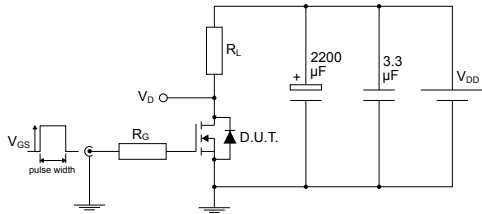
**Figure 12. Source-drain diode forward characteristics**



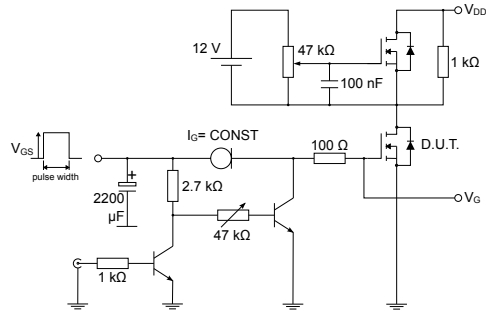
**Figure 13. Maximum avalanche energy vs temperature**



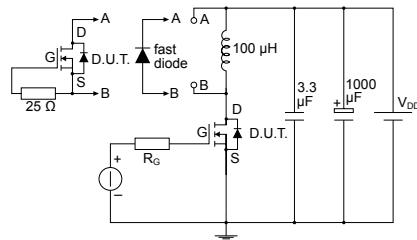
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


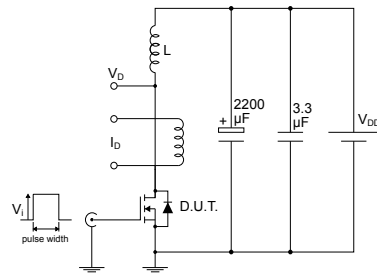
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**Figure 15. Test circuit for gate charge behavior**


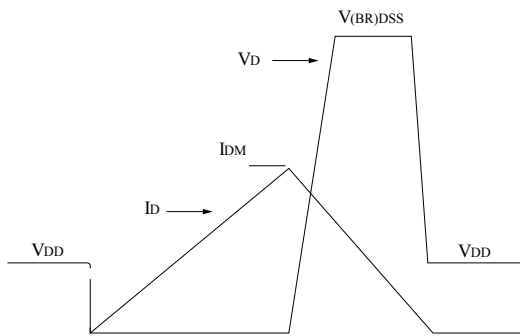
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


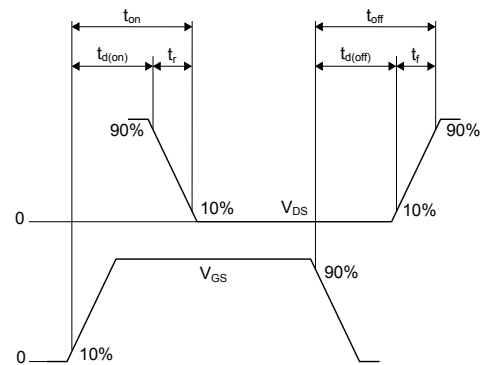
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**Figure 17. Unclamped inductive load test circuit**


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**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


AM01473v1



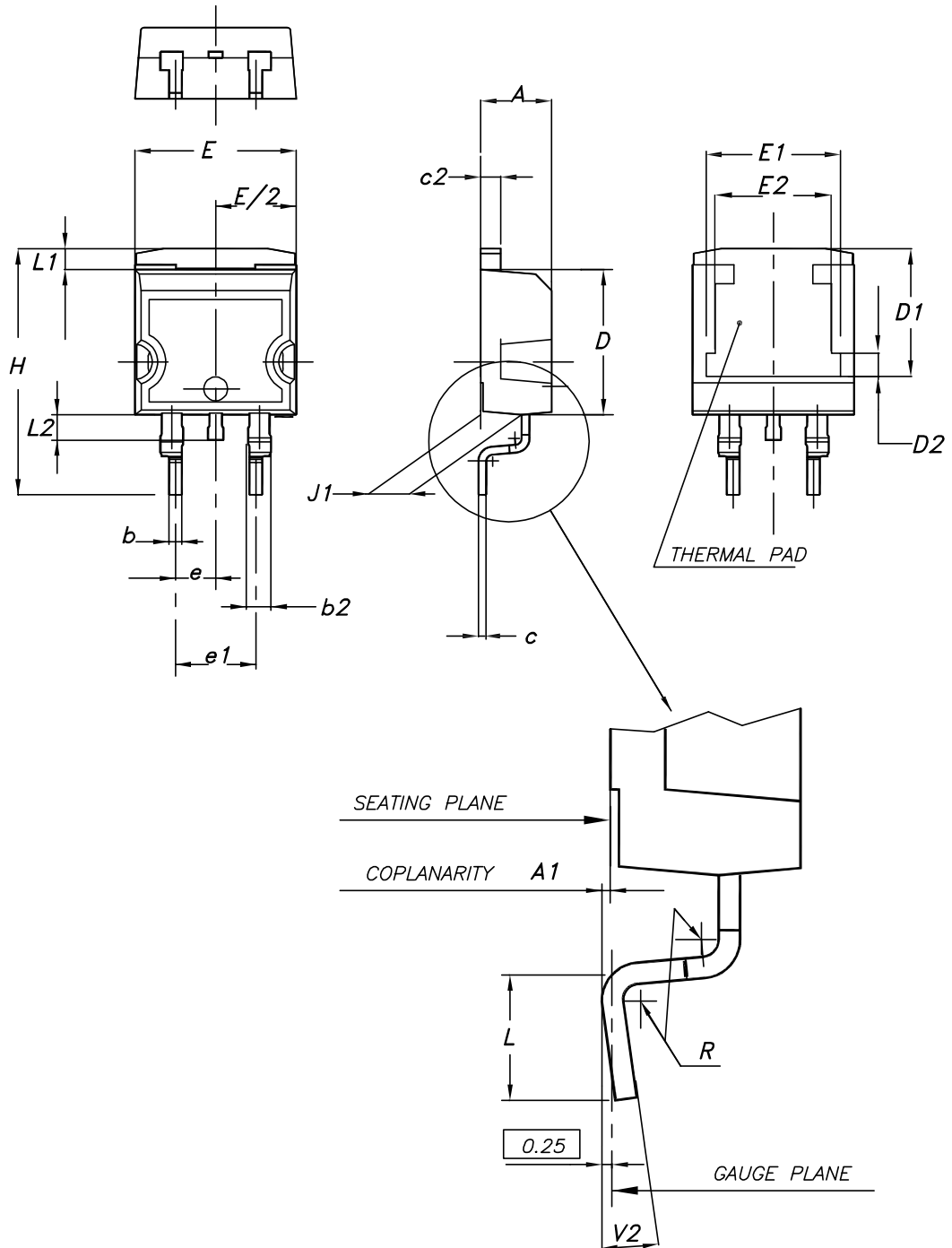
## 4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 D<sup>2</sup>PAK (TO-263) type A package information

Figure 20. D<sup>2</sup>PAK (TO-263) type A package outline

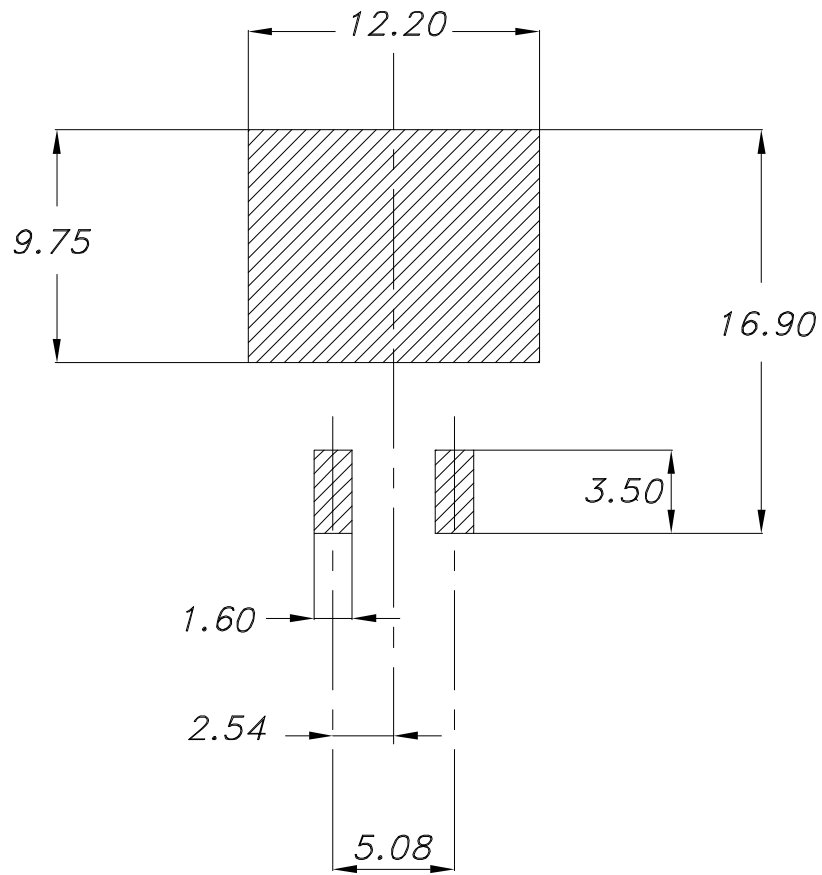


0079457\_26

**Table 8. D<sup>2</sup>PAK (TO-263) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

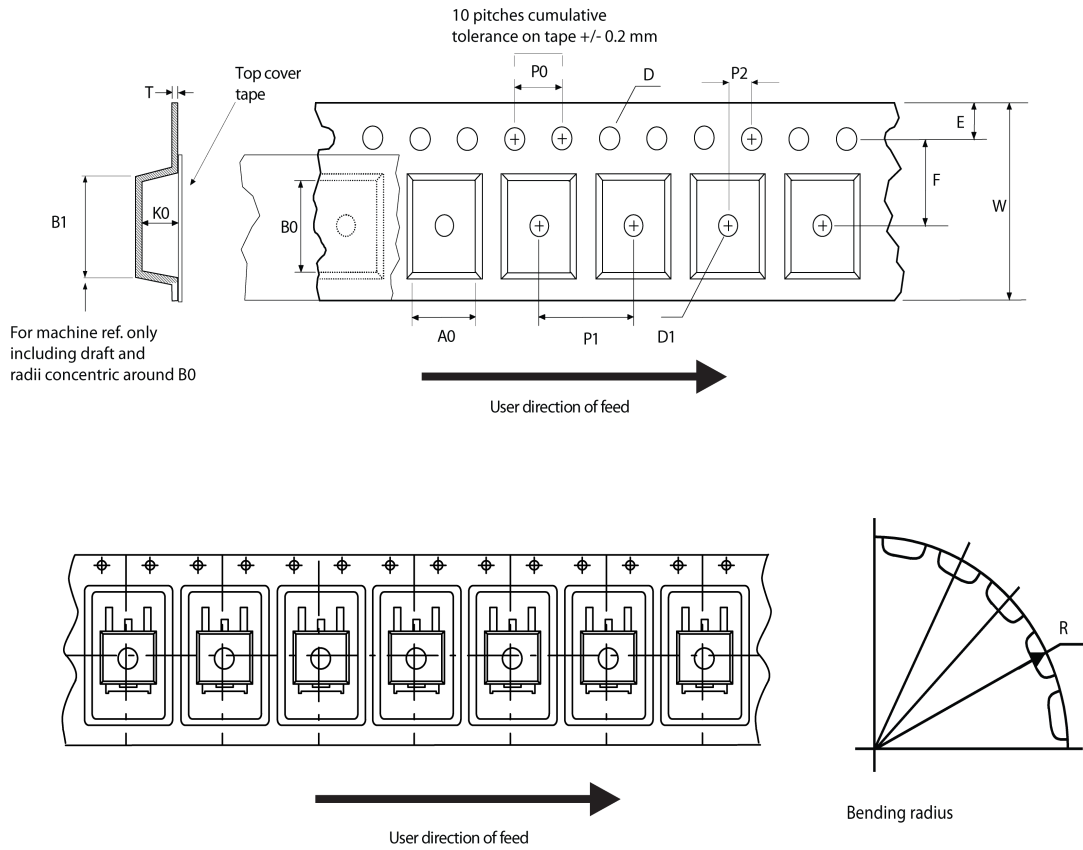
Figure 21. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)



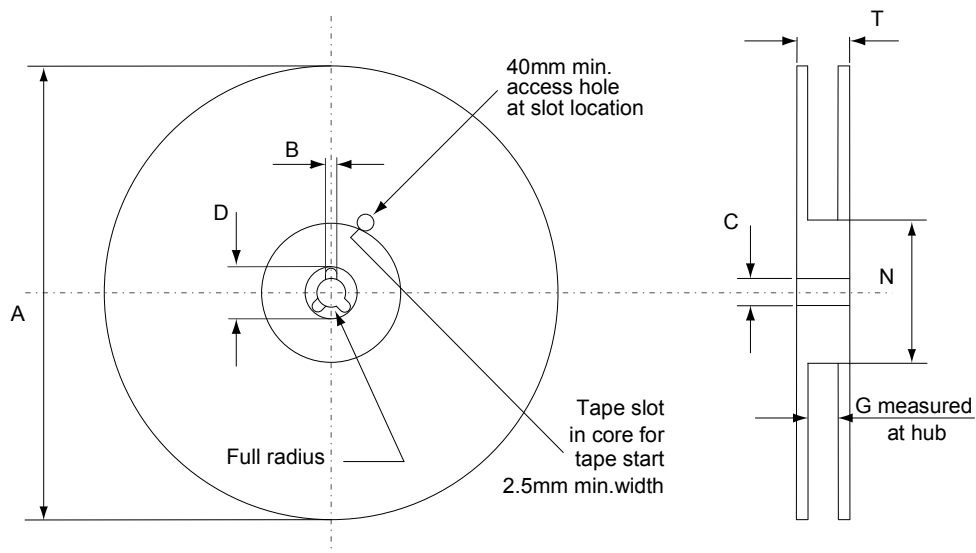
Footprint\_26

## 4.2 D<sup>2</sup>PAK packing information

Figure 22. D<sup>2</sup>PAK tape outline



AM08852v1

**Figure 23. D<sup>2</sup>PAK reel outline**


AM06038v1

**Table 9. D<sup>2</sup>PAK tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## Revision history

**Table 10. Document revision history**

Date	Version	Changes
13-Sep-2013	1	First release.
19-Nov-2013	2	<ul style="list-style-type: none"> <li>– Modified: <math>R_{DS(on)}</math> and <math>I_D</math> values in cover page</li> <li>– Modified: values in <i>Table 4</i></li> <li>– Modified: <math>R_{DS(on)}</math> typical and maximum values in <i>Table 5</i>, the entire typical values in <i>Table 6, 7 and 8</i></li> <li>– Added: <i>Section 2.1: Electrical characteristics (curves)</i></li> <li>– Minor text changes</li> </ul>
18-Jun-2019	3	<p>Removed maturity status indication from cover page. The document status is production data.</p> <p>Update <a href="#">Table 3. Avalanche characteristics</a>.</p> <p>Added <a href="#">Figure 13. Maximum avalanche energy vs temperature</a>.</p> <p>Minor text changes.</p>

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