



STP36NF06L STB36NF06L

N-channel 60V - 0.032Ω - 30A - TO-220 - D²PAK
STripFET™ II Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STP36NF06L	60V	< 0.04Ω	30A
STB36NF06L	60V	< 0.04Ω	30A

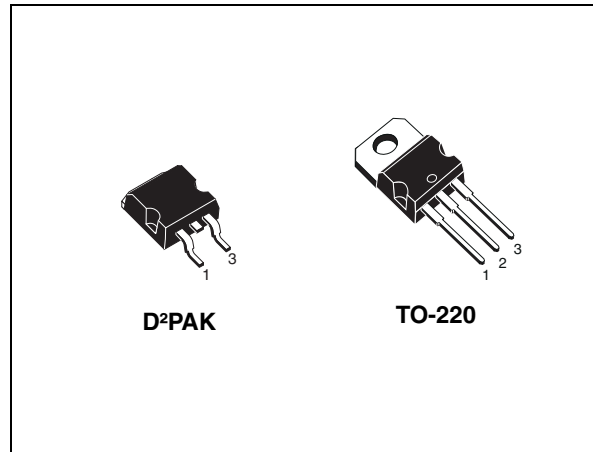
- Exceptional dv/dt capability
- 100% avalanche tested
- Low threshold drive

Description

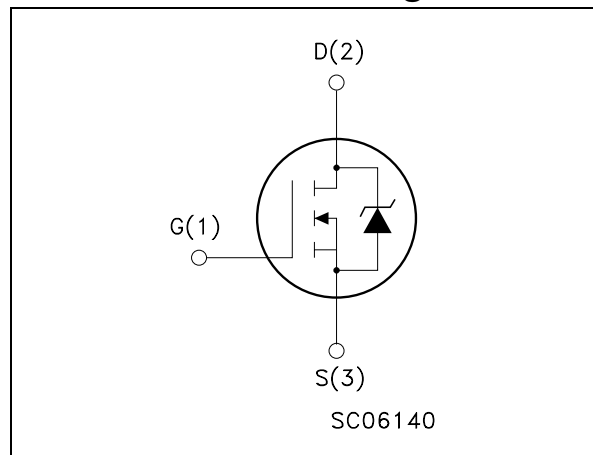
This Power MOSFET is the latest development of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order codes

Sales type	Marking	Package	Packaging
STP36NF06L	P36NF06L	TO-220	Tube
STB36NF06L	B36NF06	D ² PAK	Tape & reel

Contents:

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS}=0$)	60	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20K\Omega$)	60	V
V_{GS}	Gate-source voltage	± 18	V
I_D	Drain-current (continuous) at $T_c=25^\circ C$	30	A
I_D	Drain-current (continuous) at $T_c=100^\circ C$	21	A
$I_{DM}^{(1)}$	Drain-current (pulsed)	120	A
P_{TOT}	Total dissipation at $T_c=25^\circ C$	70	W
	Derating factor	0.47	W/°C
$dv/dt^{(2)}$	Peak diode recovery voltage slope	10	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	225	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 30A$, $di/dt \leq 400A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$. $T_j \leq T_{jmax}$
3. Starting $T_j=25^\circ C$, $I_D=15A$, $V_{DD}=30V$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.14	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (free air) max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D=250\mu A, V_{GS}=0$	60			V
I_{DSS}	Zero gate voltage drain current ($V_{GS}=0$)	$V_{DS}=\text{Max rating}$ $V_{DS}=\text{Max rating } T_c=125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS}=0$)	$V_{GS}=\pm 18V$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS}=10V, I_D=15A$ $V_{GS}=5V, I_D=15A$		0.032 0.045	0.04 0.05	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
gfs	Forward transconductance	$V_{DS}=15V, I_D=15A$		15		S
C_{iss}	Input capacitance	$V_{DS}=25V, f=1MHz, V_{GS}=0$		660		pF
C_{oss}	Output capacitance			170		pF
C_{rss}	Reverse transfer capacitance			70		pF
Q_g	Total gate charge	$V_{DD}=30V, I_D=30A$ $V_{GS}=5V$		13	17	nC
Q_{gs}	Gate-source charge			4.2		nC
Q_{gd}	Gate-drain charge			7.8		nC

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay Time Rise time	$V_{DD}=30V$, $I_D=15A$ $R_G=4.7\Omega$, $V_{GS}=5V$ (see Figure 14)		10 80		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=30V$, $I_D=15A$ $R_G=4.7\Omega$, $V_{GS}=5V$ (see Figure 14)		19 13		ns ns

Table 6. Source Drain Diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				30	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				120	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=24A$, $V_{GS}=0$			1.5	V
t_{rr}	Reverse recovery time			55		ns
Q_{rr}	Reverse recovery charge	$I_{SD}=20A$, $V_{DD}=20V$, $di/dt=100A/\mu s$, $T_j=150^\circ C$		107		nC
I_{RRM}	Reverse recovery current			3.9		A

1. Pulse width limited by safe operating area.
2. Pused: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

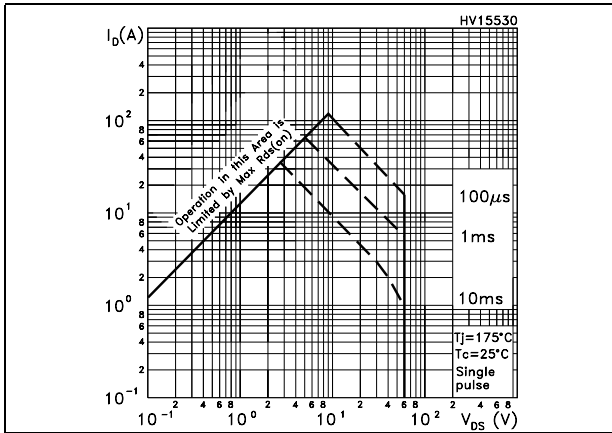


Figure 2. Thermal impedance

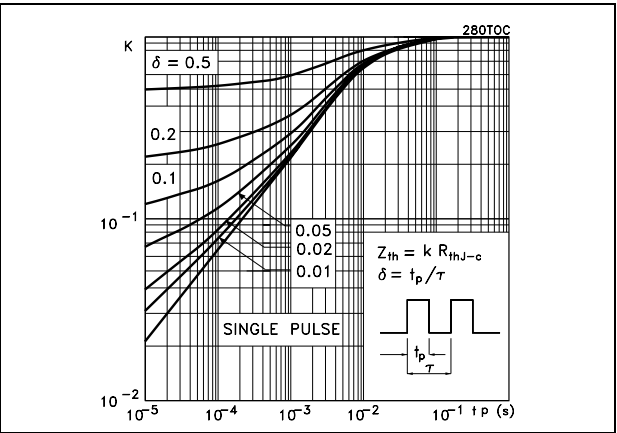


Figure 3. Output characteristics

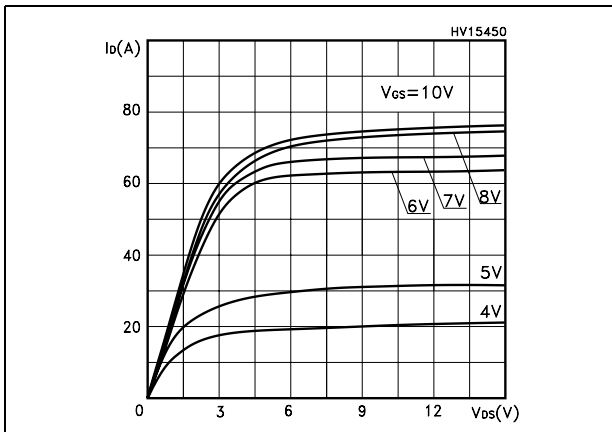


Figure 4. Transfer characteristics

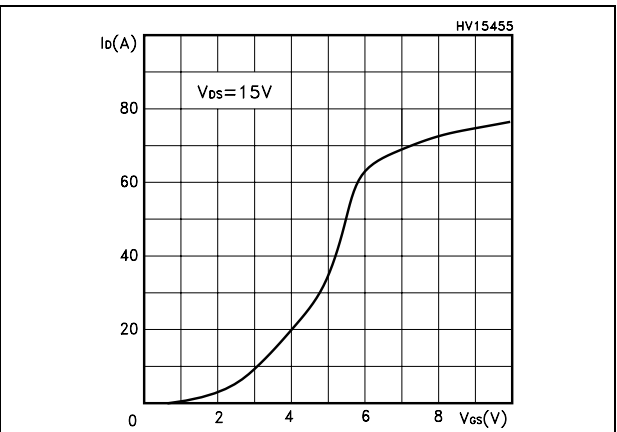


Figure 5. Transconductance

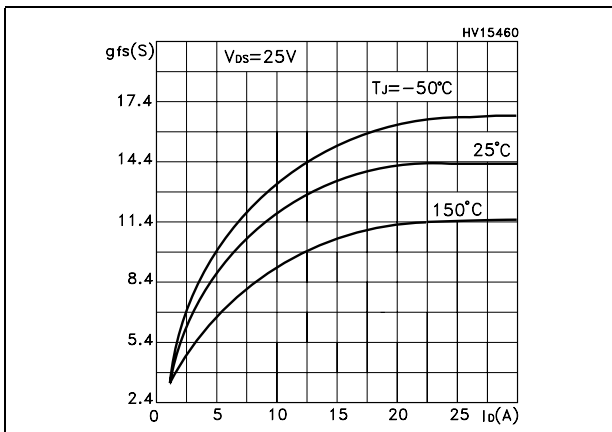


Figure 6. Static drain-source on resistance

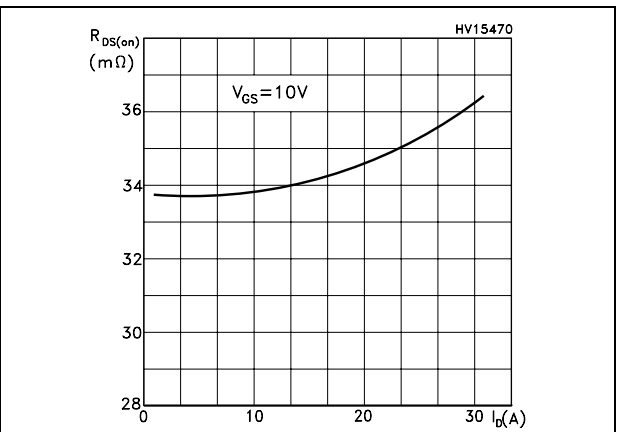


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

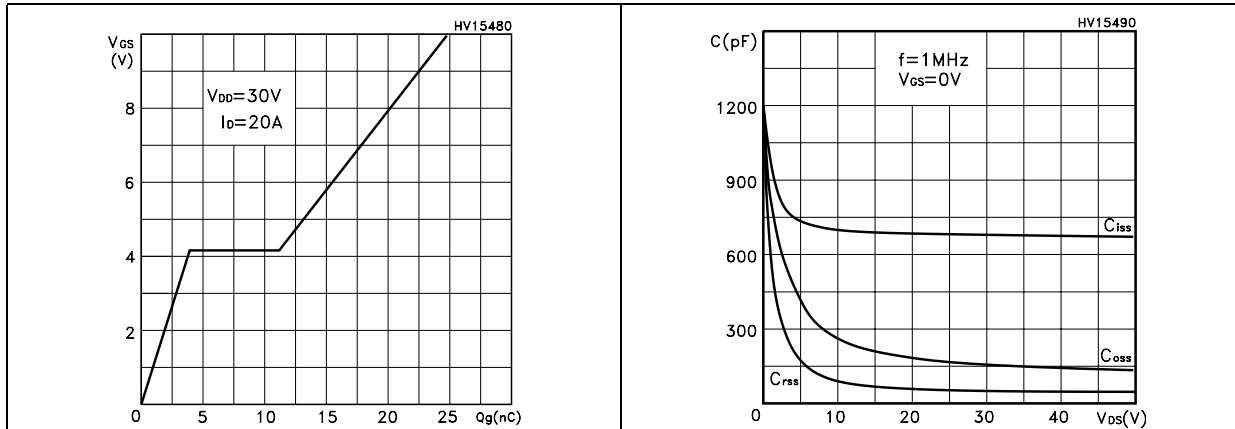


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

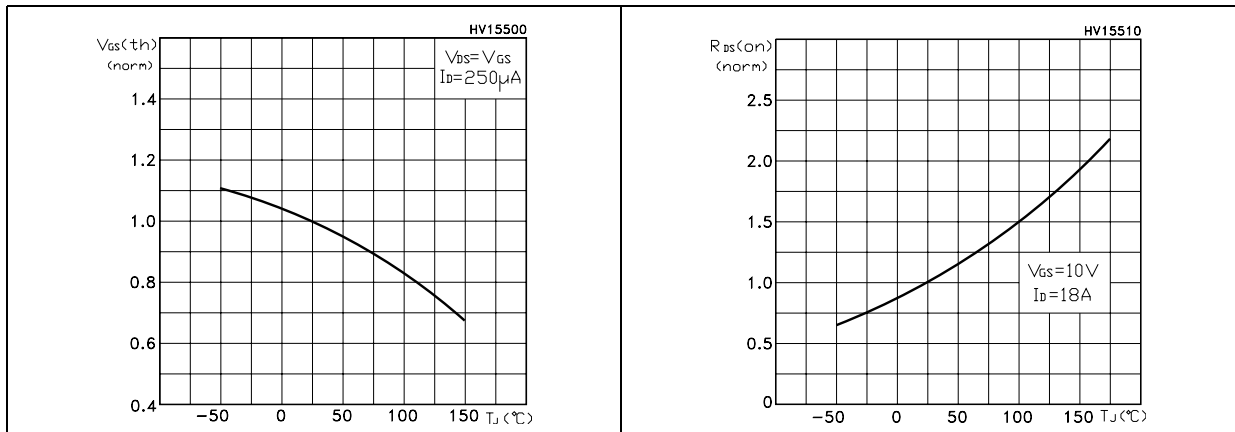
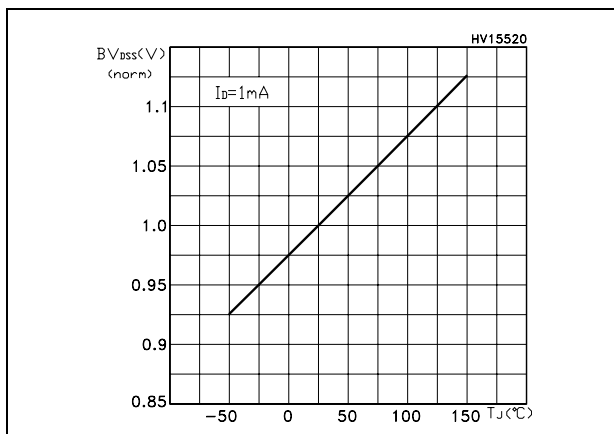


Figure 11. Normalized $B_{V_{DSS}}$ vs temperature



3 Test circuit

Figure 12. Unclamped inductive load test circuit

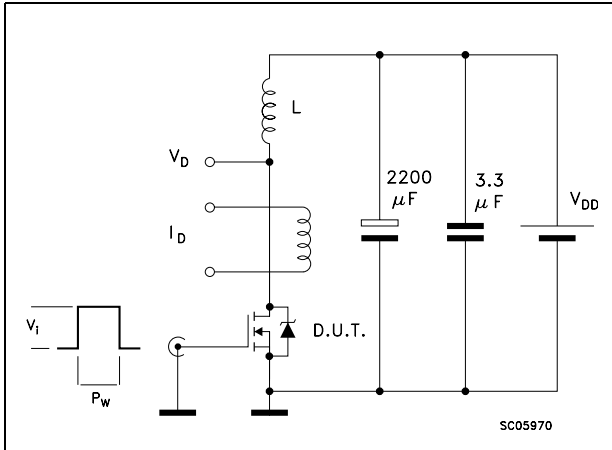


Figure 13. Unclamped inductive waveform

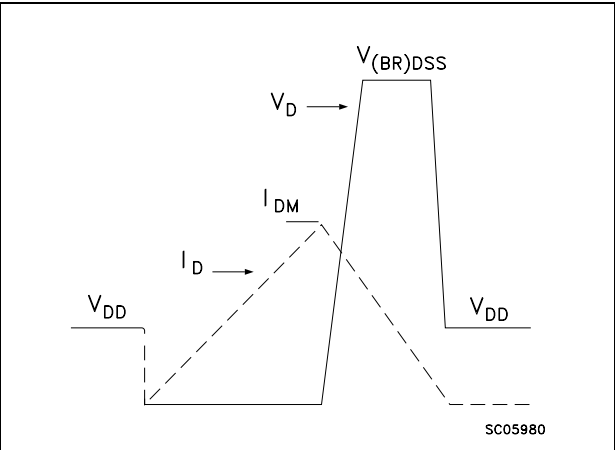


Figure 14. Switching times test circuit for resistive load

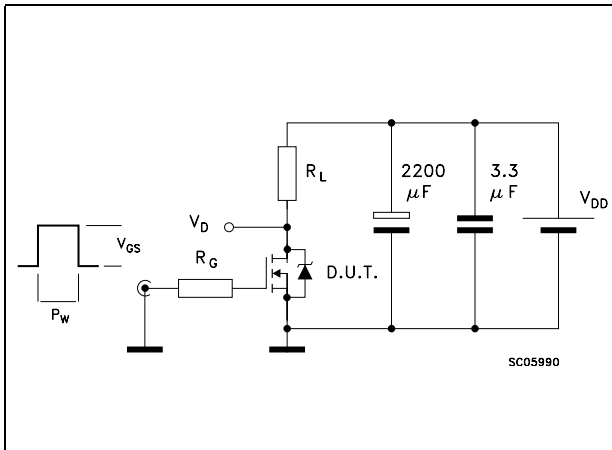


Figure 15. Gate charge test circuit

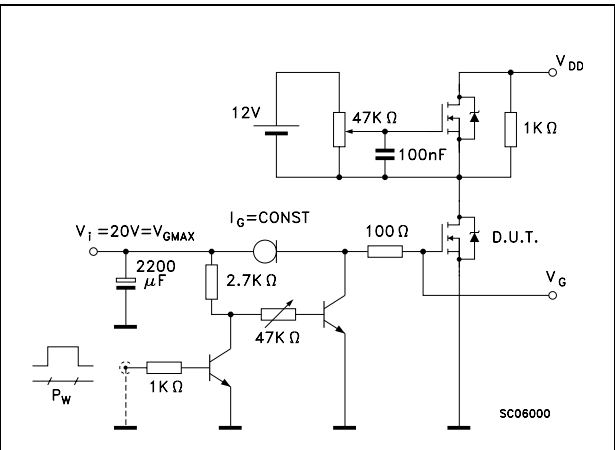


Figure 16. Test circuit for inductive load switching and diode recovery times

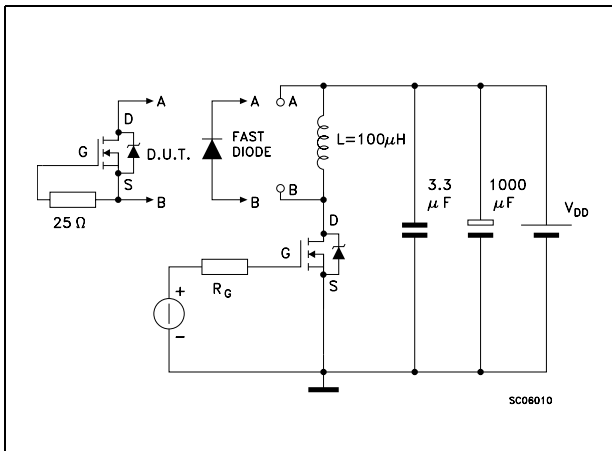
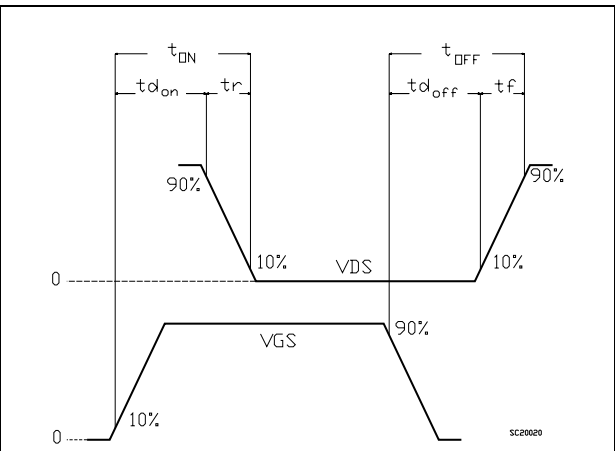


Figure 17. Switching time waveform

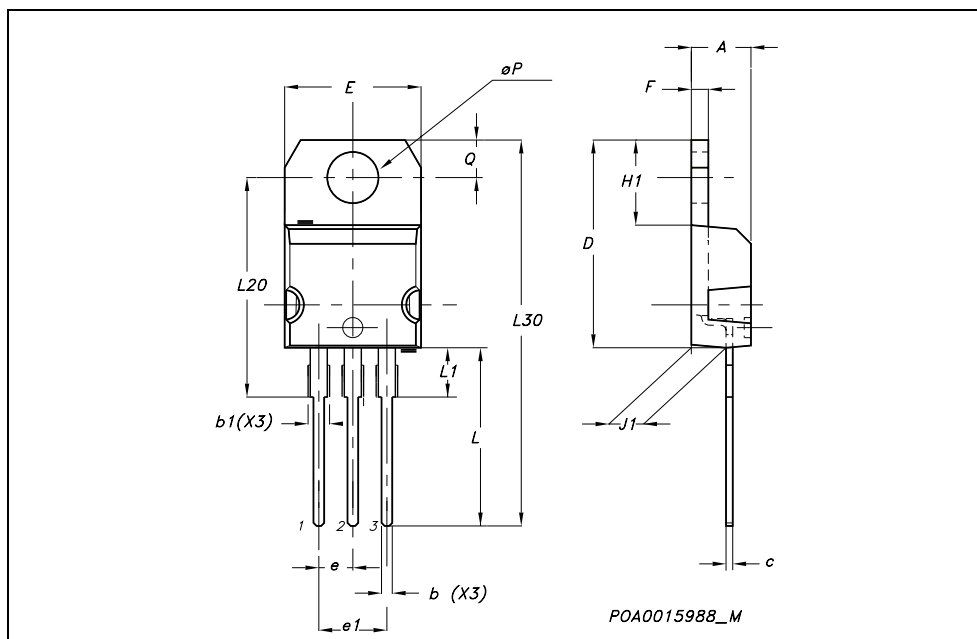


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

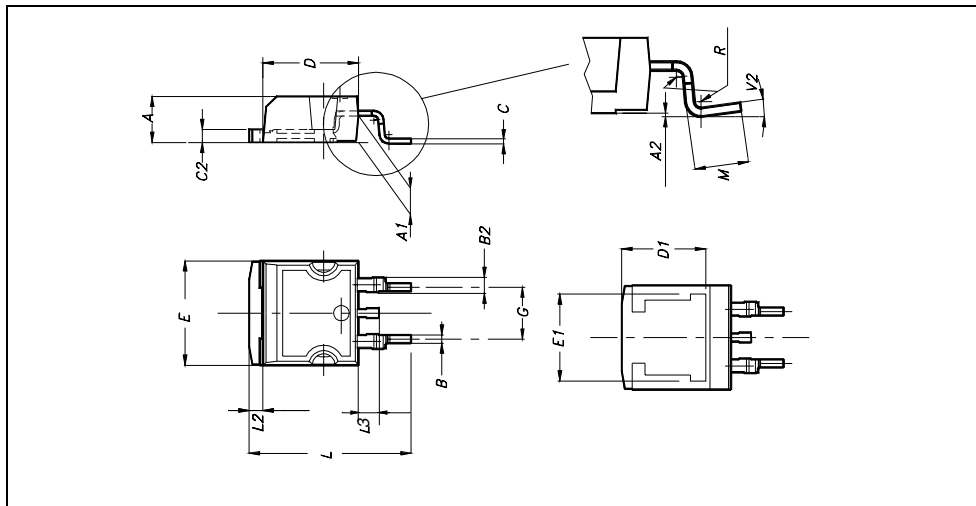
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

User Direction of Feed

TRL

FEED DIRECTION

Bending radius R min.

* on sales type

6 Revision history

Table 7. Revision history

Date	Revision	Changes
14-Jun-2003	1	First release
13-Mar-2006	2	Complete version
26-Jun-2006	3	New template, no content change

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