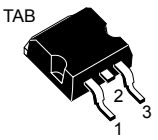
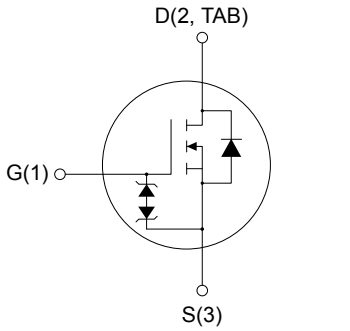
# STB41N40DM6AG

Datasheet

## Automotive-grade N-channel 400 V, 0.050 Ω typ., 41 A, MDmesh™ DM6 Power MOSFET in a D²PAK package




D²PAK




NG1D2TS3Z

| Product status link |
|---|
| STB41N40DM6AG |

| Product summary | |
|---|---|
| **Order code** | STB41N40DM6AG |
| **Marking** | 41N40DM6 |
| **Package** | D²PAK |
| **Packing** | Tape and reel |

## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STB41N40DM6AG | 400 V | 0.065 Ω | 41 A |

- AEC-Q101 qualified
- Fast-recovery body diode
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

## Applications

- Switching applications

## Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge ($Q_{rr}$), recovery time ($t_{rr}$) and excellent improvement in $R_{DS(on)}$ per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ±25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 41 | A |
| | Drain current (continuous) at $T_C$ = 100 °C | 26 | A |
| $I_{DM}$(1) | Drain current (pulsed) | 150 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 250 | W |
| dv/dt(2) | Peak diode recovery voltage slope | 50 | V/ns |
| dv/dt(3) | MOSFET dv/dt ruggedness | 100 | |
| $T_J$ | Operating junction temperature range | -55 to 150 | °C |
| $T_{stg}$ | Storage temperature range | | |

1. *Pulse width limited by safe operating area*
2. *$I_{SD}$ ≤ 41 A, di/dt ≤ 800 A/µs, $V_{DS\ peak}$ < $V_{(BR)DSS}$, $V_{DD}$ = 320 V*
3. *$V_{DS}$ ≤ 320 V*

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 0.5 | °C/W |
| $R_{thj\text{-}pcb}$(1) | Thermal resistance junction-pcb | 30 | |

1. *When mounted on an 1-inch² FR-4, 2 Oz copper board.*

**Table 3. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$) | 6 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j$ = 25°C, $I_D$ = $I_{AR}$, $V_{DD}$ = 100 V) | 760 | mJ |

# 2 Electrical characteristics

$T_C$ = 25 °C unless otherwise specified

**Table 4. On-/off-states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$= 0 V, $I_D$ = 1 mA | 400 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 400 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 400 V, $T_C$ = 125 °C(1) | | | 100 | µA |
| $I_{GSS}$ | Gate body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ±25 V | | | ±1 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 20.5 A | | 0.050 | 0.065 | Ω |

1. *Defined by design, not subject to production test.*

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 2310 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 151 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 10 | - | pF |
| $C_{oss\ eq.}$(1) | Equivalent output capacitance | $V_{DS}$ = 0 to 320 V, $V_{GS}$ = 0 V | - | 450 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz open drain | - | 1.3 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 320 V, $I_D$ = 41 A, $V_{GS}$ = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior) | - | 53 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 12 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 29 | - | nC |

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.*

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 200 V, $I_D$ = 20.5 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | - | 18 | - | ns |
| $t_r$ | Rise time | | - | 10.3 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 46 | - | ns |
| $t_f$ | Fall time | | - | 9.4 | - | ns |

**Table 7. Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 41 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | | 150 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$ = 41 A, $V_{GS}$ = 0 V | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 41 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 103 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 0.44 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 8.5 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 41 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V, $T_j$ = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 180 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 1.5 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 17 | | A |

1. *Pulse width limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

**Table 8. Gate-source Zener diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS}$ = ±1 mA, $I_D$ = 0 A | ±30 | - | - | V |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

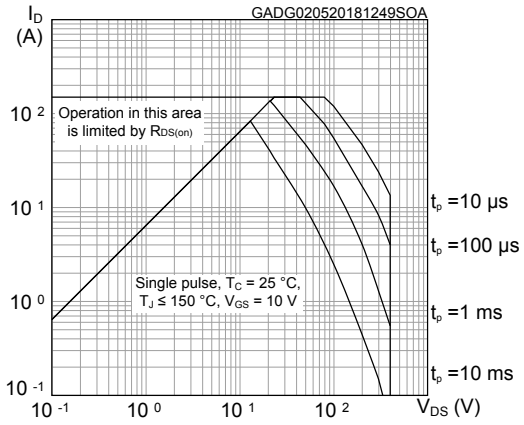



**Figure 2. Thermal impedance**

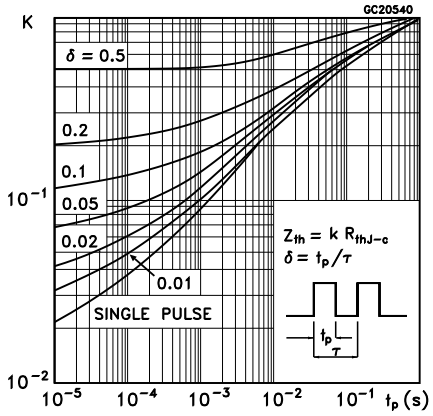



**Figure 3. Output characteristics**

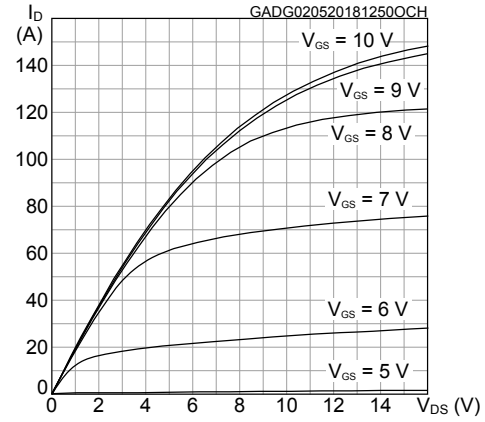



**Figure 4. Transfer characteristics**

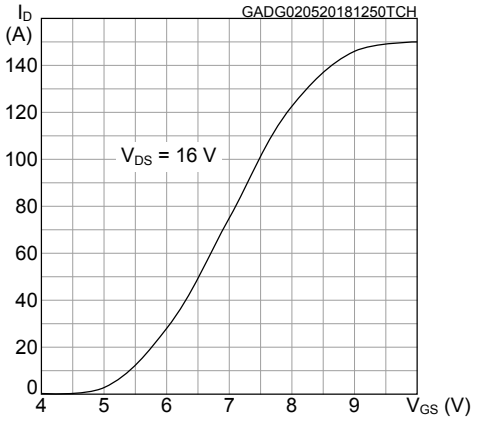



**Figure 5. Gate charge vs gate-source voltage**

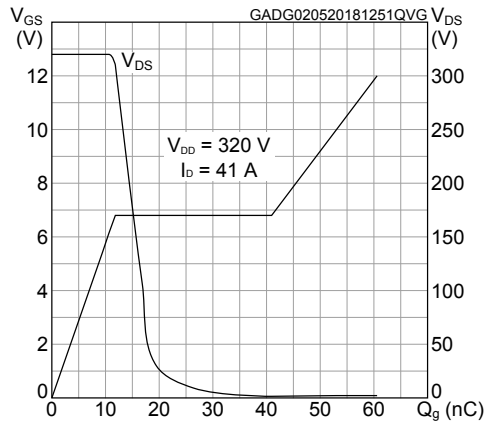



**Figure 6. Static drain-source on-resistance**

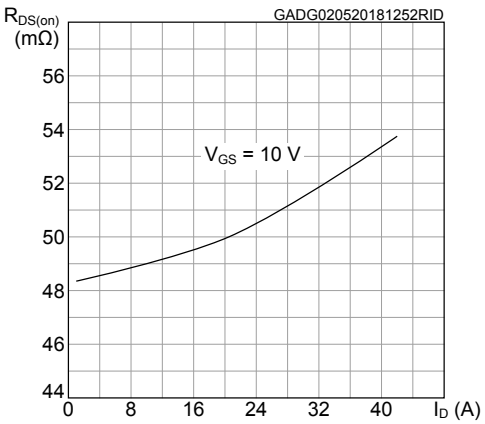


**Figure 7. Capacitance variations**

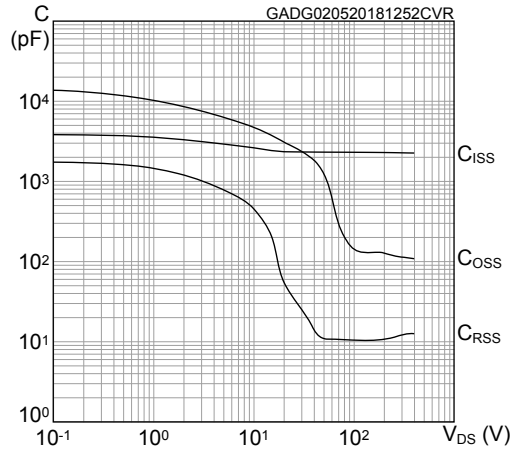



**Figure 8. Normalized gate threshold voltage vs temperature**

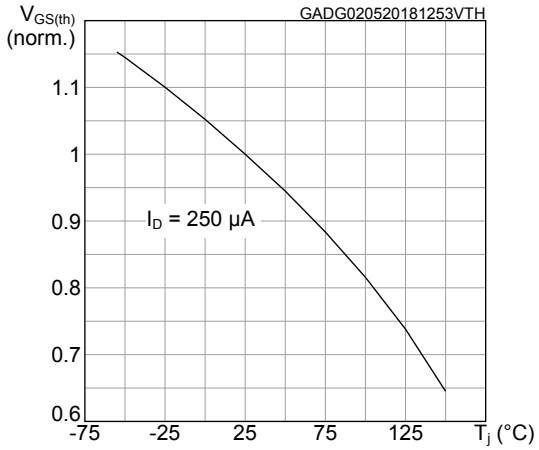



**Figure 9. Normalized on-resistance vs temperature**

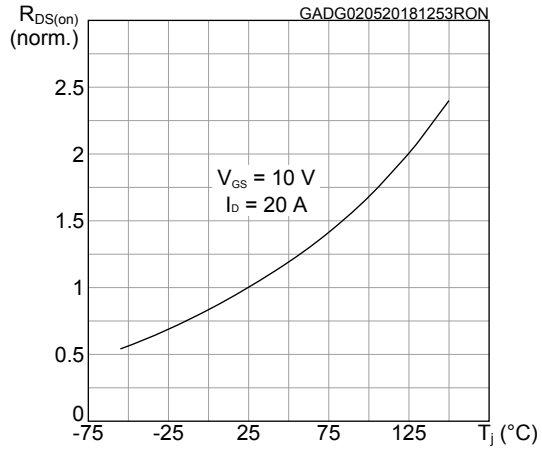



**Figure 10. Normalized $V_{BR(DSS)}$ vs temperature**

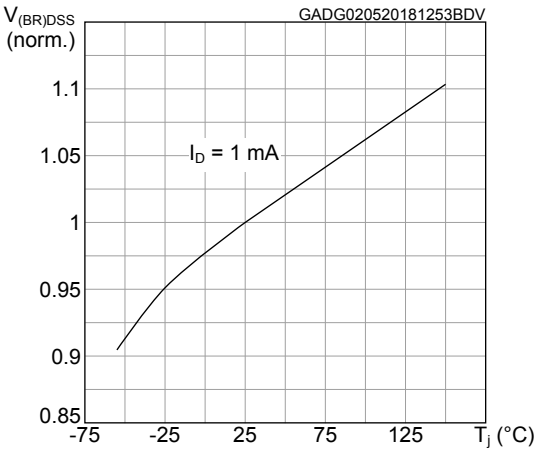



**Figure 11. Source-drain diode forward characteristics**

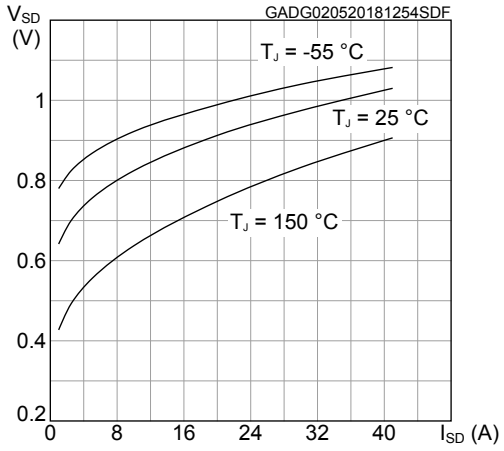
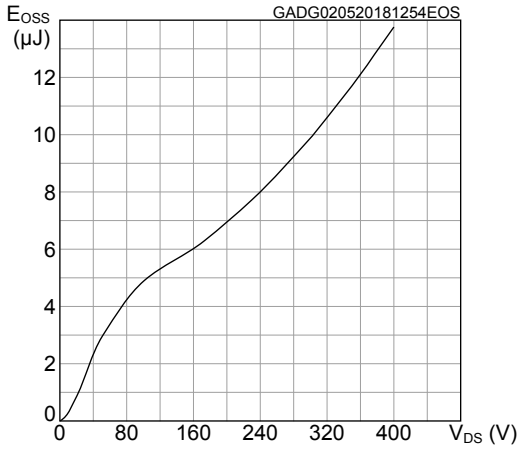



**Figure 12. Output capacitance stored energy**



# 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**

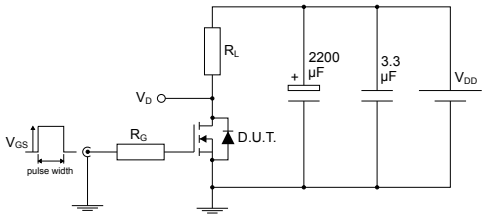



**Figure 14. Test circuit for gate charge behavior**

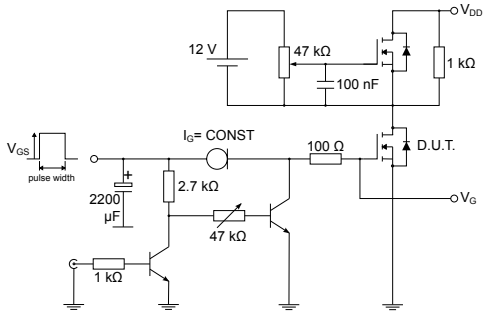



**Figure 15. Test circuit for inductive load switching and diode recovery times**

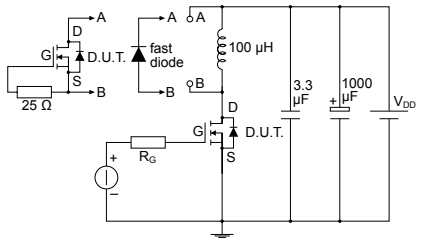



**Figure 16. Unclamped inductive load test circuit**

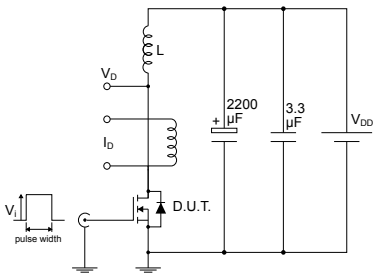



**Figure 17. Unclamped inductive waveform**

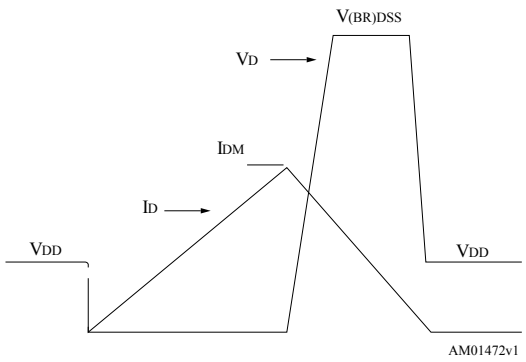
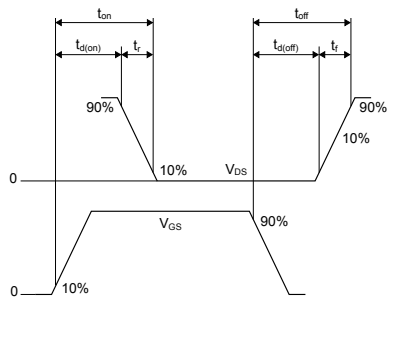



**Figure 18. Switching time waveform**



# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

## 4.1 D²PAK (TO-263) type A2 package information

**Figure 19. D²PAK (TO-263) type A2 package outline**

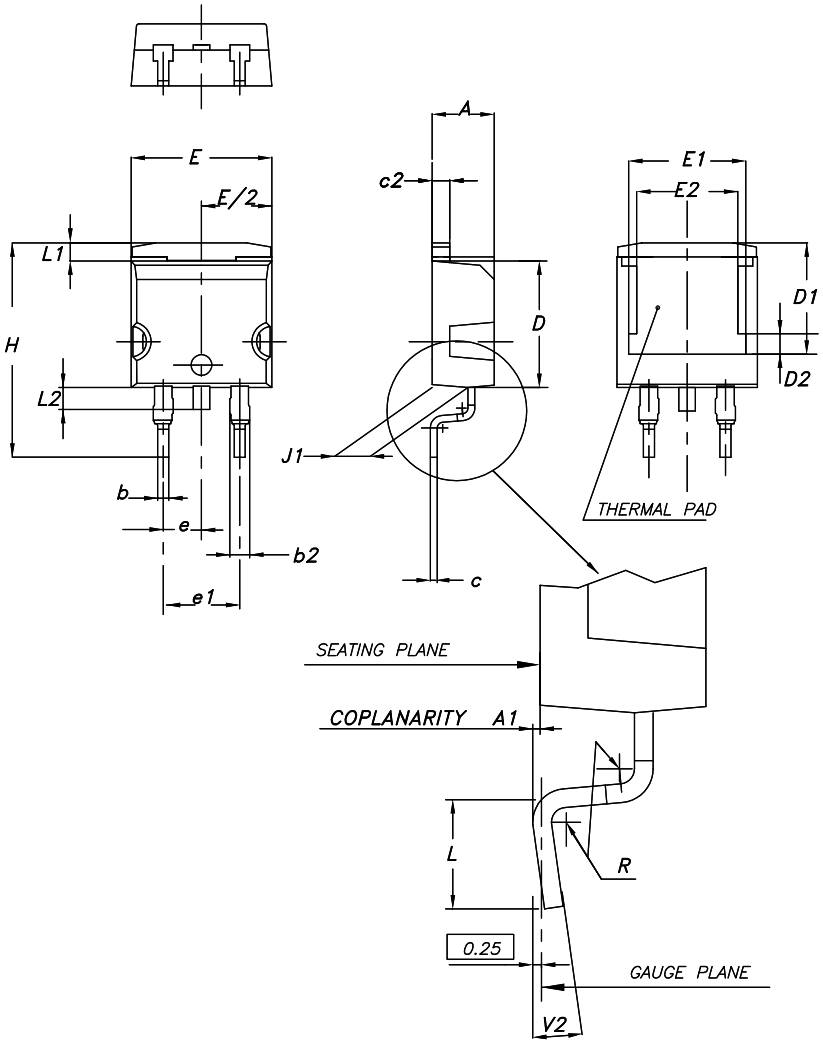



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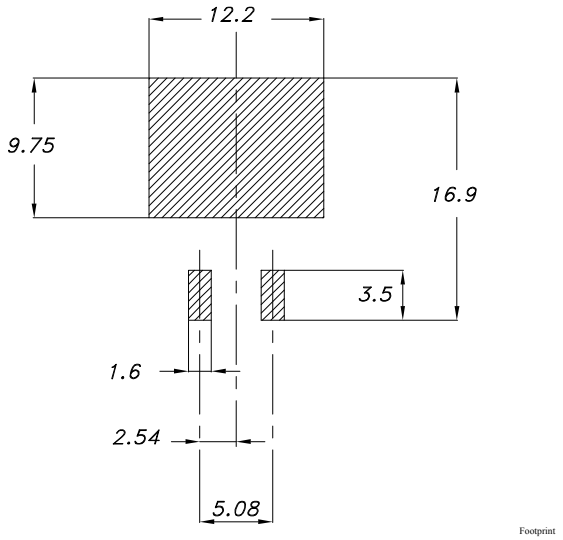
Table 9. D²PAK (TO-263) type A2 package mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| A1 | 0.03 | | 0.23 |
| b | 0.70 | | 0.93 |
| b2 | 1.14 | | 1.70 |
| c | 0.45 | | 0.60 |
| c2 | 1.23 | | 1.36 |
| D | 8.95 | | 9.35 |
| D1 | 7.50 | 7.75 | 8.00 |
| D2 | 1.10 | 1.30 | 1.50 |
| E | 10.00 | | 10.40 |
| E1 | 8.70 | 8.90 | 9.10 |
| E2 | 7.30 | 7.50 | 7.70 |
| e | | 2.54 | |
| e1 | 4.88 | | 5.28 |
| H | 15.00 | | 15.85 |
| J1 | 2.49 | | 2.69 |
| L | 2.29 | | 2.79 |
| L1 | 1.27 | | 1.40 |
| L2 | 1.30 | | 1.75 |
| R | | 0.40 | |
| V2 | 0° | | 8° |

Figure 20. D²PAK (TO-263) recommended footprint (dimensions are in mm)



## 4.2 D²PAK packing information

Figure 21. D²PAK tape outline

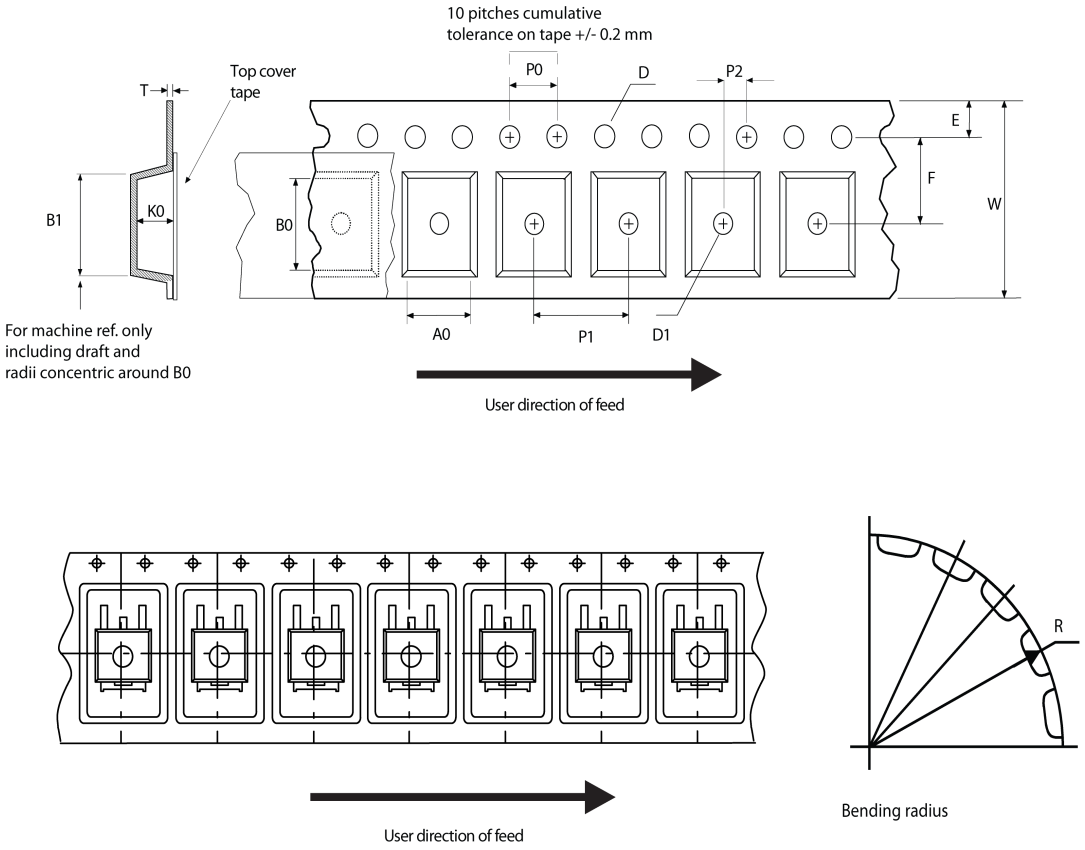
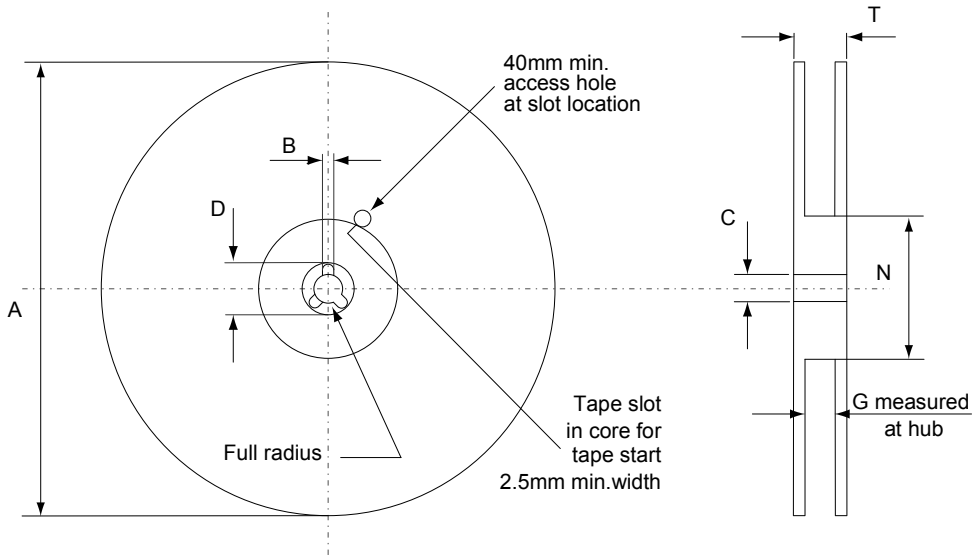


Figure 22. **D²PAK reel outline**




AM06038v1

Table 10. **D²PAK tape and reel mechanical data**

| Tape | | | Reel | | |
|---|---|---|---|---|---|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 10.5 | 10.7 | A | | 330 |
| B0 | 15.7 | 15.9 | B | 1.5 | |
| D | 1.5 | 1.6 | C | 12.8 | 13.2 |
| D1 | 1.59 | 1.61 | D | 20.2 | |
| E | 1.65 | 1.85 | G | 24.4 | 26.4 |
| F | 11.4 | 11.6 | N | 100 | |
| K0 | 4.8 | 5.0 | T | | 30.4 |
| P0 | 3.9 | 4.1 | | | |
| P1 | 11.9 | 12.1 | Base quantity | | 1000 |
| P2 | 1.9 | 2.1 | Bulk quantity | | 1000 |
| R | 50 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 23.7 | 24.3 | | | |

## Revision history

Table 11. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 17-May-2018 | 1 | Initial release. The document status is production data. |

# Contents

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