

STD12N50DM2

N-channel 500 V, 0.299 Ω typ., 11 A MDmesh™ DM2 Power MOSFET in a DPAK package

Datasheet - production data

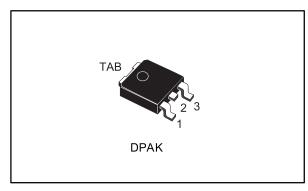
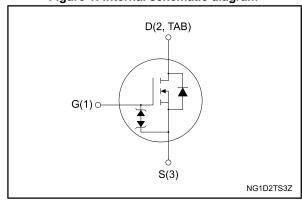


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	ID
STD12N50DM2	500 V	0.350 Ω	11 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh DM2 fast recovery diode series. It offers very low recovery charge and time (Qrr, trr) combined with low R_{DS(on)}, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STD12N50DM2	12N50DM2	DPAK	Tape and reel

Contents STD12N50DM2

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STD12N50DM2 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _G S	Gate-source voltage	±25	V
I_{D}	Drain current (continuous) at T _C = 25 °C	11	^
I _D	Drain current (continuous) at T _C = 100 °C	8	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	44	Α
Ртот	Total dissipation at T _C = 25 °C	110	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	40	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	V/ns
T _{stg}	Storage temperature range	FF to 1F0	°C
Tj	Operating junction temperature range	-55 to 150	

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	1.14	٥٥٨٨
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max	50	°C/W

Notes:

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetetive or not repetetive (pulse width limited by T _{jmax})	2.5	А
Eas	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	320	mJ

 $[\]ensuremath{^{(1)}}\mbox{Pulse}$ width limited by safe operating area.

 $^{^{(2)}}$ $I_{SD} \leq$ 11 A, di/dt \leq 400 A/µs; $V_{DS\;peak} < V_{(BR)DSS}, \, V_{DD} = 80\% \; V_{(BR)DSS}$

 $^{^{(3)}} V_{DS} \le 400 V$

⁽¹⁾When mounted on a 1-inch² FR-4, 2 oz Cu board

Electrical characteristics STD12N50DM2

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	500			V
	Zoro goto voltago	V _{GS} = 0 V, V _{DS} = 500 V			1	μΑ
I _{DSS} Zero gate voltage drain current		$V_{GS} = 0 \text{ V}, V_{DS} = 500 \text{ V},$ $T_{C} = 125 \text{ °C}^{(1)}$			100	μΑ
Igss	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±10	μΑ
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 5.5 A		0.299	0.350	Ω

Notes:

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance		-	628	1	pF
C_{oss}	Output capacitance	V _{DS} = 100 V, f = 1 MHz,	-	38	ı	pF
C _{rss}	Reverse transfer capacitance	V _{GS} = 0 V		1.2	1	pF
Coss eq. (1)	Equivalent output capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	•	69	ı	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	•	7	ı	Ω
Q_g	Total gate charge	$V_{DD} = 400 \text{ V}, I_{D} = 11 \text{ A},$	-	16	ı	nC
Q_gs	Gate-source charge	V _{GS} = 10 V (see <i>Figure 15: "Test</i>	-	4.6	-	nC
Q_{gd}	Gate-drain charge	circuit for gate charge behavior")	-	7	-	nC

Notes:

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 250 V, I _D = 5.5 A	-	12.5	-	ns
tr	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$ (see Figure 14: "Test circuit for	-	9	-	ns
t _{d(off)}	Turn-off-delay time	resistive load switching times"	ı	28	-	ns
t _f	Fall time	and Figure 19: "Switching time waveform")	-	9.8	-	ns



⁽¹⁾Defined by design, not subject to production test.

 $^{^{(1)}}$ $C_{\text{oss eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 8: Source drain diode

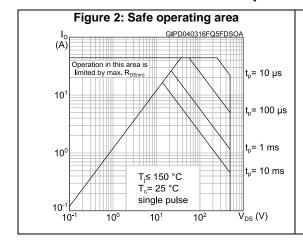
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit	
I _{SD}	Source-drain current		-		11	Α	
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		1		44	Α	
V _{SD} ⁽²⁾	Forward on voltage	V _{GS} = 0 V, I _{SD} = 11 A	-		1.6	V	
t _{rr}	Reverse recovery time	I _{SD} = 11 A, di/dt = 100 A/μs,	-	140		ns	
Qrr	Reverse recovery charge	V _{DD} = 60 V (see Figure 16: "Test circuit for inductive load switching and diode recovery	-	0.707		μC	
IRRM	Reverse recovery current	times")	-	10.1		Α	
t _{rr}	Reverse recovery time	I _{SD} = 11 A, di/dt = 100 A/μs,	-	190		ns	
Qrr	Reverse recovery charge	V _{DD} = 60 V, T _j = 150 °C (see Figure 16: "Test circuit for inductive load switching and	-	1.111		μC	
IRRM	Reverse recovery current	diode recovery times")	-	11.7		Α	

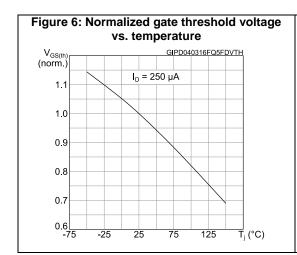
Notes:

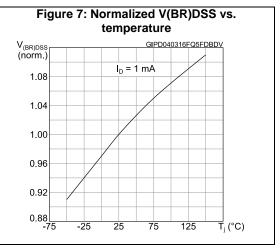
⁽¹⁾Pulse width is limited by safe operating area

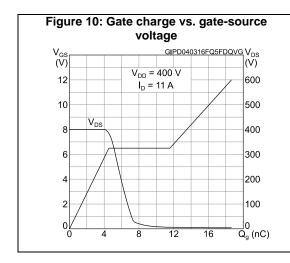
 $^{^{(2)}\}text{Pulse}$ test: pulse duration = 300 $\mu\text{s},$ duty cycle 1.5%

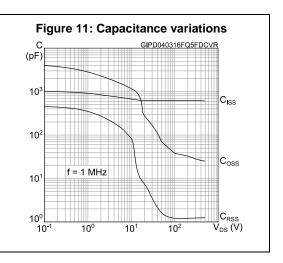
2.1 Electrical characteristics (curves)

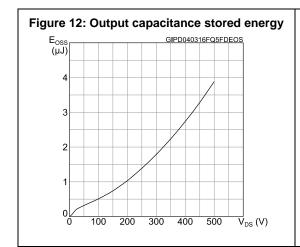


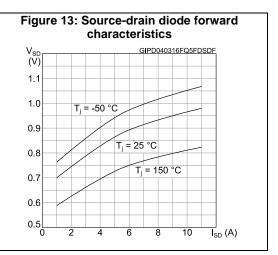












Test circuits STD12N50DM2

3 Test circuits

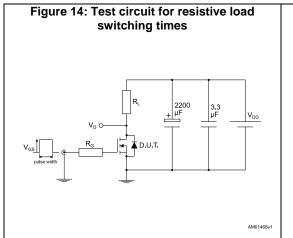


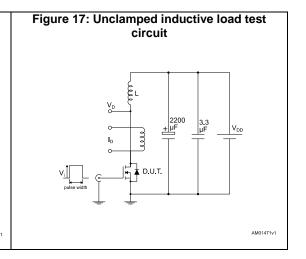
Figure 15: Test circuit for gate charge behavior

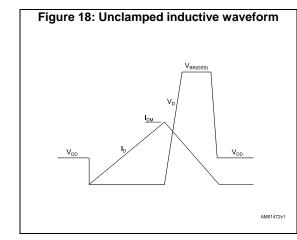
12 V 47 kΩ 100 nF D.U.T.

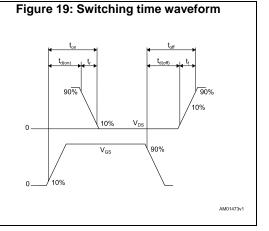
2200 PF 47 kΩ OVG

AM01466y1

Figure 16: Test circuit for inductive load switching and diode recovery times







4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 DPAK package information

Figure 20: DPAK (TO-252) type A2 package outline

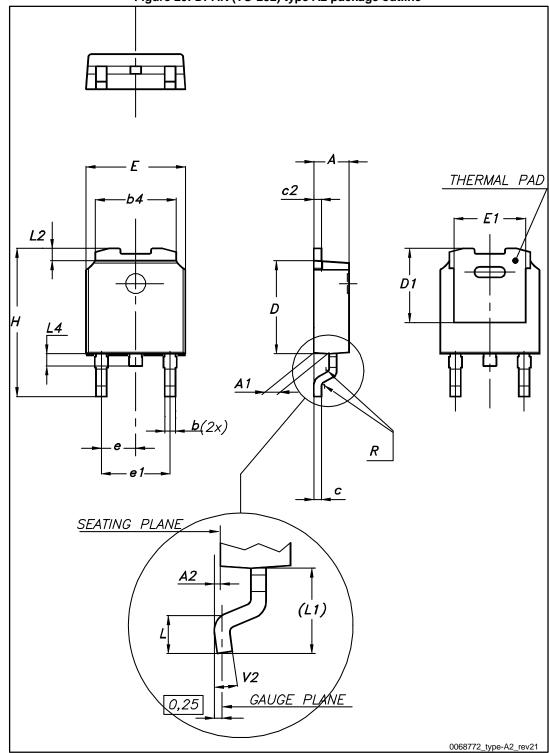


Table 9: DPAK (TO-252) type A2 mechanical data

Dim	mm				
Dim.	Min.	Тур.	Max.		
A	2.20		2.40		
A1	0.90		1.10		
A2	0.03		0.23		
b	0.64		0.90		
b4	5.20		5.40		
С	0.45		0.60		
c2	0.48		0.60		
D	6.00		6.20		
D1	4.95	5.10	5.25		
Е	6.40		6.60		
E1	5.10	5.20	5.30		
е	2.16	2.28	2.40		
e1	4.40		4.60		
Н	9.35		10.10		
L	1.00		1.50		
L1	2.60	2.80	3.00		
L2	0.65	0.80	0.95		
L4	0.60		1.00		
R		0.20			
V2	0°		8°		

Package information STD12N50DM2

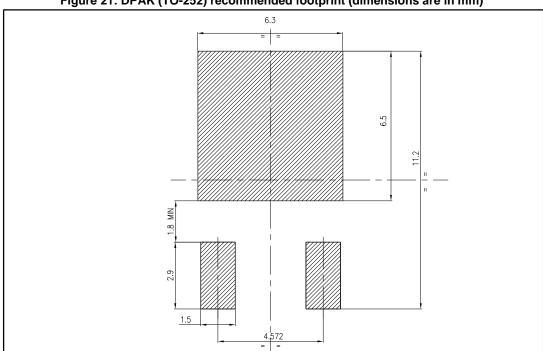
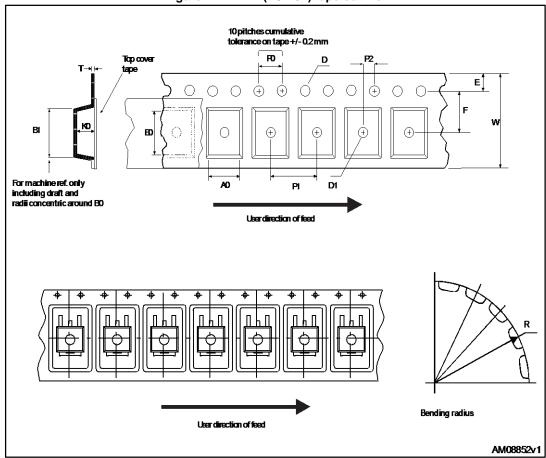


Figure 21: DPAK (TO-252) recommended footprint (dimensions are in mm)

FP_0068772_21

4.2 Packing information

Figure 22: DPAK (TO-252) tape outline



40mm min. access hole at slot location С Ν Α G measured Tape slot at hub in core for Full radius tape start 2.5mm min.width

Figure 23: DPAK (TO-252) reel outline

Table 10: DPAK (TO-252) tape and reel mechanical data

AM06038v1

Таре				Reel	
Dim.	mm .	Dim.	r	nm	
Dim.	Min.	Max.	Dilli.	Min.	Max.
A0	6.8	7	А		330
В0	10.4	10.6	В	1.5	
B1		12.1	С	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
Ш	1.65	1.85	N	50	
F	7.4	7.6	Т		22.4
K0	2.55	2.75			
P0	3.9	4.1	Bas	se qty.	2500
P1	7.9	8.1	Bul	k qty.	2500
P2	1.9	2.1			
R	40				
Т	0.25	0.35			
W	15.7	16.3			

STD12N50DM2 Revision history

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
26-Aug-2014	1	First release.
07-Mar-2016	2	Text and formatting changes throughout document In Section 1: "Electrical ratings": - updated Table 4: "Avalanche characteristics" In Section 2: "Electrical characteristics" - updated Table 6: "Dynamic", Table 7: "Switching times" and Table 8: "Source drain diode" Added Section 2.1: "Electrical characteristics (curves)" Updated Section 4: "Package information"

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