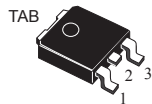
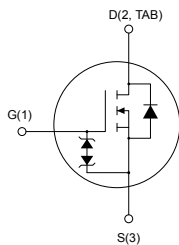


## N-channel 600 V, 345 mΩ typ., 10 A MDmesh DM6 Power MOSFET in a DPAK package


**DPAK**


AM01476v1\_tab

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STD12N60DM6	600 V	390 mΩ	10 A

- Fast-recovery body diode
- Lower R<sub>DS(on)</sub> per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q<sub>rr</sub>), recovery time (t<sub>rr</sub>) and excellent improvement in R<sub>DS(on)</sub> per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.



#### Product status link

[STD12N60DM6](#)

#### Product summary

<b>Order code</b>	STD12N60DM6
<b>Marking</b>	12N60DM6
<b>Package</b>	DPAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	10	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6.3	
$I_{DM}^{(1)}$	Drain current (pulsed)	28	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	90	W
$I_{AR}^{(2)}$	Avalanche current, repetitive or not repetitive	3	A
$E_{AS}^{(3)}$	Single pulse avalanche energy	195	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	100	V/ns
$di/dt^{(4)}$	Peak diode recovery current slope	1000	A/ $\mu\text{s}$
$dv/dt^{(5)}$	MOSFET $dv/dt$ ruggedness	100	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area.
2. Pulse width limited by  $T_J$  max.
3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .
4.  $I_{SD} \leq 10\text{ A}$ ,  $V_{DS} (\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .
5.  $V_{DS} \leq 480\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.39	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	$^\circ\text{C/W}$

1. When mounted on an 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			100	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 5\text{ A}$		345	390	m $\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	508	-	pF
$C_{oss}$	Output capacitance		-	28	-	pF
$C_{rss}$	Reverse transfer capacitance		-	4.7	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	100	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5.8	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 10\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	17	-	nC
$Q_{gs}$	Gate-source charge		-	3.8	-	nC
$Q_{gd}$	Gate-drain charge		-	9.3	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	11	-	ns
$t_r$	Rise time		-	4.3	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	26	-	ns
$t_f$	Fall time		-	7.3	-	ns

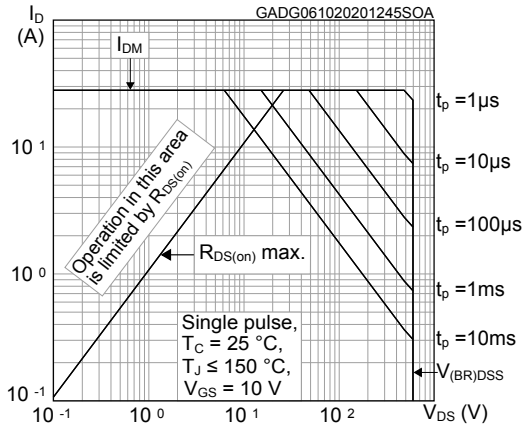
**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 10\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	80		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	0.288		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	7.2		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	148		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	0.680		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9.2		A

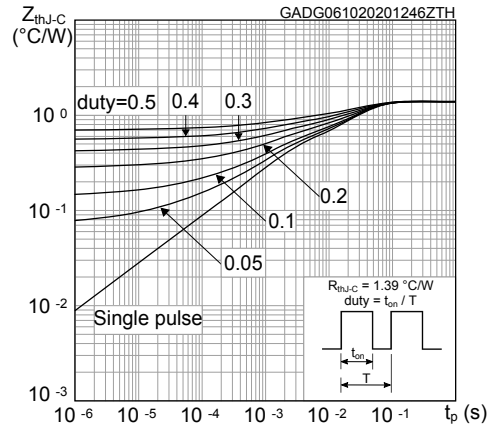
1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

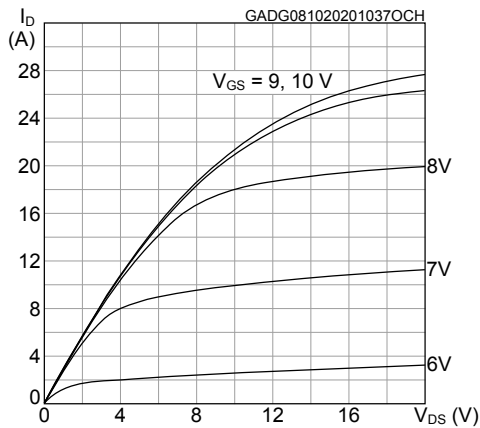
**Figure 1. Safe operating area**



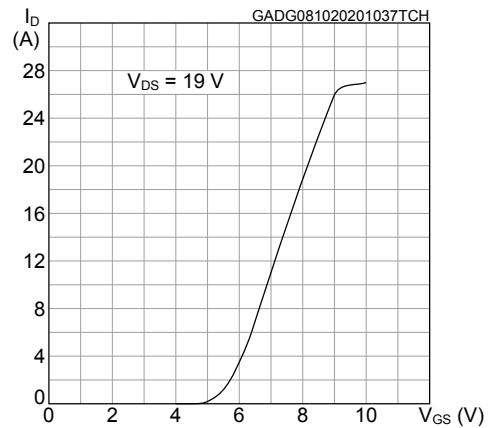
**Figure 2. Maximum transient thermal impedance**



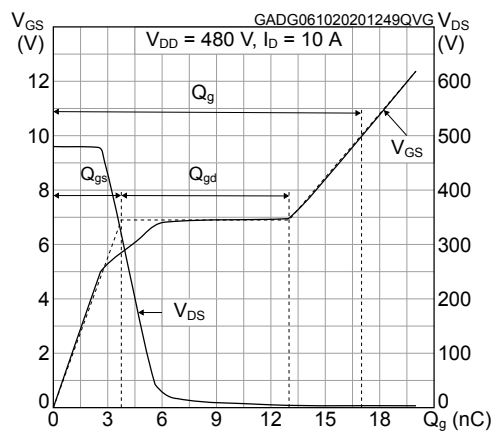
**Figure 3. Typical output characteristics**



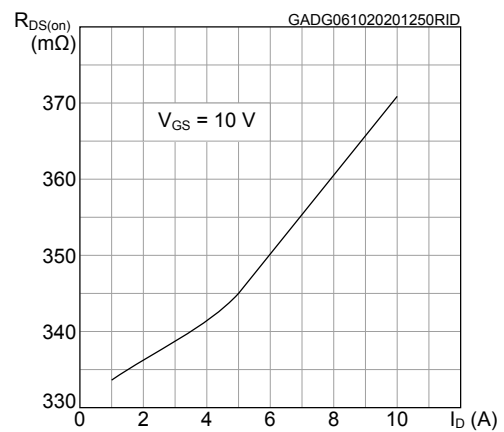
**Figure 4. Typical transfer characteristics**



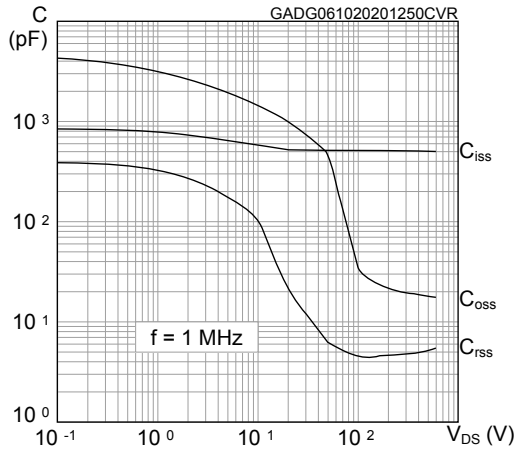
**Figure 5. Typical gate charge characteristics**



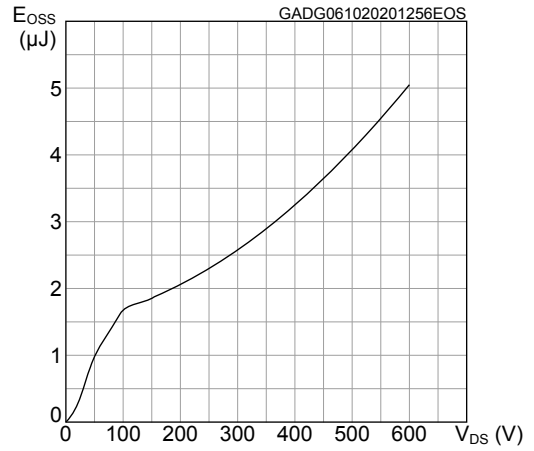
**Figure 6. Typical drain-source on-resistance**



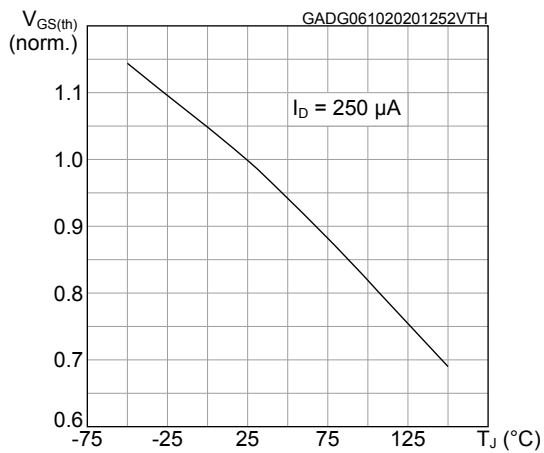
**Figure 7. Typical capacitance characteristics**



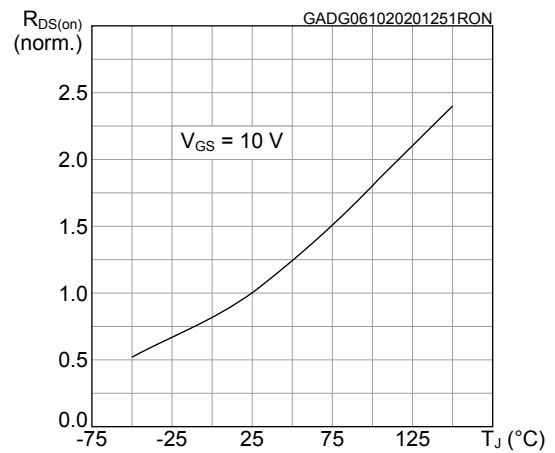
**Figure 8. Typical output capacitance stored energy**



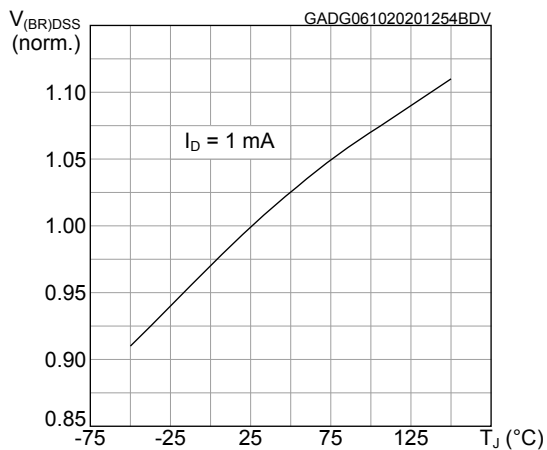
**Figure 9. Normalized gate threshold vs temperature**



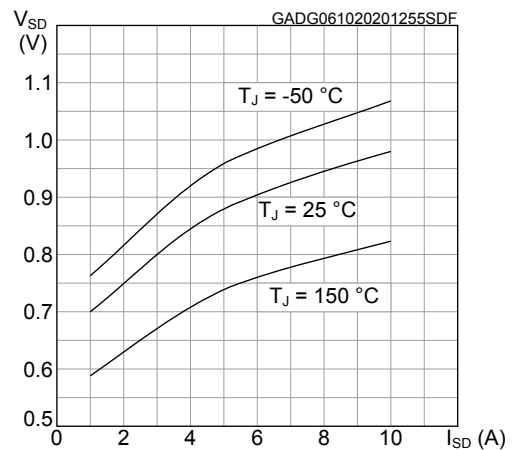
**Figure 10. Normalized on-resistance vs temperature**



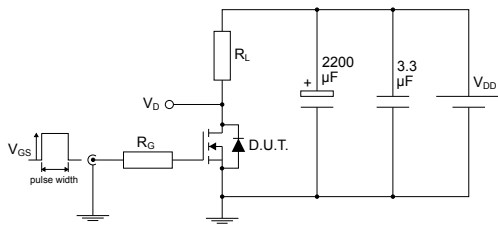
**Figure 11. Normalized breakdown voltage vs temperature**



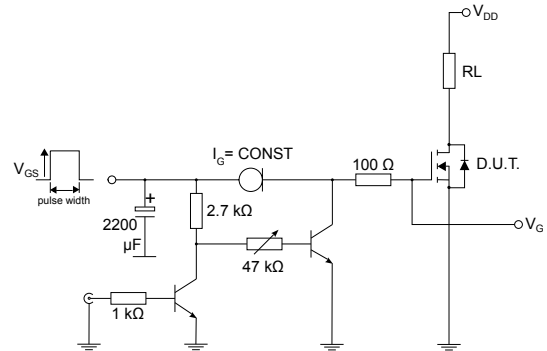
**Figure 12. Typical reverse diode forward characteristics**



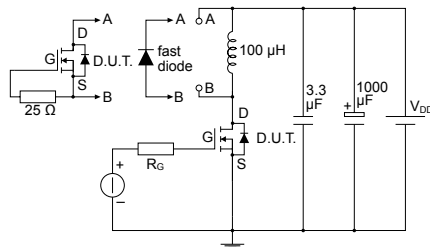
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


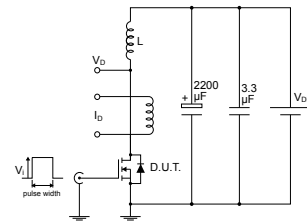
AM01468v1

**Figure 14. Test circuit for gate charge behavior**


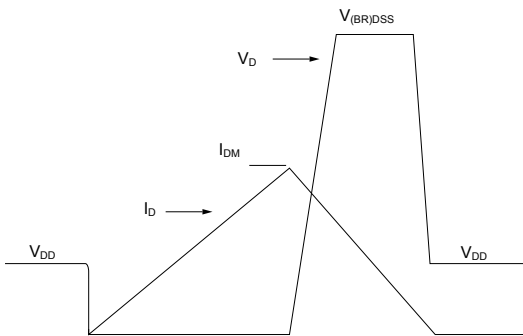
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**Figure 15. Test circuit for inductive load switching and diode recovery times**


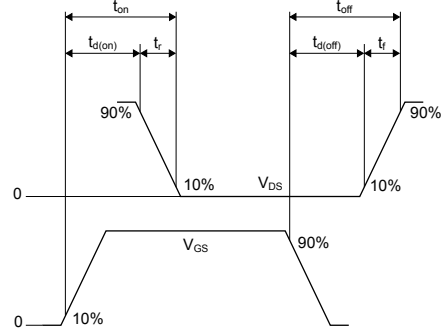
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**Figure 16. Unclamped inductive load test circuit**


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**Figure 17. Unclamped inductive waveform**


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**Figure 18. Switching time waveform**


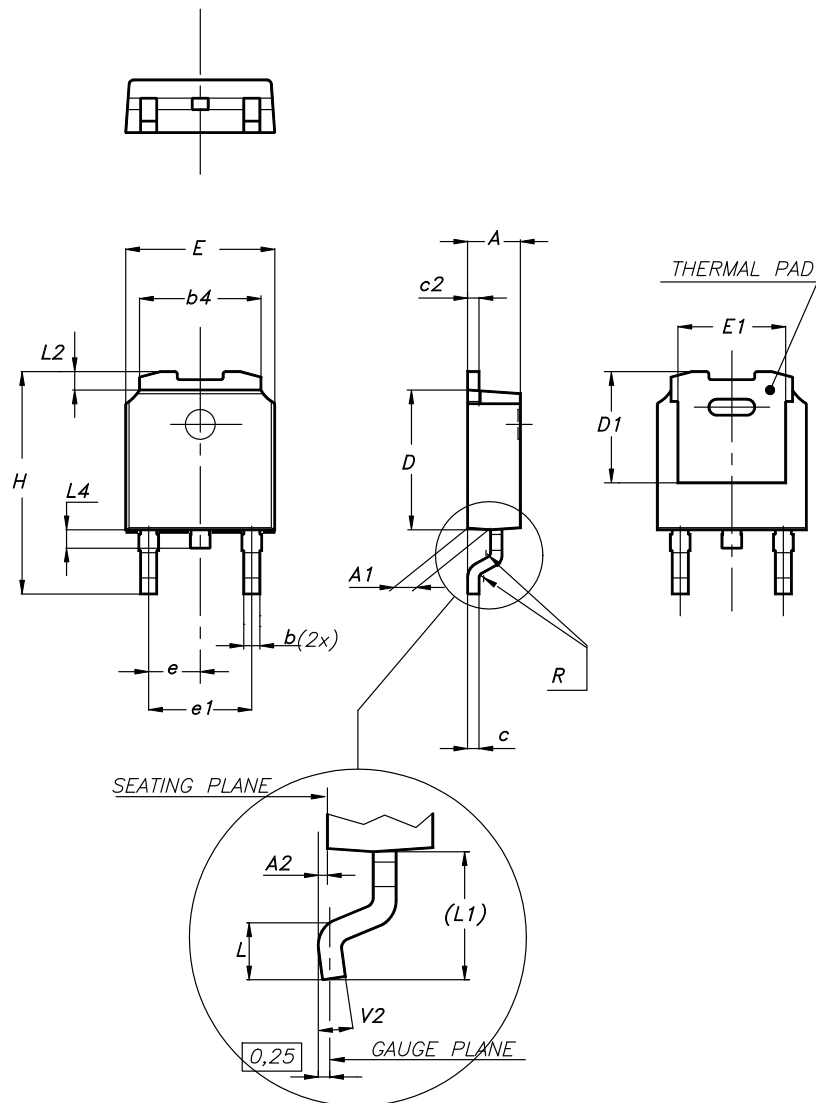
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## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 DPAK (TO-252) type A2 package information

**Figure 19.** DPAK (TO-252) type A2 package outline



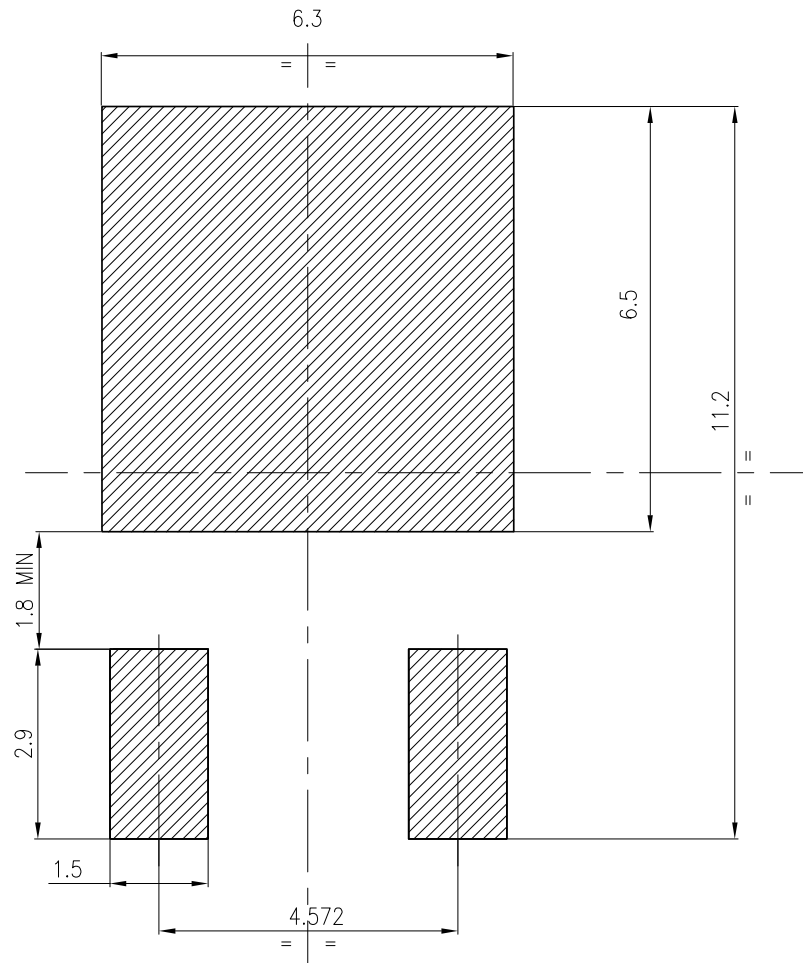
0068772\_type-A2\_rev30



**Table 7. DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

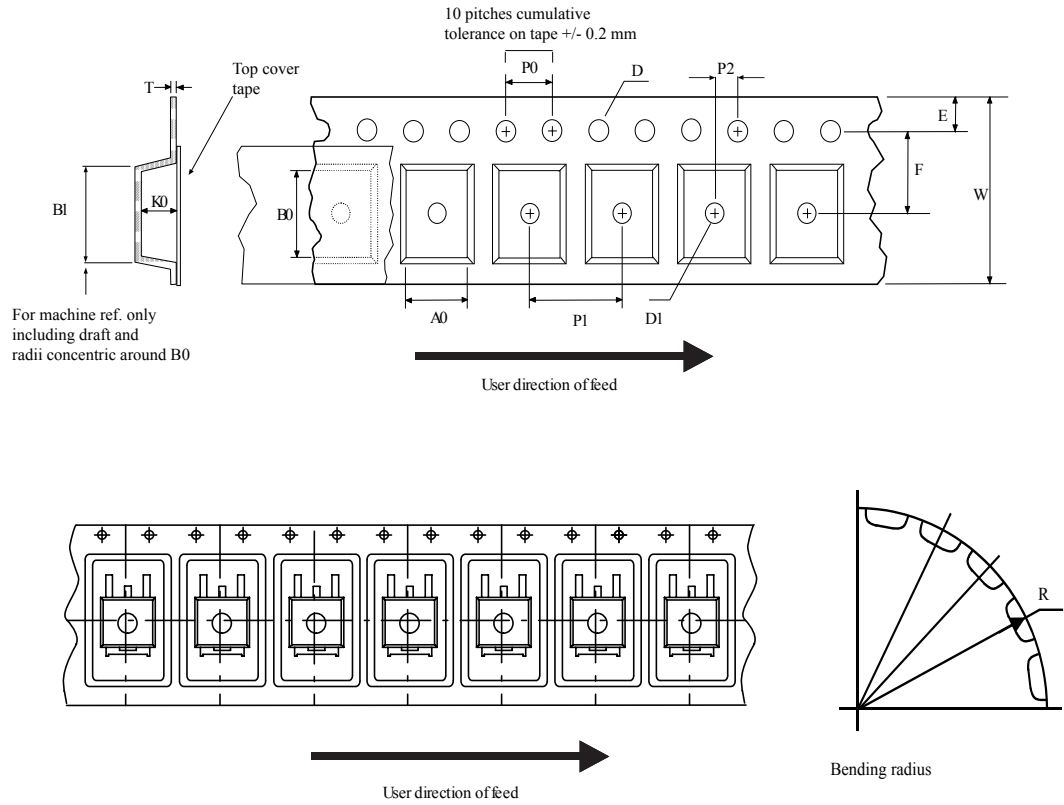
Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)



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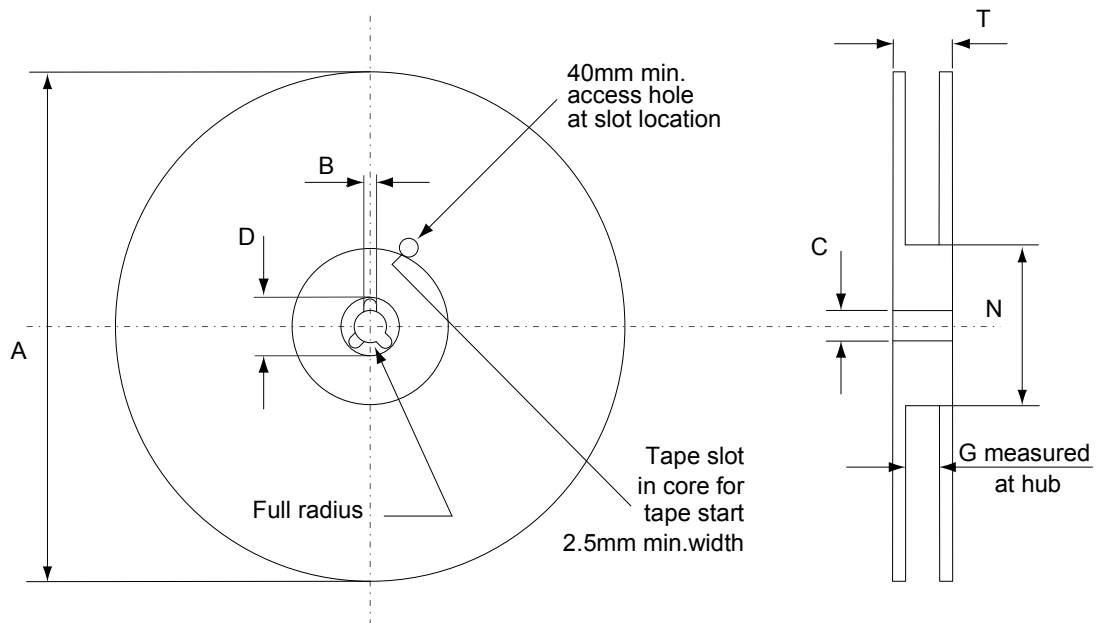
## 4.2 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



AM08852v1

**Figure 22. DPAK (TO-252) reel outline**



AM06038v1

**Table 8. DPAK (TO-252) tape and reel mechanical data**

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 9. Document revision history**

Date	Version	Changes
09-Oct-2020	1	First release.

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