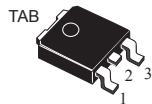
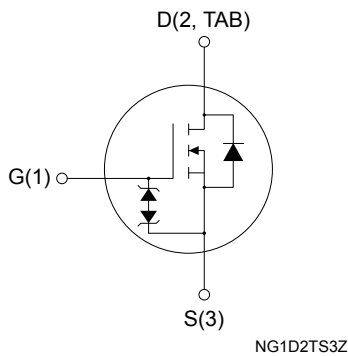


## Automotive-grade N-channel 500 V, 320 mΩ typ., 11 A MDmesh DM2 Power MOSFET in a DPAK package



DPAK




NG1D2TS3Z



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STD13N50DM2AG	500 V	360 mΩ	11 A

- AEC-Q101 qualified 
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge ( $Q_{rr}$ ) and time ( $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

#### Product status

STD13N50DM2AG

#### Product summary

<b>Order code</b>	STD13N50DM2AG
<b>Marking</b>	13N50DM2
<b>Package</b>	DPAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	±25	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	11	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	8	
$I_{DM}^{(1)}$	Drain current (pulsed)	28	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ °C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	°C
$T_j$	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 11\text{ A}$ ,  $di/dt \leq 800\text{ A}/\mu\text{s}$ ;  $V_{DS\ peak} < V_{(BR)DSS}$ ;  $V_{DD} = 400\text{ V}$
3.  $V_{DS} \leq 400\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.14	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

1. When mounted on a 1-inch<sup>2</sup> FR-4, 2 oz Cu board

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	2	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	230	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified).

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	500			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 500\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 500\text{ V}, T_C = 125\text{ °C}^{(1)}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}$		320	360	m $\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	597	-	pF
$C_{oss}$	Output capacitance		-	38	-	pF
$C_{riss}$	Reverse transfer capacitance		-	3.5	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	69	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 400\text{ V}, I_D = 11\text{ A}, V_{GS} = 0\text{ to } 10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	11.7	-	nC
$Q_{gs}$	Gate-source charge		-	3.8	-	nC
$Q_{gd}$	Gate-drain charge		-	4.2	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}, I_D = 5.5\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	13	-	ns
$t_r$	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	26	-	ns
$t_f$	Fall time		-	8	-	ns

**Table 7. Source-drain diode**

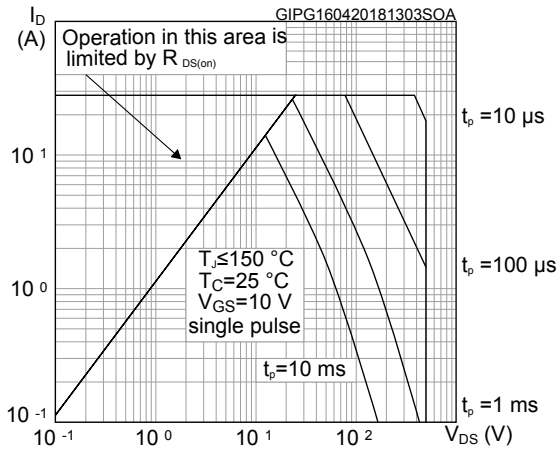
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 11\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	68		ns
$Q_{rr}$	Reverse recovery charge		-	200		nC
$I_{RRM}$	Reverse recovery current		-	5.9		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	107		ns
$Q_{rr}$	Reverse recovery charge		-	450		nC
$I_{RRM}$	Reverse recovery current		-	8.5		A

1. Pulse width is limited by safe operating area

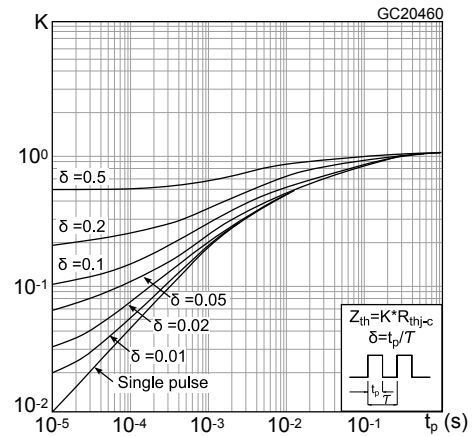
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

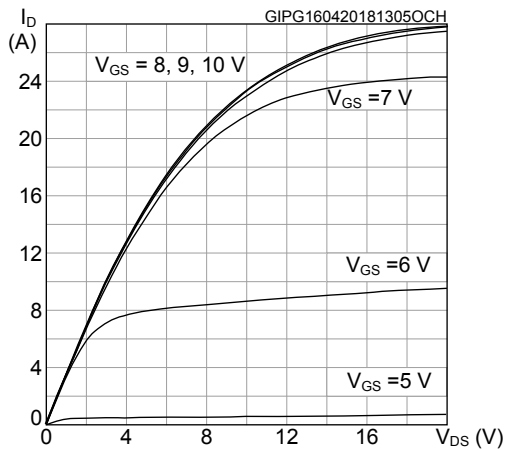
**Figure 1. Safe operating area**



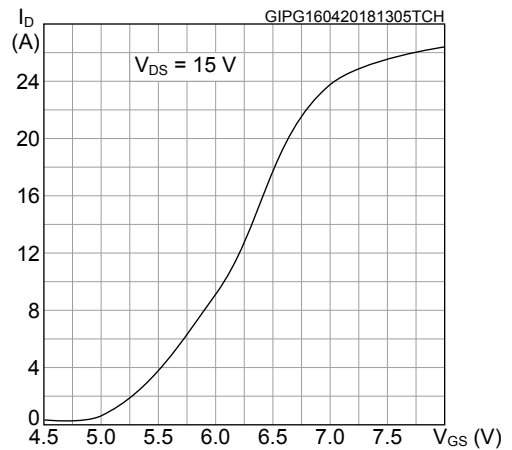
**Figure 2. Normalized transient thermal impedance**



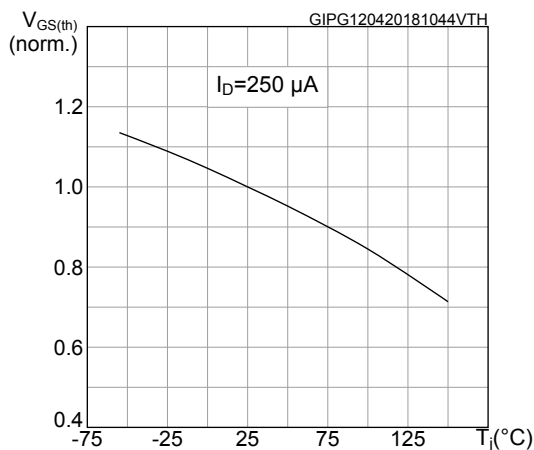
**Figure 3. Typical output characteristics**



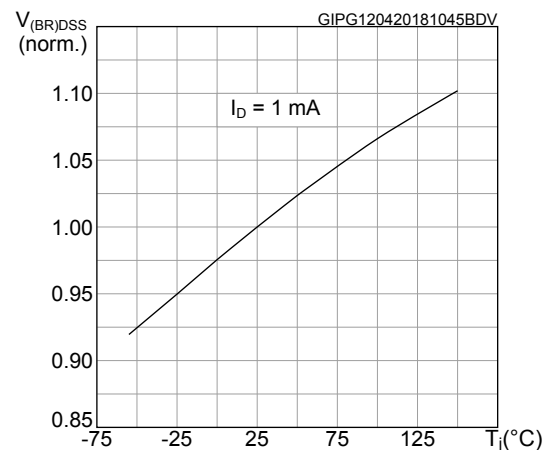
**Figure 4. Typical transfer characteristics**



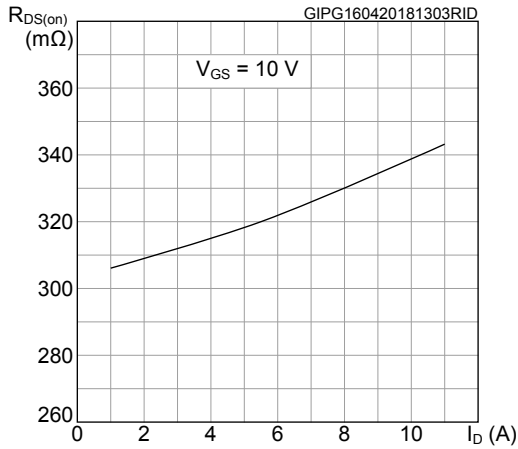
**Figure 5. Normalized gate threshold vs temperature**



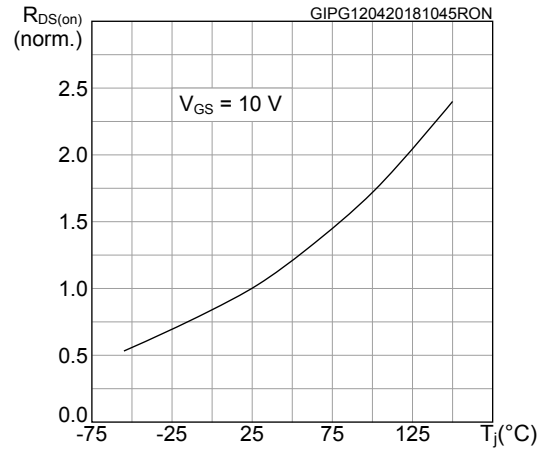
**Figure 6. Normalized breakdown voltage vs temperature**



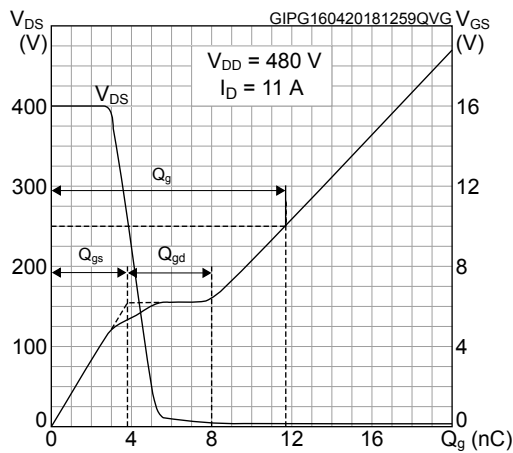
**Figure 7. Typical drain-source on-resistance**



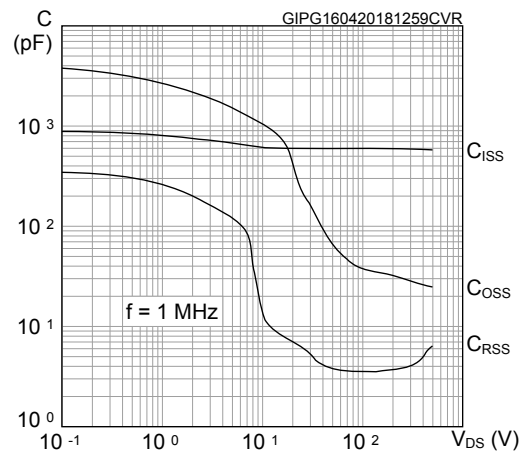
**Figure 8. Normalized on-resistance vs. temperature**



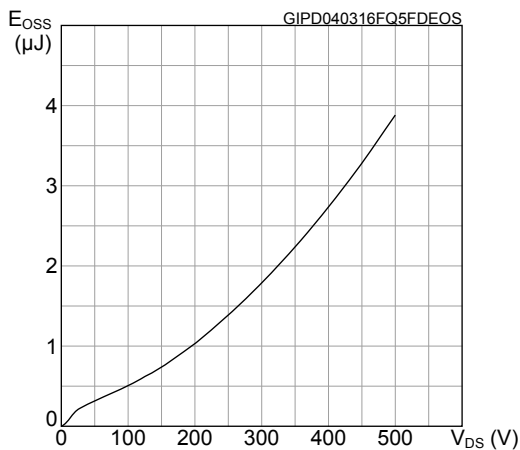
**Figure 9. Typical gate charge characteristics**



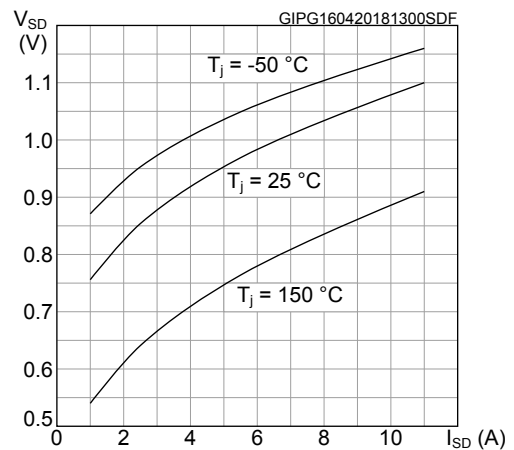
**Figure 10. Typical capacitance characteristics**



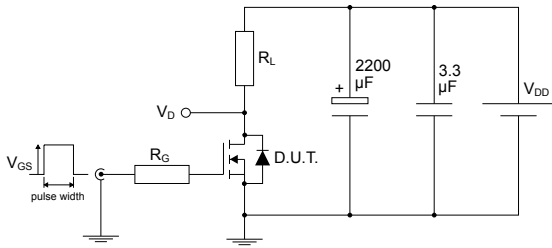
**Figure 11. Typical output capacitance stored energy**



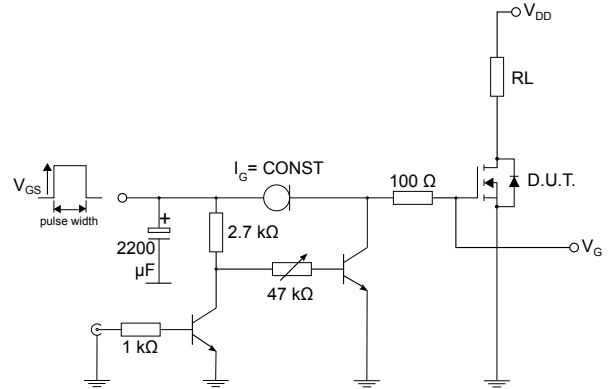
**Figure 12. Typical reverse diode forward characteristics**



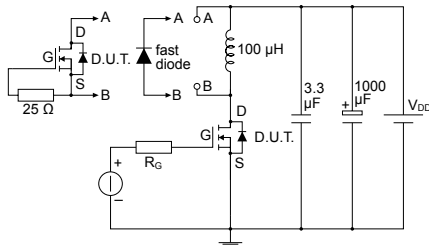
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


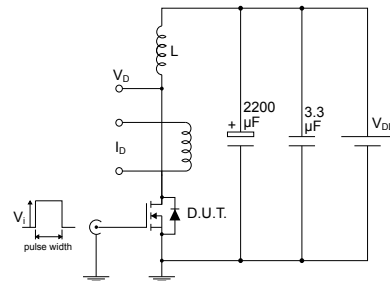
AM01468v1

**Figure 14. Test circuit for gate charge behavior**


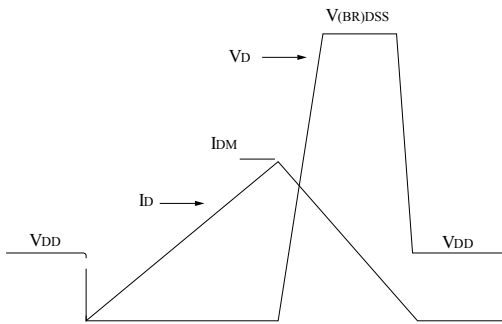
AM01469v10

**Figure 15. Test circuit for inductive load switching and diode recovery times**


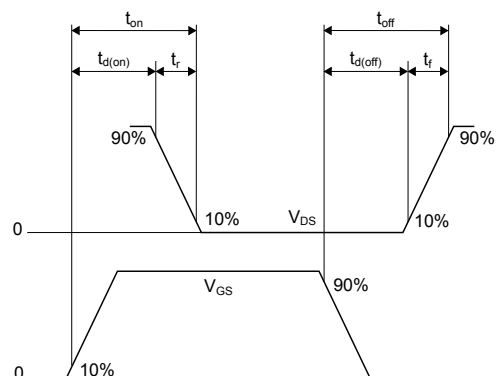
AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

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## 4 Package information

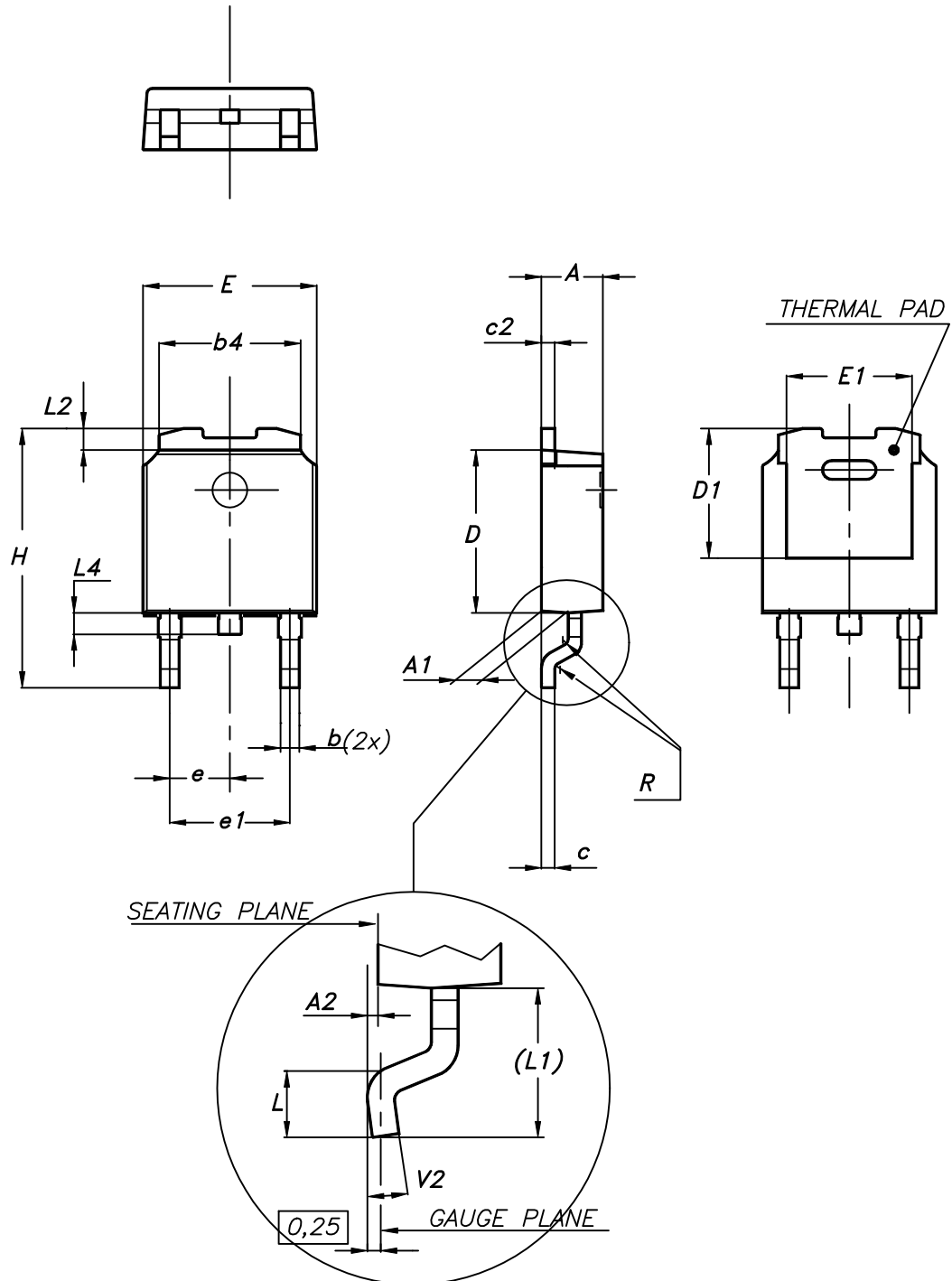
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### 4.1 DPAK (TO-252) type A2 package information

Figure 19. DPAK (TO-252) type A2 package outline

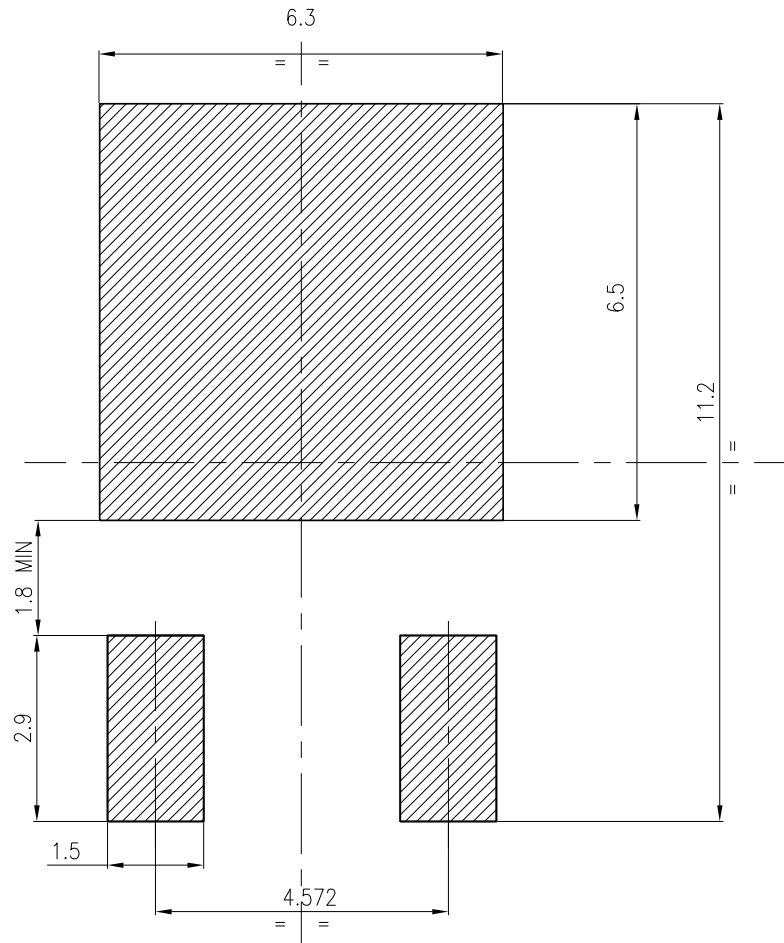


0068772\_type-A2\_rev26

**Table 8. DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

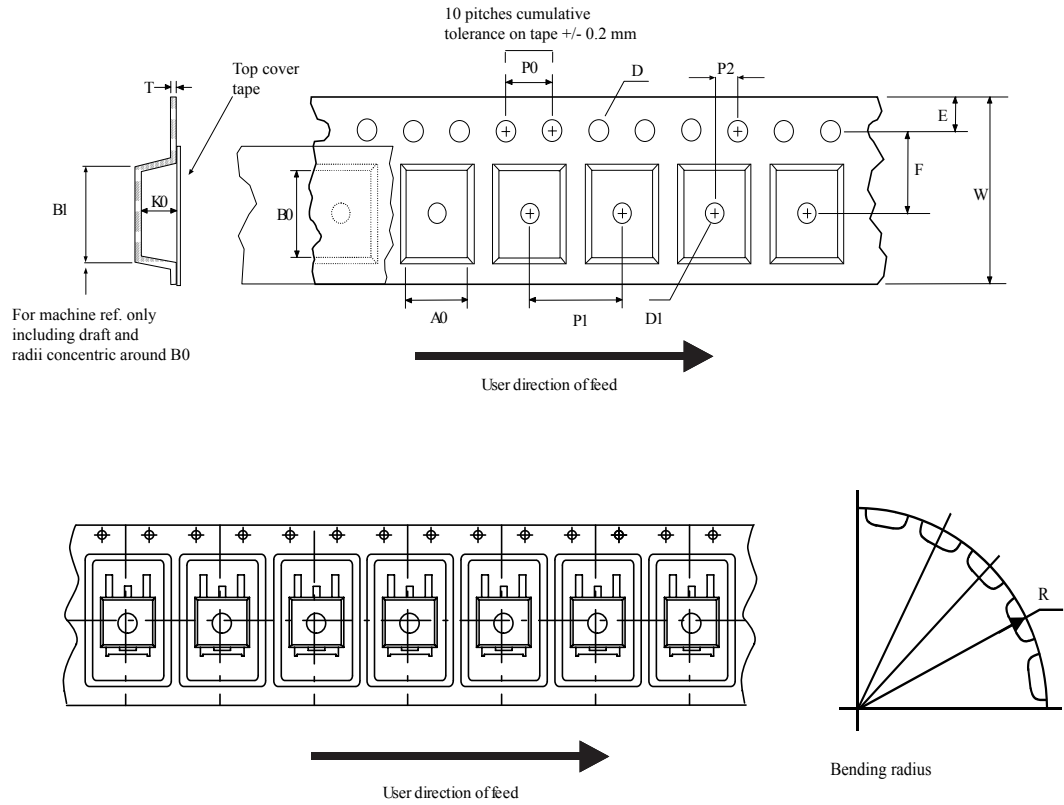
Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)



FP\_0068772\_26

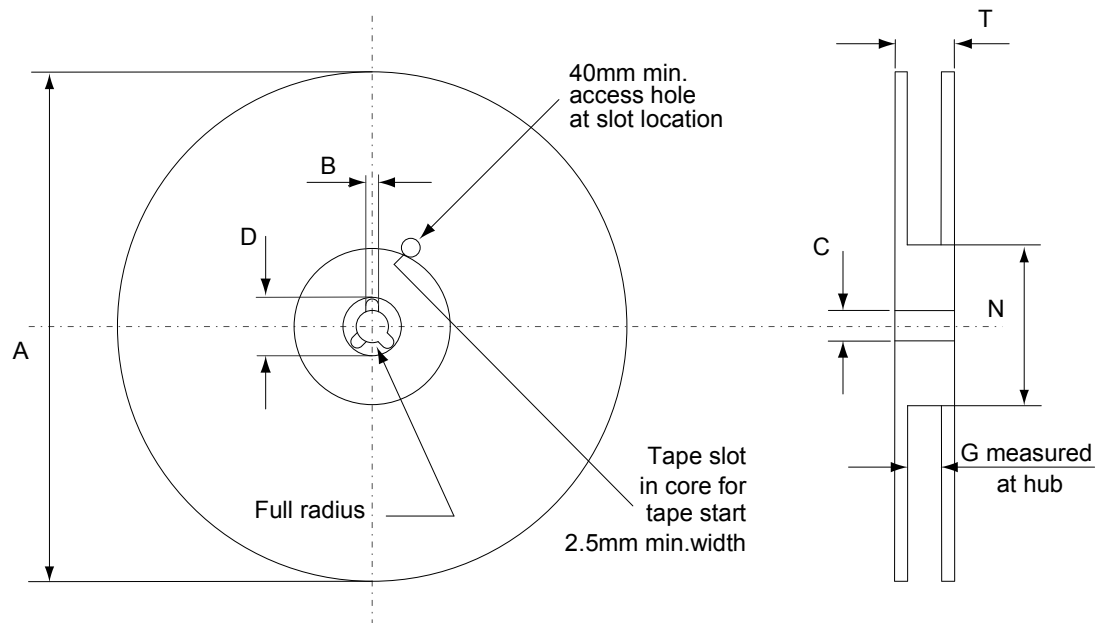
## 4.2 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



AM08852v1

**Figure 22. DPAK (TO-252) reel outline**



AM06038v1

**Table 9. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
23-Jun-2017	1	First release.
16-Apr-2018	2	<p>Removed maturity status indication from cover page. The document status is production data.</p> <p>Modified title, <a href="#">Table 1. Absolute maximum ratings</a>, <a href="#">Table 3. Avalanche characteristics</a>, <a href="#">Table 4. Static</a>, <a href="#">Table 5. Dynamic</a>, <a href="#">Table 6. Switching times</a>, <a href="#">Table 7. Source drain diode</a>.</p> <p>Modified <a href="#">Section 2.1 Electrical characteristics (curves)</a>.</p> <p>Minor text changes.</p>
27-Jun-2018	3	Updated <a href="#">Section 4 Package information</a> .
31-Oct-2019	4	<p>Modified Features table on cover page and <a href="#">Table 4. Static</a>.</p> <p>Updated <a href="#">Section 4.1 DPAK (TO-252) type A2 package information</a>.</p> <p>Minor text changes.</p>

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[SSM6P69NU,LF](#) [DMP22D4UFO-7B](#)