

## N-channel 40 V, 2.5 mΩ typ., 80 A STripFET™ F6 Power MOSFET in a DPAK package

Datasheet - preliminary data

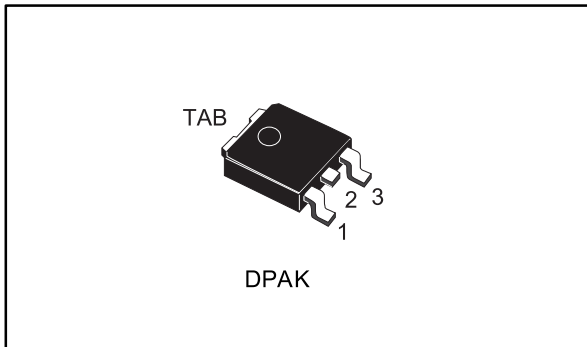


Figure 1: Internal schematic diagram

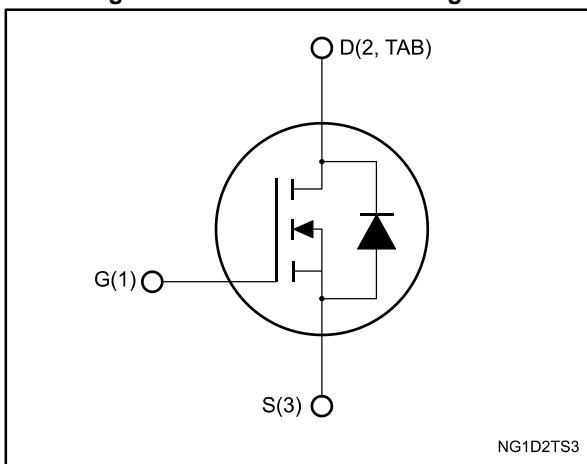


Table 1: Device summary

Order code	Marking	Package	Packing
STD180N4F6	180N4F6	DPAK	Tape and reel

### Features

Order code	V <sub>BS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STD180N4F6	40 V	2.8 mΩ	80 A	130 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications
- Power tools

### Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	80	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	80	
$I_{DM}$	Drain current (pulsed)	320	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	130	W
$T_{stg}$	Storage temperature range	-55 to 175	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

**Notes:**

<sup>(1)</sup> Limited by package

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.15	$^\circ\text{C/W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-pcb	50	

**Notes:**

<sup>(1)</sup> When mounted on FR-4 board of 1 inch<sup>2</sup>, 2 oz Cu.

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 4: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	40			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$ , $T_{\text{case}} = 125\text{ °C}$			100	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 40\text{ A}$		2.5	2.8	m $\Omega$

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	7735	-	pF
$C_{oss}$	Output capacitance		-	745	-	
$C_{rss}$	Reverse transfer capacitance		-	560	-	
$Q_g$	Total gate charge	$V_{DD} = 20\text{ V}$ , $I_D = 80\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	130	-	nC
$Q_{gs}$	Gate-source charge		-	36	-	
$Q_{gd}$	Gate-drain charge		-	42	-	

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$ , $I_D = 40\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	24	-	ns
$t_r$	Rise time		-	150	-	
$t_{d(off)}$	Turn-off delay time		-	106	-	
$t_f$	Fall time		-	57	-	

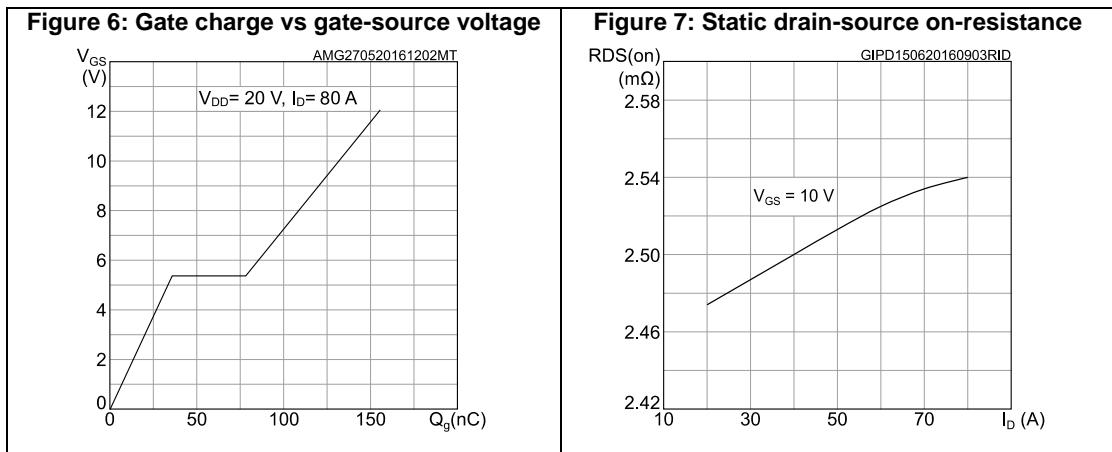
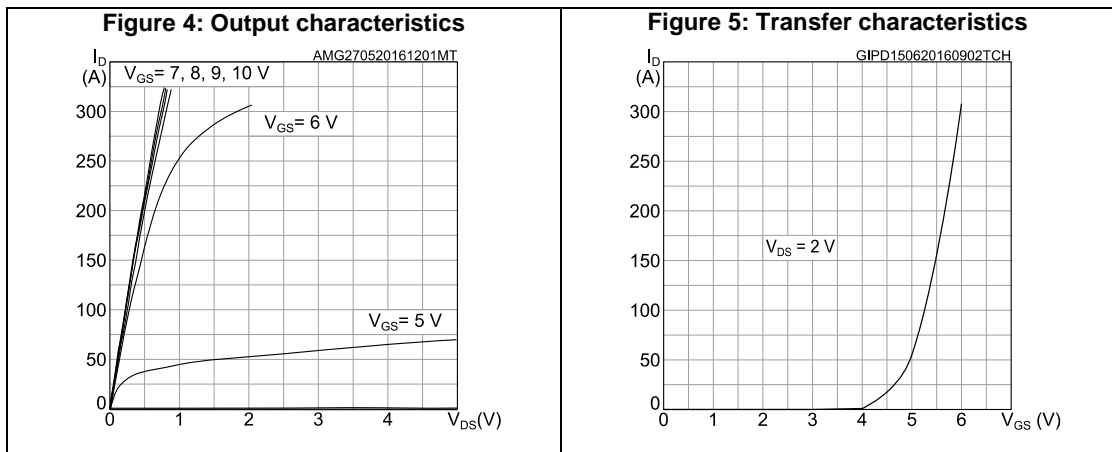
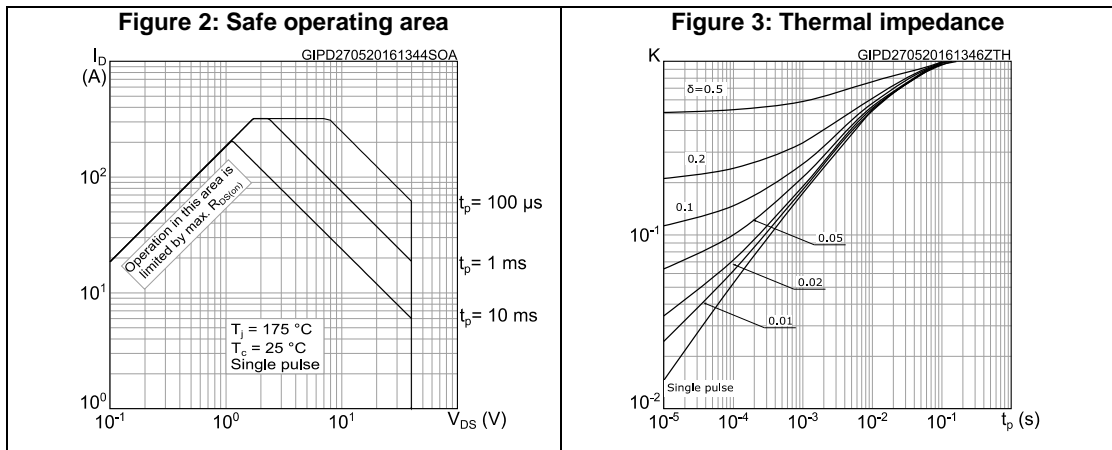
Table 7: Source-drain diode

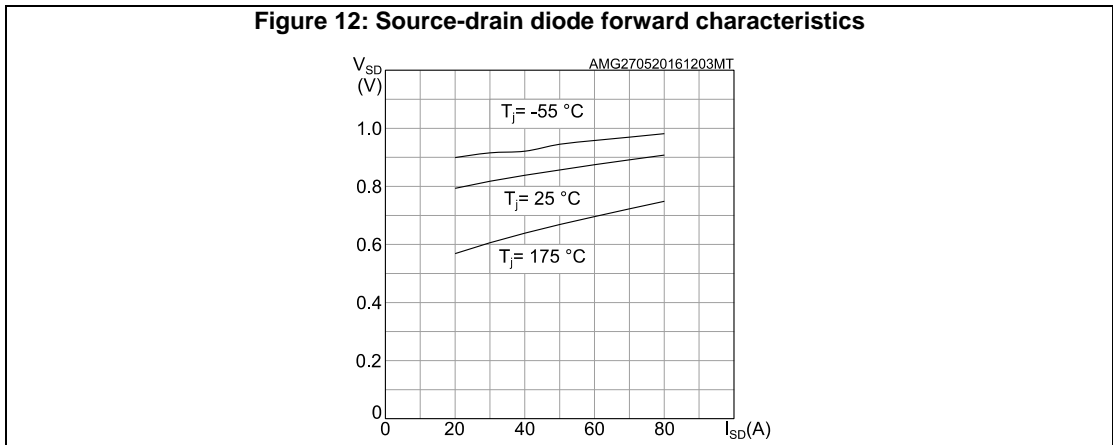
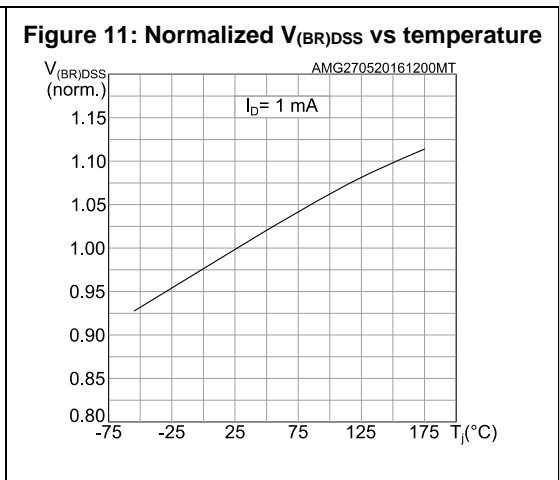
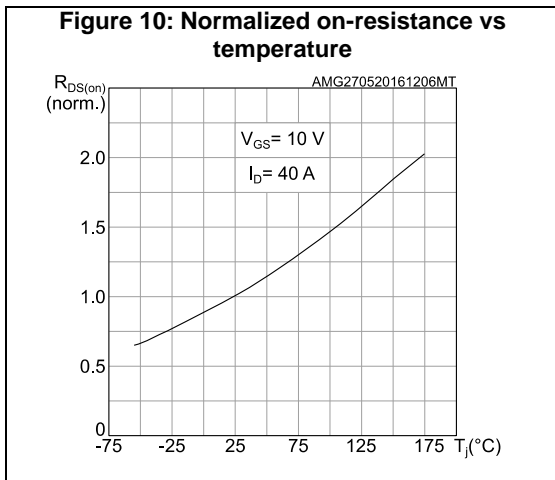
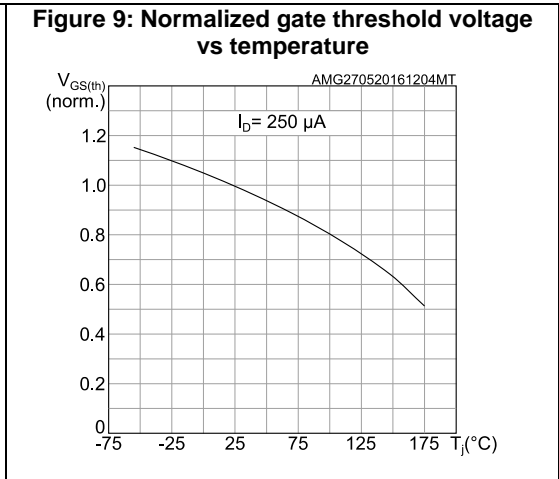
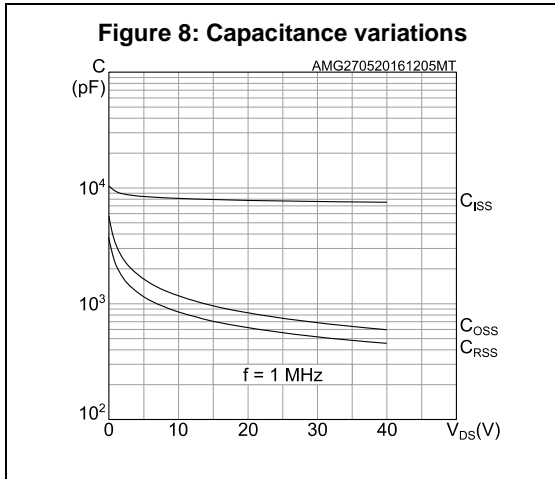
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 80 \text{ A}$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 80 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 32 \text{ V}$ , $T_j = 25 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	36		ns
$Q_{rr}$	Reverse recovery charge		-	40		nC
$I_{RRM}$	Reverse recovery current		-	2.3		A

**Notes:**

(1) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

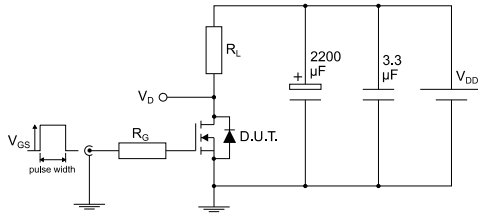
## 2.1 Electrical characteristics (curves)





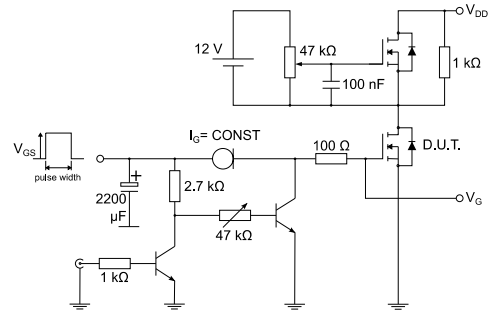
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



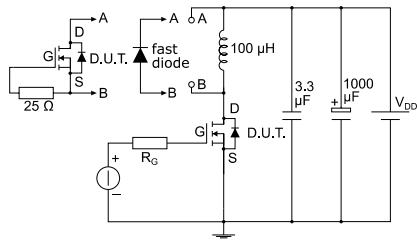
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**Figure 14: Test circuit for gate charge behavior**



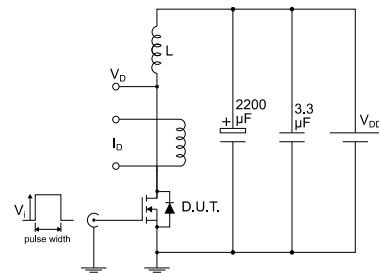
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



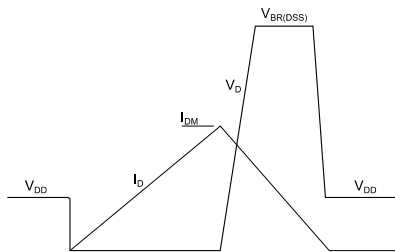
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**Figure 16: Unclamped inductive load test circuit**



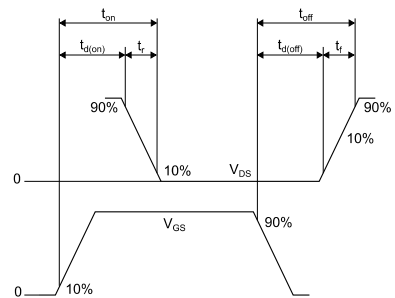
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**Figure 17: Unclamped inductive waveform**



AM01472v1

**Figure 18: Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 DPAK package information

Figure 19: DPAK (TO-252) type A2 package outline

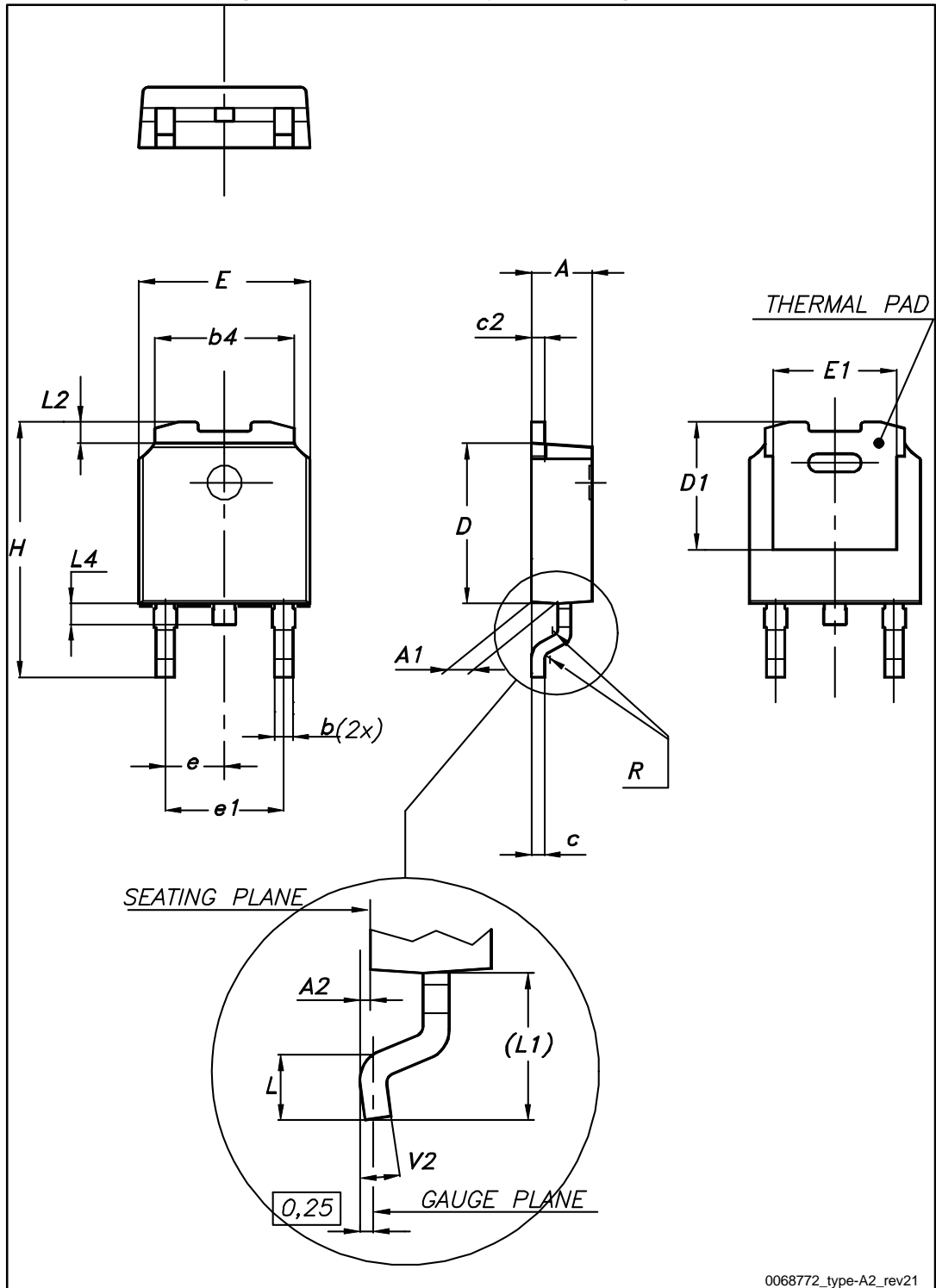
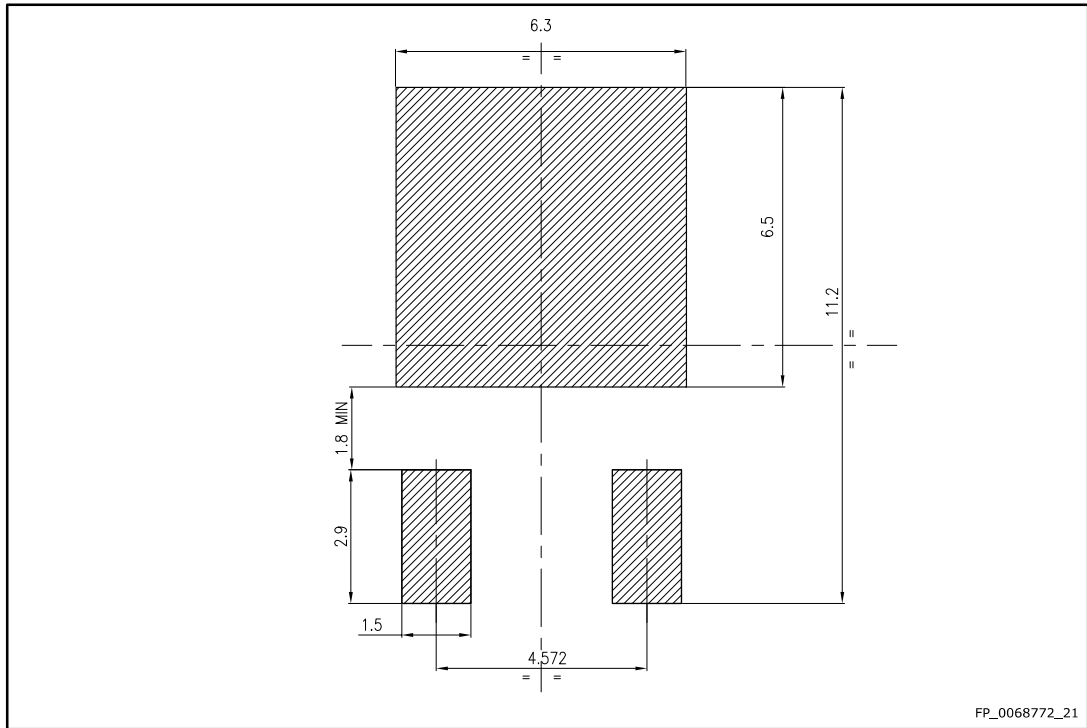


Table 8: DPAK (TO-252) type A2 mechanical data

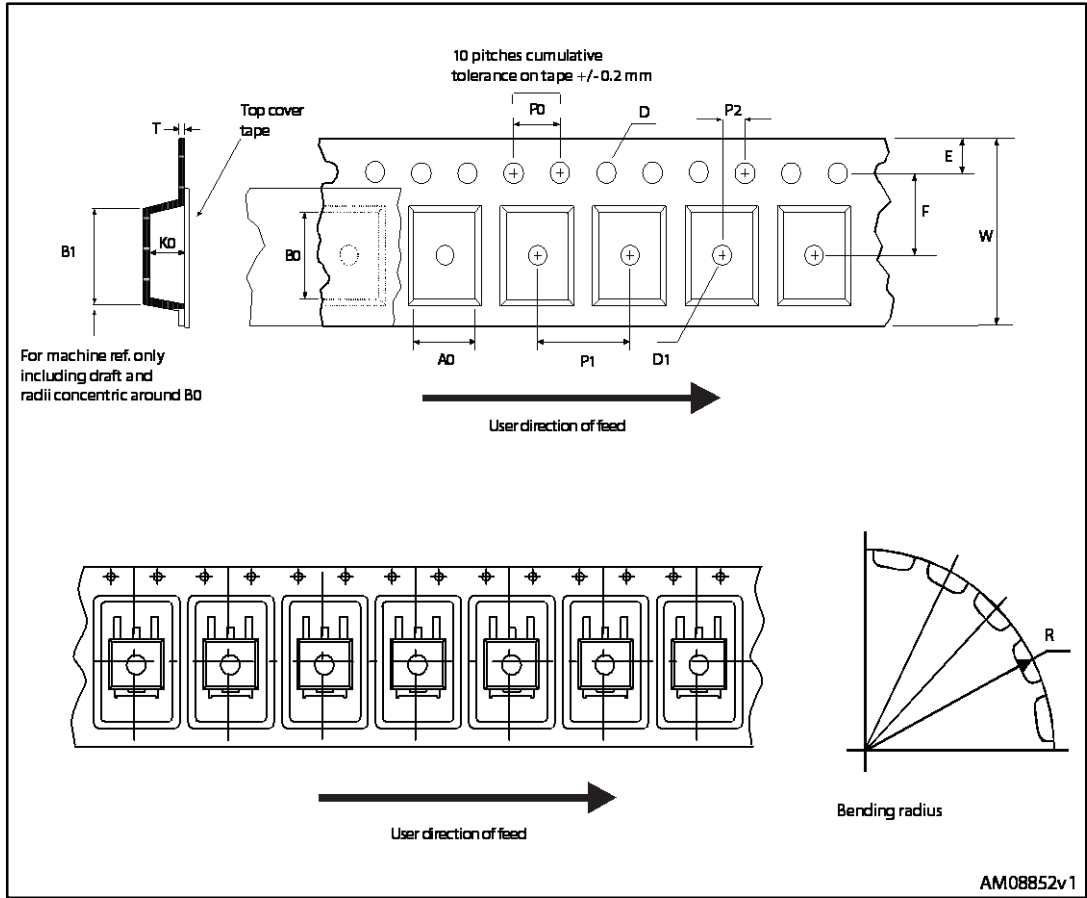
Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20: DPAK (TO-252) recommended footprint (dimensions are in mm)



### 4.2 DPAK packing information

Figure 21: DPAK (TO-252) tape outline



AM08852v1

Figure 22: DPAK (TO-252) reel outline

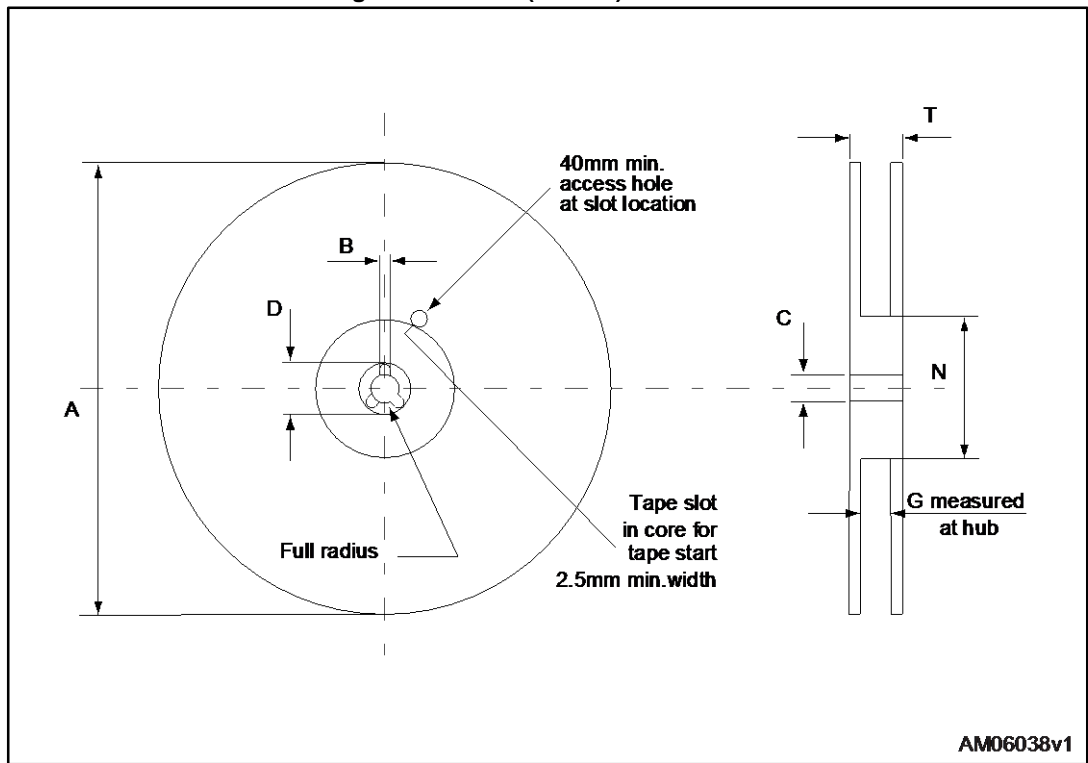


Table 9: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 5 Revision history

**Table 10: Document revision history**

Date	Revision	Changes
10-Nov-2015	1	First release.
26-Jul-2016	2	Updated title in cover page. Updated $R_{DS(on) \max}$ value in Features. Updated <a href="#">Table 4: "Static"</a> and <a href="#">Table 5: "Dynamic"</a> . Added <a href="#">Section 2.1: "Electrical characteristics (curves)"</a> and <a href="#">Section 4.2: "DPAK packing information"</a> . Minor text changes.

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