

Automotive-grade N-channel 30 V, 25 mΩ typ., 10 A STripFET™ H6 Power MOSFET in a DPAK package

Datasheet - production data

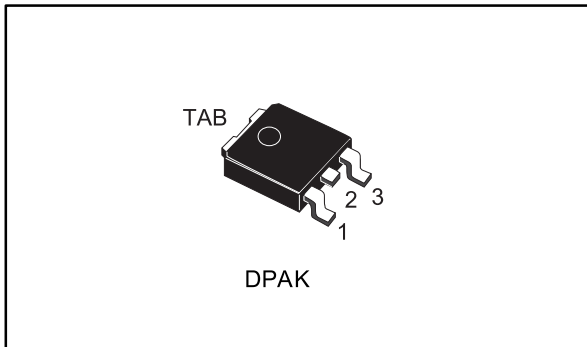
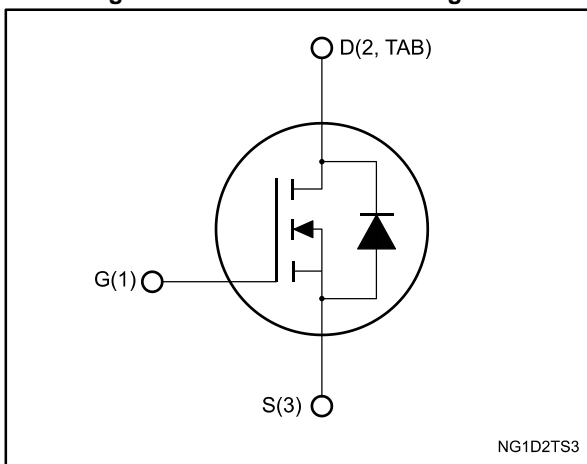


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STD19N3LLH6AG	30 V	33 mΩ	10 A	30 W

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Logic level

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STD19N3LLH6AG	19N3LLH6	DPAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ °C}$ ⁽¹⁾	10	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	10	
I_{DM} ⁽²⁾	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ °C}$	30	W
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Operating junction temperature		

Notes:

⁽¹⁾ Current limited by package. At $T_{case} = 25\text{ °C}$ the silicon is able to sustain 22 A.

⁽²⁾ Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	5	°C/W
$R_{thj-pcb}$ ⁽¹⁾	Thermal resistance junction-pcb	50	

Notes:

⁽¹⁾When mounted on a 1-inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV} ⁽¹⁾	Avalanche current, repetitive or not repetitive	10	A
E_{AS} ⁽²⁾	Single pulse avalanche energy	130	mJ

Notes:

⁽¹⁾ Pulse width limited by T_{jmax} .

⁽²⁾ starting $T_j = 25\text{ °C}$, $I_D = I_{AV}$, $V_{DD} = 25\text{ V}$.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 30\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 30\text{ V}$, $T_{\text{case}} = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 20\text{ V}$			± 100	nA
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 5\text{ A}$		25	33	m Ω
		$V_{\text{GS}} = 4.5\text{ V}$, $I_{\text{D}} = 5\text{ A}$		33	50	

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	321	-	pF
C_{oss}	Output capacitance		-	68	-	
C_{riss}	Reverse transfer capacitance		-	34	-	
Q_{g}	Total gate charge	$V_{\text{DD}} = 15\text{ V}$, $I_{\text{D}} = 10\text{ A}$, $V_{\text{GS}} = 4.5\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	3.7	-	nC
Q_{gs}	Gate-source charge		-	1	-	
Q_{gd}	Gate-drain charge		-	1.7	-	

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d}(\text{on})}$	Turn-on delay time	$V_{\text{DD}} = 15\text{ V}$, $I_{\text{D}} = 5\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	2.4	-	ns
t_{r}	Rise time		-	2.5	-	
$t_{\text{d}(\text{off})}$	Turn-off delay time		-	12.8	-	
t_{f}	Fall time		-	2.5	-	

Table 8: Source-drain diode

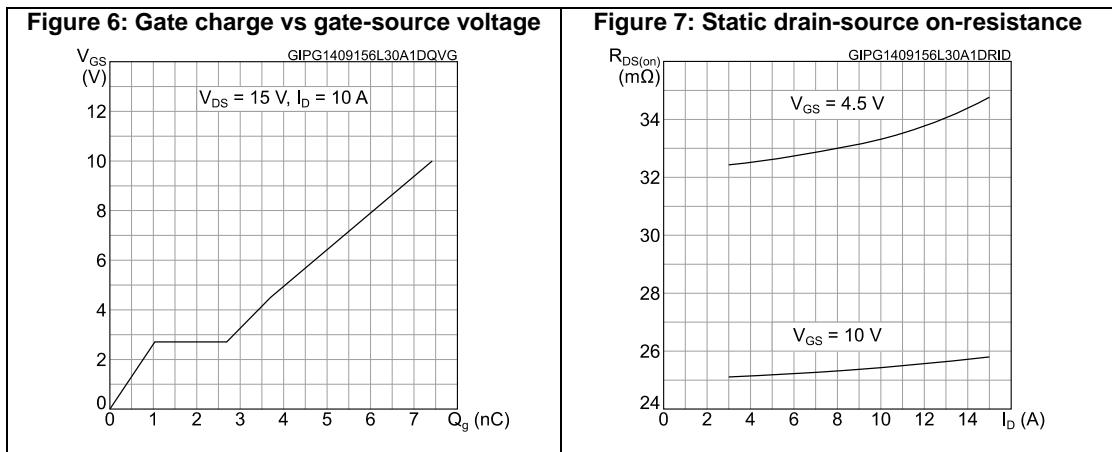
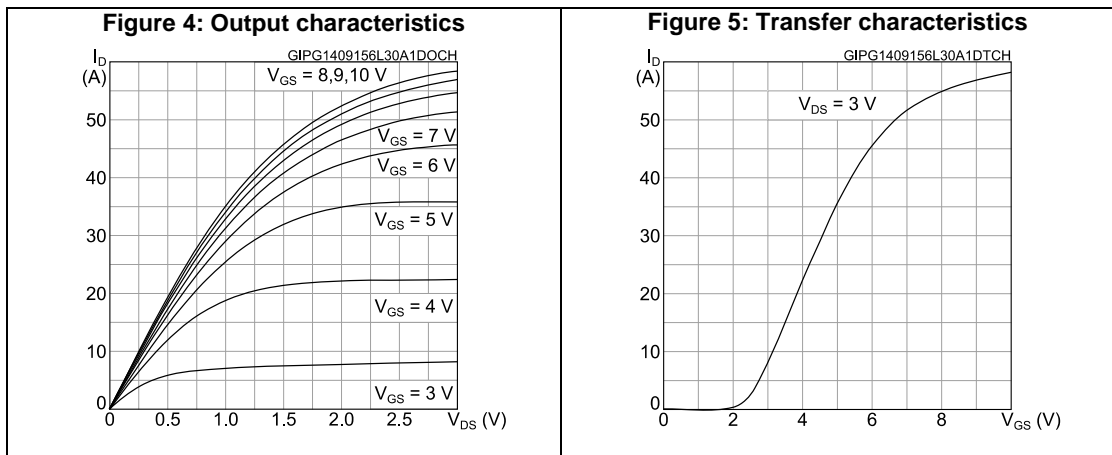
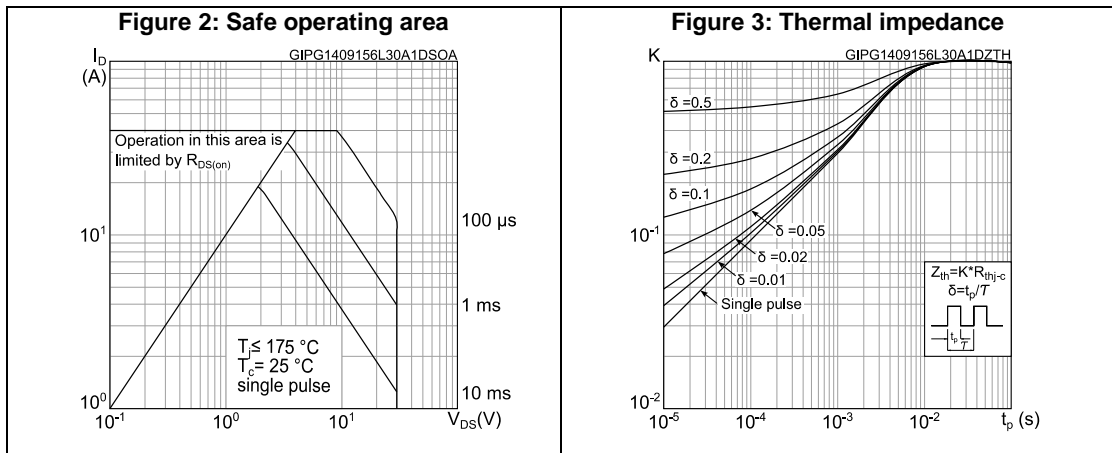
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		40	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 10\text{ A}$	-		1.12	V
t_{rr}	Reverse recovery time	$I_{SD} = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 24\text{ V}$ (see Figure 15 : "Test circuit for inductive load switching and diode recovery times")	-	15.1		ns
Q_{rr}	Reverse recovery charge		-	7.5		nC
I_{RRM}	Reverse recovery current		-	1		A

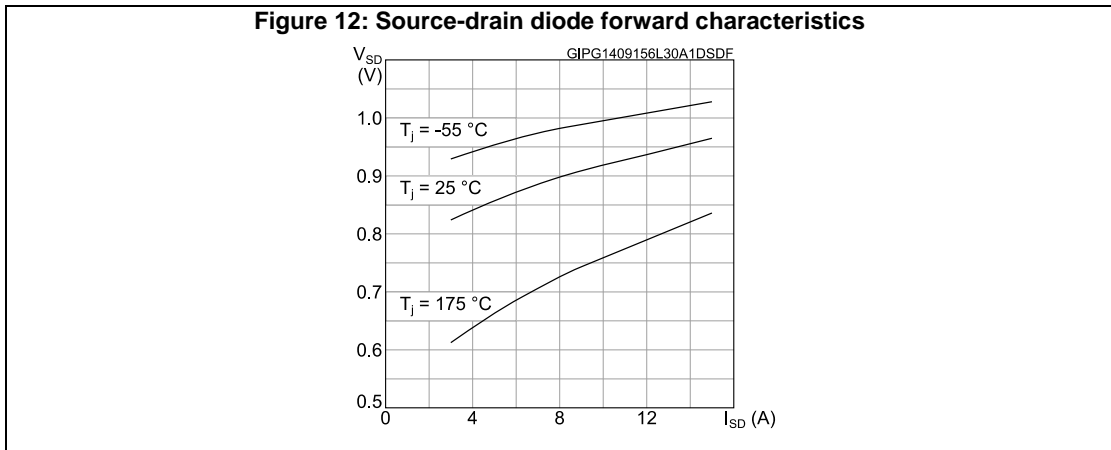
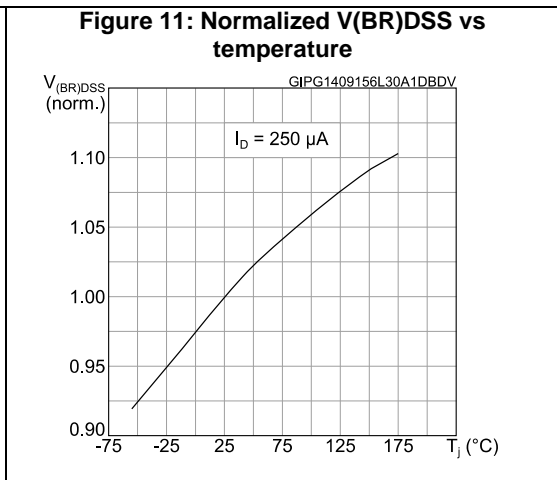
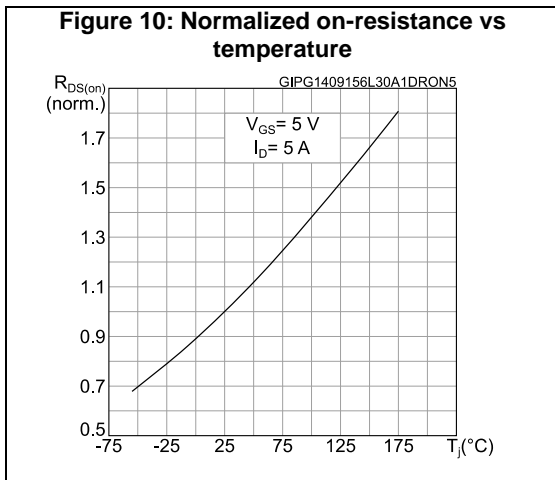
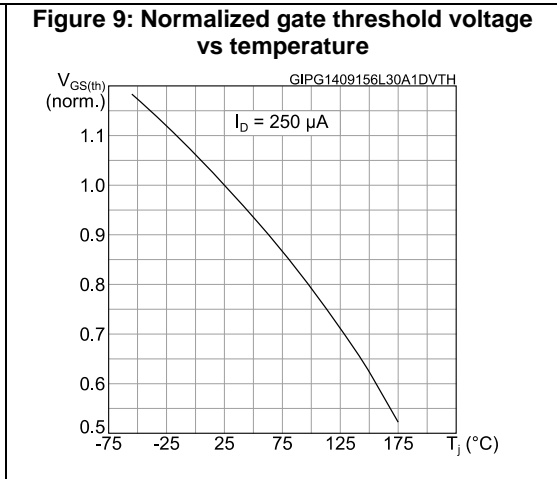
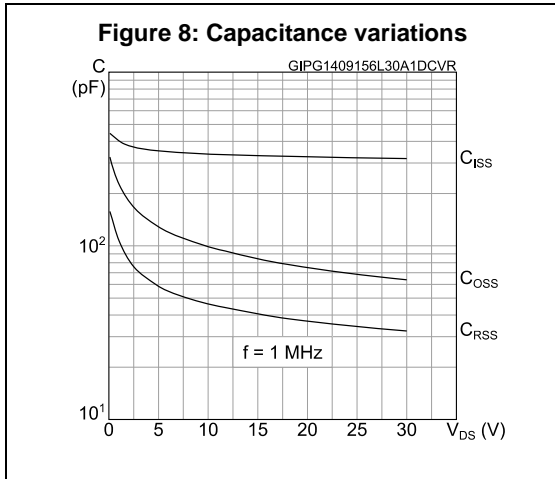
Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)





3 Test circuits

Figure 13: Test circuit for resistive load switching times



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Figure 14: Test circuit for gate charge behavior



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Figure 15: Test circuit for inductive load switching and diode recovery times



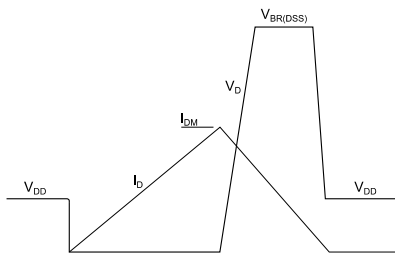
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Figure 16: Unclamped inductive load test circuit



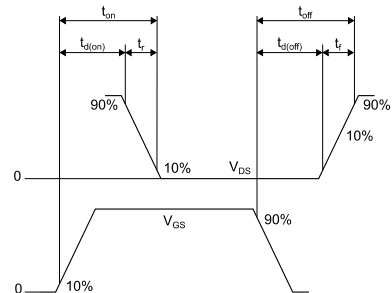
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Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 19: DPAK (TO-252) type A package outline

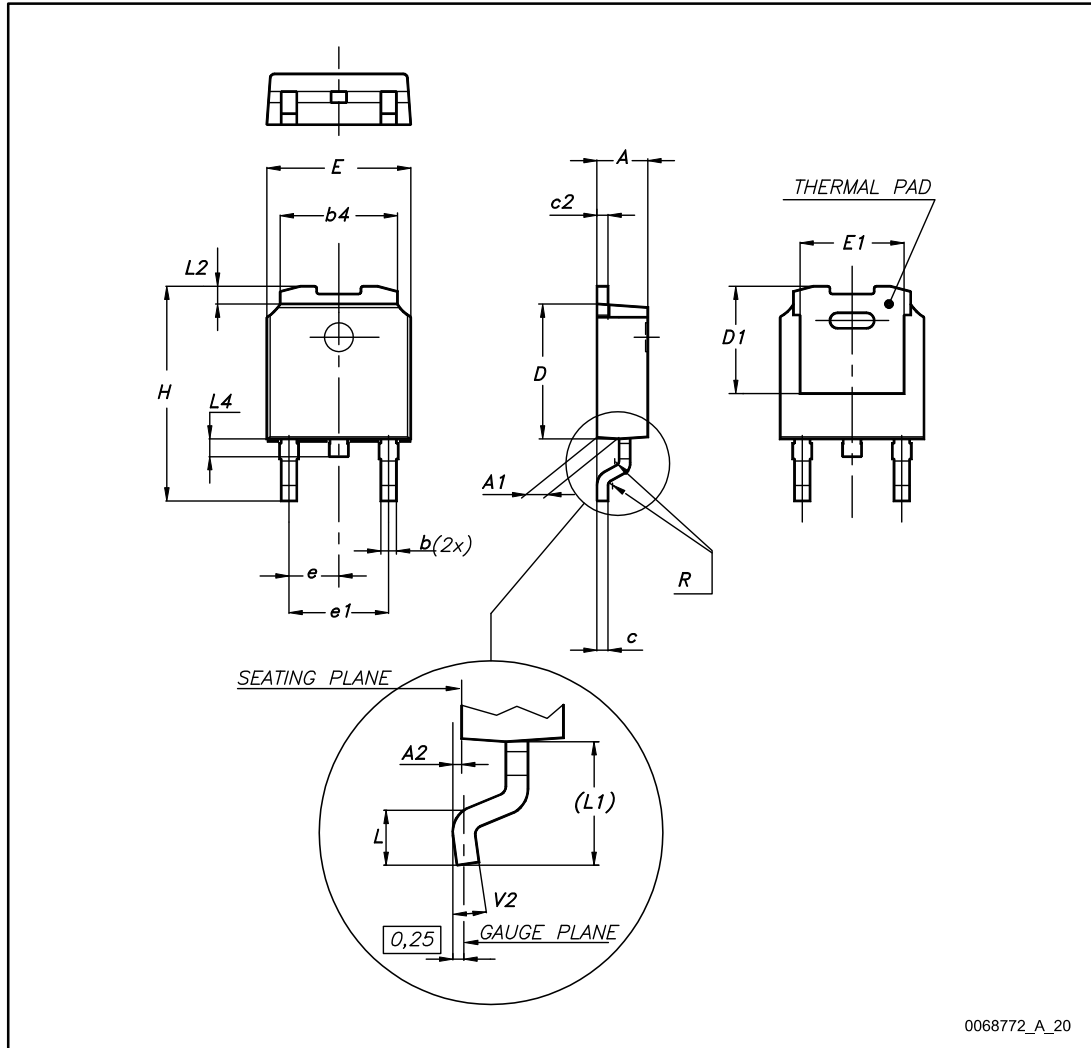
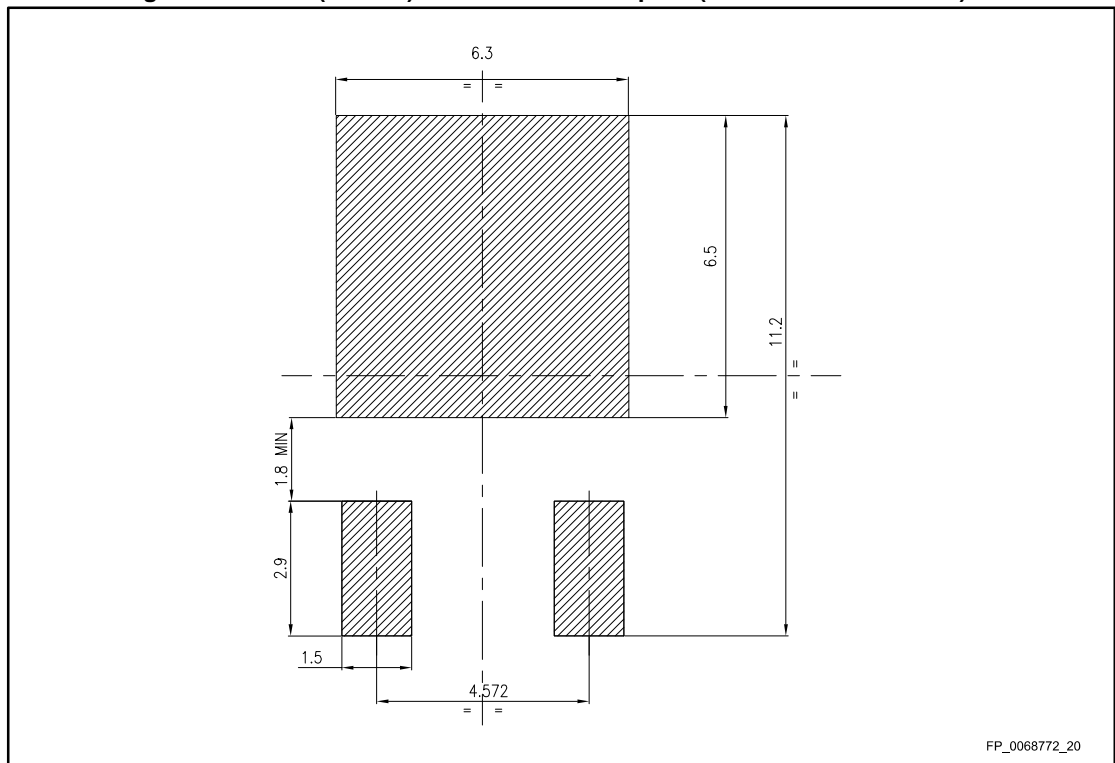


Table 9: DPAK (TO-252) type A mechanical data

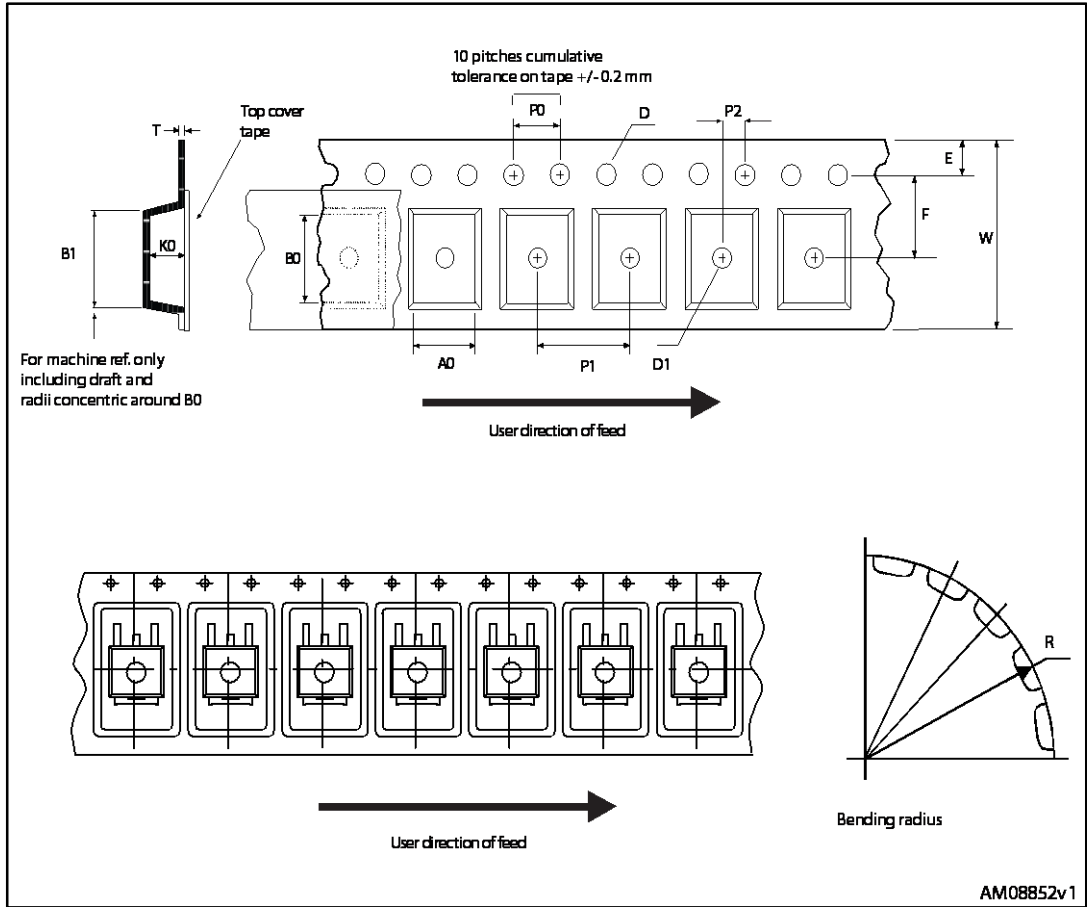
Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) packing information

Figure 21: DPAK (TO-252) tape outline



5 Revision history

Table 11: Document revision history

Date	Revision	Changes
01-Oct-2015	1	Initial version
13-Oct-2015	2	On cover page: - updated title In section Electrical characteristics: - updated table Dynamic Updated section Test circuits

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