STD1NK60-1

N-channel 600 V, 7.3 Ω typ., 1 A SuperMESH™ Power MOSFET in an IPAK package

Datasheet - production data

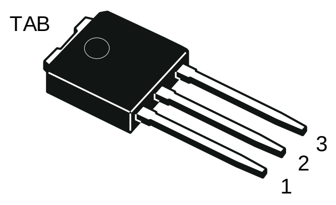
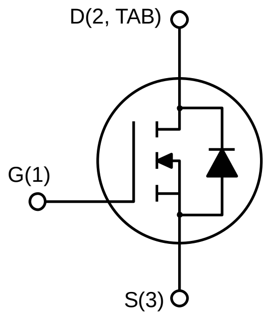


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD1NK60-1	600 V	8.5 Ω	1 A	30 W

- Extremely high dv/dt capability
- ESD improved capability
- 100% avalanche tested
- Gate charge minimized

Applications

- Low power battery chargers
- Swith mode low power supplies (SMPS)
- Low power, ballast, CFL (compact fluorescent lamps)

Description

This high voltage device is an N-channel Power MOSFET developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1: Device summary

Order code	Marking	Package	Packing
STD1NK60-1	D1NK60	IPAK	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	600	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	1.0	A
I_D	Drain current (continuous) at T_C = 100 °C	0.63	A
I_{DM} (1)	Drain current (pulsed)	4	A
P_{TOT}	Total dissipation at T_C = 25 °C	30	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_{jmax})	1	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	25	mJ
dv/dt (2)	Peak diode recovery voltage slope	3	V/ns
T_j	Operating junction temperature range	- 55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

(1) Pulse width limited by safe operating area.

(2) I_{SD} ≤ 1.0 A, di/dt ≤ 100 A/μs; V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ T_{JMAX}

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	4.2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	100	°C/W

2 Electrical characteristics

T_C = 25 ° C unless otherwise specified

Table 4: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V T_C = 125 °C (1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS}=0 V, V_{GS}= ±30 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.25	3	3.7	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 0.5 A		7.3	8.5	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	156	-	pF
C_{oss}	Output capacitance		-	23.5	-	pF
C_{rss}	Reverse transfer capacitance		-	3.8	-	pF
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 1 A V_{GS}= 0 to 10 V (see *Figure 16: "Test circuit for gate charge behavior"*)	-	7	-	nC
Q_{gs}	Gate-source charge		-	1.1	-	nC
Q_{gd}	Gate-drain charge		-	3.7	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 300 V, I_D = 0.5 A, R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 15: "Test circuit for resistive load switching times"* and *Figure 20: "Switching time waveform"*)	-	6.5	-	ns
t_r	Rise time		-	5	-	ns
$t_{d(off)}$	Turn-off delay time		-	19	-	ns
t_f	Fall time		-	25	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		1	A
I_{SDM}(1)	Source-drain current (pulsed)		-		4	A
V_{SD}(2)	Forward on voltage	I_{SD} = 1.0 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 1.0 A, di/dt = 100 A/µs, V_{DD} = 25 V (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	140		ns
Q_{rr}	Reverse recovery charge		-	240		nC
I_{RRM}	Reverse recovery current		-	3.3		A
t_{rr}	Reverse recovery time	I_{SD} = 1.0 A, di/dt = 100 A/µs, V_{DD} = 25 V, T_j = 150 °C (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	229		ns
Q_{rr}	Reverse recovery charge		-	377		nC
I_{RRM}	Reverse recovery current		-	3.3		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µ s, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

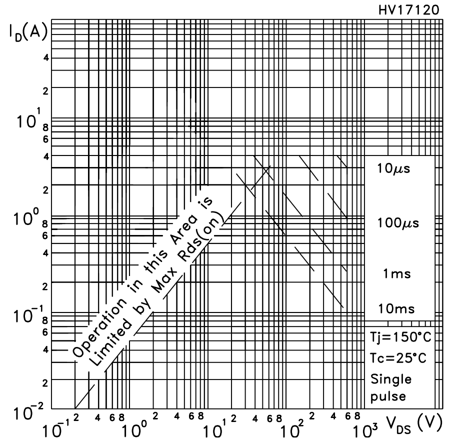


Figure 3: Thermal impedance

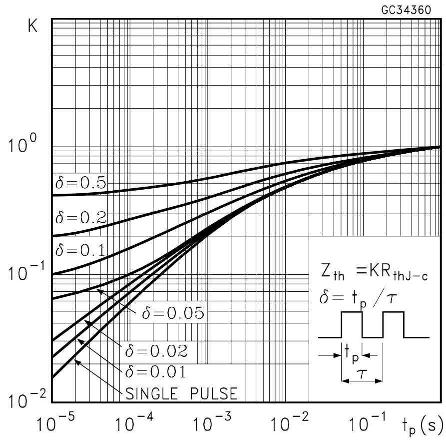


Figure 4: Output characteristics

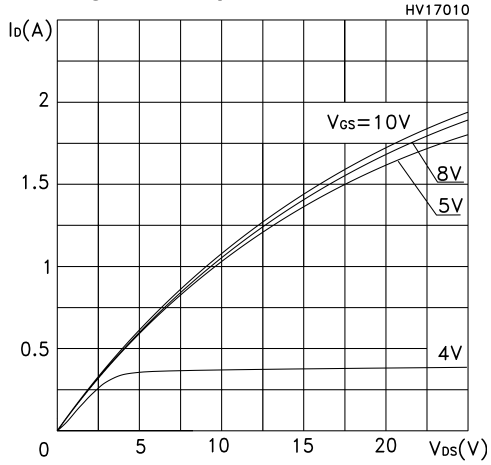


Figure 5: Transfer characteristics

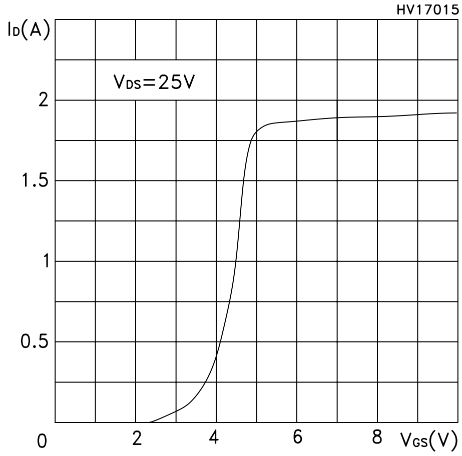


Figure 6: Gate charge vs gate-source voltage

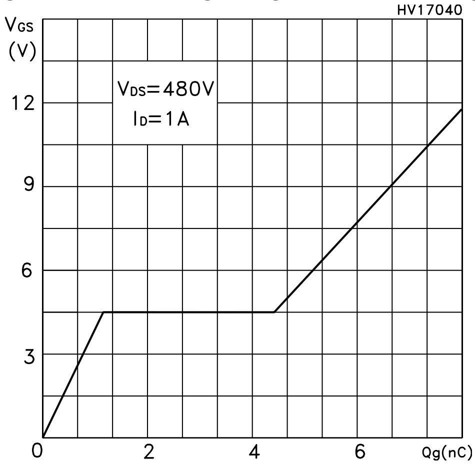


Figure 7: Capacitance variations

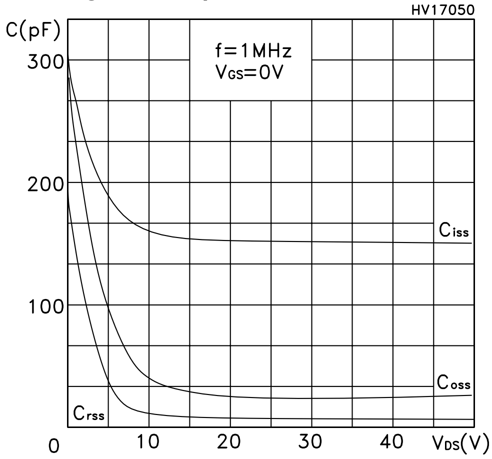


Figure 8: Static drain-source on-resistance

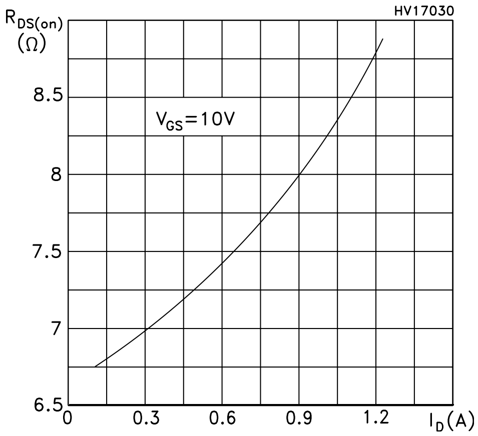


Figure 9: Normalized gate threshold voltage vs temperature

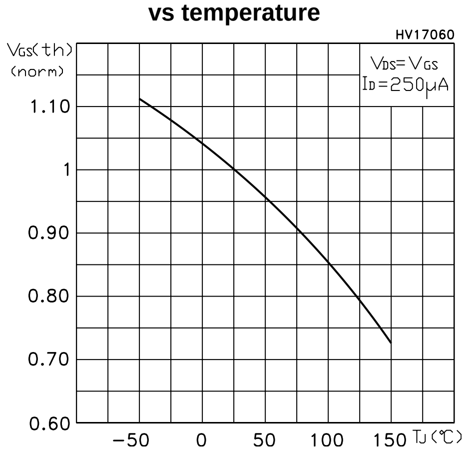


Figure 10: Normalized on-resistance vs temperature

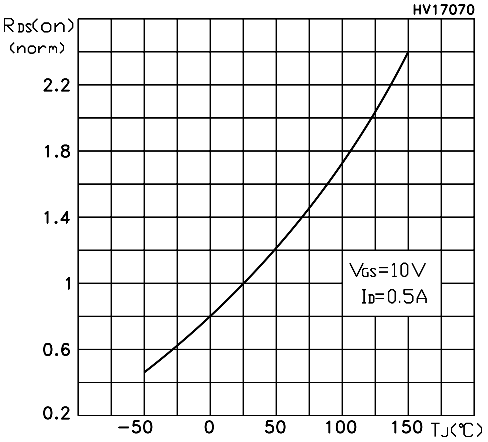


Figure 11: Source-drain forward characteristics

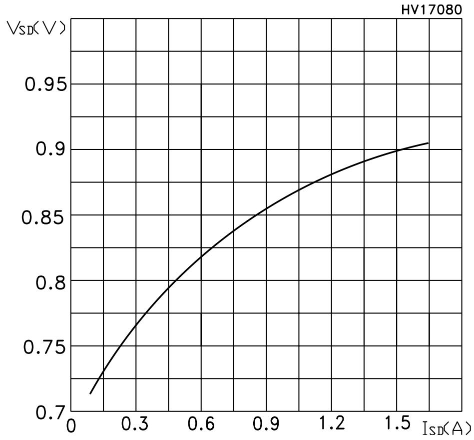


Figure 12: Normalized $V_{(BR)DSS}$ vs temperature

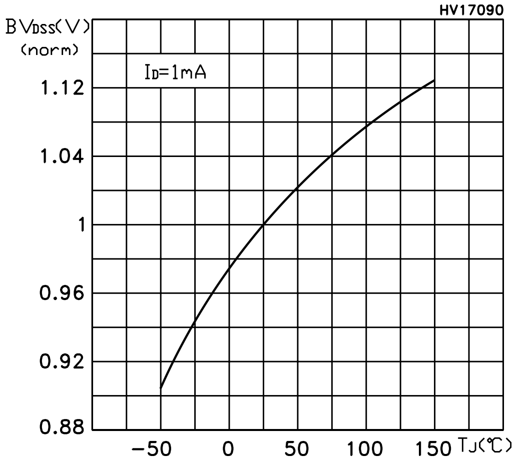


Figure 13: Maximum avalanche energy vs temperature

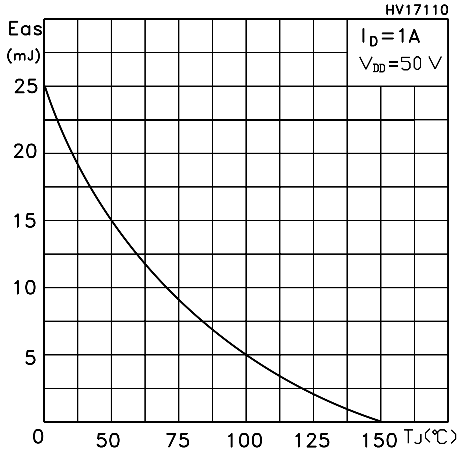
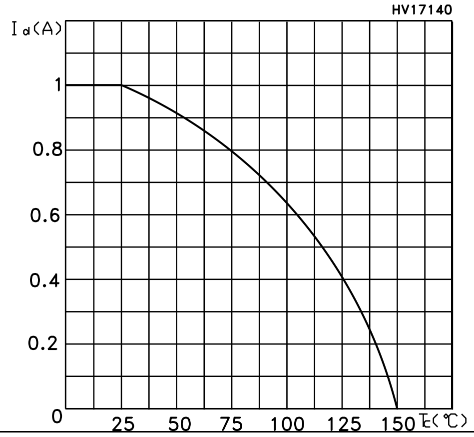


Figure 14: Maximum Id current vs T_c



3 Test circuits

Figure 15: Test circuit for resistive load switching times

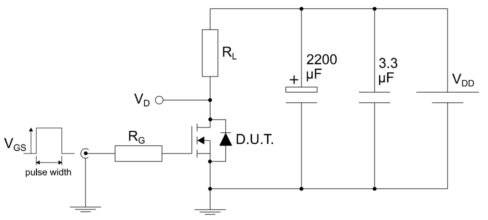


Figure 16: Test circuit for gate charge behavior

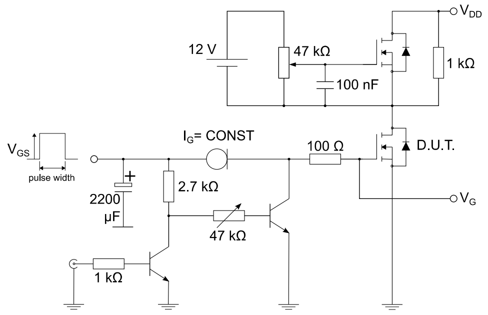


Figure 17: Test circuit for inductive load switching and diode recovery times

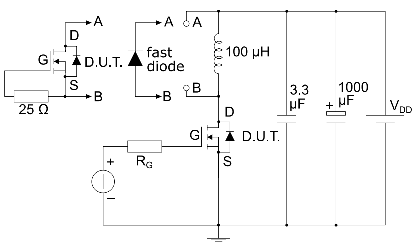


Figure 18: Unclamped inductive load test circuit

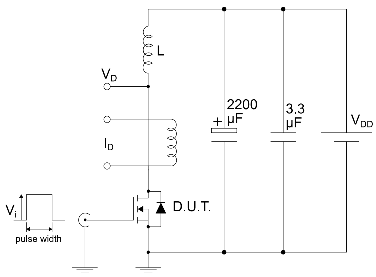


Figure 19: Unclamped inductive waveform

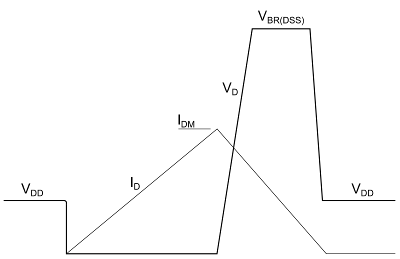
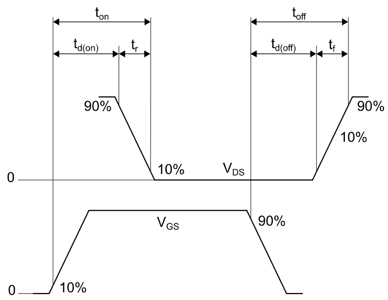


Figure 20: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 IPAK (TO-251) type A package information

Figure 21: IPAK (TO-251) type A package outline

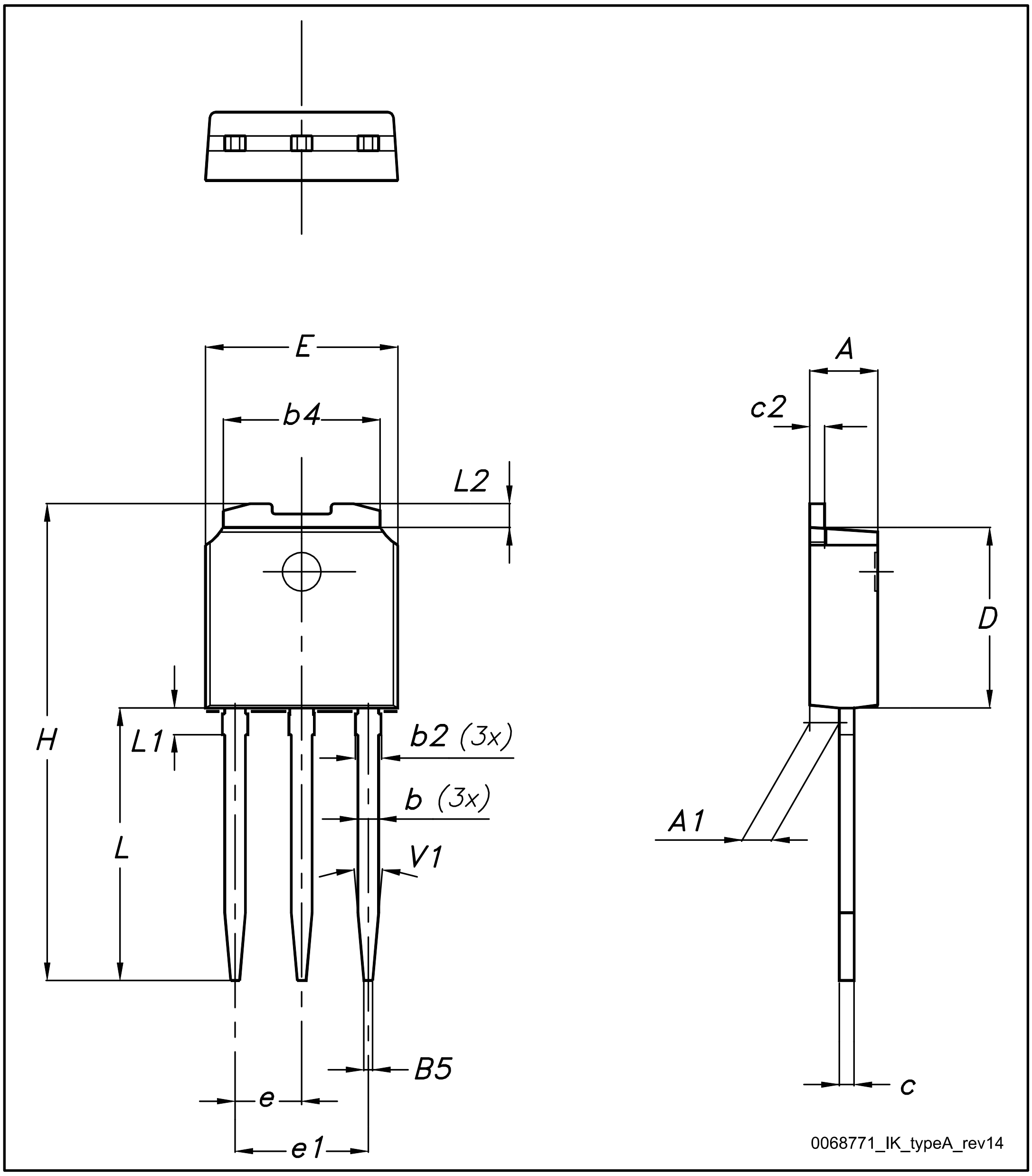


Table 8: IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.2 IPAK (TO-251) type C package information

Figure 22: IPAK (TO-251) type C package outline

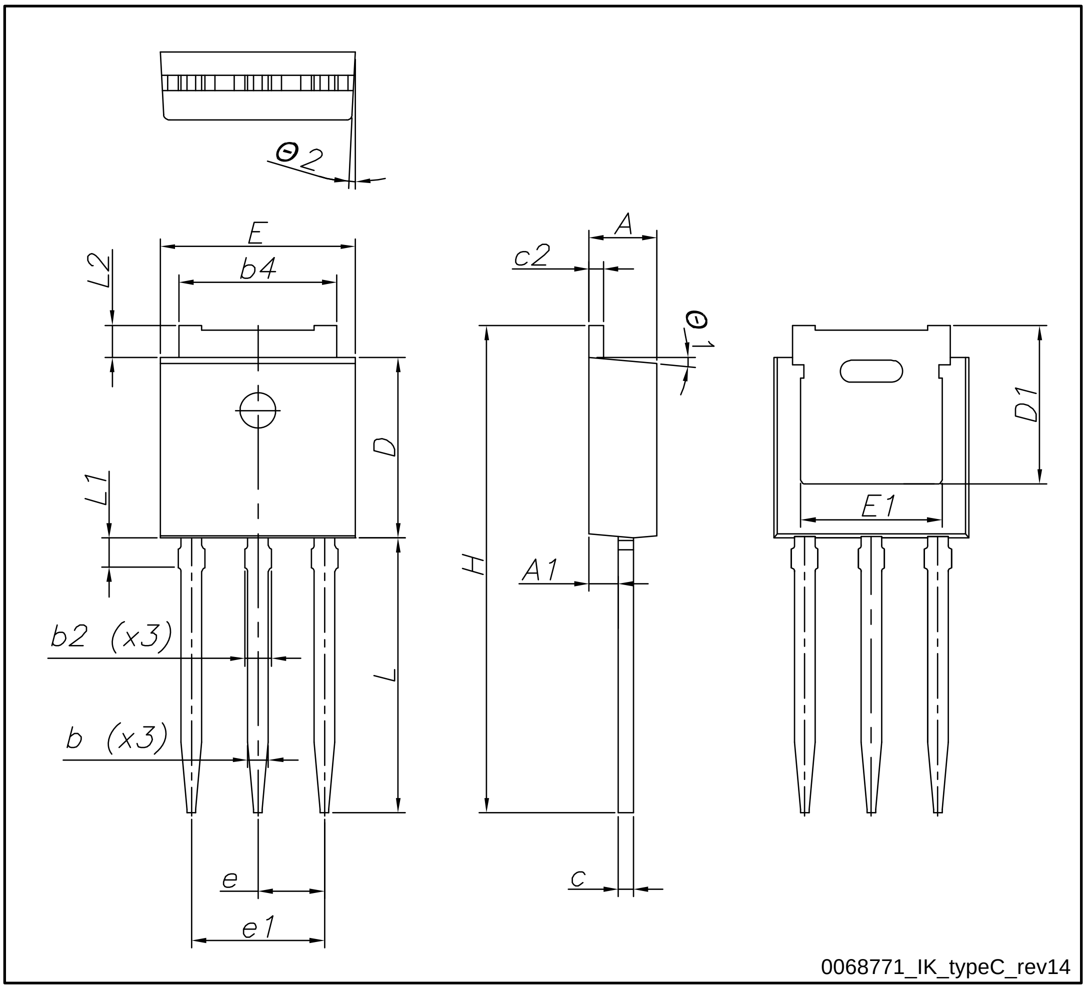


Table 9: IPAK (TO-251) type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.90	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
09-Feb-2017	1	First release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY