

## N-channel 600 V, 7.3 $\Omega$ typ., 1 A SuperMESH™ Power MOSFET in a DPAK package

Datasheet - production data

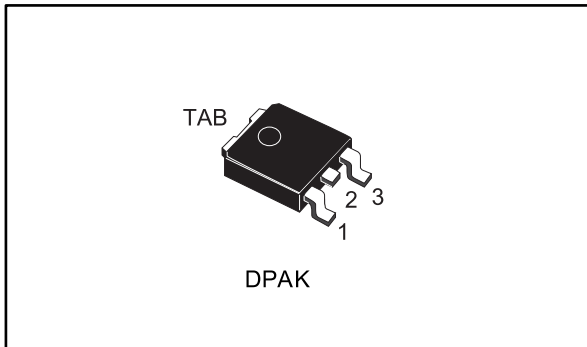
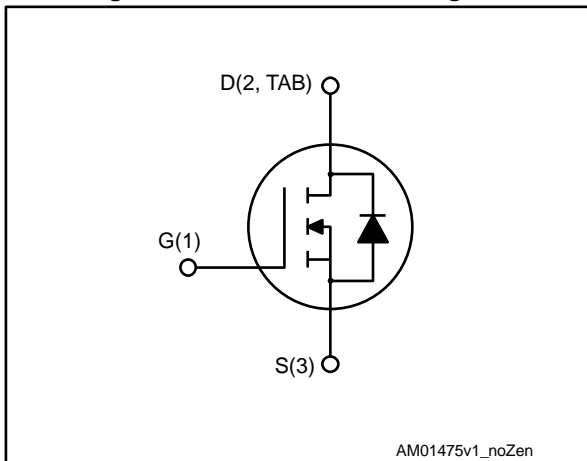


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STD1NK60T4	600 V	8.5 $\Omega$	1 A	30 W

- Extremely high dv/dt capability
- ESD improved capability
- 100% avalanche tested
- Gate charge minimized

### Applications

- Low power battery chargers
- Switch mode low power supplies (SMPS)
- Low power, ballast, CFL (compact fluorescent lamps)

### Description

This high voltage device is an N-channel Power MOSFET developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1: Device summary

Order code	Marking	Package	Packing
STD1NK60T4	D1NK60	DPAK	Tape and reel

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage	600	V
V <sub>DGR</sub>	Drain-gate voltage (R <sub>GS</sub> = 20 kΩ)	600	V
V <sub>GS</sub>	Gate-source voltage	±30	V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	1.0	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	0.63	A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	4	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	30	W
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>jmax</sub> )	1	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	25	mJ
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	3	V/ns
T <sub>j</sub>	Operating junction temperature range	- 55 to 150	°C
T <sub>stg</sub>	Storage temperature range		

**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area.

<sup>(2)</sup>I<sub>SD</sub> ≤ 1.0 A, di/dt ≤ 100 A/μs; V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ T<sub>JMAX</sub>

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	4.2	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient	100	°C/W

## 2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified

**Table 4: On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ $T_C = 125\text{ }^\circ\text{C}$ <sup>(1)</sup>			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS}=0\text{ V}$ , $V_{GS}=\pm 30\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2.25	3	3.7	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 0.5\text{ A}$		7.3	8.5	$\Omega$

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	156	-	pF
$C_{oss}$	Output capacitance		-	23.5	-	pF
$C_{rss}$	Reverse transfer capacitance		-	3.8	-	pF
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 1\text{ A}$ $V_{GS} = 0\text{ to }10\text{ V}$ (see <a href="#">Figure 16: "Test circuit for gate charge behavior"</a> )	-	7	-	nC
$Q_{gs}$	Gate-source charge		-	1.1	-	nC
$Q_{gd}$	Gate-drain charge		-	3.7	-	nC

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 0.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 20: "Switching time waveform"</a> )	-	6.5	-	ns
$t_r$	Rise time		-	5	-	ns
$t_{d(off)}$	Turn-off delay time		-	19	-	ns
$t_f$	Fall time		-	25	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		1	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		4	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1.0 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 1.0 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 25 \text{ V}$ , (see <a href="#">Figure 17: "Test circuit for inductive load switching and diode recovery times"</a> )	-	140		ns
$Q_{rr}$	Reverse recovery charge		-	240		nC
$I_{RRM}$	Reverse recovery current		-	3.3		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 1.0 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 25 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 17: "Test circuit for inductive load switching and diode recovery times"</a> )	-	229		ns
$Q_{rr}$	Reverse recovery charge		-	377		nC
$I_{RRM}$	Reverse recovery current		-	3.3		A

**Notes:**

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300  $\mu\text{ s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

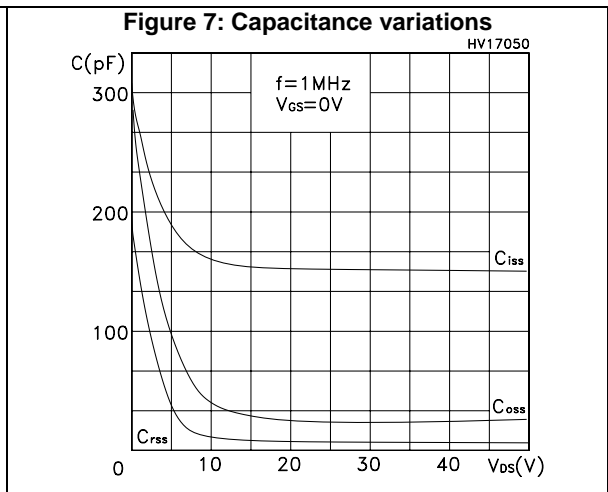
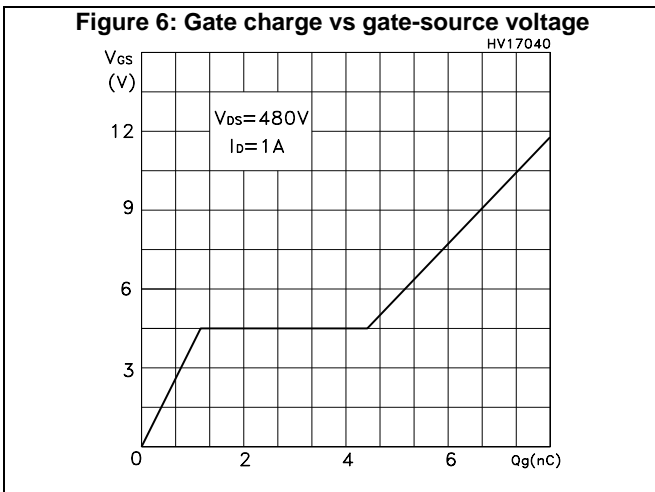
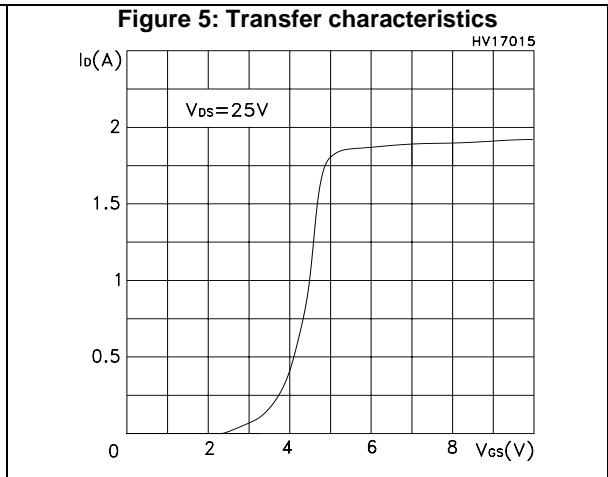
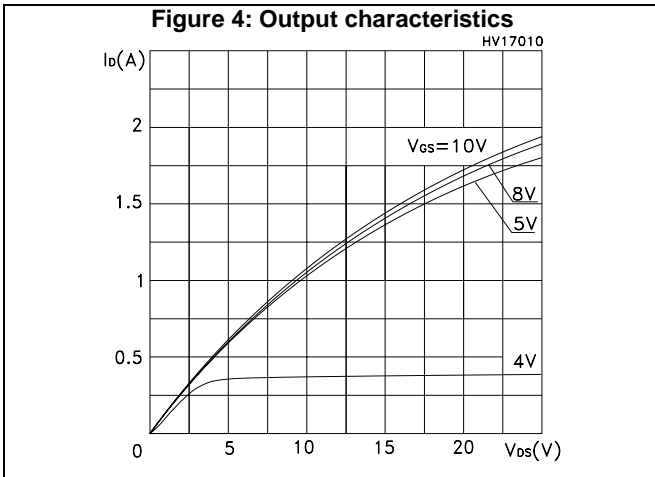
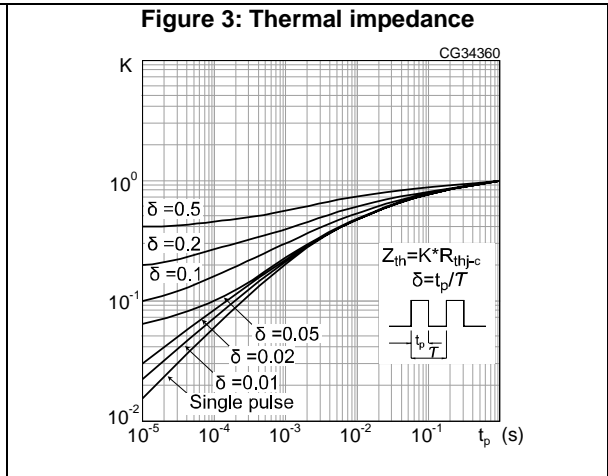
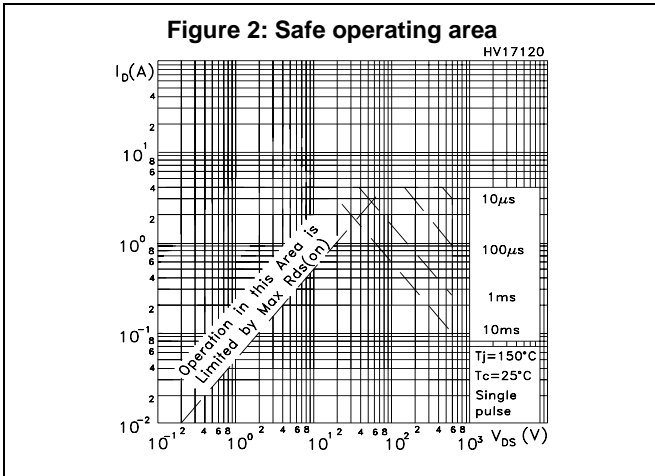


Figure 8: Static drain-source on-resistance

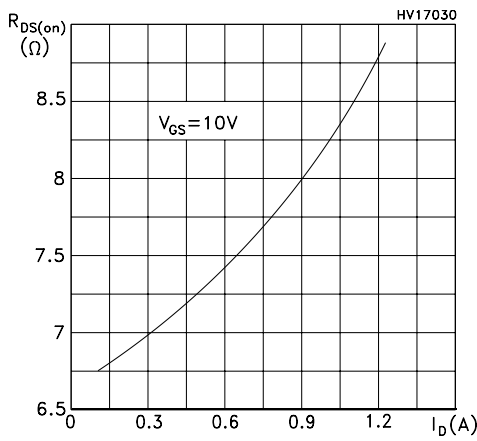


Figure 9: Normalized gate threshold voltage vs temperature

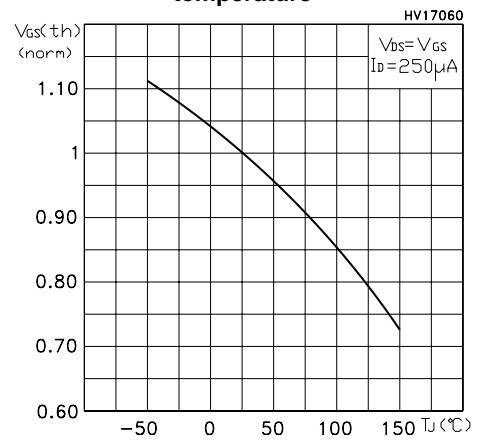


Figure 10: Normalized on-resistance vs temperature

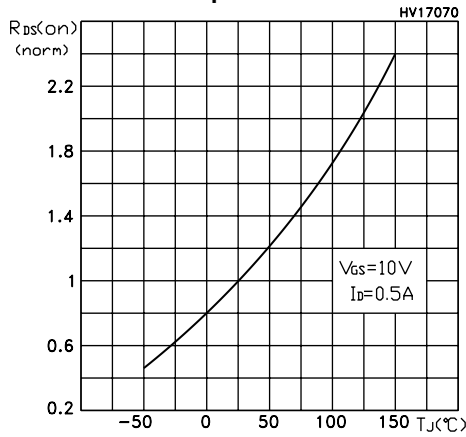


Figure 11: Source-drain forward characteristics

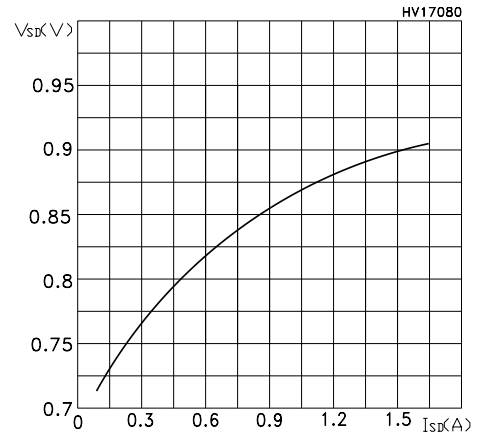


Figure 12: Normalized  $V_{(BR)DSS}$  vs temperature

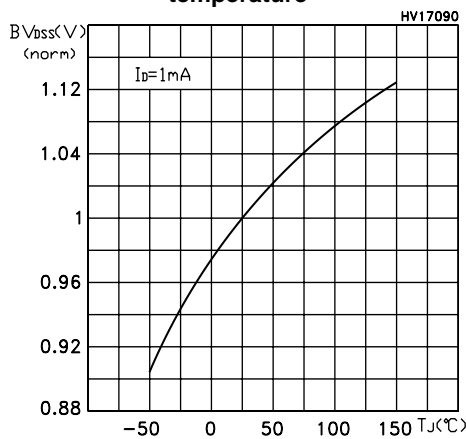


Figure 13: Maximum avalanche energy vs temperature

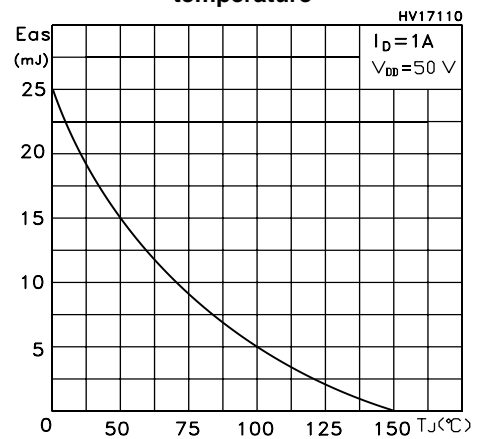
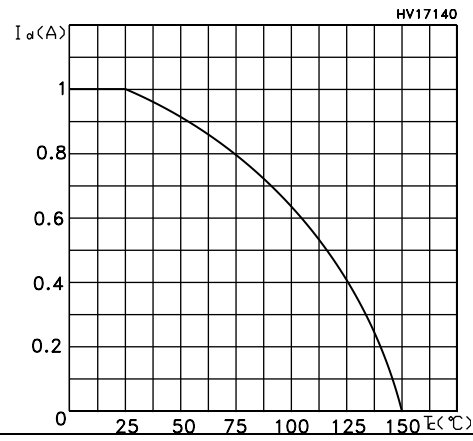


Figure 14: Maximum  $I_a$  current vs  $T_c$





### 3 Test circuits

**Figure 15: Test circuit for resistive load switching times**



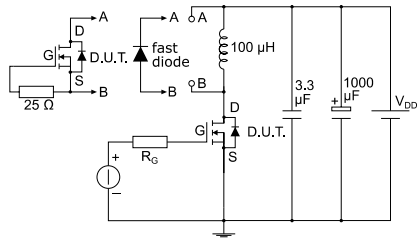
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**Figure 16: Test circuit for gate charge behavior**



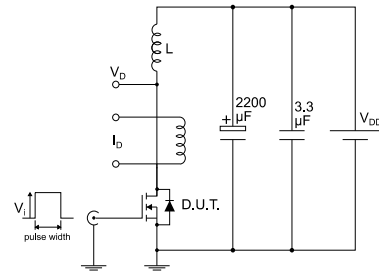
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**Figure 17: Test circuit for inductive load switching and diode recovery times**



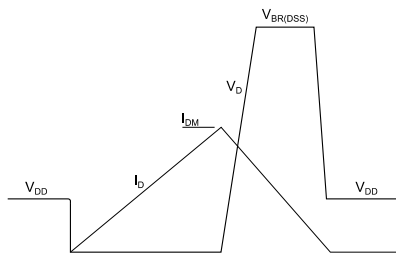
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**Figure 18: Unclamped inductive load test circuit**



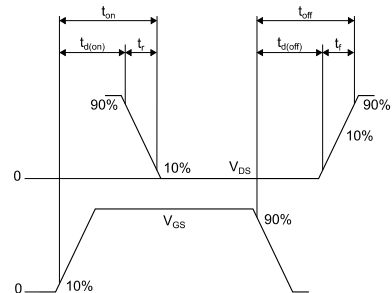
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**Figure 19: Unclamped inductive waveform**



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**Figure 20: Switching time waveform**



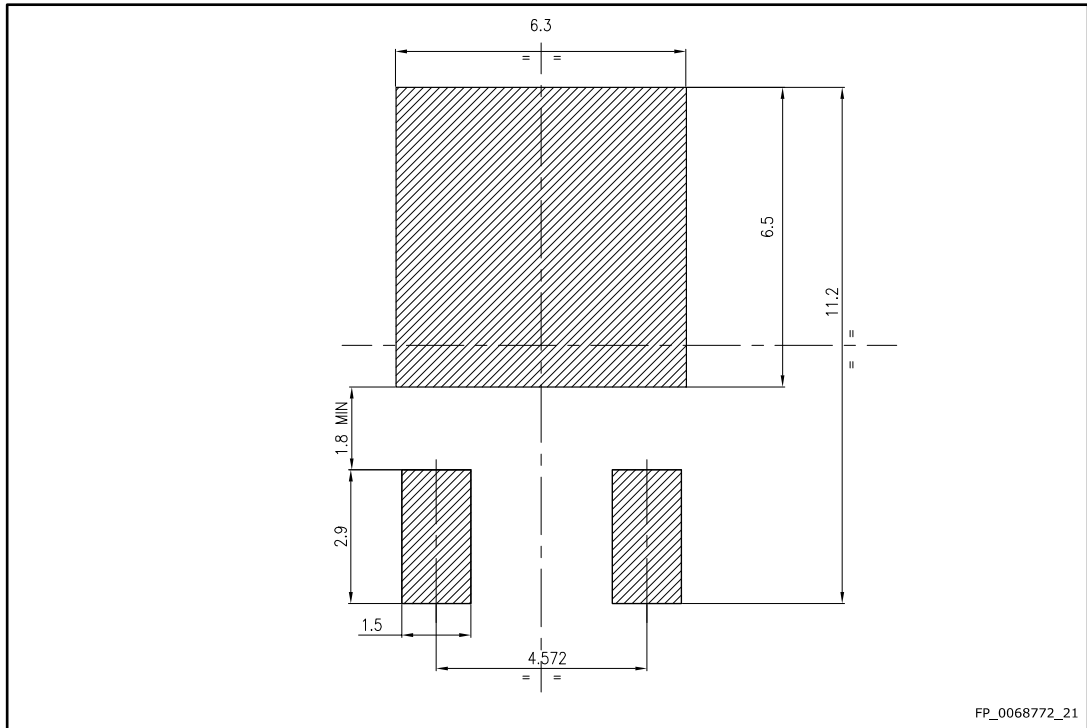
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Table 8: DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 22: DPAK (TO-252) recommended footprint (dimensions are in mm)



### 4.2 DPAK (TO-252) type C package information

Figure 23: DPAK (TO-252) type C package outline

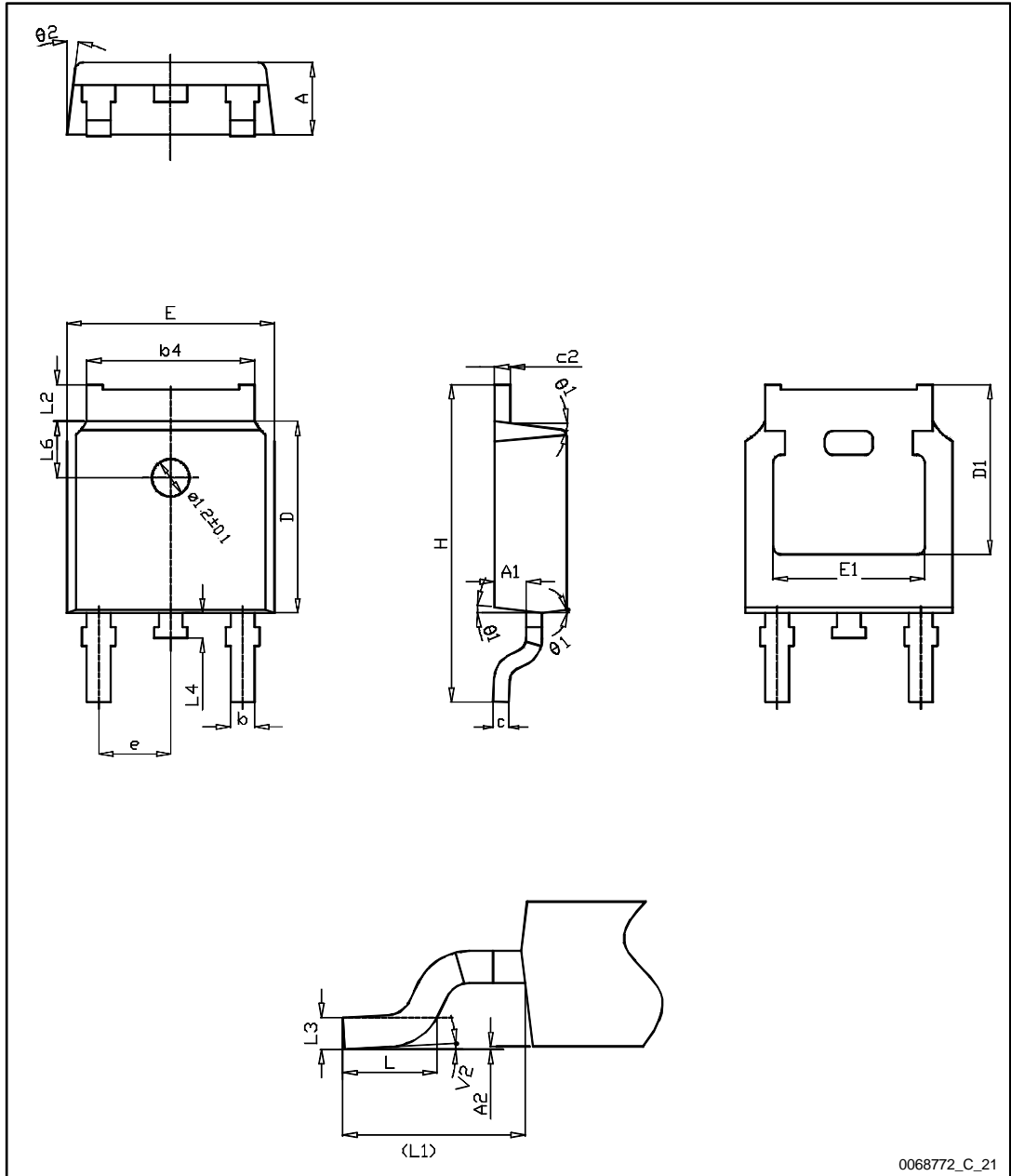
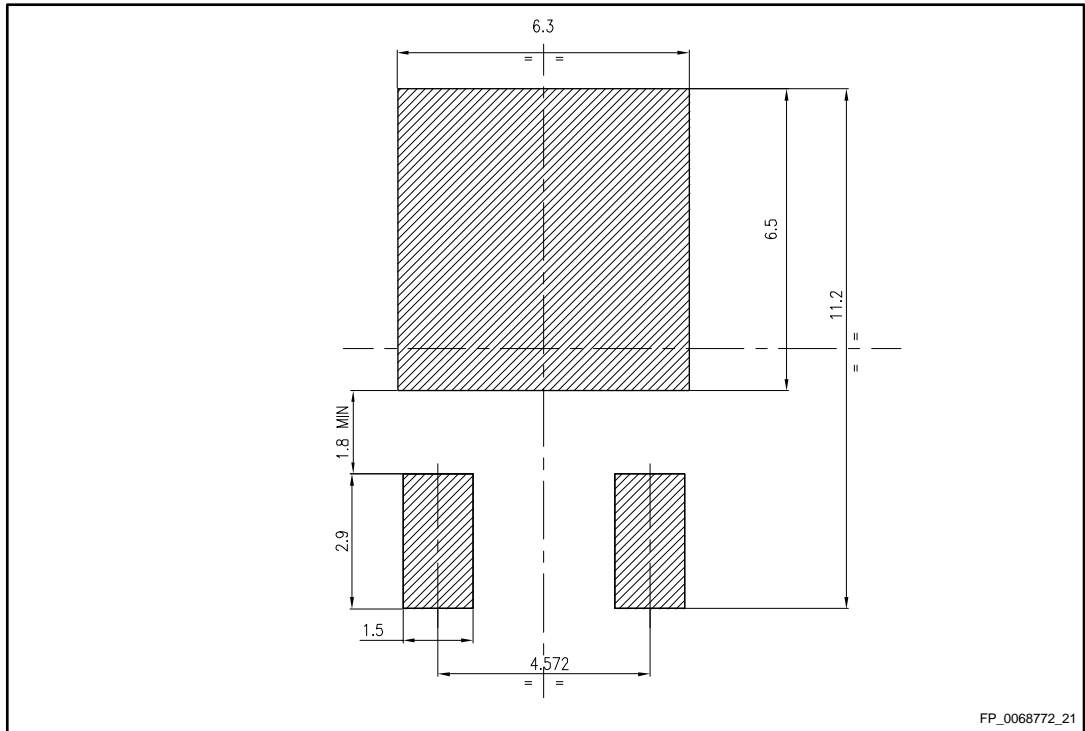


Table 9: DPAK (TO-252) type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 24: DPAK (TO-252) recommended footprint (dimensions are in mm)



### 4.3 Packing information

Figure 25: DPAK (TO-252) tape outline

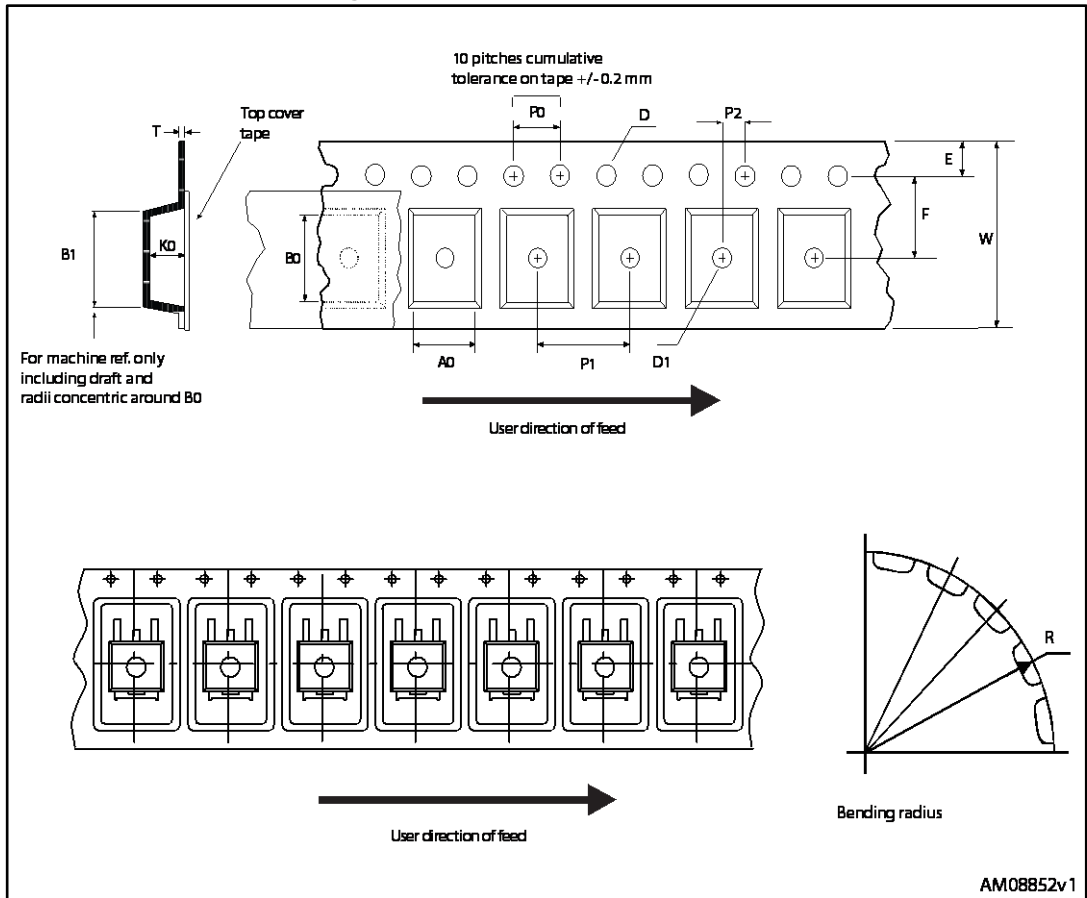




Figure 26: DPAK (TO-252) reel outline

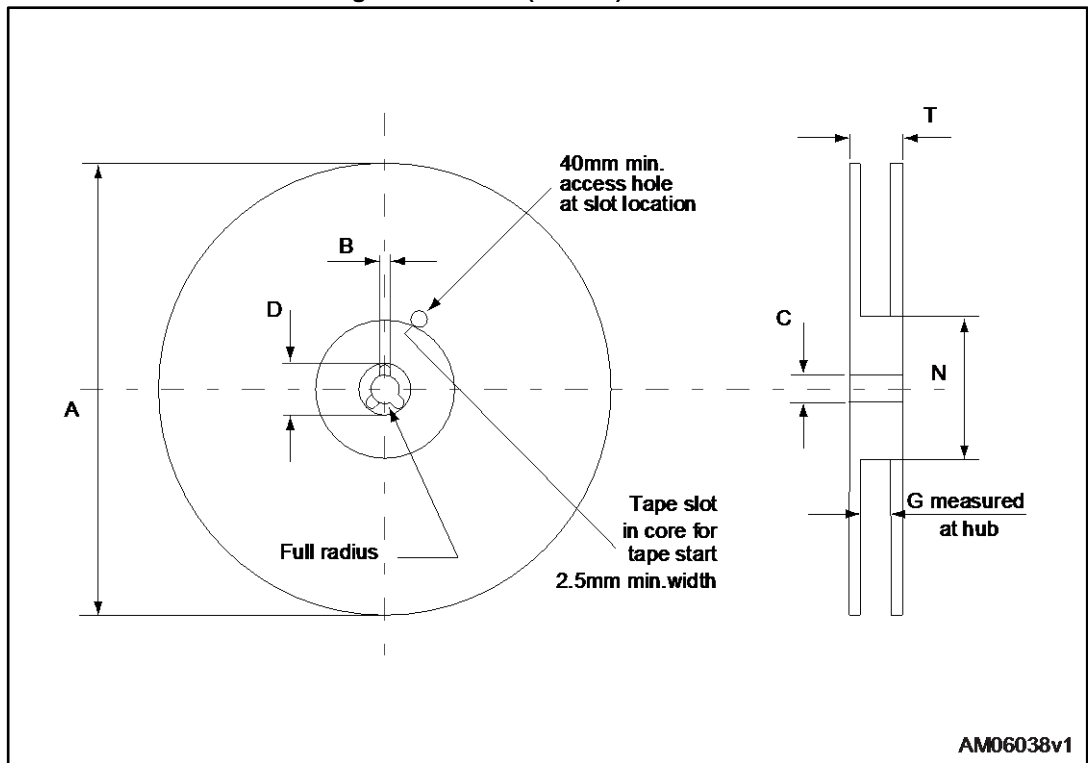


Table 10: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
06-Feb-2017	1	First release.

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