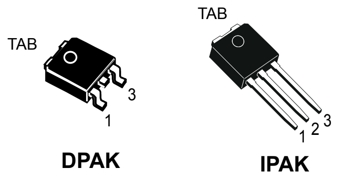
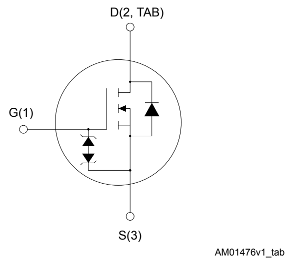
STD2HNK60Z, STD2HNK60Z-1

Datasheet

N-channel 600 V, 3.5 Ω typ., 2 A SuperMESH Power MOSFETs in DPAK and IPAK packages





Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D
STD2HNK60Z	600 V	4.8 Ω	2 A
STD2HNK60Z-1			

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status links
STD2HNK60Z
STD2HNK60Z-1

Product summary	
Order code	STD2HNK60Z
Marking	D2HNK60Z
Package	DPAK
Packing	Tape and reel
Order code	STD2HNK60Z-1
Marking	D2HNK60Z
Package	IPAK
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	2.0	A
	Drain current (continuous) at T_C = 100 °C	1.26	
I_{DM} (1)	Drain current (pulsed)	8	A
P_{TOT}	Total power dissipation at T_C = 25 °C	45	W
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	2	kV
dv/dt(2)	Peak diode recovery voltage slope	4.5	V/ns
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 2 A, di/dt ≤ 200 A/μs, V_{DS} (peak) ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		DPAK	IPAK	
R_{thJC}	Thermal resistance, junction-to-case	2.77		°C/W
R_{thJA}	Thermal resistance, junction-to-ambient		100	°C/W
R_{thJB} (1)	Thermal resistance, junction-to-board	50		°C/W

1. *When mounted on 1 inch² FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (t_p limited by T_J max)	2	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}; V_{DD} = 50 V)	120	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C (1)			50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 1 A		3.5	4.8	Ω

1. *Specified By Design – Not tested in production.*

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	280		pF
C_{oss}	Output capacitance		-	38		pF
C_{rss}	Reverse transfer capacitance		-	7		pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	30		pF
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 2 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	11	15 (2)	nC
Q_{gs}	Gate-source charge		-	2.25		nC
Q_{gd}	Gate-drain charge		-	6		nC

1. *$C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *Specified By Design – Not tested in production.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 1 A, R_G = 4.7 Ω , V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	10	-	ns
t_r	Rise time		-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	23	-	ns
t_f	Fall time		-	50	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2	A
I_{SDM} (1)	Source-drain current (pulsed)		-		8	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 2 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 2 A, di/dt = 100 A/μs, V_{DD} = 20 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	178		ns
Q_{rr}	Reverse recovery charge		-	445		nC
I_{RRM}	Reverse recovery current		-	5		A
t_{rr}	Reverse recovery time	I_{SD} = 2 A, di/dt = 100 A/μs, V_{DD} = 20 V, T_J = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	200		ns
Q_{rr}	Reverse recovery charge		-	500		nC
I_{RRM}	Reverse recovery current		-	5		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 μs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

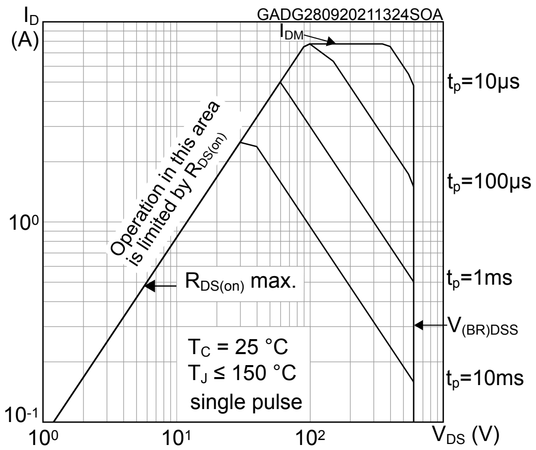


Figure 2. Thermal impedance

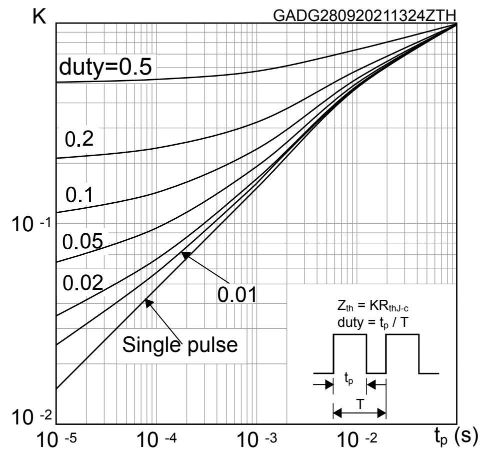


Figure 3. Output characterisics

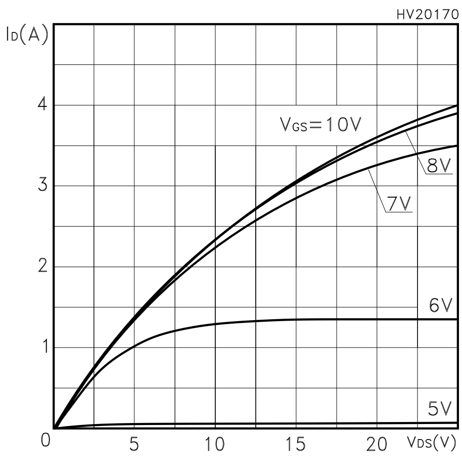


Figure 4. Transfer characteristics

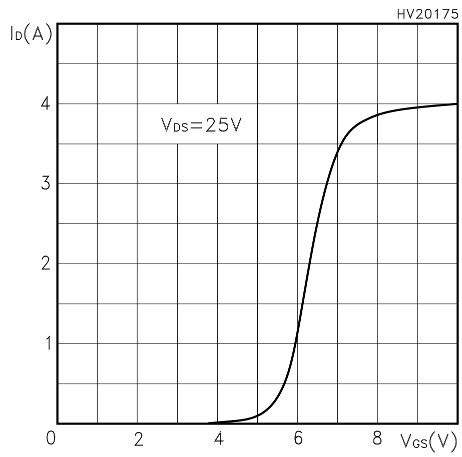


Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

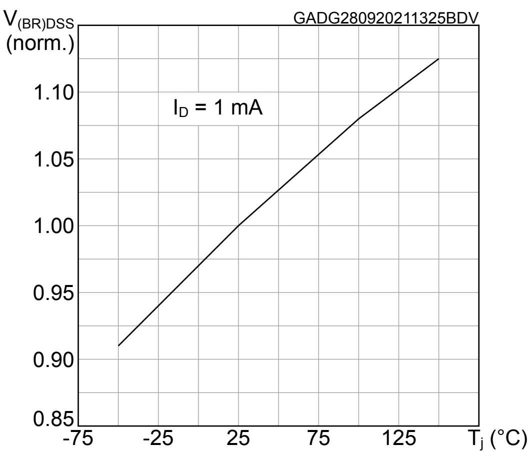


Figure 6. Static drain-source on-resistance

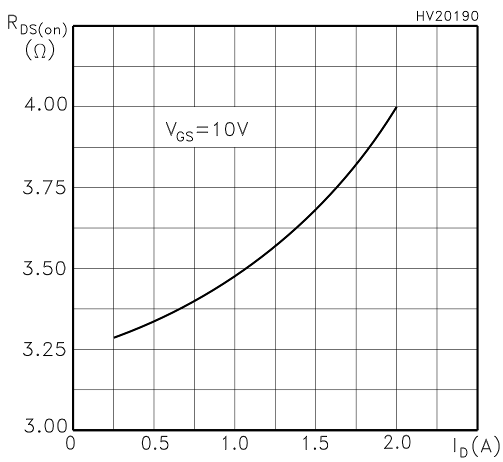


Figure 7. Gate charge vs gate-source voltage

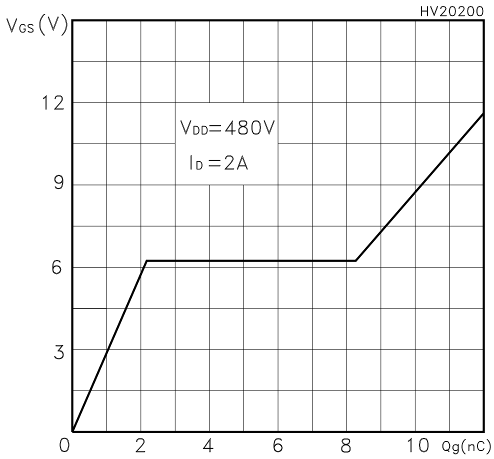


Figure 8. Capacitance variations

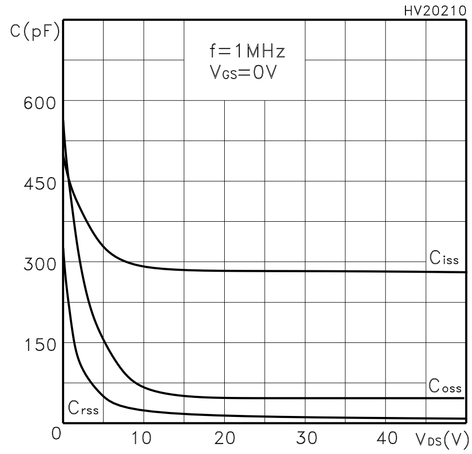


Figure 9. Normalized gate threshold voltage vs temperature

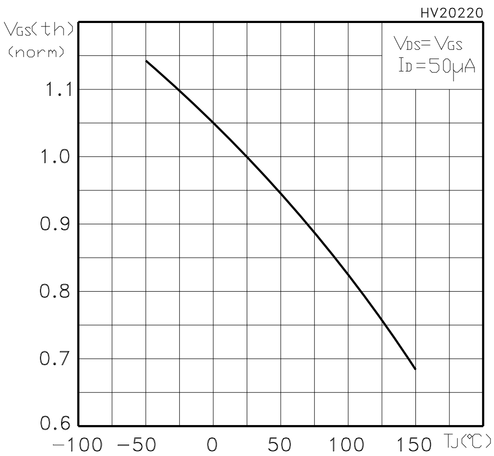


Figure 10. Normalized on-resistance vs temperature

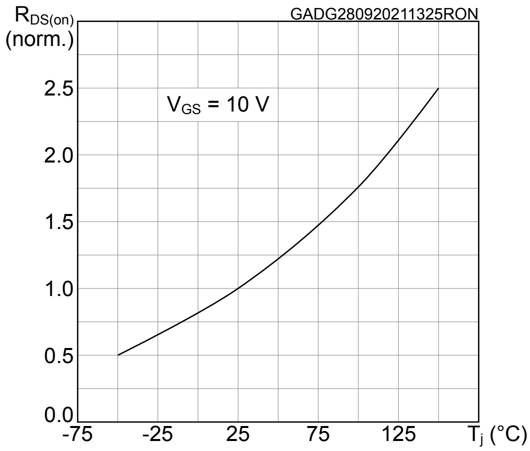


Figure 11. Source-drain diode forward characteristics

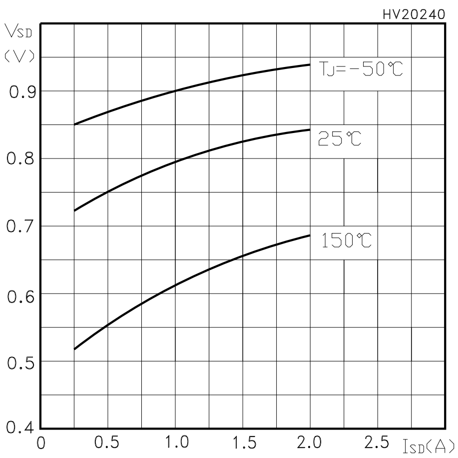
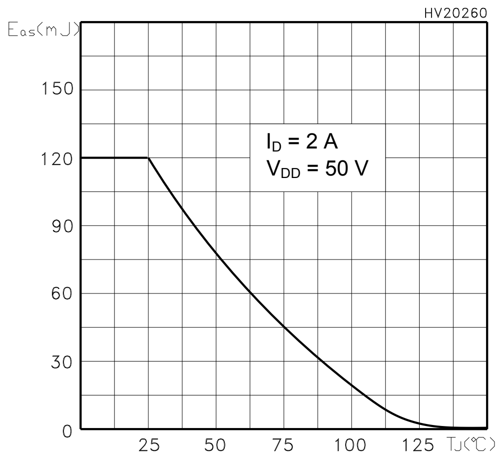


Figure 12. Maximum avalanche energy vs temperature



3 Test circuits

Figure 13. Test circuit for resistive load switching times

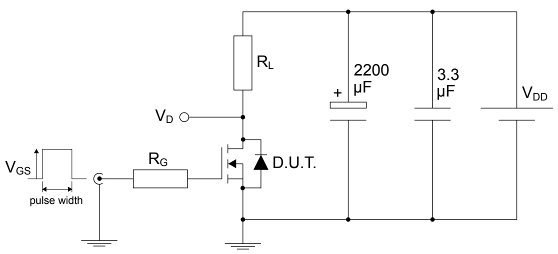


Figure 14. Test circuit for gate charge behavior

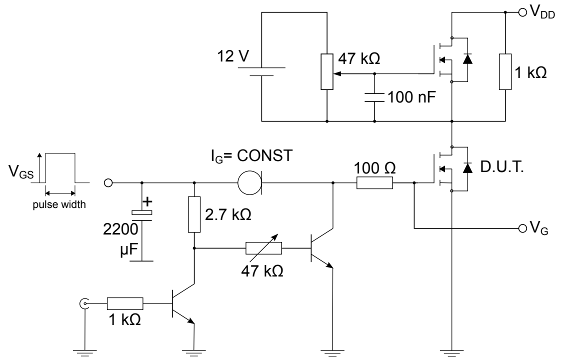


Figure 15. Test circuit for inductive load switching and diode recovery times

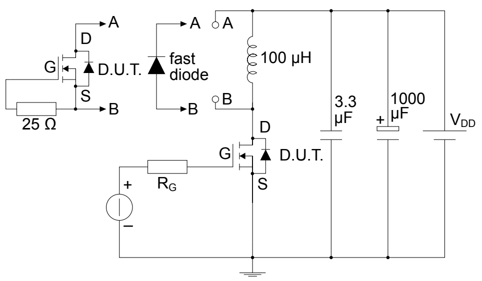


Figure 16. Unclamped inductive load test circuit

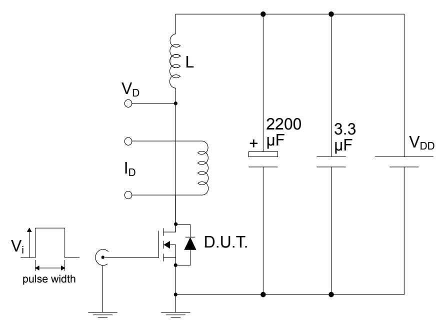


Figure 17. Unclamped inductive waveform

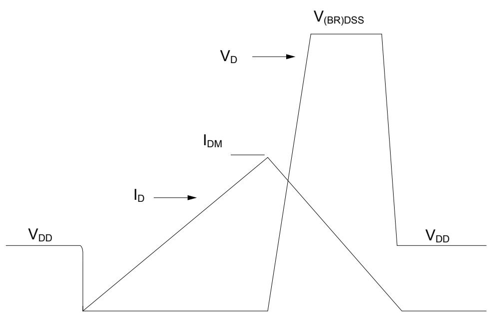
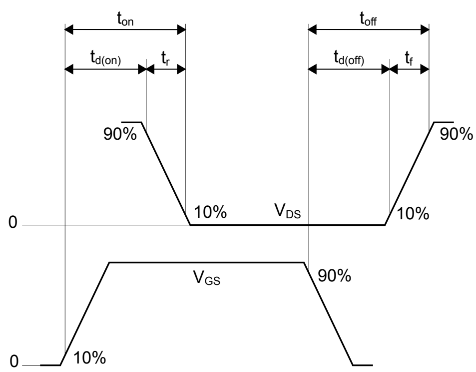


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 19. **DPAK (TO-252) type A package outline**

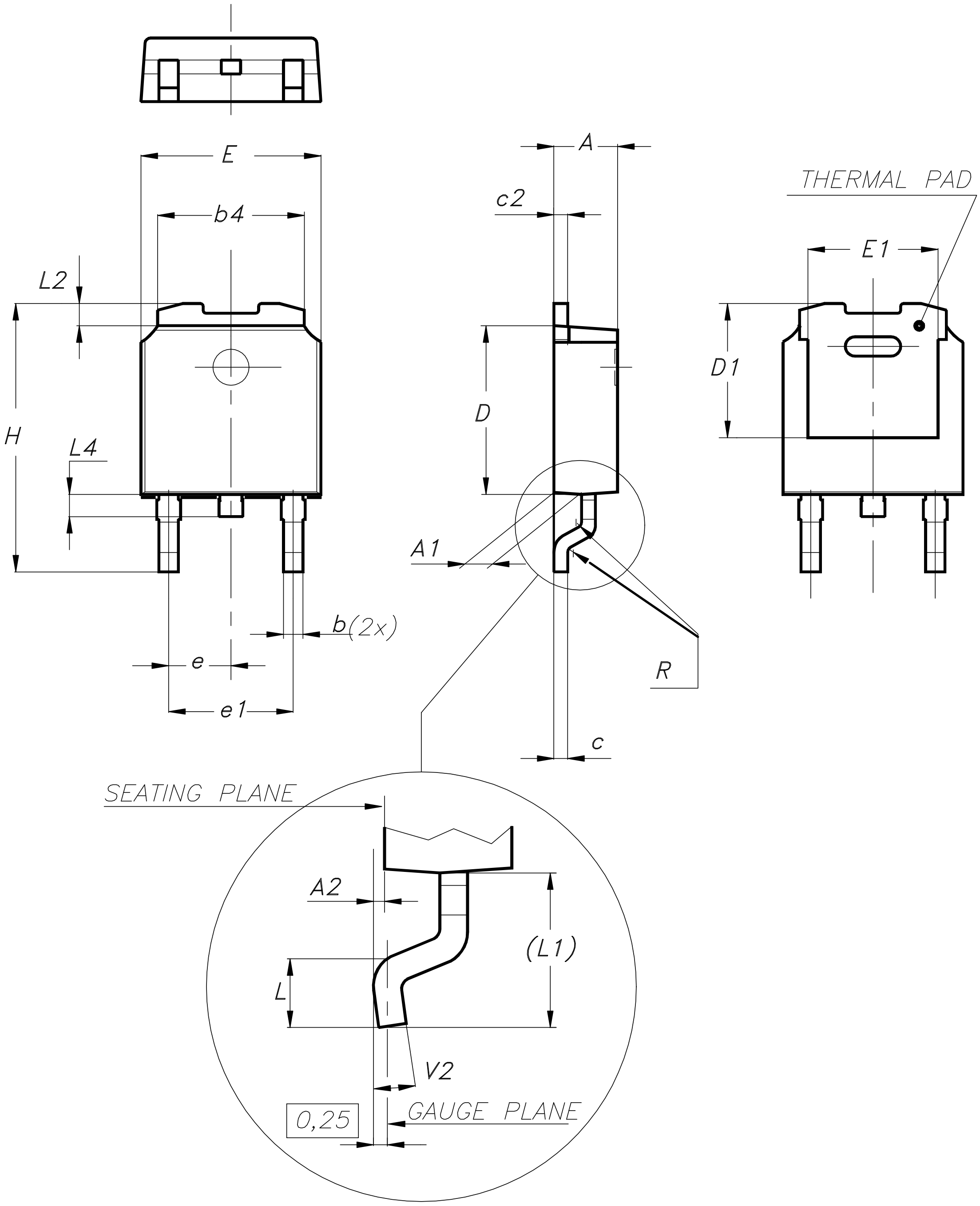


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Table 8. **DPAK (TO-252) type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C package information

Figure 20. **DPAK (TO-252) type C package outline**

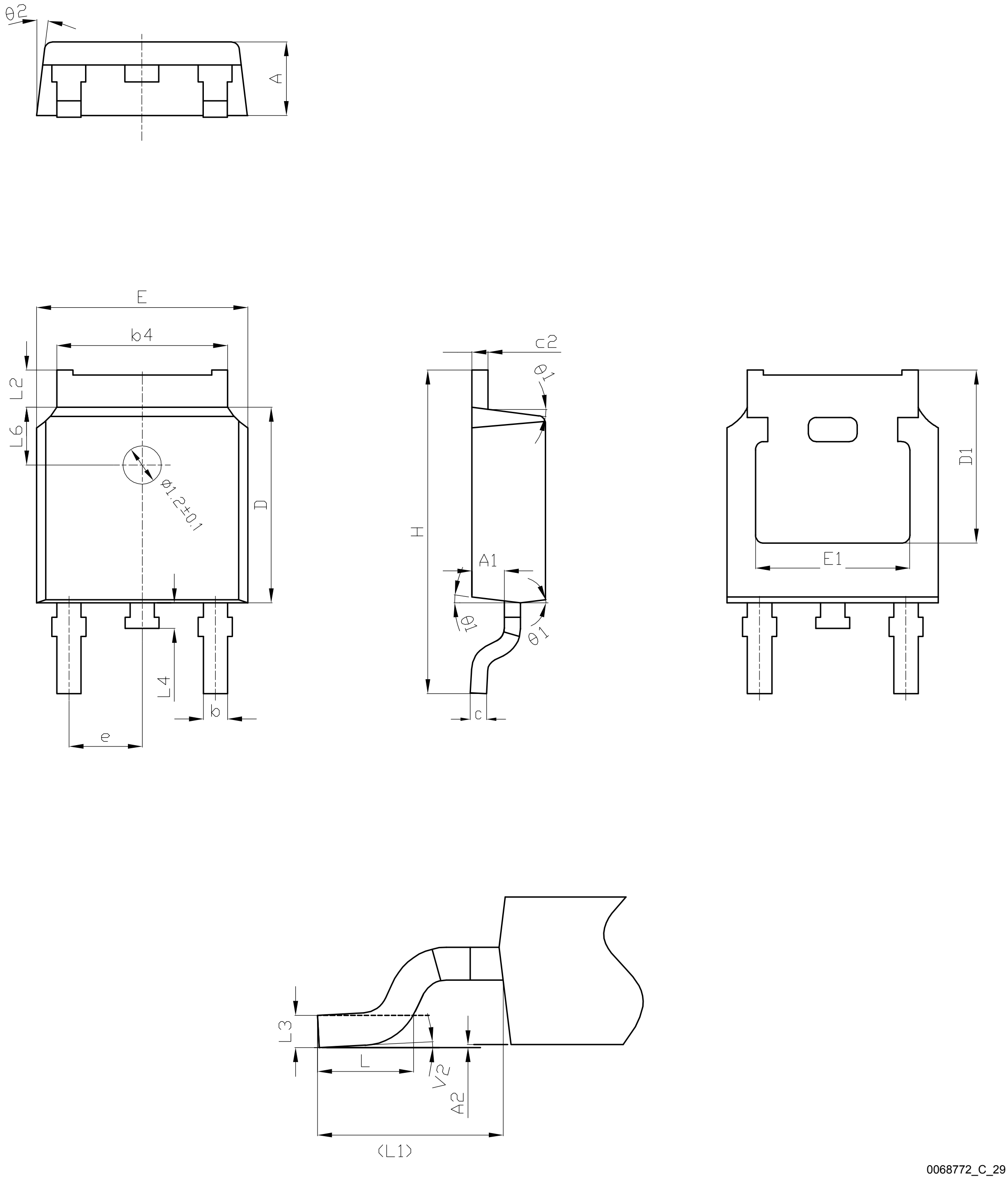
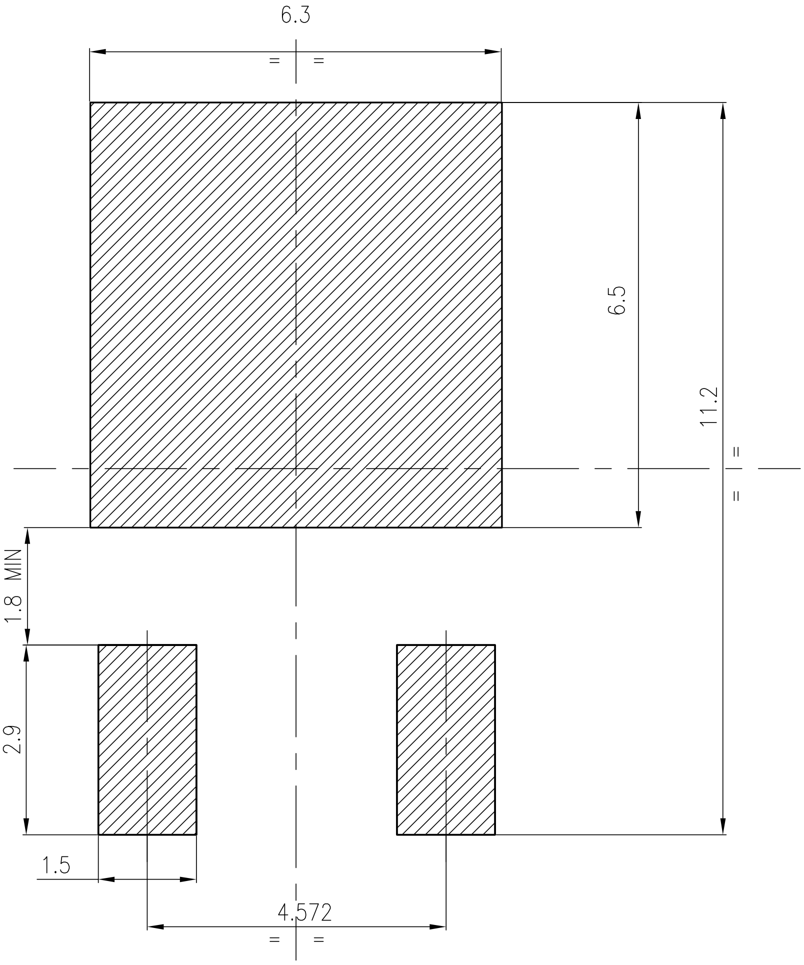


Table 9. DPAK (TO-252) type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 21. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



4.3 DPAK (TO-252) packing information

Figure 22. DPAK (TO-252) tape outline

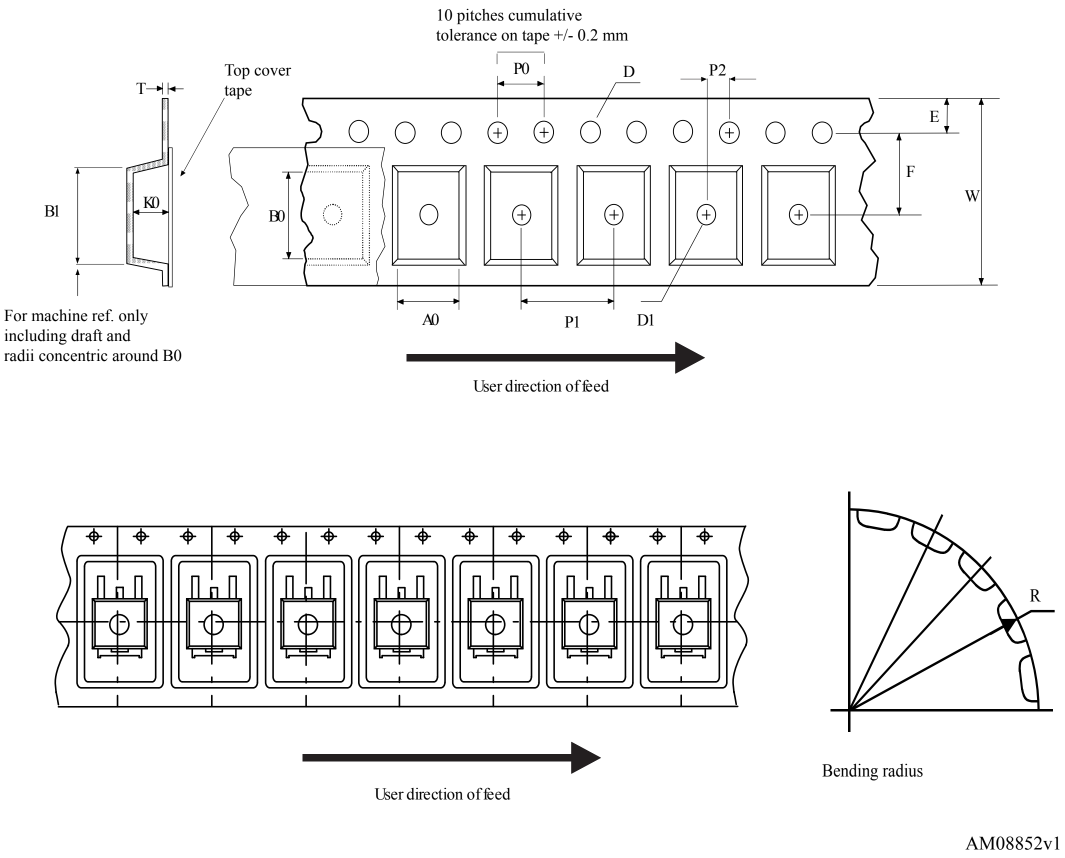


Figure 23. **DPAK (TO-252) reel outline**

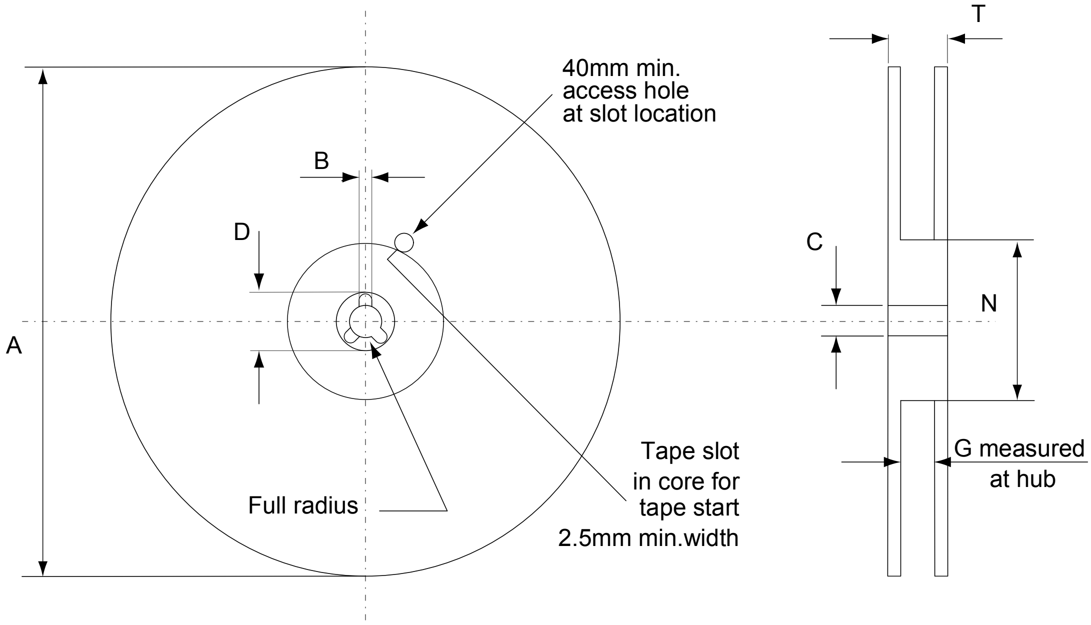


Table 10. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 IPAK (TO-251) type A package information

Figure 24. **IPAK (TO-251) type A package outline**

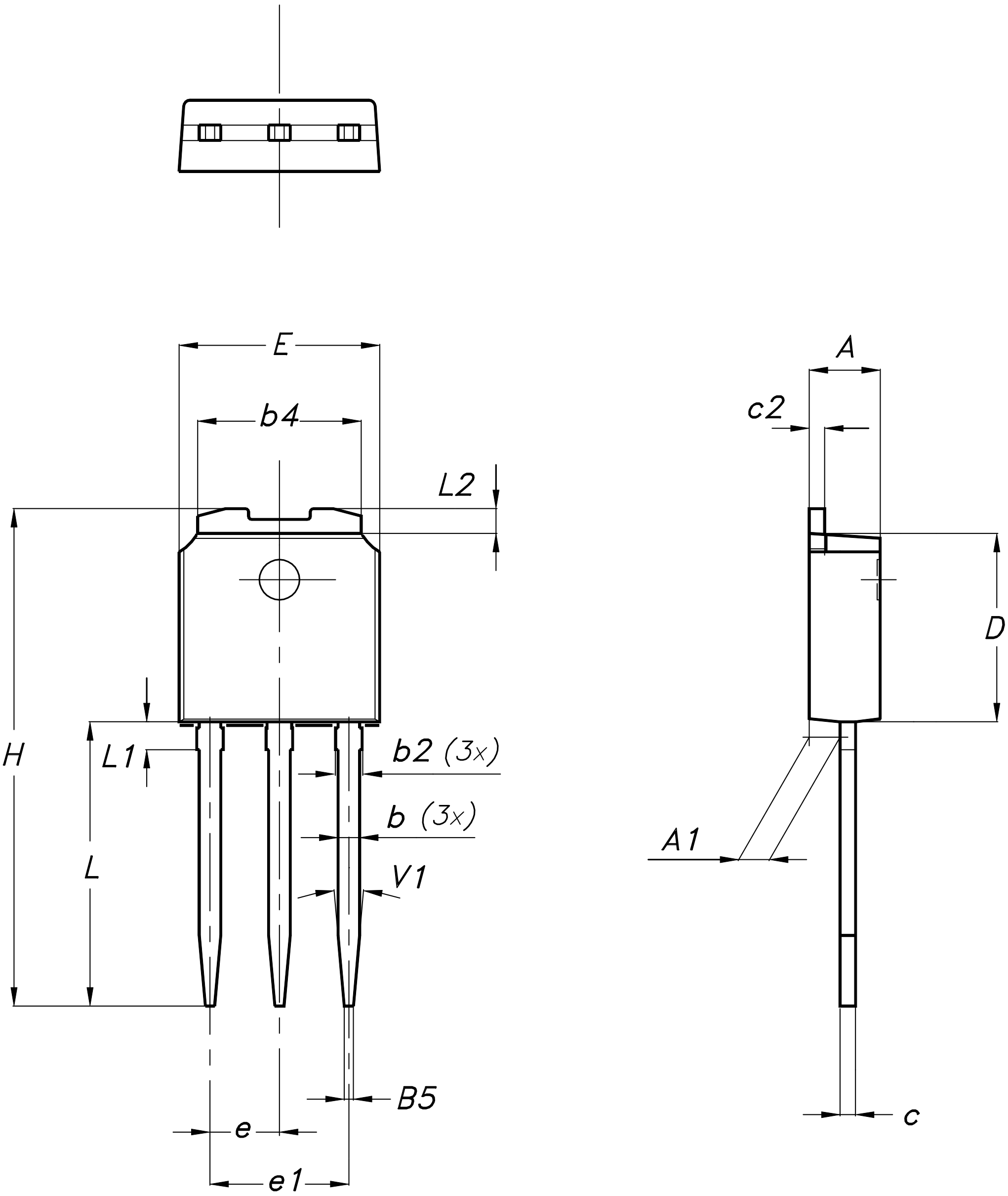


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Table 11. IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.5 IPAK (TO-251) type C package information

Figure 25. **IPAK (TO-251) type C package outline**

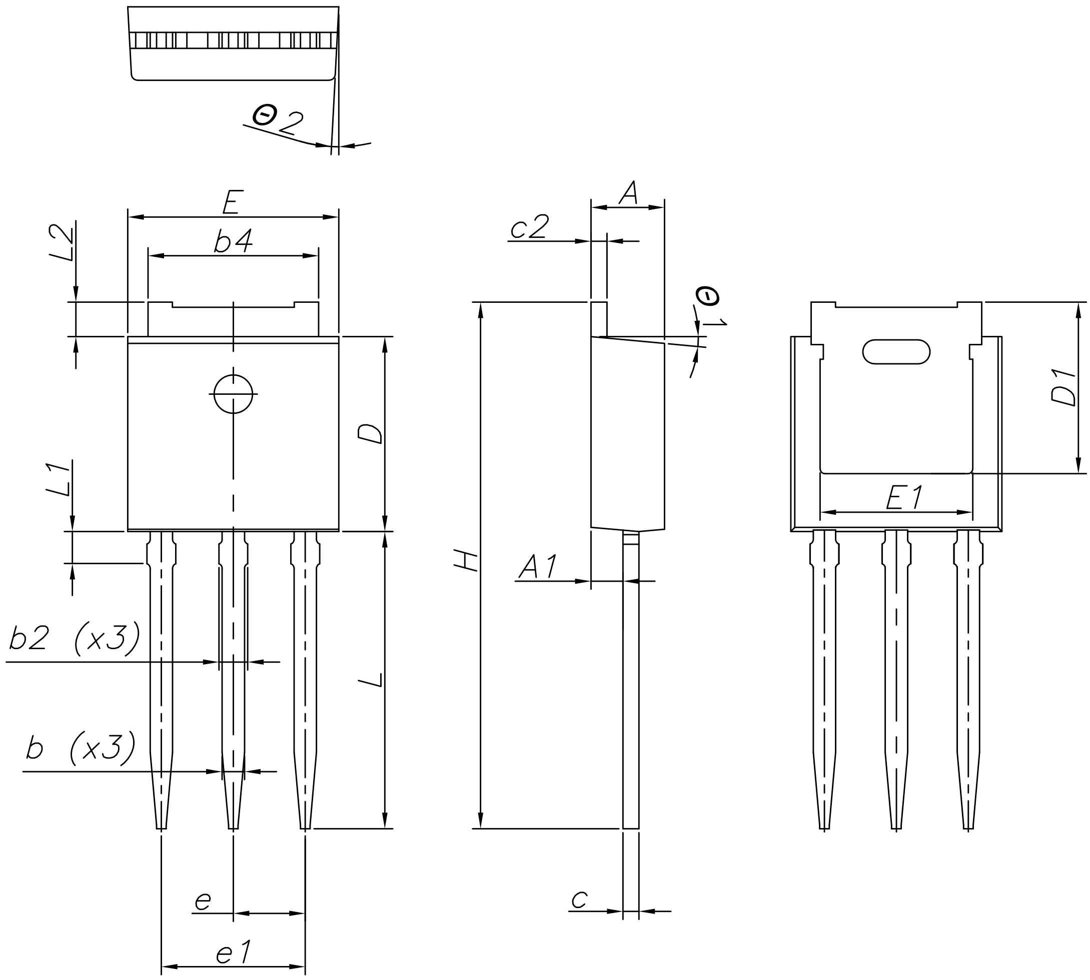

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Table 12. **IPAK (TO-251) type C package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

Revision history

Table 13. **Document revision history**

Date	Revision	Changes
09-Mar-2004	1	First release.
23-Mar-2004	2	Modified title
02-Apr-2005	3	Added new *section: Electrical characteristics (curves)*
06-Mar-2006	4	Inserted DPAK. The document has been reformatted
25-May-2012	5	Corrected unit in *Table 5: On/off states*
04-Jun-2018	6	Removed maturity status indication from cover page. The document status is production data. Updated title and features in cover page, *Section 1 Electrical ratings*, *Section 2 Electrical characteristics* and *Section 4 Package information.* Minor text changes.
06-Oct-2021	7	The part numbers STF2HNK60Z and STQ2HNK60ZR-AP have been moved to a separate datasheet and the document has been updated accordingly. Modified Table 7. Source-drain diode. Modified Figure 1. Safe operating area , Figure 2. Thermal impedance, Figure 5. Normalized $V_{(BR)DSS}$ vs temperature and Figure 10. Normalized on-resistance vs temperature. Updated Section 4 Package information.

Contents