STD2NC45-1

N-channel 450 V, 4.1 Ω, 1.5 A, IPAK SuperMESH™ Power MOSFET

Features

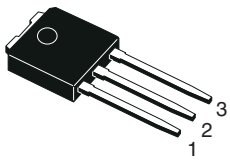
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- New high voltage benchmark

Application

- Switching applications

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products.



IPAK

Figure 1. Internal schematic diagram

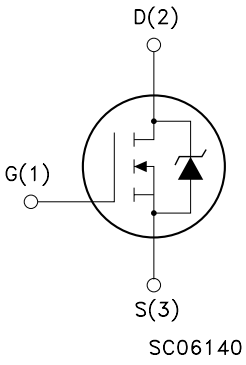


Table 1. Device summary

Order code	Marking	Package	Packaging
STD2NC45-1	D2NC45	IPAK	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	450	V
V_{GS}	Gate- source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25°C	1.5	A
I_D	Drain current (continuous) at T_C = 100°C	0.95	A
I_{DM} (1)	Drain current (pulsed)	6	A
P_{TOT}	Total dissipation at T_C = 25°C	30	W
	Derating factor	0.24	W/°C
dv/dt (2)	Peak diode recovery voltage slope	3	V/ns
T_{stg}	Storage temperature	–65 to 150	°C
T_j	Max. operating junction temperature		°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 0.5A$, di/dt ≤ 100 A/µs, V_{DD} =80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	4.1	°C/W
Rthj-amb	Thermal resistance junction-ambient max	100	°C/W
T_l	Maximum lead temperature for soldering purpose	275	°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	1.5	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, I_D=I_{AS}, V_{DD}=50V)	25	mJ

2 Electrical characteristics

(T_{CASE} = 25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} = 0	450			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating, T_C = 125°C				1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 30V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2.3	3	3.7	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 0.5A		4.1	4.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 0.5A	-	1.1		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0	-	160 27.5 4.7		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 360V, I_D = 1.5A, V_{GS} = 10V, R_G = 4.7Ω *(see Figure 17)*	-	7 1.3 3.2	10	nC nC nC

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 225V, I_D = 0.5A R_G = 4.7Ω V_{GS} = 10V *(see Figure 16)*	-	6.7 4	-	ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	V_{DD} = 360V, I_D = 1.5A, R_G = 4.7Ω, V_{GS} = 10V *(see Figure 16)*	-	8.5 12 18	-	ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		1.5 6.0	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 1.5A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 1.5A, di/dt = 100A/µs V_{DD} = 100V, T_j = 150°C *(see Figure 21)*	-	225 530 4.7		ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for IPAK

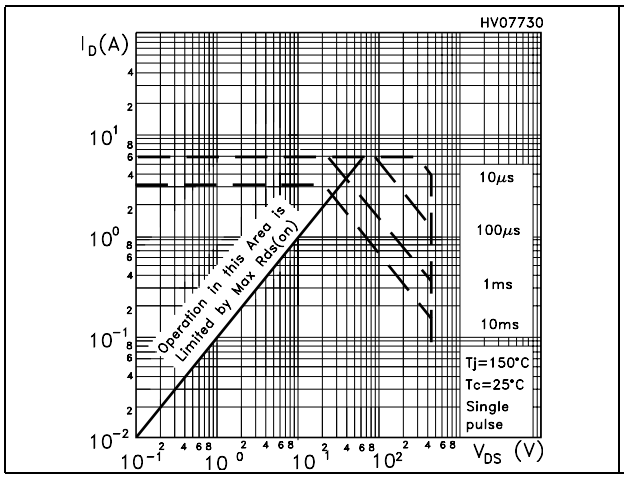


Figure 3. Thermal impedance for IPAK

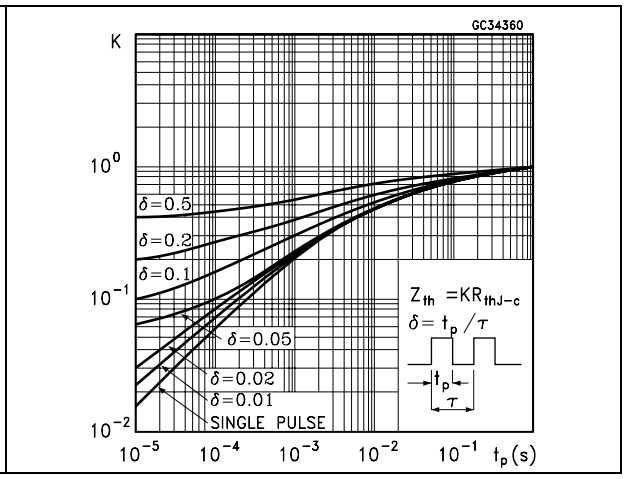


Figure 4. Output characteristics

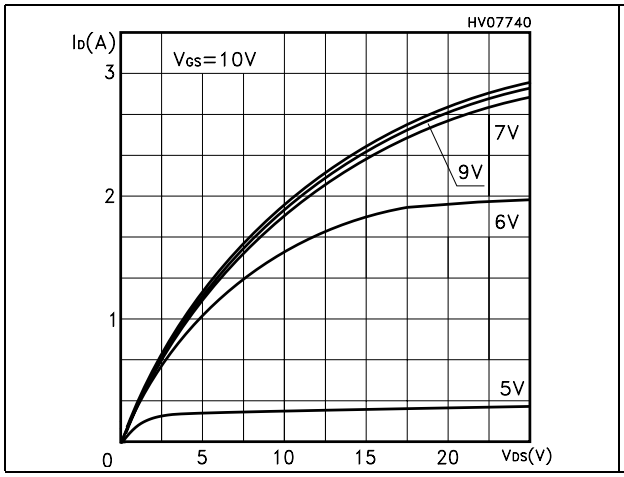


Figure 5. Transfer characteristics

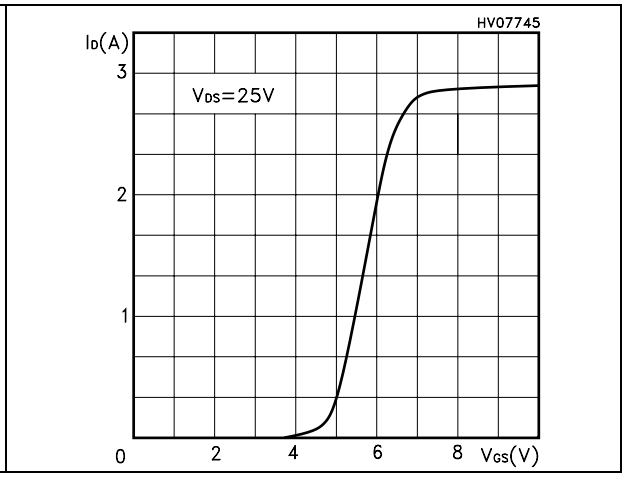


Figure 6. Transconductance

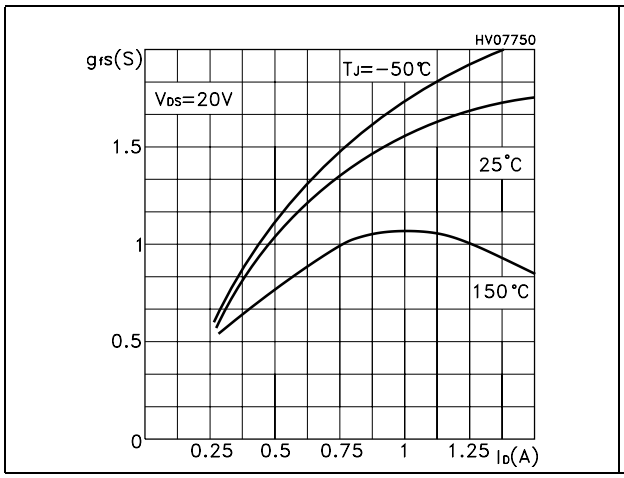


Figure 7. Static drain-source on resistance

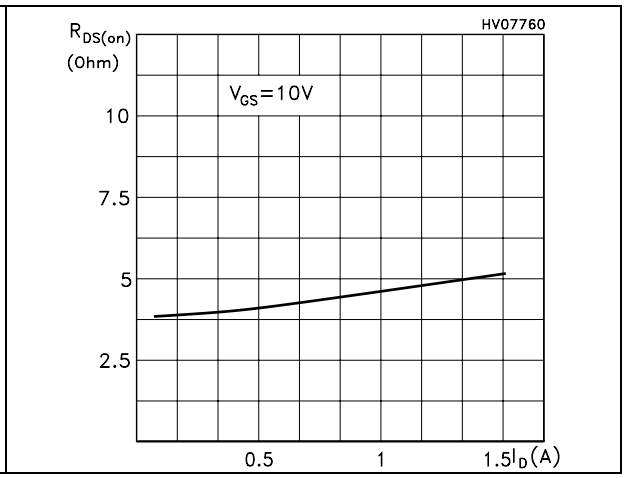


Figure 8. Gate charge vs gate-source voltage

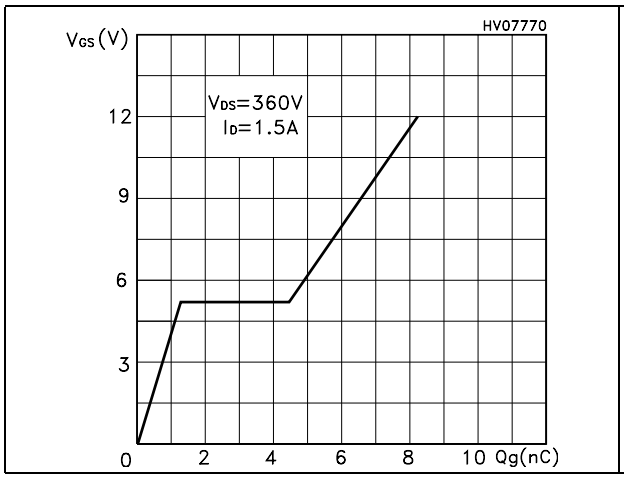


Figure 9. Capacitance variations

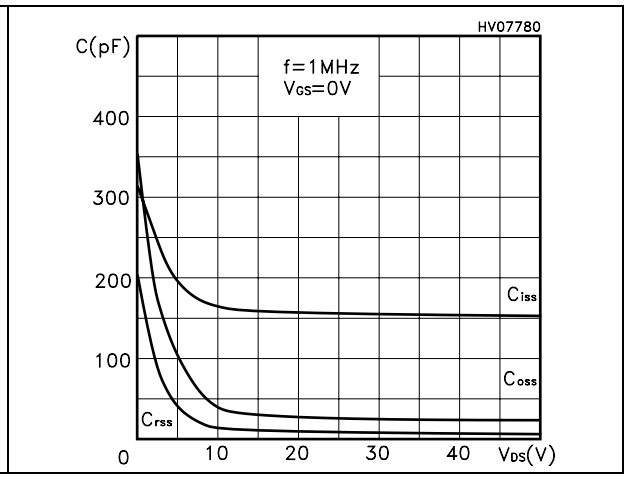


Figure 10. Normalized gate threshold voltage vs temperature

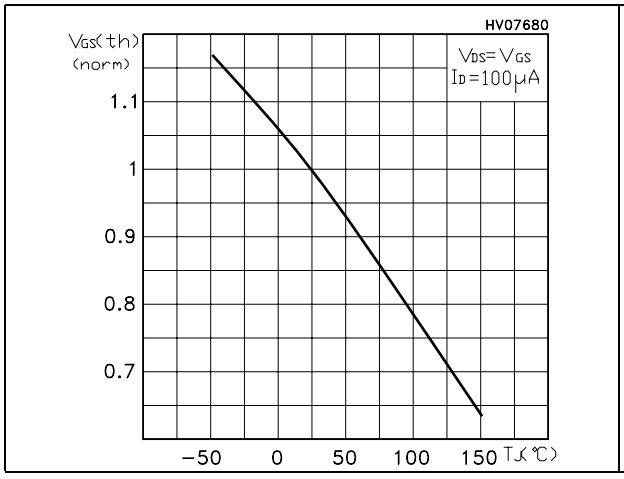


Figure 11. Normalized on resistance vs temperature

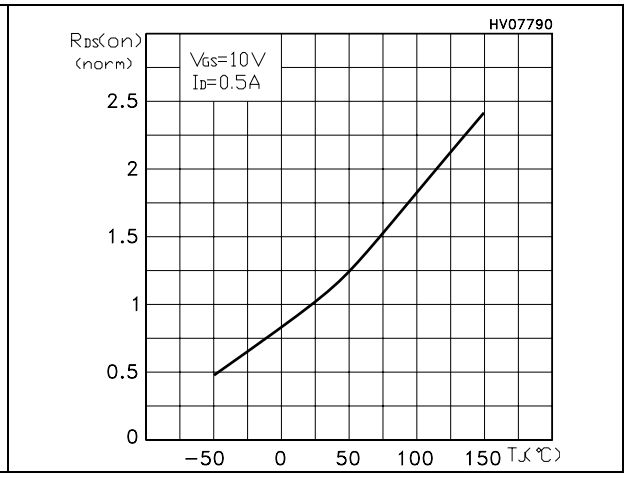


Figure 12. Source-drain diode forward characteristics

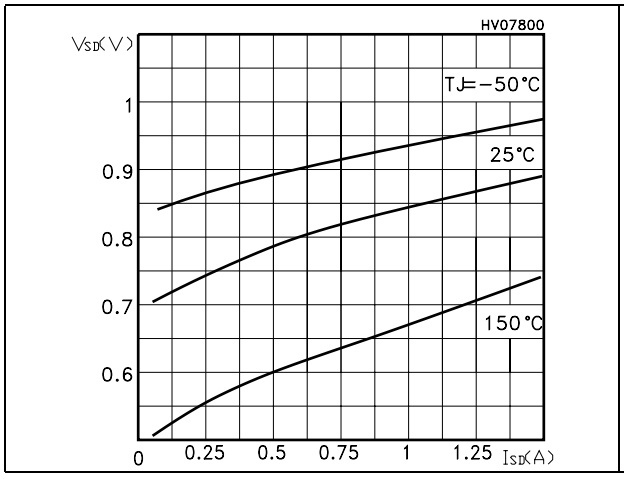


Figure 13. Normalized B_{VDSS} vs temperature

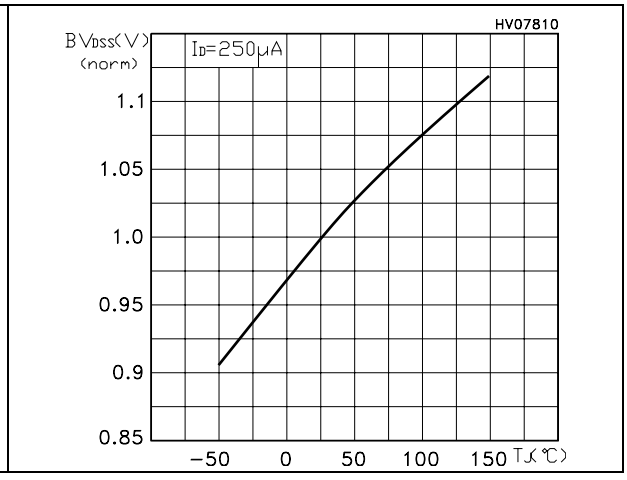


Figure 14. Max Id current vs Temperature

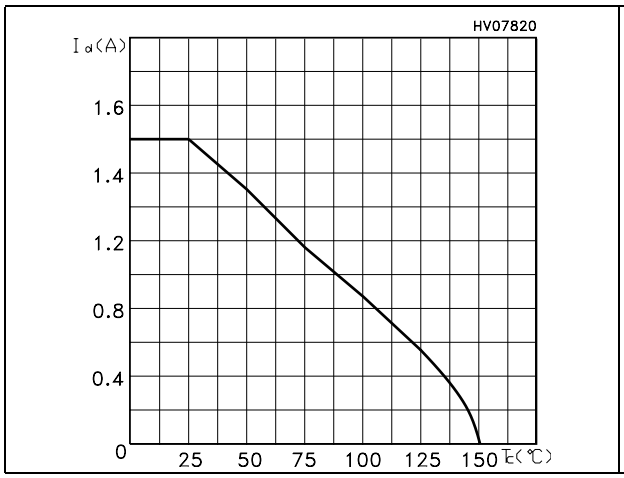
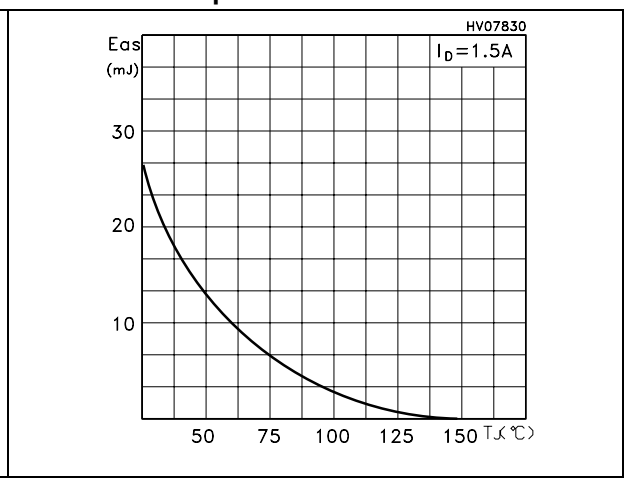


Figure 15. Maximum avalanche energy vs temperature



3 Test circuits

Figure 16. Switching times test circuit for resistive load

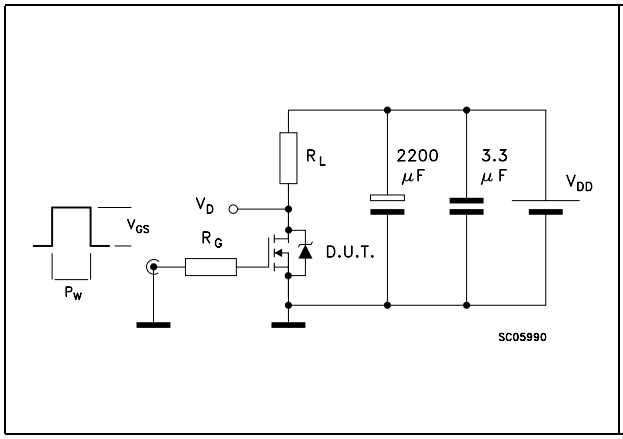


Figure 17. Gate charge test circuit

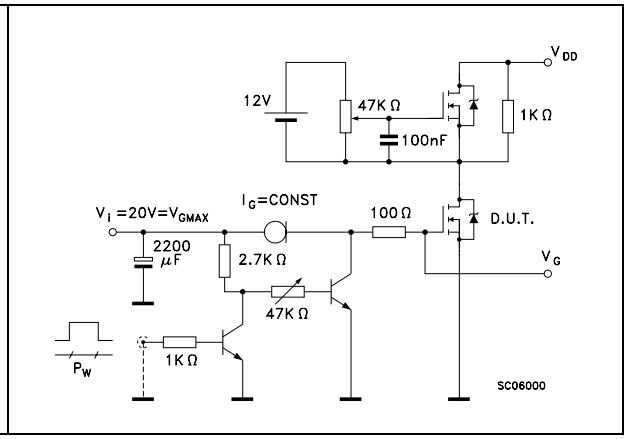


Figure 18. Test circuit for inductive load switching and diode recovery times

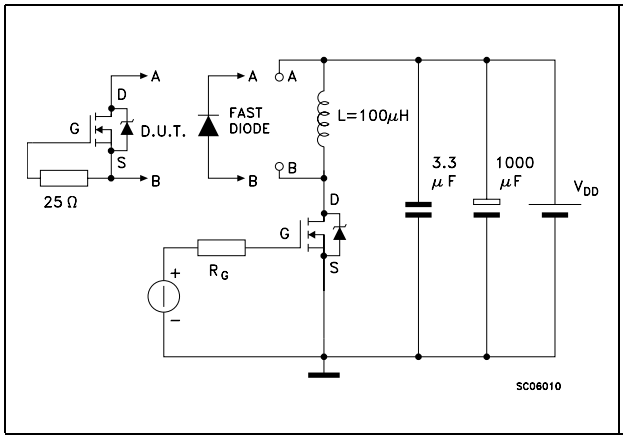


Figure 19. Unclamped inductive load test circuit

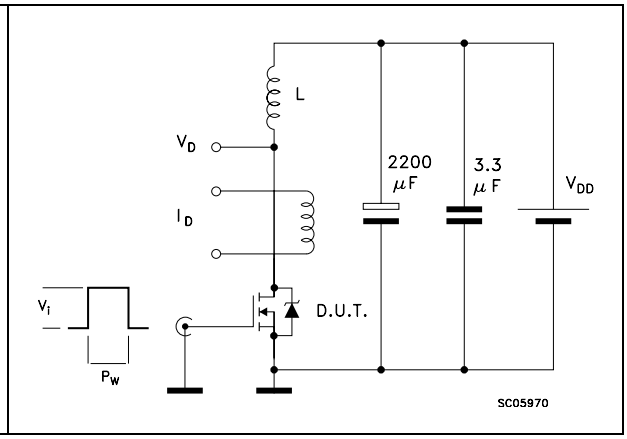


Figure 20. Unclamped inductive waveform

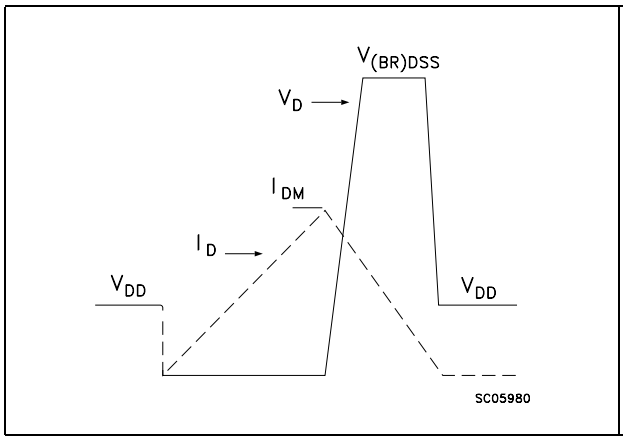
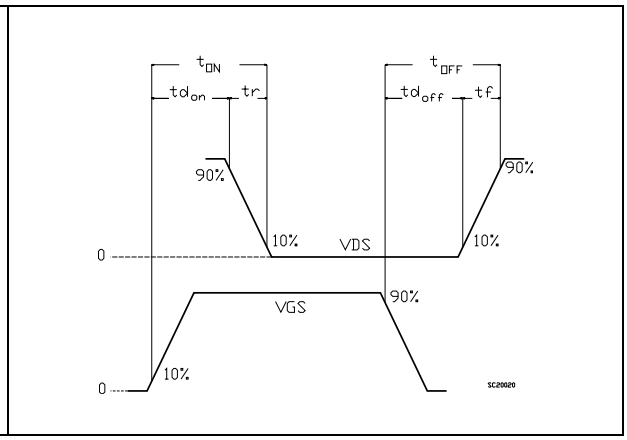


Figure 21. Switching time waveform

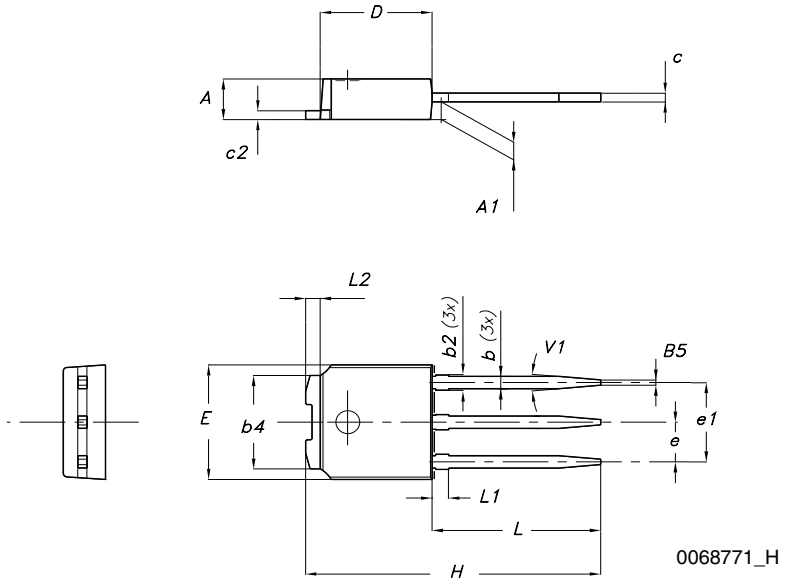


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10 °	



5 Revision history

Table 9. Revision history

Date	Revision	Changes
21-Jun-2004	2	Complete version
12-Jul-2006	3	New template
17-Apr-2009	4	Updated mechanical data New ECOPACK® statement in *Section 4: Package mechanical data*

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