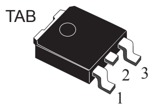
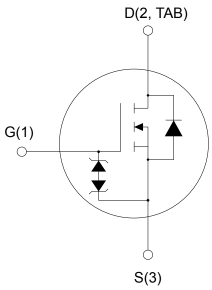
STD5N52U

Datasheet

N-channel 525 V, 1.25 Ω typ., 4.4 A, UltraFASTmesh™ Power MOSFET in a DPAK package



DPAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD5N52U	525 V	1.50 Ω	4.4 A	70 W

- Outstanding dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very low $R_{DS(on)}$
- Extremely low t_{rr}

Applications

- Switching applications

Description

This device is N-channel Power MOSFET developed using UltraFASTmesh™ technology, which combines the advantages of reduced on resistance, Zener gate protection and very high dv/dt capability with an enhanced fast body-drain recovery diode.

Product status link
STD5N52U

Product summary	
Order code	STD5N52U
Marking	5N52U
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	4.4	A
I_D	Drain current (continuous) at T_C= 100 °C	2.8	
I_{DM} (1)	Drain current (pulsed)	17.6	A
P_{TOT}	Total power dissipation at T_C = 25 °C	70	W
dv/dt	Peak diode recovery voltage slope	20	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	2.8	kV

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 4.4 A, di/dt ≤ 400 A/µs, $V_{DS\ peak}$ < $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.79	°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-pcb	50	

1. *When mounted on a 1-inch² FR-4, 2 oz Cu board*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_{jmax})	4.4	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	170	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	525			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 525 V			10	µA
		V_{GS} = 0 V, V_{DS} = 525 V, T_C = 125 °C[(1)]			500	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.2 A		1.25	1.50	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 25 V, f = 1 MHz, V_{GS} = 0 V	-	529	-	pF
C_{oss}	Output capacitance		-	71	-	pF
C_{rss}	Reverse transfer capacitance		-	13.4	-	pF
$C_{oss\ eq.}$ [(1)]	Equivalent output capacitance	V_{DS} = 0 V to 420 V, V_{GS} = 0 V	-	11	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	6	-	Ω
Q_g	Total gate charge	V_{DD} = 416 V, I_D = 4.4 A,	-	16.9	-	nC
Q_{gs}	Gate-source charge	V_{GS} = 0 to 10 V	-	4.2	-	nC
Q_{gd}	Gate-drain charge	(see Figure 15. Test circuit for gate charge behavior)	-	8.4	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 260 V, I_D = 2.2 A,	-	11.4	-	ns
t_r	Rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	13.6	-	
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and	-	23.1	-	
t_f	Fall time	Figure 19. Switching time waveform)	-	15	-	

Table 7. **Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.4	A
I_{SDM} [1]	Source-drain current (pulsed)		-		17.6	A
V_{SD}	Forward on voltage	V_{GS} = 0 V, I_{SD} = 4.4 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 4.4 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	55		ns
Q_{rr}	Reverse recovery charge		-	95		nC
I_{RRM}	Reverse recovery current		-	3.5		A
t_{rr}	Reverse recovery time	I_{SD} = 4.4 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	120		ns
Q_{rr}	Reverse recovery charge		-	266		nC
I_{RRM}	Reverse recovery current		-	4.5		A

1. *Pulse width is limited by safe operating area*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%*

Table 8. **Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D = 0 V	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

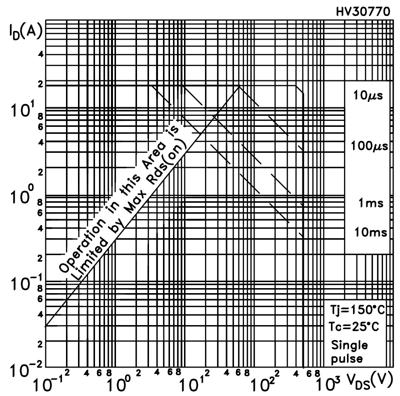


Figure 3. Thermal impedance

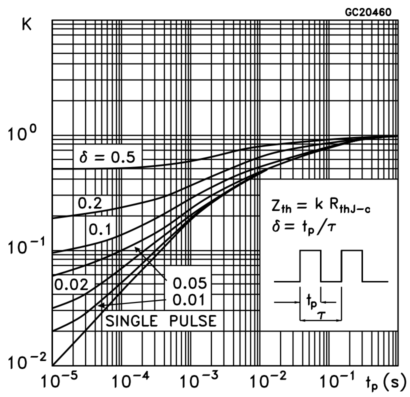


Figure 4. Output characteristics

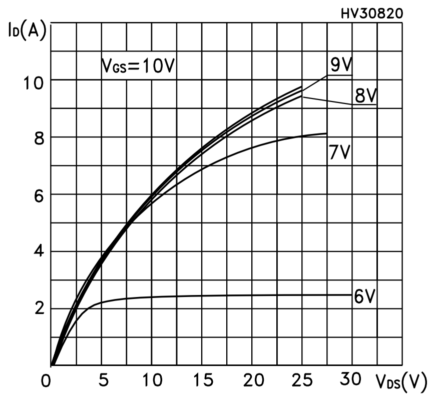


Figure 5. Transfer characteristics

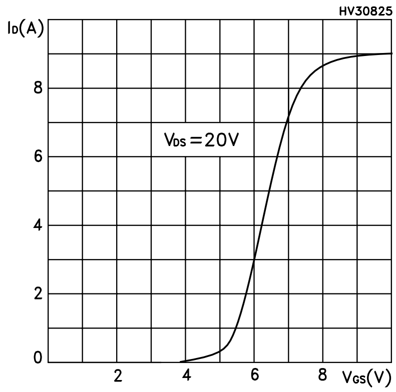


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

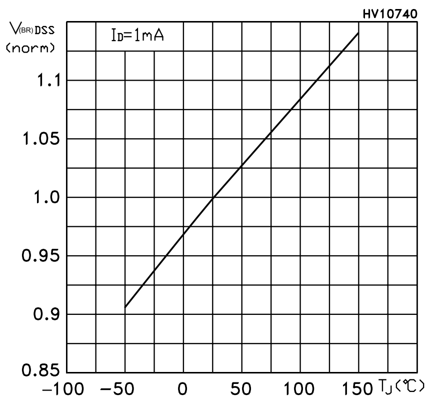


Figure 7. Static drain-source on-resistance

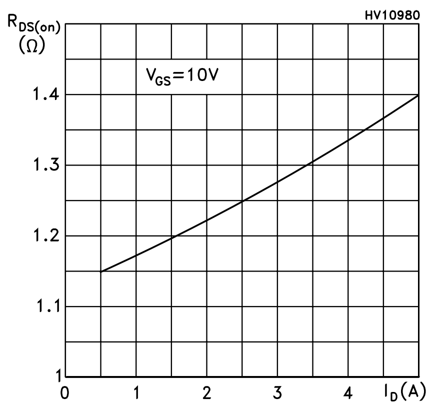


Figure 8. **Gate charge vs gate-source voltage**

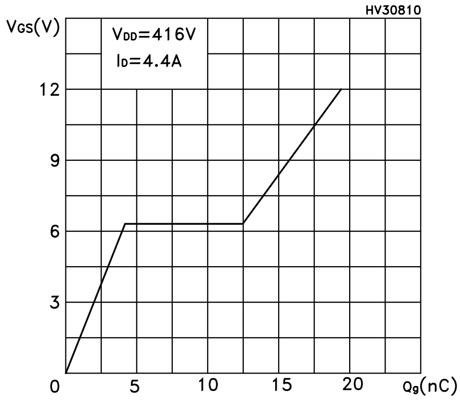


Figure 9. **Capacitance variations**

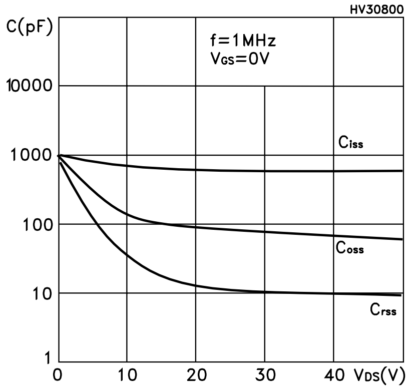


Figure 10. **Normalized gate threshold voltage vs temperature**

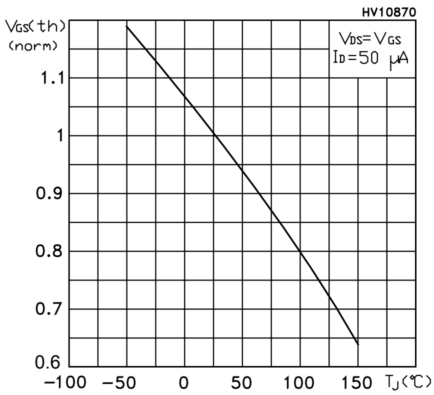


Figure 11. **Normalized on-resistance vs temperature**

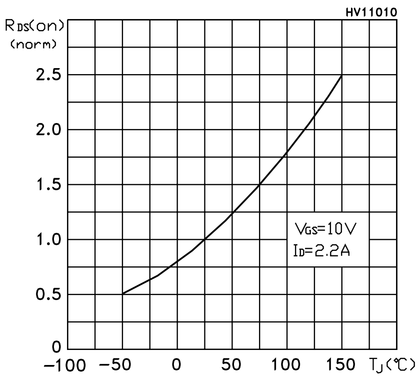


Figure 12. **Source-drain diode forward characteristics**

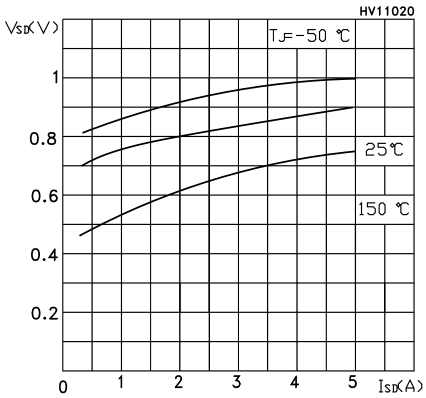
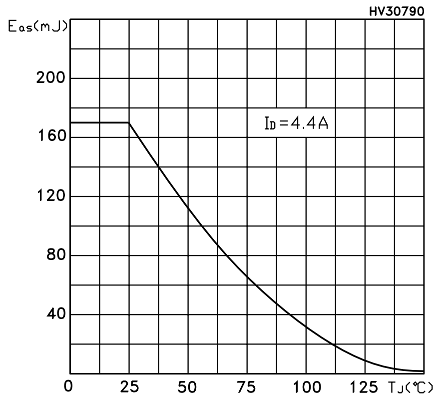


Figure 13. **Maximum avalanche energy vs temperature**



3 Test circuits

Figure 14. Test circuit for resistive load switching times

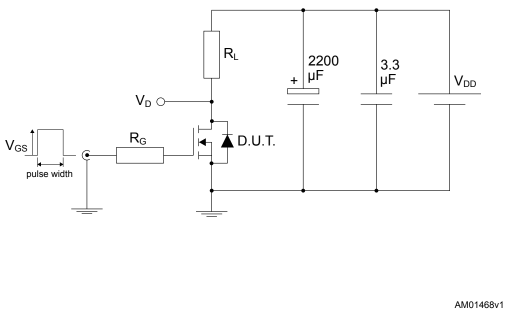


Figure 15. Test circuit for gate charge behavior

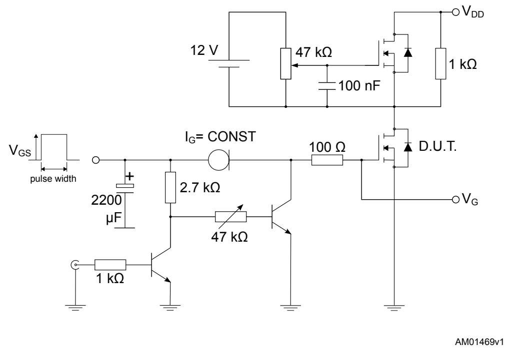


Figure 16. Test circuit for inductive load switching and diode recovery times

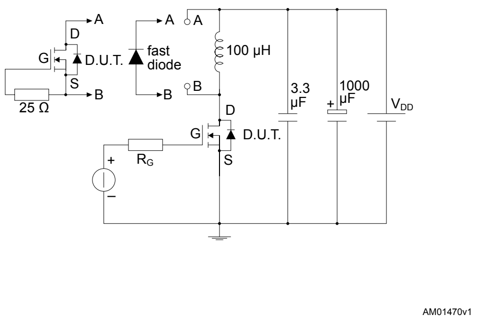


Figure 17. Unclamped inductive load test circuit

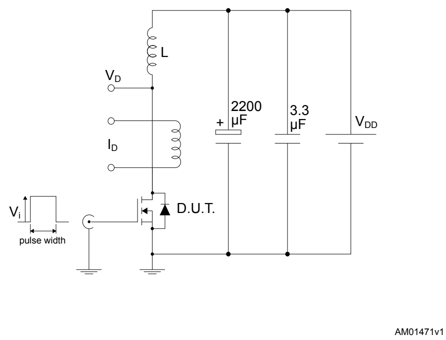


Figure 18. Unclamped inductive waveform

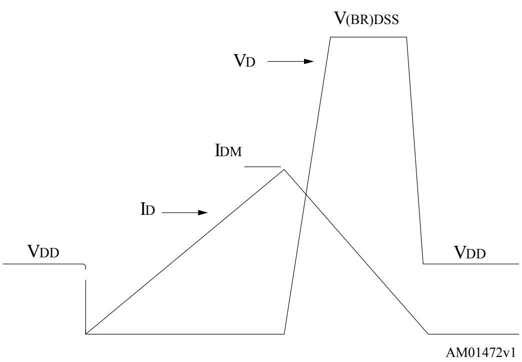
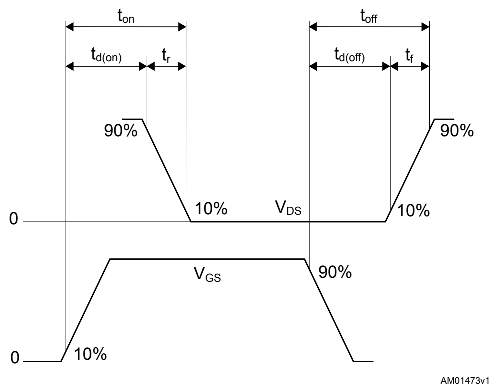


Figure 19. Switching time waveform

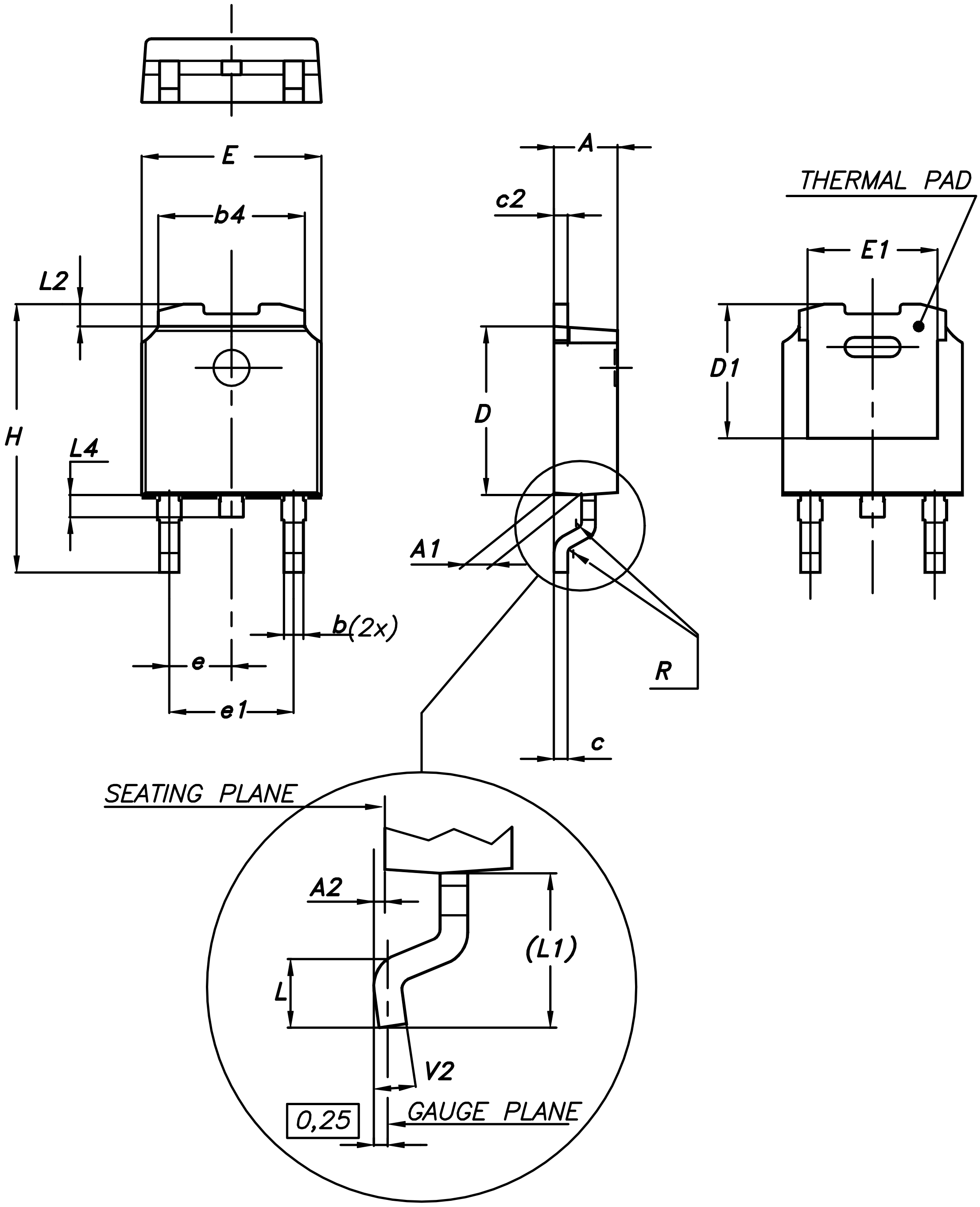


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 20. DPAK (TO-252) type A package outline



0068772_A_26

Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type E package information

Figure 21. **DPAK (TO-252) type E package outline**

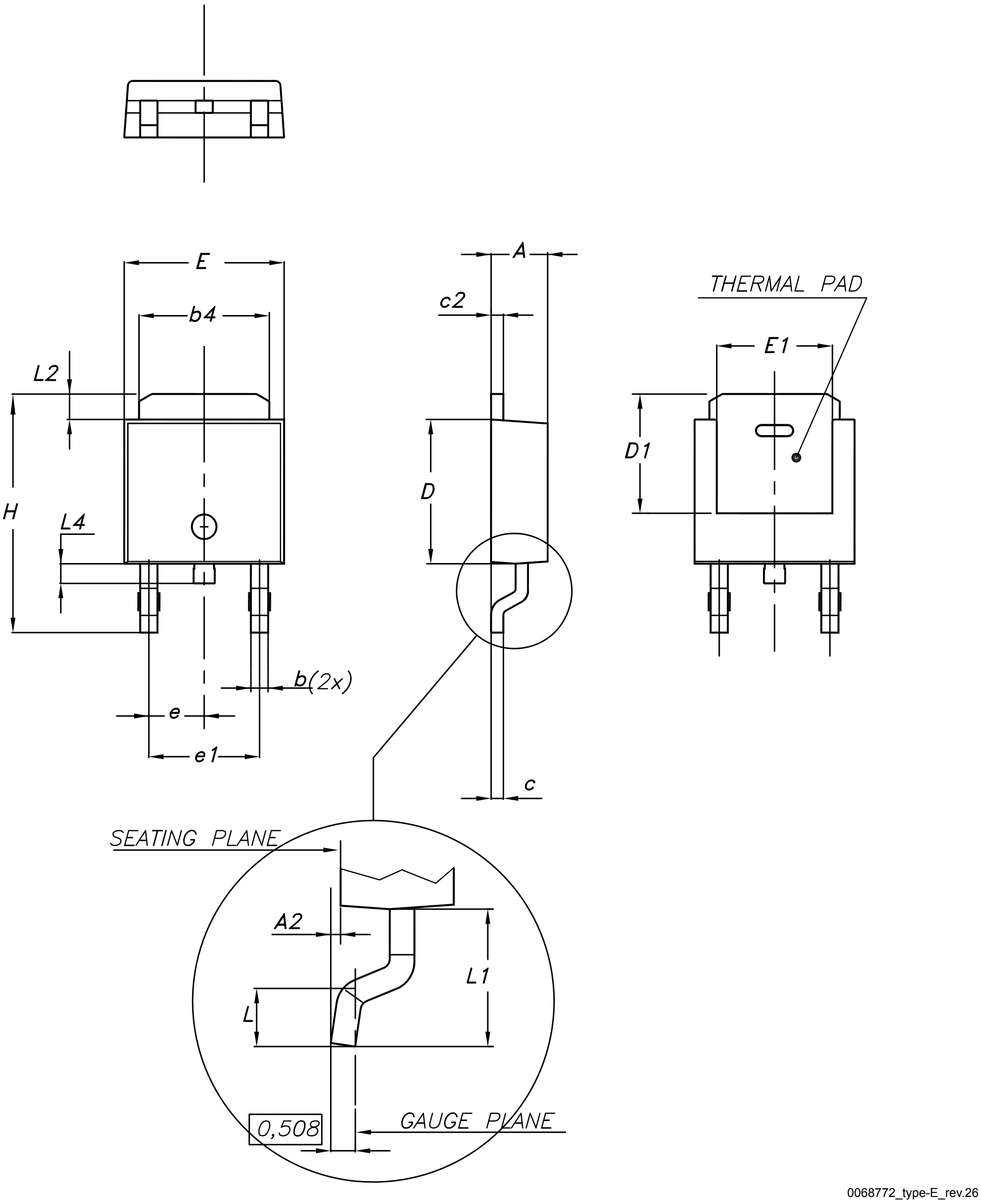
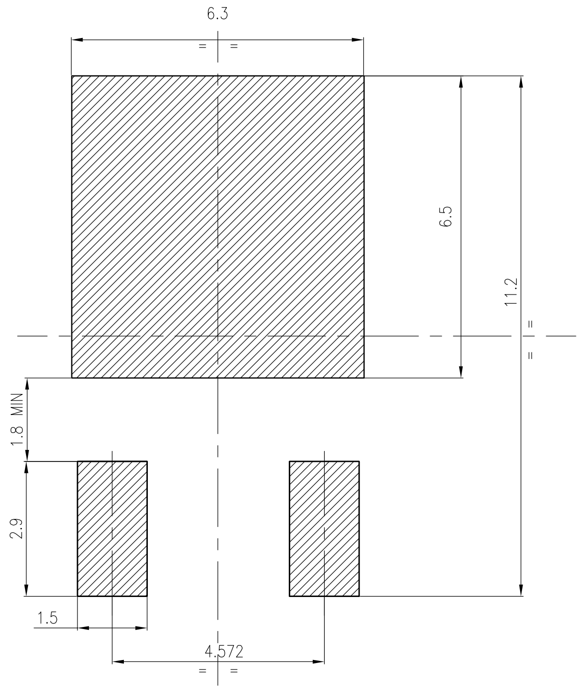


Table 10. DPAK (TO-252) type E mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 22. DPAK (TO-252) recommended footprint (dimensions are in mm)



4.3 DPAK (TO-252) packing information

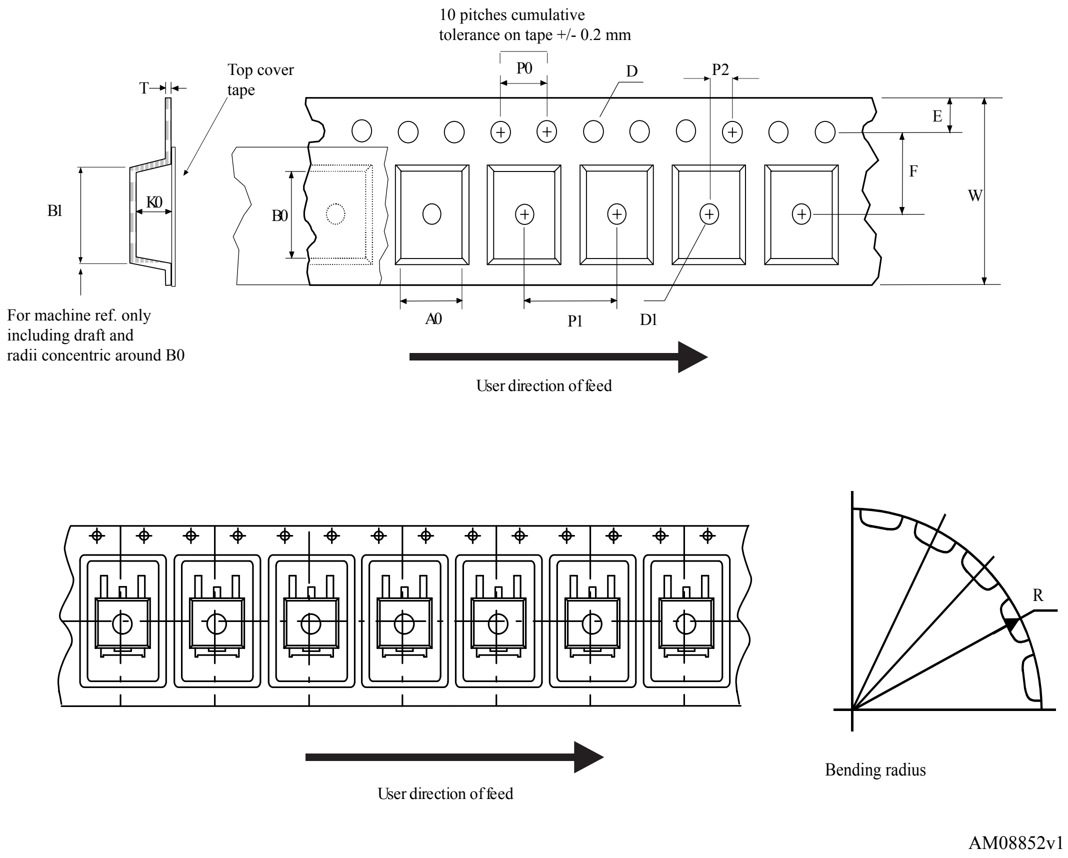


Figure 23. DPAK (TO-252) tape outline

Figure 24. DPAK (TO-252) reel outline

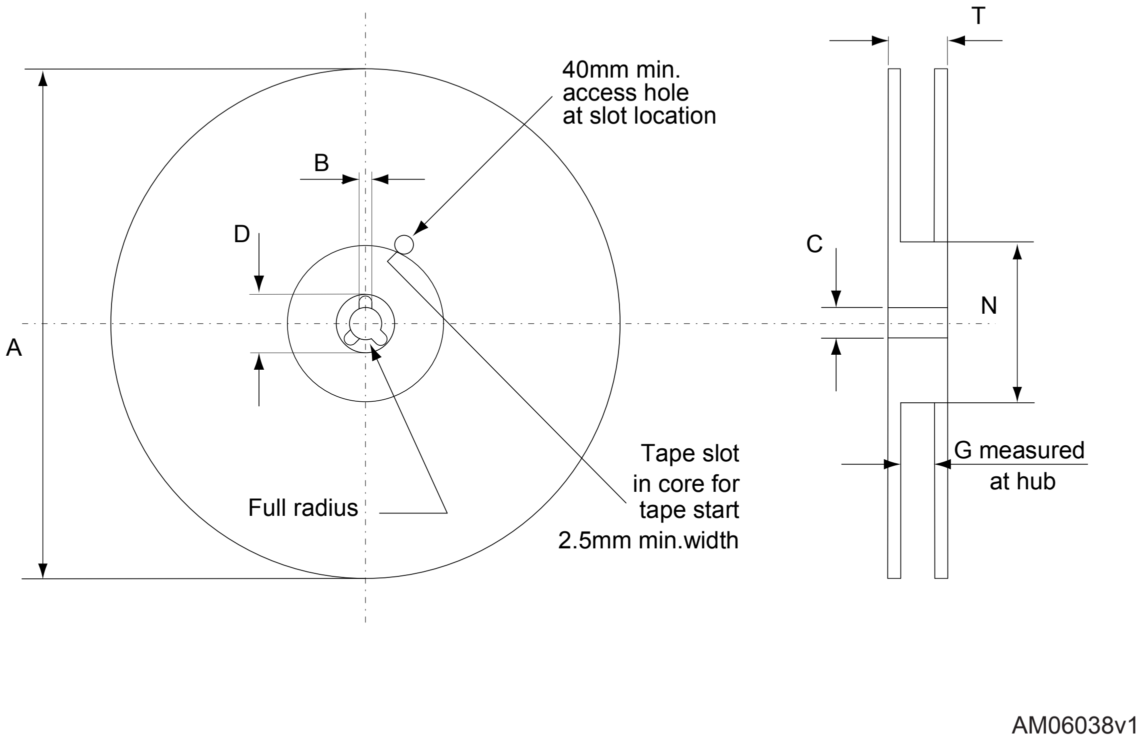


Table 11. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 12. Document revision history

Date	Version	Changes
06-May-2009	1	First release.
28-Sep-2011	2	Inserted new device in I2PAK. Updated tables 1, 2 and 3 with the new package. Updated Section 4: Package mechanical data with the new package and Section 5: Packaging mechanical data. Minor text changes.
24-Apr-2014	3	Updated Section 4.1: DPAK, STD5N52U. Modified: Q_{rr} unit in Table 7. Modified: Figure 8 and 11. The part number STI5N52U has been moved to a separate datasheet.
10-Dec-2018	4	Part number STF5N52U was moved to a separate datasheet and the document was updated accordingly.

Contents