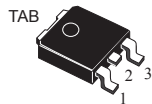
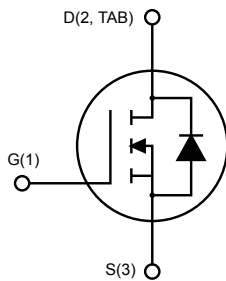



## Automotive-grade N-channel 500 V, 0.7 $\Omega$ typ., 7.5 A, MDmesh Power MOSFET in a DPAK package


**DPAK**


AM01475v1\_noZen

### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STD5NM50AG	500 V	0.8 $\Omega$	7.5 A

- AEC-Q101 qualified 
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

### Applications

- Switching applications

### Description

This N-channel Power MOSFET is developed using STMicroelectronics' revolutionary MDmesh technology, which associates the multiple drain process with the company's PowerMESH horizontal layout. This device offers extremely low on-resistance, high  $dv/dt$  and excellent avalanche characteristics. Utilizing ST's proprietary strip technique, this Power MOSFET boasts an overall dynamic performance which is superior to similar products on the market.



#### Product status link

[STD5NM50AG](#)

#### Product summary

<b>Order code</b>	STD5NM50AG
<b>Marking</b>	D5NM50
<b>Package</b>	DPAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Gate-source voltage	500	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20\text{ k}\Omega$ )	500	V
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	7.5	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	4.7	
$I_{DM}^{(1)}$	Drain current (pulsed)	30	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	100	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS\ peak} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.25	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

1. When mounted on a 1-inch<sup>2</sup> FR-4, 2 oz Cu board

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_{jmax}$ )	2.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	300	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified).

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 500\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 500\text{ V}, T_C = 125\text{ °C}^{(1)}$			10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 30\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$		0.7	0.8	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance		-	415	-	pF
$C_{oss}$	Output capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	88	-	pF
$C_{rss}$	Reverse transfer capacitance		-	12	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	50	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	3	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 400\text{ V}, I_D = 7.5\text{ A},$ $V_{GS} = 0\text{ to } 10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	13	-	nC
$Q_{gs}$	Gate-source charge		-	5	-	nC
$Q_{gd}$	Gate-drain charge		-	6	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}, I_D = 2.5\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	16	-	ns
$t_r$	Rise time		-	8	-	ns
$t_{d(Voff)}$	Off-voltage rise time	$V_{DD} = 400\text{ V}, I_D = 5\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times and Figure 17. Switching time waveform)	-	14	-	ns
$t_f$	Fall time		-	6	-	ns
$t_c$	Cross-over time		-	13	-	ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		30	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 7.5\text{ A}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$	-	185		ns
$Q_{rr}$	Reverse recovery charge		-	1.1		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	11.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$	-	270		ns
$Q_{rr}$	Reverse recovery charge		-	1.6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	12	

1. Pulse width is limited by safe operating area
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

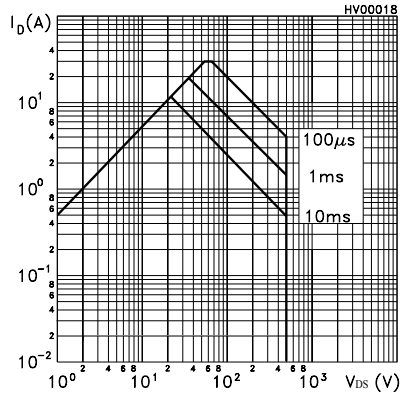


Figure 2. Thermal impedance

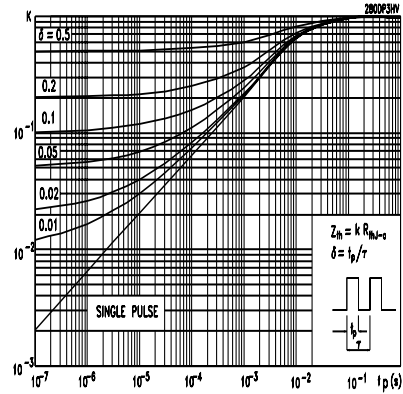


Figure 3. Output characteristics

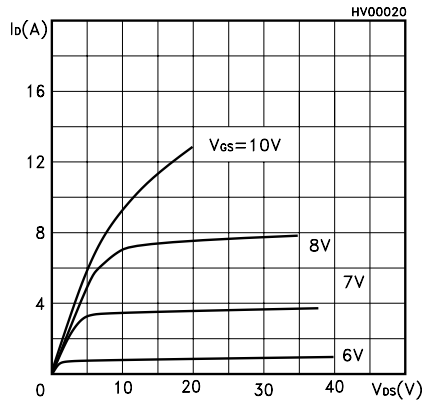


Figure 4. Transfer characteristics

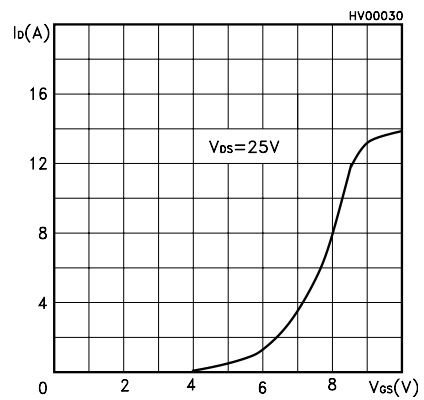


Figure 5. Normalized gate threshold voltage vs temperature

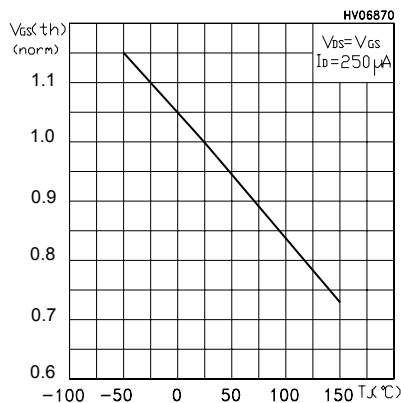
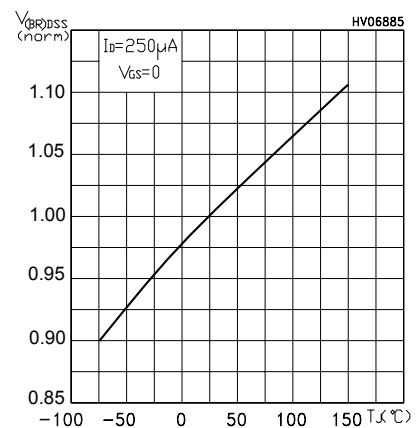
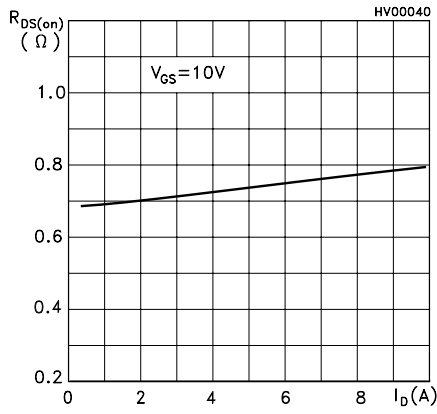


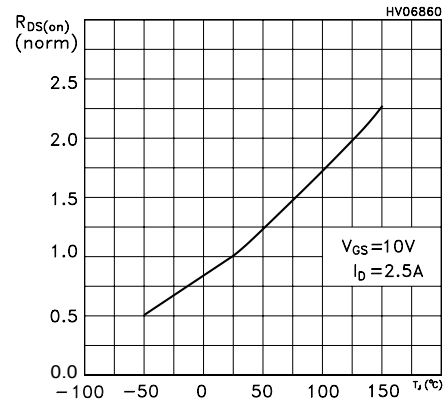
Figure 6. Normalized  $V_{(BR)DSS}$  vs temperature



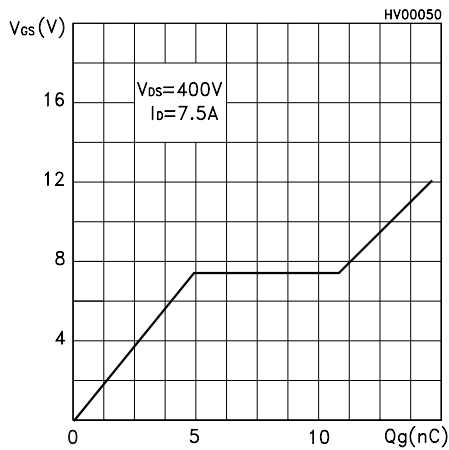
**Figure 7. Static drain-source on-resistance**



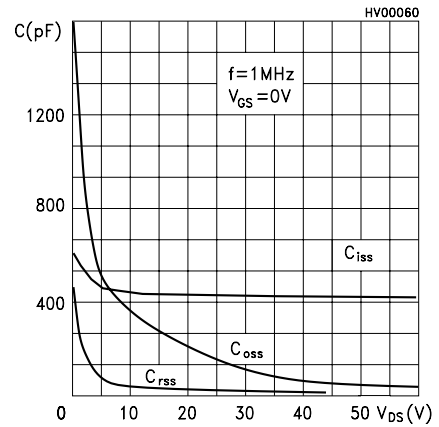
**Figure 8. Normalized on-resistance vs temperature**



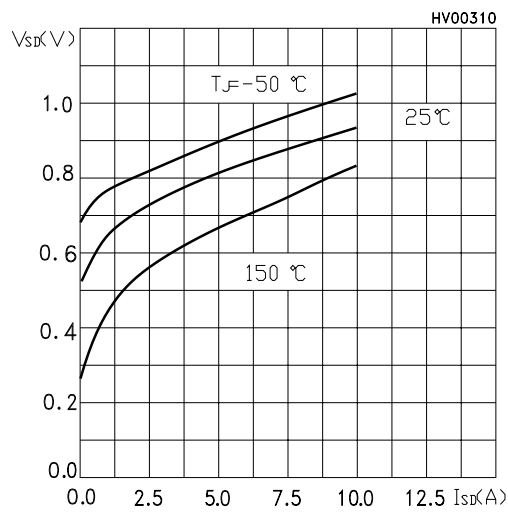
**Figure 9. Gate charge vs gate-source voltage**



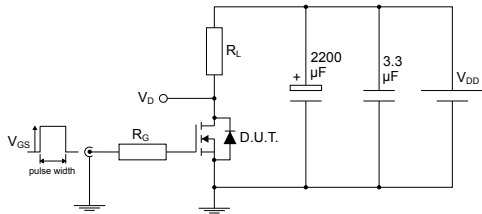
**Figure 10. Capacitance variations**



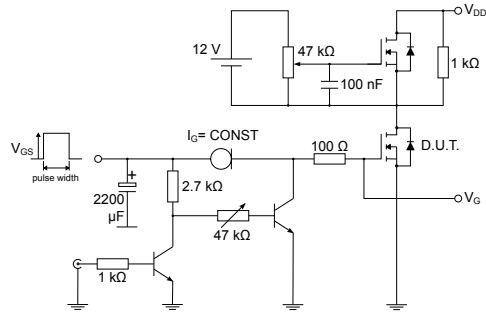
**Figure 11. Source-drain diode forward characteristics**



### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**


AM01468v1

**Figure 13. Test circuit for gate charge behavior**


AM01469v1

**Figure 14. Test circuit for inductive load switching and diode recovery times**

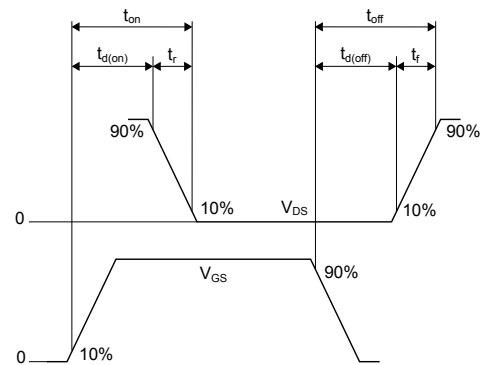

AM01470v1

**Figure 15. Unclamped inductive load test circuit**


AM01471v1

**Figure 16. Unclamped inductive waveform**


AM01472v1

**Figure 17. Switching time waveform**


AM01473v1

## 4 Package information

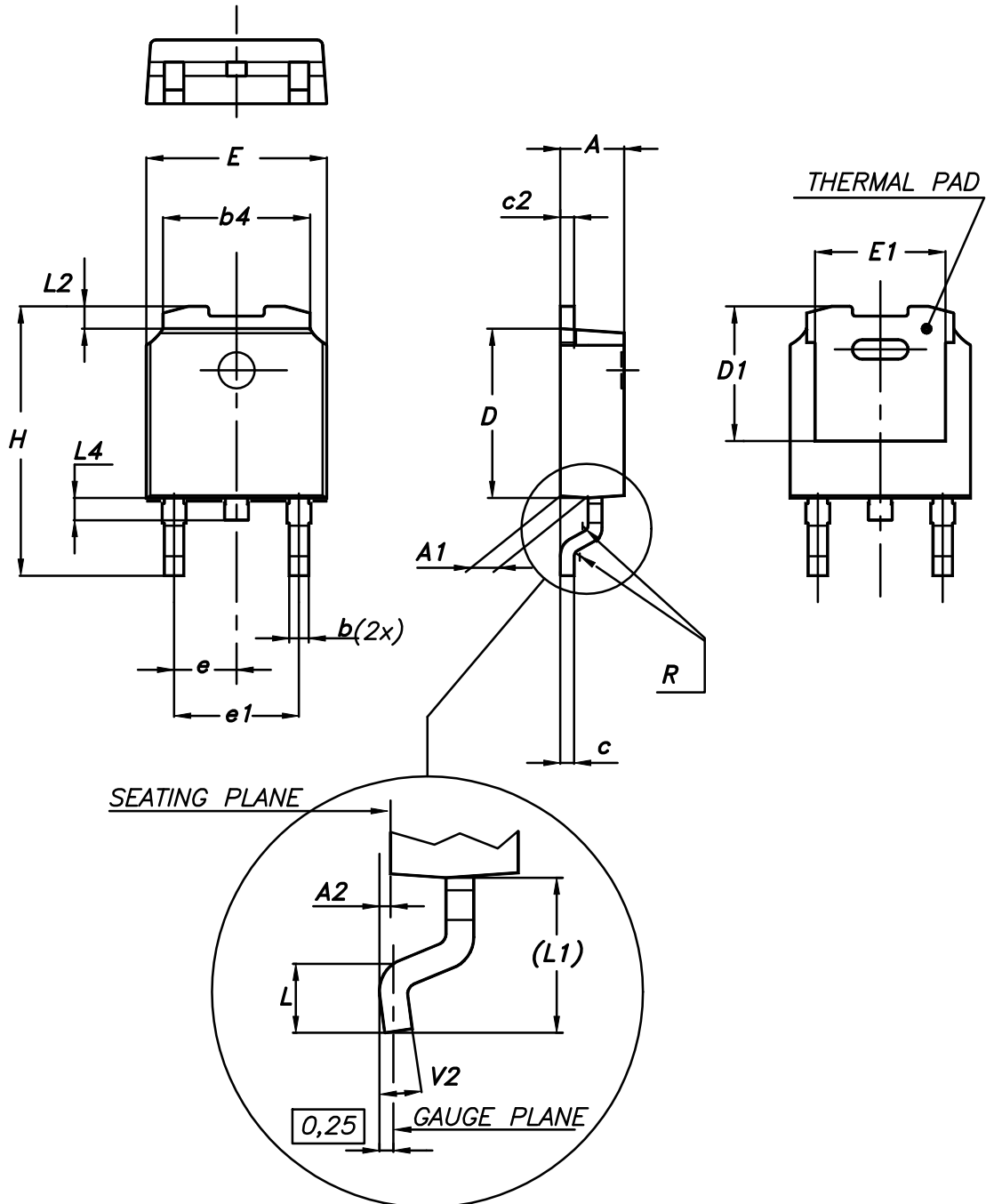
---

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.



### 4.1 DPAK (TO-252) type A package information

Figure 18. DPAK (TO-252) type A package outline

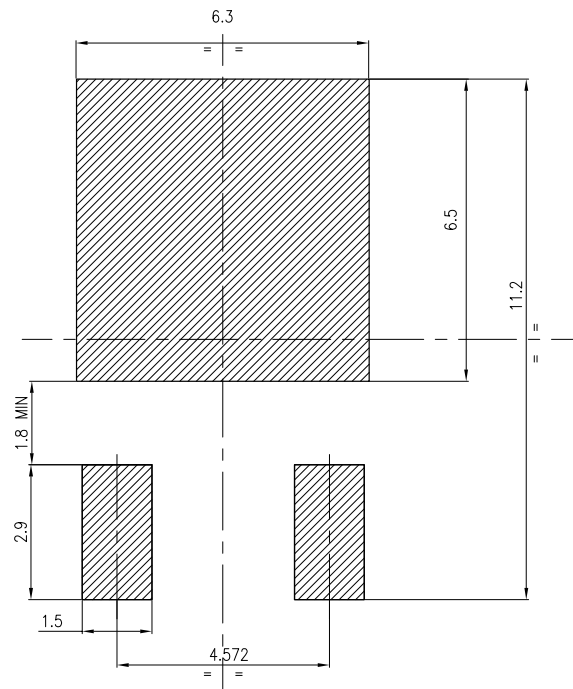


0068772\_A\_26

**Table 8. DPAK (TO-252) type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

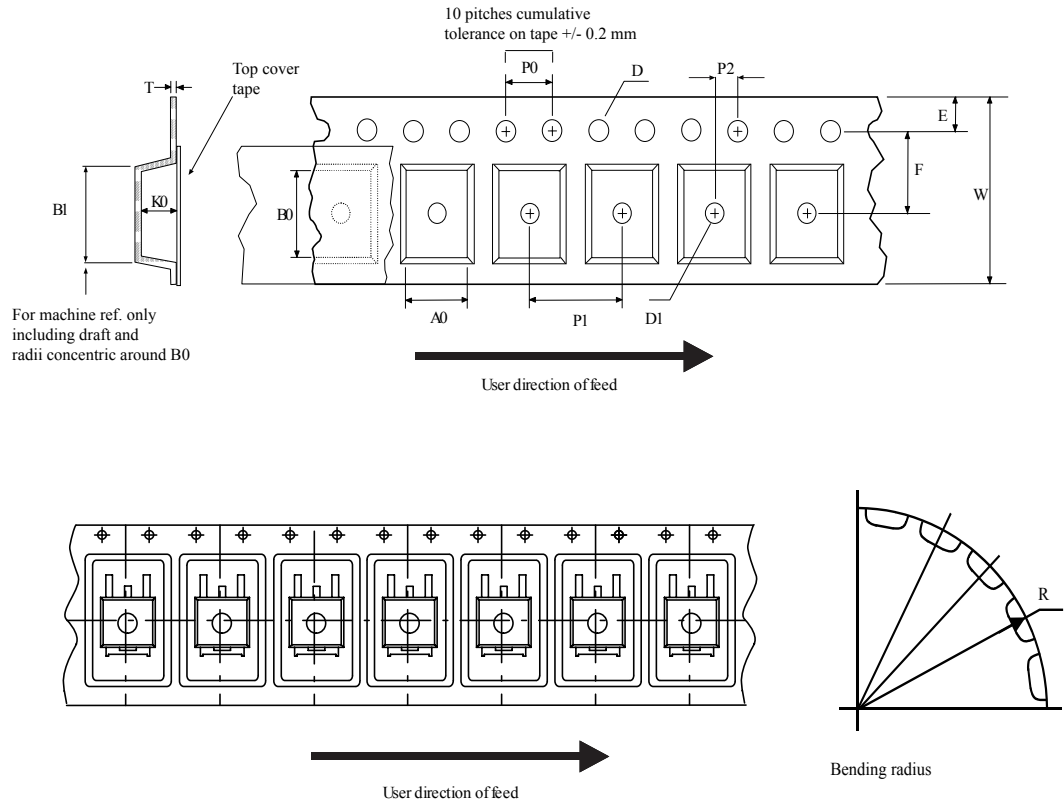
Figure 19. DPAK (TO-252) type A recommended footprint (dimensions are in mm)



FP\_0068772\_26

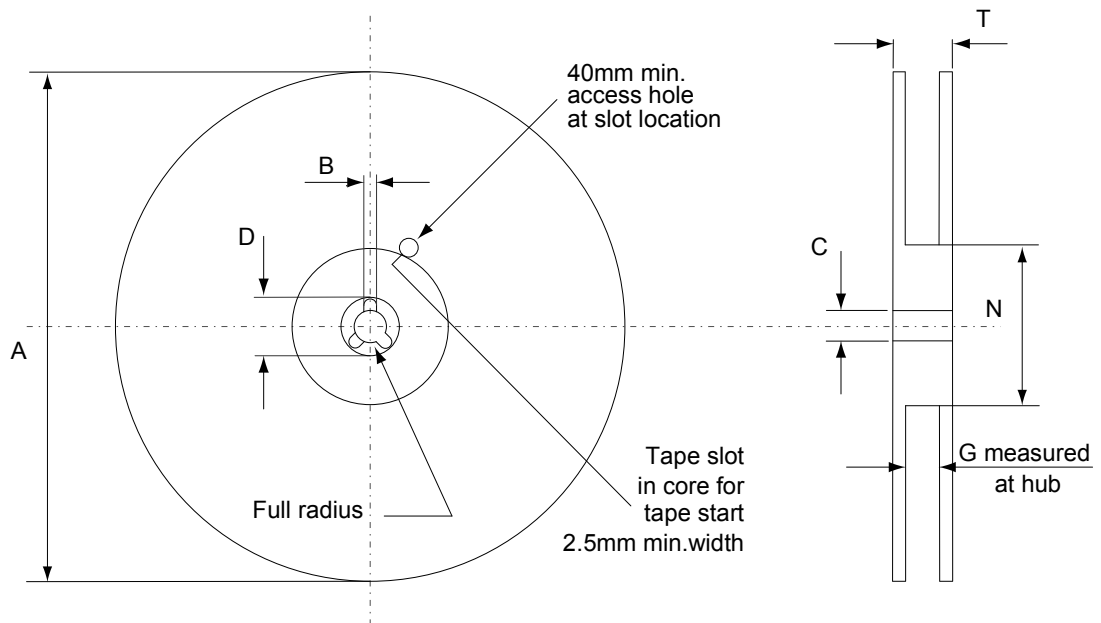
## 4.2 DPAK (TO-252) packing information

Figure 20. DPAK (TO-252) tape outline



AM08852v1

**Figure 21. DPAK (TO-252) reel outline**



AM06038v1

**Table 9. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 10. Document revision history**

Date	Version	Changes
12-Sep-2018	1	Initial release.
09-Apr-2019	2	Updated <a href="#">Section 4.1 DPAK (TO-252) type A package information</a> . Minor text changes.

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>2</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>3</b>
<b>2.1</b>	Electrical characteristics (curves) .....	5
<b>3</b>	<b>Test circuits</b> .....	<b>7</b>
<b>4</b>	<b>Package information</b> .....	<b>8</b>
<b>4.1</b>	DPAK (TO-252) type A package information .....	8
<b>4.2</b>	DPAK (TO-252) packing information .....	11
	<b>Revision history</b> .....	<b>14</b>

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved



## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [MOSFET](#) category:*

*Click to view products by [STMicroelectronics](#) manufacturer:*

Other Similar products are found below :

[614233C](#) [648584F](#) [IRFD120](#) [JANTX2N5237](#) [FCA20N60\\_F109](#) [FDZ595PZ](#) [2SK2545\(Q,T\)](#) [405094E](#) [423220D](#) [TPCC8103,L1Q\(CM](#)  
[MIC4420CM-TR](#) [VN1206L](#) [SBVS138LT1G](#) [614234A](#) [715780A](#) [NTNS3166NZT5G](#) [SSM6J414TU,LF\(T](#) [751625C](#) [BUK954R8-60E](#)  
[DMN3404LQ-7](#) [NTE6400](#) [SQJ402EP-T1-GE3](#) [2SK2614\(TE16L1,Q\)](#) [2N7002KW-FAI](#) [DMN1017UCP3-7](#) [EFC2J004NUZTDG](#) [ECH8691-](#)  
[TL-W](#) [FCAB21350L1](#) [P85W28HP2F-7071](#) [DMN1053UCP4-7](#) [NTE221](#) [NTE2384](#) [NTE2903](#) [NTE2941](#) [NTE2945](#) [NTE2946](#) [NTE2960](#)  
[NTE2967](#) [NTE2969](#) [NTE2976](#) [NTE455](#) [NTE6400A](#) [NTE2910](#) [NTE2916](#) [NTE2956](#) [NTE2911](#) [DMN2080UCB4-7](#) [TK10A80W,S4X\(S](#)  
[SSM6P69NU,LF](#) [DMP22D4UFO-7B](#)