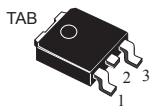
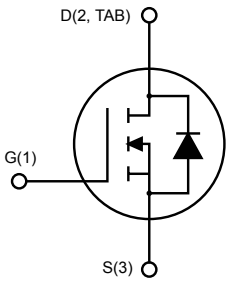
N-channel 500 V, 0.7 Ω typ., 7.5 A, MDmesh™ Power MOSFET in a DPAK package



DPAK



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD5NM50T4	500 V	0.8 Ω	7.5 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This N-channel Power MOSFET is developed using STMicroelectronics' revolutionary MDmesh™ technology, which associates the multiple drain process with the company's PowerMESH™ horizontal layout. This device offers extremely low on-resistance, high dv/dt and excellent avalanche characteristics. Utilizing ST's proprietary strip technique, this Power MOSFET boasts an overall dynamic performance which is superior to similar products on the market.

Product status link
STD5NM50T4

Product summary	
Order code	STD5NM50T4
Marking	D5NM50
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Gate-source voltage	500	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	500	V
V_{GS}	Gate- source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	7.5	A
I_D	Drain current (continuous) at T_C= 100 °C	4.7	
I_{DM} (1)	Drain current (pulsed)	30	A
P_{TOT}	Total dissipation at T_C = 25 °C	100	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 5 A, di/dt ≤ 400 A/µs, $V_{DS\ peak}$ < $V_{(BR)DSS}$, V_{DD} = 400 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.25	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	50	

1. *When mounted on a 1-inch² FR-4, 2 oz Cu board*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_{jmax})	2.5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	300	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	500			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 500 V			1	µA
		V_{GS} = 0 V, V_{DS} = 500 V, T_C = 125 °C(1)			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±30 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.5 A		0.7	0.8	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 25 V, f = 1 MHz, V_{GS} = 0 V	-	415	-	pF
C_{oss}	Output capacitance		-	88	-	pF
C_{rss}	Reverse transfer capacitance		-	12	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	50	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 7.5 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	13	-	nC
Q_{gs}	Gate-source charge		-	5	-	nC
Q_{gd}	Gate-drain charge		-	6	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V, I_D = 2.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	16	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(Voff)}$	Off-voltage rise time	V_{DD} = 400 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Test circuit for inductive load switching and diode recovery times and Figure 17. Switching time waveform)	-	14	-	ns
t_f	Fall time		-	6	-	ns
t_c	Cross-over time		-	13	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7.5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		30	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 7.5 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs,	-	185		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	1.1		µC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	11.5		A
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs,	-	270		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_j = 150 °C	-	1.6		µC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	12		A

1. *Pulse width is limited by safe operating area*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

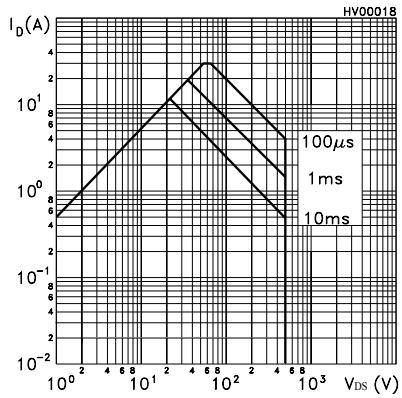


Figure 2. Thermal impedance

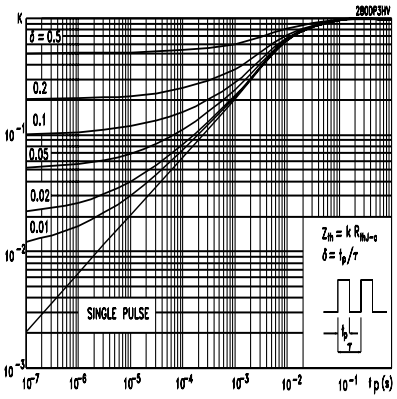


Figure 3. Output characteristics

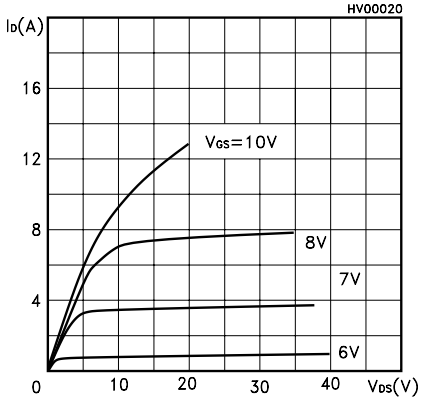


Figure 4. Transfer characteristics

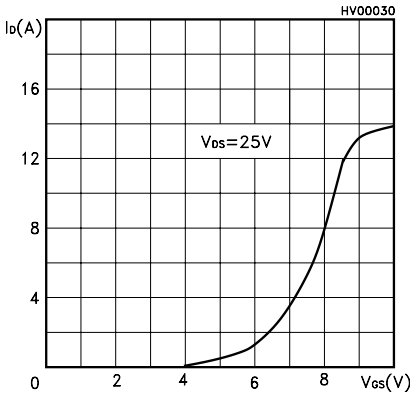


Figure 5. Normalized gate threshold voltage vs temperature

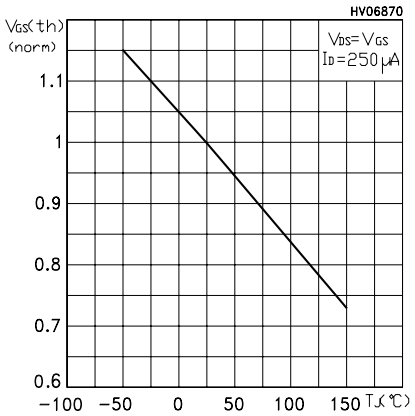


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

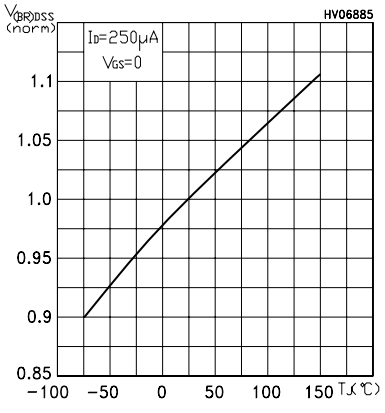


Figure 7. **Static drain-source on-resistance**

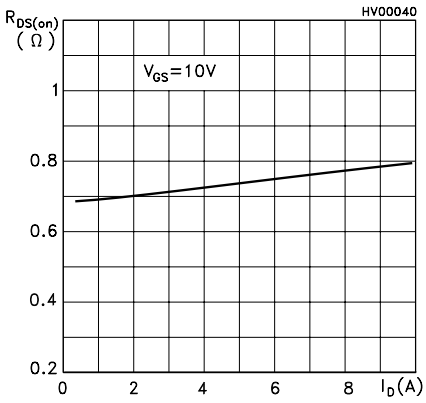


Figure 8. **Normalized on-resistance vs temperature**

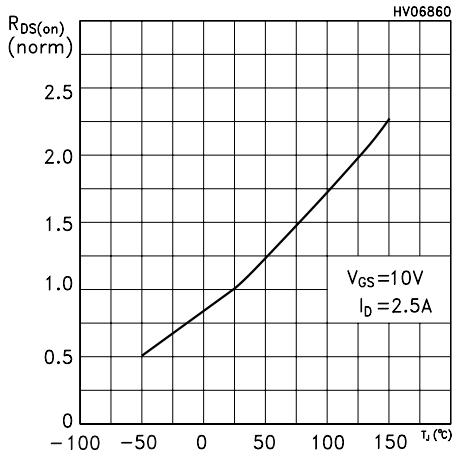


Figure 9. **Gate charge vs gate-source voltage**

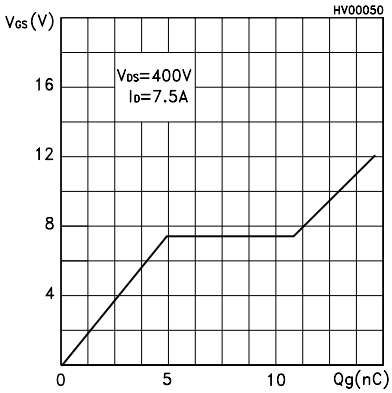


Figure 10. **Capacitance variations**

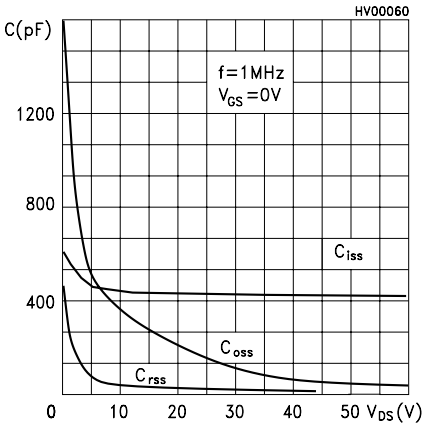
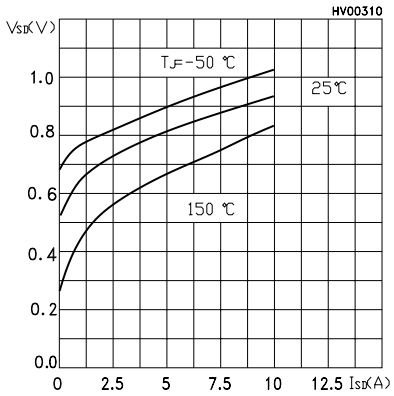


Figure 11. **Source-drain diode forward characteristics**



3 Test circuits

Figure 12. Test circuit for resistive load switching times

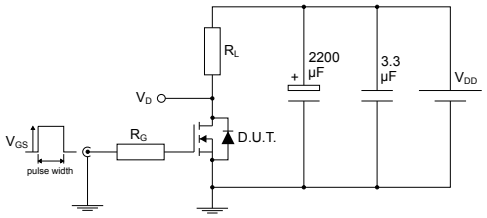


Figure 13. Test circuit for gate charge behavior

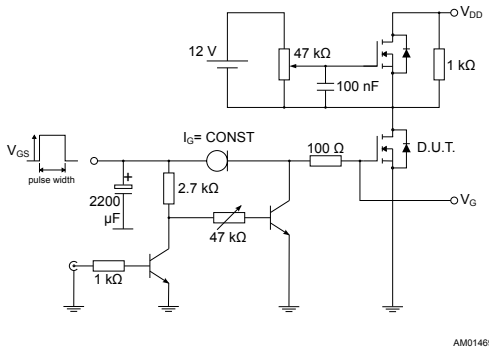


Figure 14. Test circuit for inductive load switching and diode recovery times

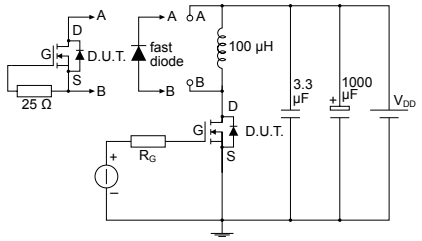


Figure 15. Unclamped inductive load test circuit

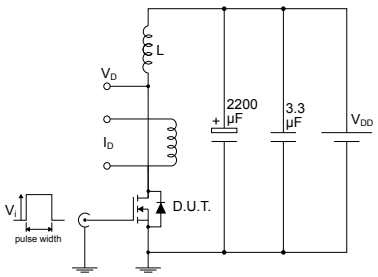


Figure 16. Unclamped inductive waveform

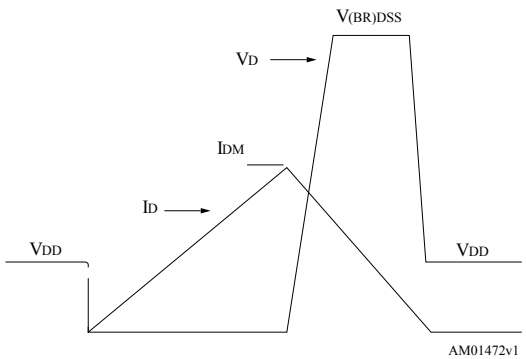
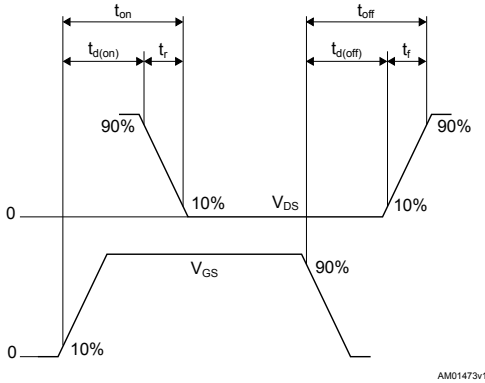


Figure 17. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 18. **DPAK (TO-252) type A2 package outline**

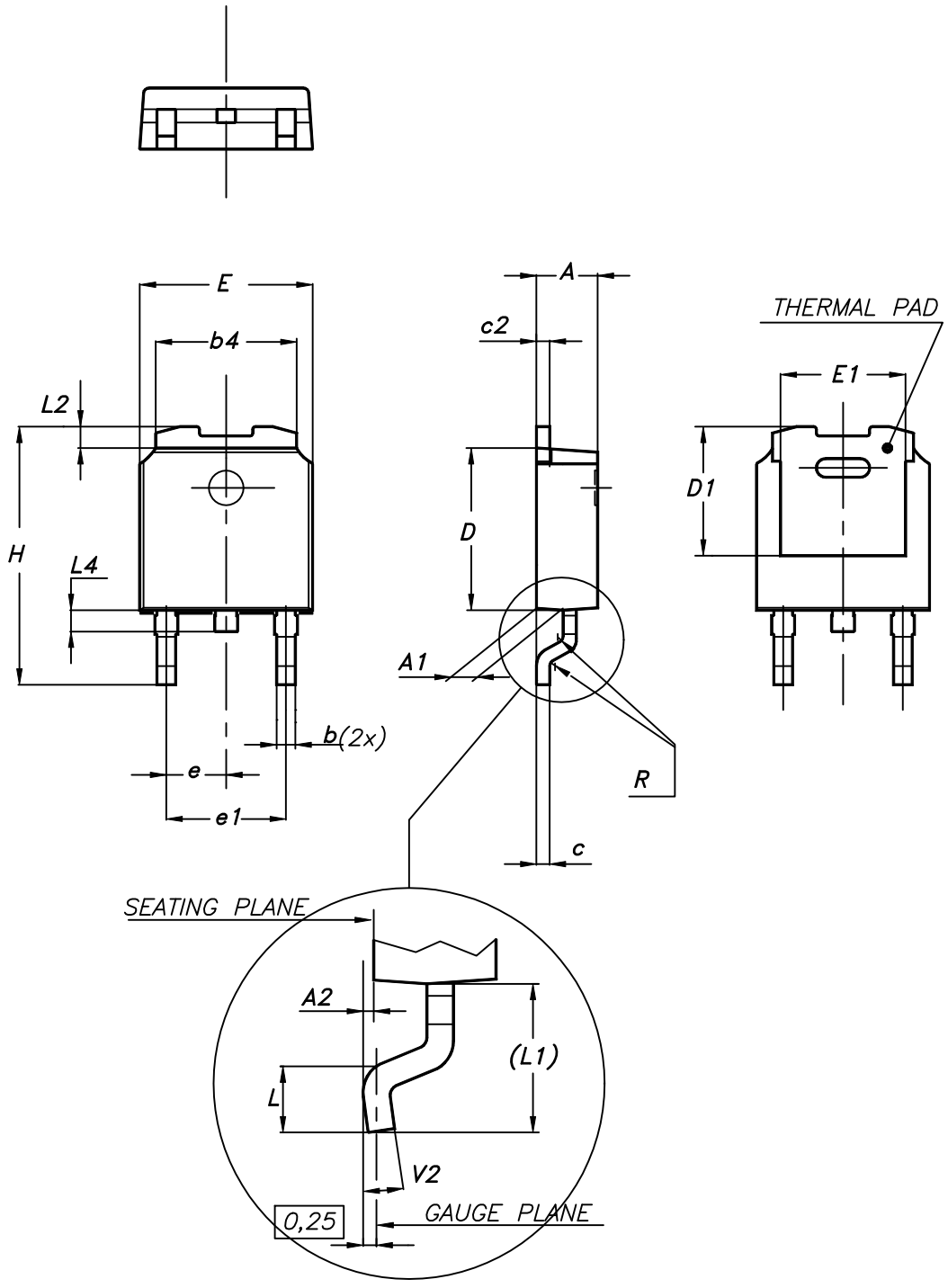


Table 8. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C2 package information

Figure 19. **DPAK (TO-252) type C2 package outline**

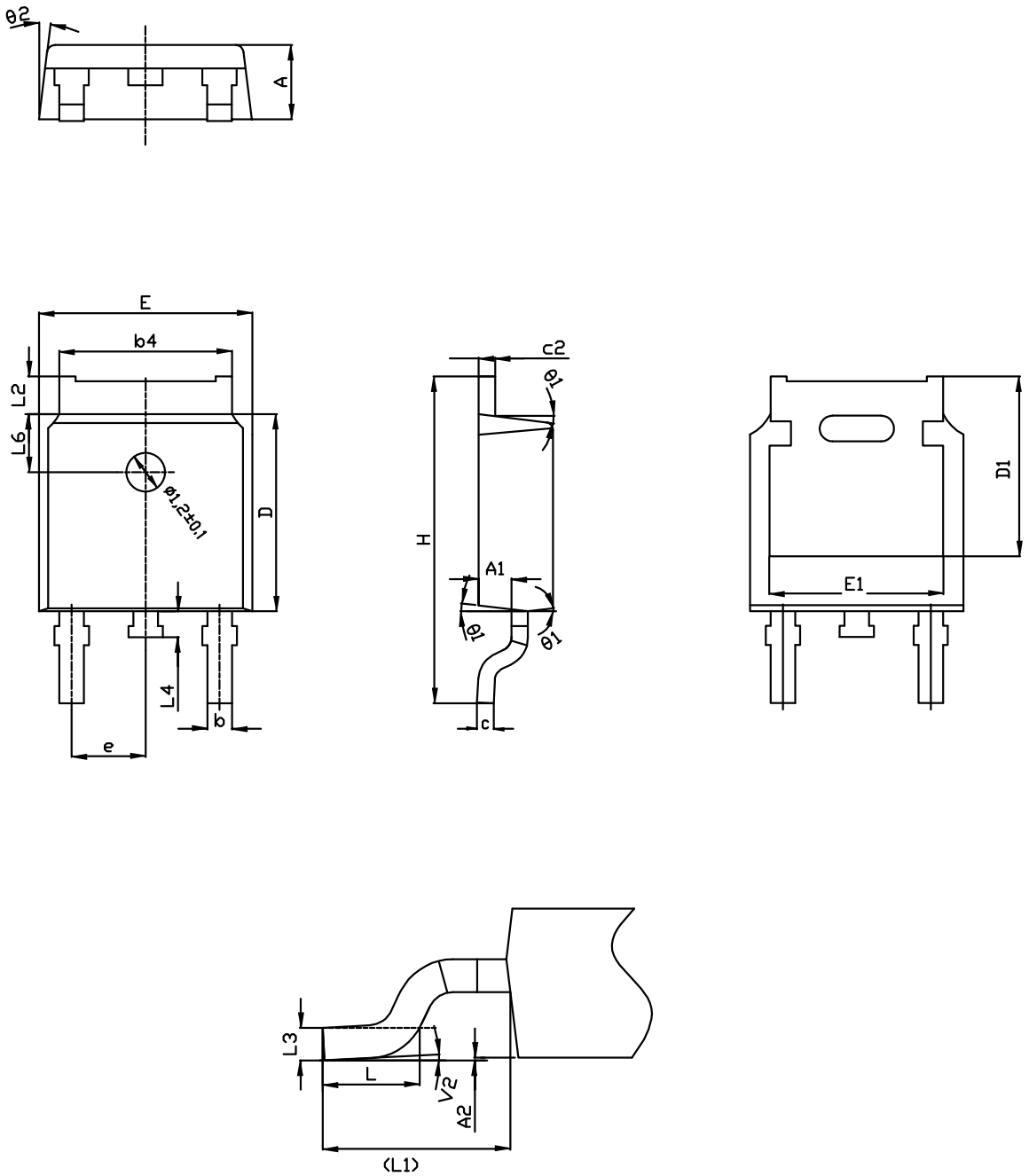


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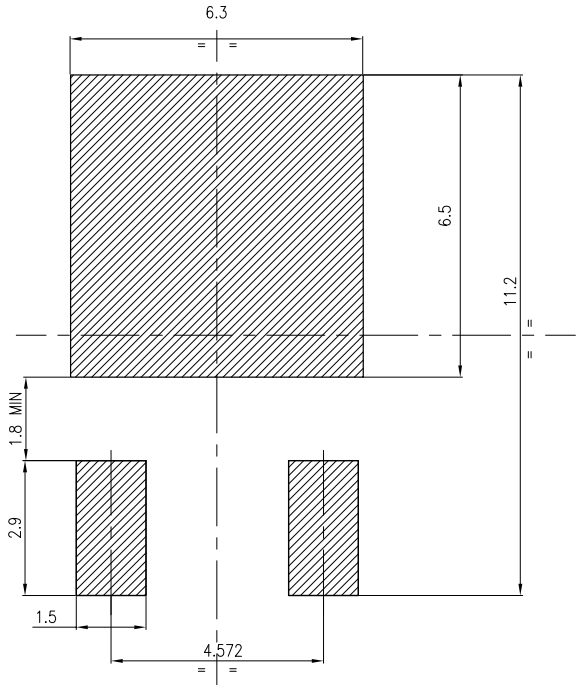
Table 9. **DPAK (TO-252) type C2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 20. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



4.3 DPAK (TO-252) packing information

Figure 21. **DPAK (TO-252) tape outline**

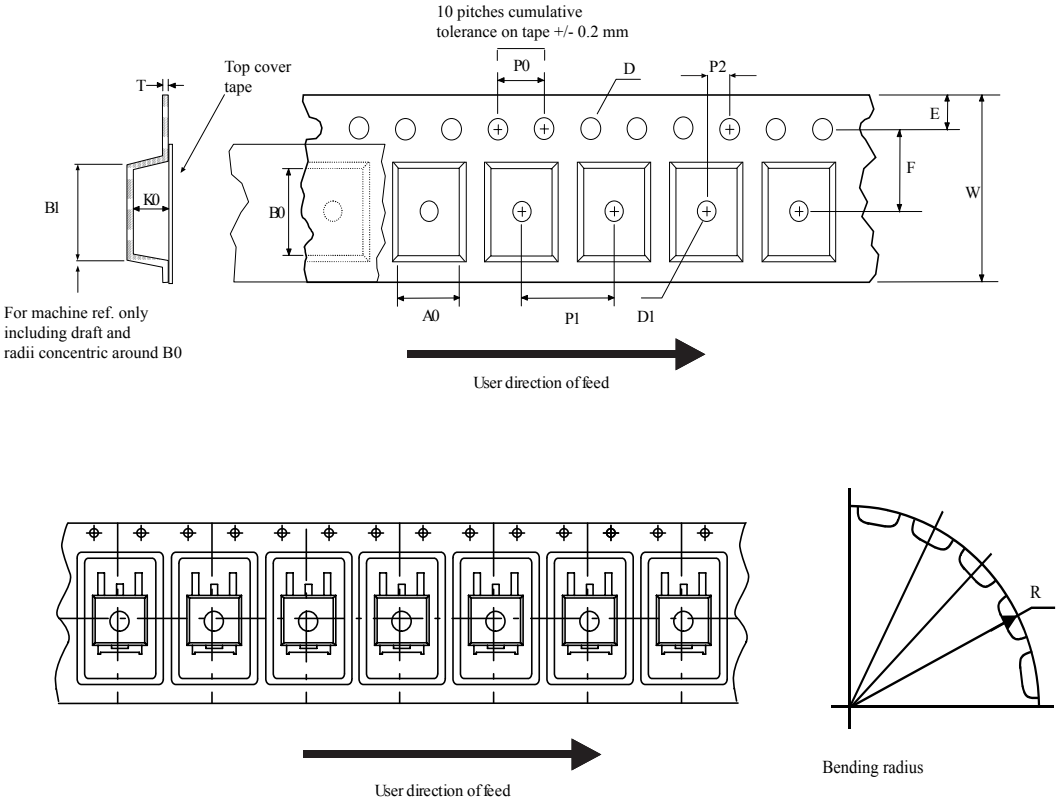


Figure 22. **DPAK (TO-252) reel outline**

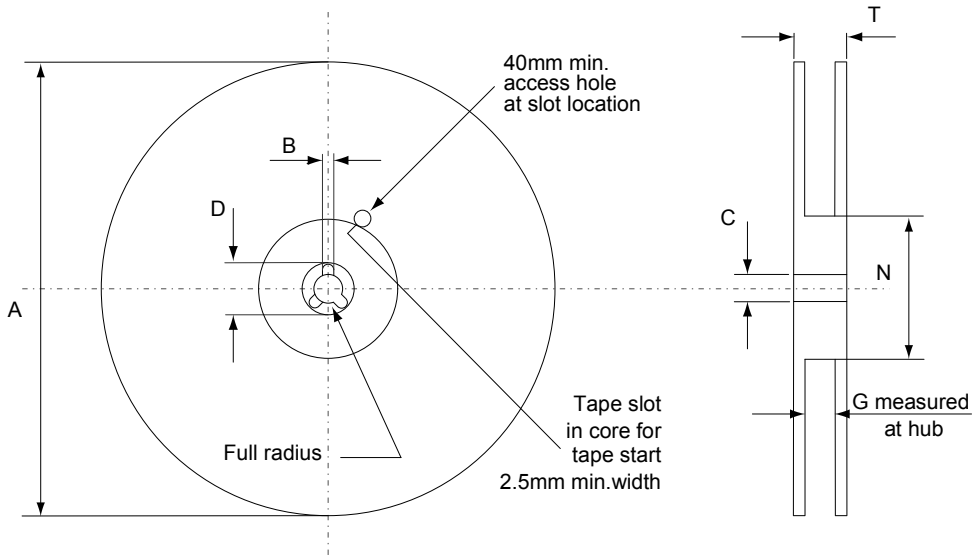


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Table 10. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 11. **Document revision history**

Date	Version	Changes
07-Sep-2018	11	The part number STD5NM50-1 have been moved to a separate datasheet. Modified title, features, description and applications on cover page. Modified Table 2. Thermal data. Modified Section 2.1 Electrical characteristics (curves). Updated Section 3 Test circuits. Updated Section 4 Package information. Minor text changes.

Contents

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